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Multifunctional molybdenum disulfide flash memory using a PEDOT:PSS floating gate

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Abstract

Two-dimensional transition metal dichalcogenide materials (TMDs), such as molybdenum disulfide (MoS_2), have been considered promising candidates for future electronic applications owing to their electrical, mechanical, and optical properties. Here, we present a new concept for multifunctional MoS_2 flash memory by combining a MoS_2 channel with a PEDOT:PSS floating layer. The proposed MoS_2 memory devices exhibit a switching ratio as high as 2.3×10^7, a large memory window (54.6 ± 7.80 V), and high endurance (>1,000 cycles). As the PEDOT:PSS film enables a low-temperature solution-coating process and mechanical flexibility, the proposed P-memory can be embedded on a polyimide substrate over a rigid silicon substrate, offering high mechanical endurance (over 1,000 cycle bending test). Furthermore, both MoS_2 and PEDOT:PSS have a bandgap that is desirable in optoelectronic memory operation, where charge carriers are stored differently in the floating gate depending on light illumination. As a new application that combines photodiodes and memory functions, we demonstrate multilevel memory programming based on light intensity and color.

Introduction

With the advent of the fourth industrial revolution, consumer electronics are in dire need of versatility beyond conventional electronic functions[1–4]. For example, conventional memory technology requires high-performance memory characteristics, such as fast switching, long-term retention, and high endurance[5–8]. On the other hand, current electronics demand the development of multifunctional memory devices with characteristics such as mechanical flexibility[9–11], multilevel storage[12,13], neuromorphic functions[14,15], and tunable memory operation[16], along with the conventional expectation of excellent memory features. However, existing silicon-based memory processes and structures have limitations in developing new features when the multifunctional memory deviates from the conventional complementary metal–oxide–semiconductor process frame. Therefore, with the development of new materials, the development of new electronic device concepts is crucial.

Meanwhile, as emerging semiconductor materials, transition metal dichalcogenides (TMDs) have attracted considerable attention[17–21]. TMDs have the potential to provide multifunctional material platforms due to a variety of physical properties, including their atomically thin nature[22], van der Waals interface[23], and controllable energy band structure[24–26]. Moreover, TMDs have shown the possibility of new electronic device features such as gate-tunable memristic behavior[16,27], neuromorphic functions[28], and optoelectronic properties[29,30].

Here, we present multifunctional nonvolatile memory using a molybdenum disulfide (MoS_2) semiconductor and a poly(3,4-ethylenedioxythinophene):poly(styrene sulfonate) (PEDOT:PSS)[31] floating gate (P-memory). The combination of the MoS_2 semiconductor and PEDOT:PSS floating gate provides a switching current ratio as high as 2.3×10^7, a large memory window up to 62 V, excellent

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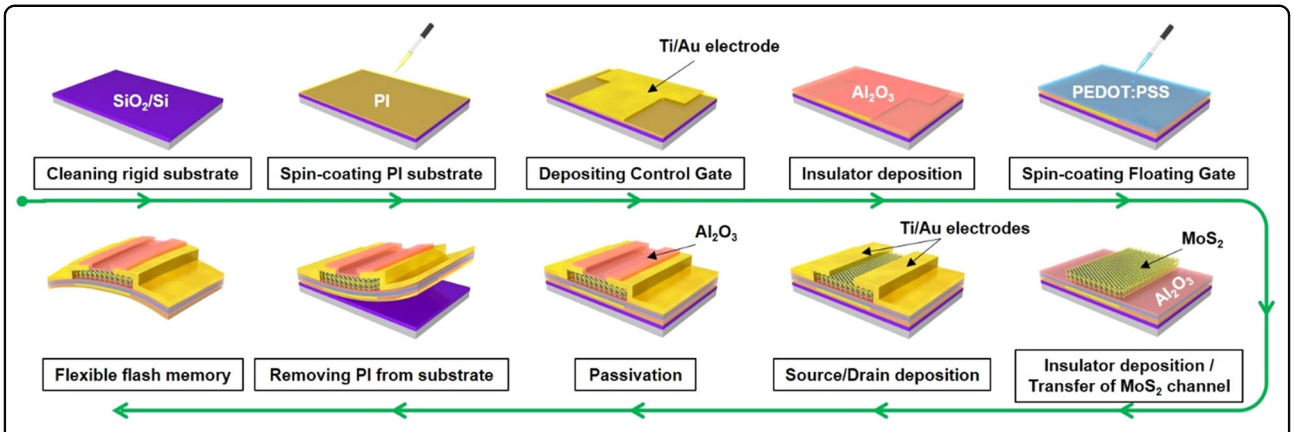

Scheme 1 Fabrication process for flexible MoS_2 flash memory using a PEDOT:PSS floating gate and solution-coated polyimide (PI) as a flexible substrate.

endurance (>1000 cycles), and a long retention time (>2000 s). We also investigate device-to-device variation by examining 30 P-memory devices fabricated with the same fabrication process. This process results in uniform memory operation properties with average $I_{erase}/I_{program}$ of $2.18 \times 10^6 \pm 4.77 \times 10^6$, memory window of 54.3 V ± 7.80 V, threshold voltage under the programmed state $V_{TH,\ programmed}$ of 16.40 ± 8.25 V, and threshold voltage under the erased state $V_{TH,\ erased}$ of −40.53 ± 5.87 V. Furthermore, the proposed P-memory has photo-programmable memory behavior, as photoinduced charge carriers contribute to programming and erasing operations in P-memory. As a result, we demonstrate photo-sensing with nonvolatile memory behavior to distinguish illumination light intensity and color. This information is stored directly inside the floating gate. Finally, we implement P-memory embedded onto a flexible polyimide (PI) substrate, as both MoS_2 and PEDOT:PSS can be simply deposited regardless of the substrate type. The fabricated P-memory on the PI substrate exhibits excellent memory operation ($I_{erase}/I_{program} = 1.07 \times 10^6$) with a high mechanical endurance (over 1000 cycle bending test). This result suggests that the multifunctional characteristics of a flash memory device can be obtained from a new material combination of layered MoS_2 and PEDOT:PSS polymer in a floating-gate transistor structure.

Materials and methods

Device fabrication

The device fabrication process is schematically shown in Fig. S1. A Si/SiO_2 substrate was treated with O_2 plasma for 5 min. A synthesized highly resistive PEDOT:PSS solution was spin-coated on the substrate at 8000 rpm for 60 s through a 0.45 μm syringe filter. The thin film was then thermally annealed on a hot plate at 150 °C for 10 min. After floating-gate formation on the Si/SiO_2 substrate, Al_2O_3 of 80 nm thickness as the tunneling dielectric layer (TDL) was deposited on the PEDOT:PSS floating-gate layer using ALD. To utilize MoS_2 flakes as the channel, mechanically exfoliated MoS_2 flakes were transferred onto the TDL by peeling them from a bulk crystal using Scotch tape. To complete the P-memory device fabrication, Ti/Au (20 nm/100 nm) source/drain electrodes, respectively, were patterned by photolithography using AZ GXR-601 photoresist, followed by E-beam evaporation and an etching process. Next, a 20 nm-thick Al_2O_3 passivation layer (PL) was deposited on the P-memory device by using ALD. For flexible memories, a flexible substrate was prepared by spin coating solution-based PI on a cleaned SiO_2/Si substrate (3000 rpm for 30 s). Then, the flexible device was fabricated following the same process as shown in Scheme 1. As the last step, the flexible memory was peeled off by carefully separating the edges of the flexible memory and rigid substate with tweezers, which completed the flexible memory fabrication process.

Synthesis of the highly resistive PEDOT:PSS solution

Poly(4-styrene sulfonate) (PSS) was used as a dispersant and dopant for PEDOT. The weight ratio of PEDOT:PSS was controlled to be 1:7.5. To synthesize the PEDOT:PSS dispersion, PSS (18.75 g) was added to distilled water (1000 g), and the mixture was stirred for 30 min. Then, nitrogen gas (99.999%) was bubbled through the solution for 60 min at a rate of 3 L min^{-1} to prevent oxidation by the dissolved oxygen in the water. To this solution, the EDOT monomer (2.50 g, 1.76×10^{-2} mol) was added and stirred with a mechanical stirrer for 30 min. The synthesis of the PEDOT:PSS dispersion was carried out using an Fe^{3+}-catalyzed oxidative polymerization process. The oxidizing agents iron(III) sulfate (0.035 g, 8.79×10^{-5} mol) and sodium persulfate (5.02 g, 2.1×10^{-2} mol) were dissolved in 100 mL of distilled water by sonication and added to the reaction solution. Polymerization was

Table 1 Previously reported solvent exchange processes for water-based PEDOT:PSS solutions.

Method	Solvent	Stability of re-dispersion	Problems (limitations)	Ref.
Mixture & Evaporation	NMP, DMAC, DMF, etc.	Not verified	- Limited solvent (High b.p > 150 °C) ☞ High drying temperature requirement, poor coating - Environmentally restricted materials (NMP, DMAC, DMF) by EU, 'REACH' (2018.10.31~Present)	19
Mixture (3:1 v/v)	DMSO, DMF, THF	Not verified	- Simple mixing, not solvent exchange	20
Synthesis of Alkyl derivative PEDOT	Chloroform, DMF	Good	- Far less conductive - Very complex, small production	21
Synthesis of PEDOT:PSS in organic solvent	Methanol, THF, Toluene, etc.	Moderate	- Far less conductive - Complex and complicated	22
Ultrafiltration	All with high ∂H (>19.4) such as EtOH, EG, etc.	Very Good	<Advantages> - Various solvents (both high and low b.p) - Highly conductive (no loss of conductivity) - Simple, fast, and conducive to mass production	This work

performed for 40 h at 25 °C with bubbling nitrogen gas. After polymerization of the PEDOT:PSS dispersion, the product was mixed with 500 mL of a mixture of cation and anion ion exchange resin for 1 h and filtered with a 30 μm mesh filter. Table 1 shows previous reports about solvent exchange processes for water-based PEDOT:PSS solutions.

Device characterization

The memory operation characteristics of MoS_2 flash memory devices were determined with a Keithley 4200-SCS semiconductor characterization system equipped with a probe station in the dark under ambient atmosphere. For determining the photoinduced memory operation properties, illumination sources of 638 nm and 405 nm (MCLS1, Thorlabs) and 532 nm (MGL-FN-532, CNI) were used. The incident power densities of the illumination light were measured by a laser power meter (PM100A, Thorlabs). To perform a cyclic bending test, the flexible MoS_2 flash memory was loaded onto a multimodal bending tester, which repeated the sequence of a tensile stress (1 s)/flat (1 s) cycle 1000 times. The surface morphology and thickness profile of MoS_2 were measured using atomic force microscopy (XE7, Park Systems).

Results and discussion

Flash memory structure based on MoS_2 and PEDOT:PSS

First, we fabricated the P-memory on a rigid SiO_2/Si substrate. The memory device is composed of multilayer MoS_2 (thickness of 94.09 nm) as the channel; PEDOT:PSS of 80 nm thickness as the floating gate; 80 nm- and 40 nm-thick Al_2O_3 as a TDL and a PL, respectively; Ti/Au (20 nm/100 nm) as source/drain electrodes, respectively; and a 300 nm SiO_2/Si substrate as a blocking dielectric layer (BDL) and a control gate (CG) (Fig. 1a). Further details of the fabrication process are provided in Fig. S1, and thickness scans are shown in Fig. S2.

We spin-coated a PEDOT:PSS layer on top of a BDL SiO_2 layer, and thereby, the PEDOT:PSS acted as a charge trapping layer for data storage operation (Fig. 1b, c). To understand the effects of the floating-gate layer, we characterized the MoS_2 transistor depending on the existence of the PEDOT:PSS floating gate using the same device structure and fabrication conditions. The MoS_2 transistor without the PEDOT:PSS floating gate exhibited transfer characteristics without *I-V* hysteresis (Fig. 1d). On the other hand, the P-memory with the PEDOT:PSS floating gate exhibited transfer characteristic with a large memory window of 54.6 V ± 7.80 V, indicating that the PEDOT:PSS floating gate between the TDL and BDL layers acts as a charge storage layer (Fig. 1e and Fig. S3), showing a switching ratio as high as 2.3×10^7.

Electrical characteristics of the P-memory

To investigate the endurance of the P-memory, we performed 1000 consecutive sweeps of programming and erasing operations ($V_{program} = 60$ V and $V_{erase} = -60$ V) (Fig. 1f). The measured endurance of the P-memory exhibited stable programming and erasing operations with average I_{erase} of 1.4 ± 0.25 μA, $I_{program}$ of 9.46 ± 11.7 pA, and $I_{erase}/I_{program}$ of 1.07×10^6 under 1000 consecutive sweep cycles. We also evaluated the dynamic behavior of the P-memory (Fig. S4). Stable switching behavior between the programmed and erased states was

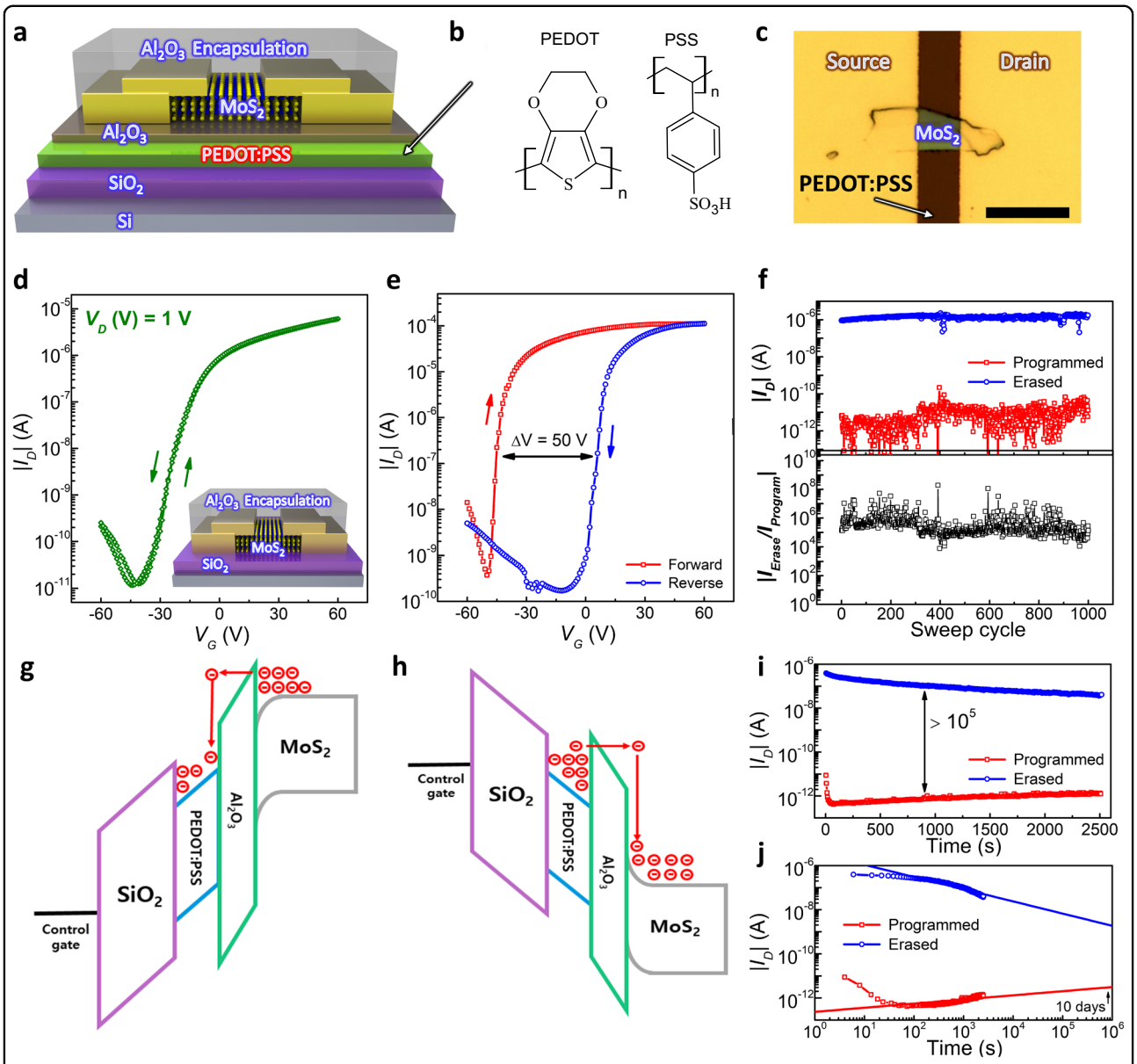

Fig. 1 MoS_2 flash memory using a PEDOT:PSS floating gate. a Three-dimensional schematic illustration of MoS_2 flash memory using a PEDOT:PSS floating gate. **b** Molecular structure of PEDOT:PSS. **c** Optical microscope image of fabricated MoS_2 flash memory. Scale bar is 20 μm. **d** Transfer characteristics showing negligible hysteresis of the MoS_2 transistor without the PEDOT:PSS floating gate under forward and reverse gate bias sweeps at $V_D = 1$ V. **e** Transfer characteristics of MoS_2 flash memory with a PEDOT:PSS floating gate. **f** Endurance of MoS_2 flash memory. I_D plot under the programmed state (red dot) and erased state (blue dot) for 1000 consecutive sweep cycles. One cycle consists of a program and erase voltage sweep from −60 V to 60 V and from 60 V to −60 V at $V_D = 1$ V. Endurance of the I_D switching ratio ($I_{erase}/I_{program}$) as a function of 1000 consecutive sweep cycles (bottom). Energy band diagram of the MoS_2 memory device with a PEDOT:PSS floating gate for **g** programming and **h** erasing operation. **i** Retention characteristics of the MoS_2 memory device with a PEDOT:PSS floating gate under programmed and erased states. The memory device was programmed at $V_C = 30$ V and erased at $V_C = -30$ V. **j** Retention characteristics of the extrapolated line on a double logarithmic scale.

obtained depending on the applied voltage pulses, with a programming pulse of 45 V at 400 ms and an erasing pulse of −45 V at 400 ms for a fixed $V_D = 1$ V. Figure 1g, h shows simplified energy band diagrams of the P-memory under programming and erasing operations considering an energy bandgap of MoS_2 of 5.15–5.39 eV[26,32]. Electron carriers enter the PEDOT:PSS floating gate through the TDL Al_2O_3 layer by the mechanisms of Fowler-Nordheim tunneling[33] and trap-assisted tunneling (TAT)[34], resulting in a positive shift of V_{TH}. Under a negative applied V_G (i.e., $V_G < -20$ V), the trapped electrons pass through the energy barrier inside the floating gate, causing a negative

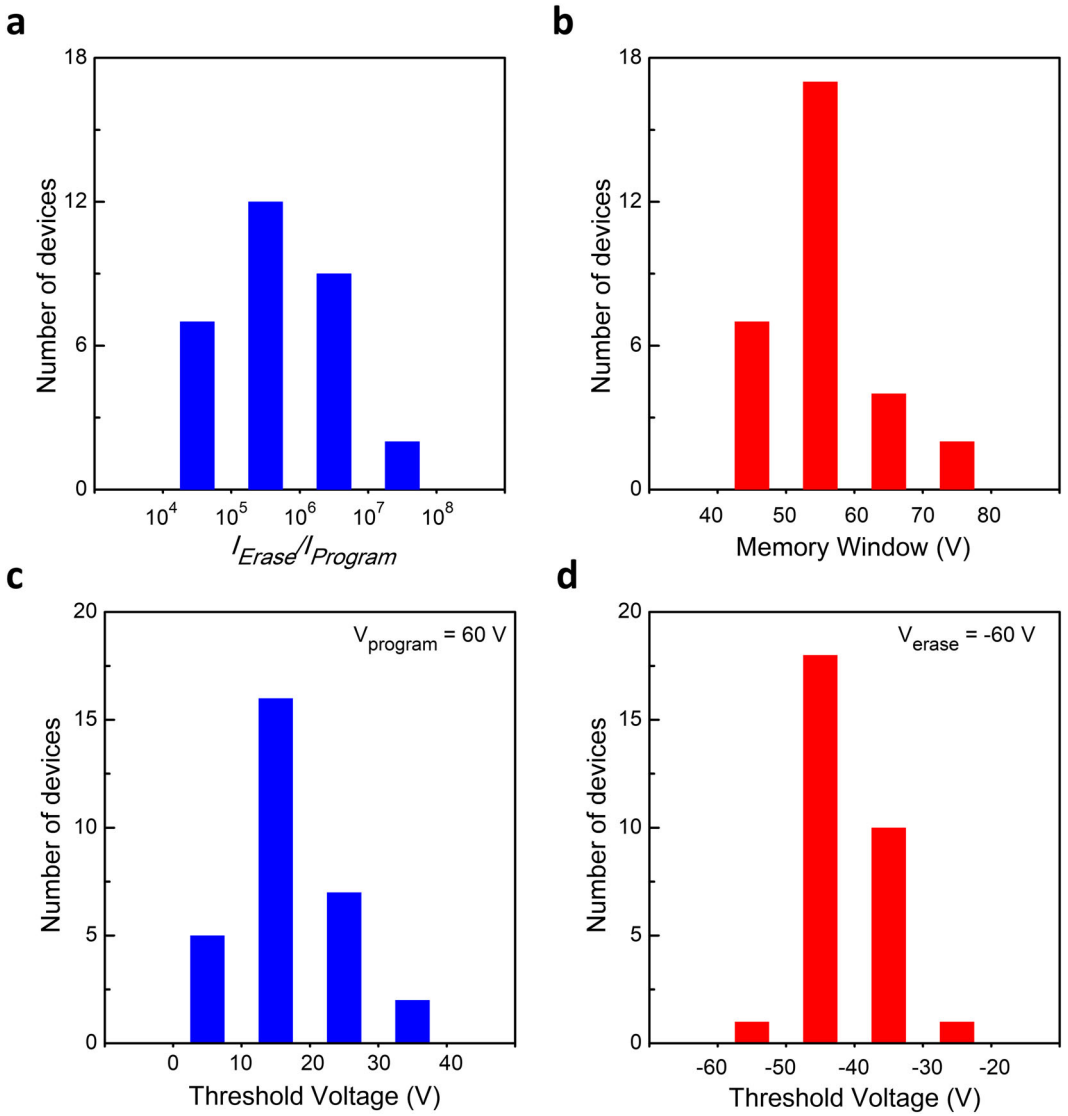

Fig. 2 Statistical analysis of the properties of 30 distinct MoS2 flash memories. Histogram showing the statistical distribution of **a** $I_{erase}/I_{program}$, **b** the memory window, (**c**) the threshold voltage at $V_{program} = 60$ V, and **d** the threshold voltage at $V_{erase} = -60$ V.

shift of V_{TH}. By enlarging the applied CG voltage V_{CG} bias in the P-memory, the degree of V_{TH} shift was controlled (Fig. S5). With greater applied V_G and thus energy band bending to inject more electron carriers into the floating gate, a larger shift of V_{TH} can be obtained.

To investigate the reproducibility and uniformity of the P-memory, we fabricated and characterized 30 devices. Figure 2a, b shows the statistical variation of the $I_{program}/I_{erase}$ ratio (average value $= 2.18 \times 10^6 \pm 4.77 \times 10^6$) and the memory window (average value $= 54.6$ V $\pm$ 7.80), respectively, in the 30 devices. The distribution shows that the devices with an $I_{program}/I_{erase}$ ratio $\geq 10^5$ comprise ~75% of the 30 devices. In addition, 17 devices have a memory window ranging from 50 V to 60 V, ~50% of the total. Figure 2c, d presents the V_{TH} distribution in the programmed state ($V_{program} = 60$ V) and erased state ($V_{erase} = -60$ V), respectively. The obtained average V_{TH} is 16.40 ± 8.25 V in the programmed state and −40.53 ± 5.87 V in the erased state. Details of the 30 P-memory device characteristics are given in Figs. S6 and S7.

Photoactivation effect on the P-memory

In the P-memory, the illumination light wavelength and intensity information can be stored as multilayered MoS_2- and PEDOT:PSS-polymer-generated photoactivated excess carriers (Fig. 3a, b). To study the photoactivation effect on the operation of the P-memory, we illuminated it with light (excitation wavelength $\lambda_{ex} = 405$ nm and incident

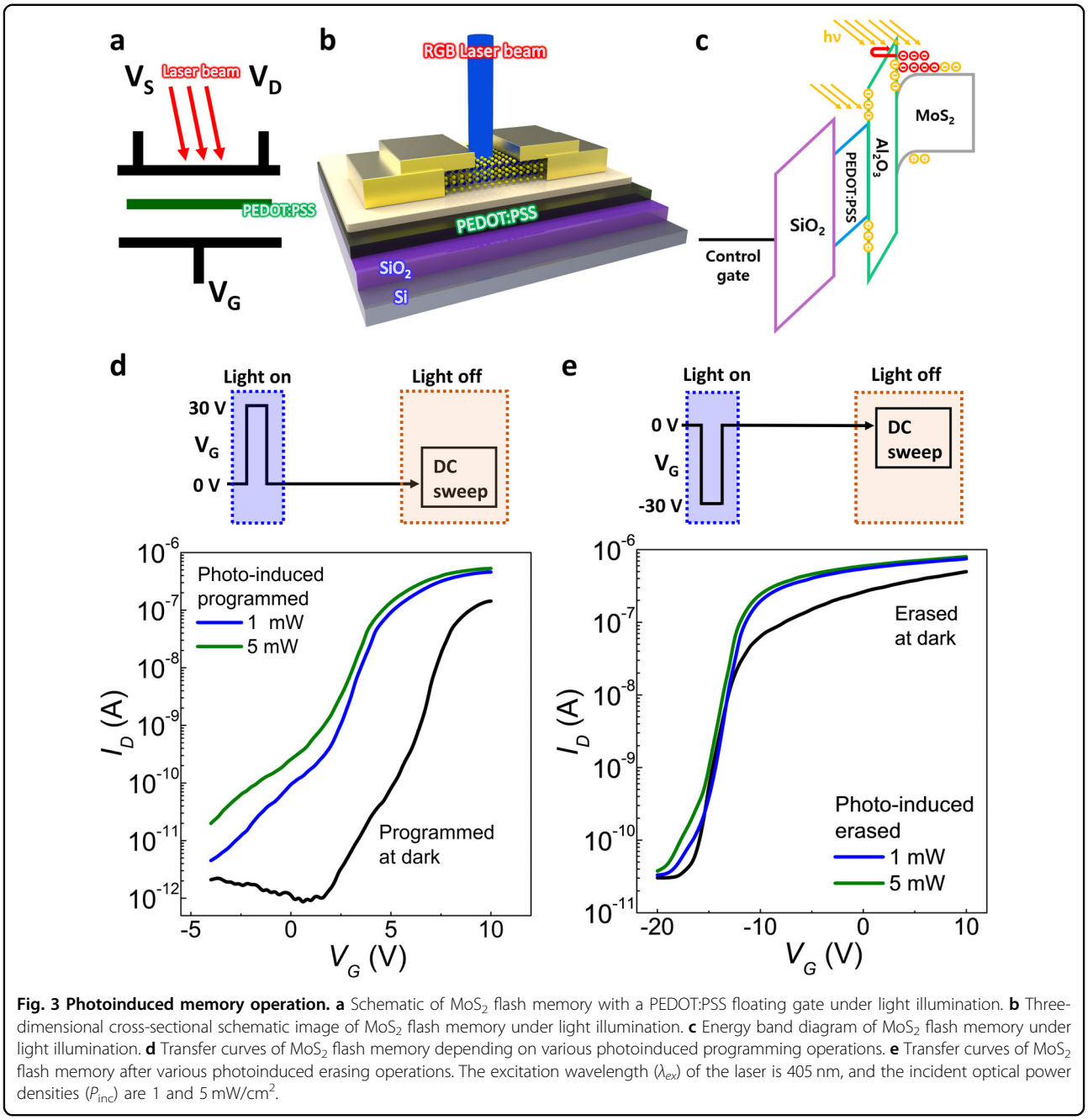

Fig. 3 Photoinduced memory operation. a Schematic of MoS_2 flash memory with a PEDOT:PSS floating gate under light illumination. **b** Three-dimensional cross-sectional schematic image of MoS_2 flash memory under light illumination. **c** Energy band diagram of MoS_2 flash memory under light illumination. **d** Transfer curves of MoS_2 flash memory depending on various photoinduced programming operations. **e** Transfer curves of MoS_2 flash memory after various photoinduced erasing operations. The excitation wavelength (λ_{ex}) of the laser is 405 nm, and the incident optical power densities (P_{inc}) are 1 and 5 mW/cm^2.

optical power densities $P_{inc} = 1$ and 5 mW/cm^2) during programming and erasing operations (i.e., photoinduced programming and photoinduced erasing, respectively). After the respective photoinduced programming and erasing operations, we performed a DC sweep of the P-memory to observe how light illumination influences the charge programming and erasing behavior (Fig. 3d, e). When programming in the dark state was activated, V_{TH} shifted to the positive side, showing $V_{TH} = 7.18$ V, whereas when the programming was operated under a light illumination of $P_{inc} = 1$ mW/cm^2, a smaller V_{TH} shift to $V_{TH} = 4.23$ V was observed. The observed phenomenon is attributable to the charge screening effect of the photogenerated excess carriers, preventing tunneling of electron carriers into the floating PEDOT:PSS layer (Fig. 3c). As a result, a smaller V_{TH} shift is induced by the programming under light illumination.

It was observed that a higher $P_{inc} = 5$ mW/cm^2 resulted in more photogenerated excess carriers that contributed to the screening effect, and thus, less of a

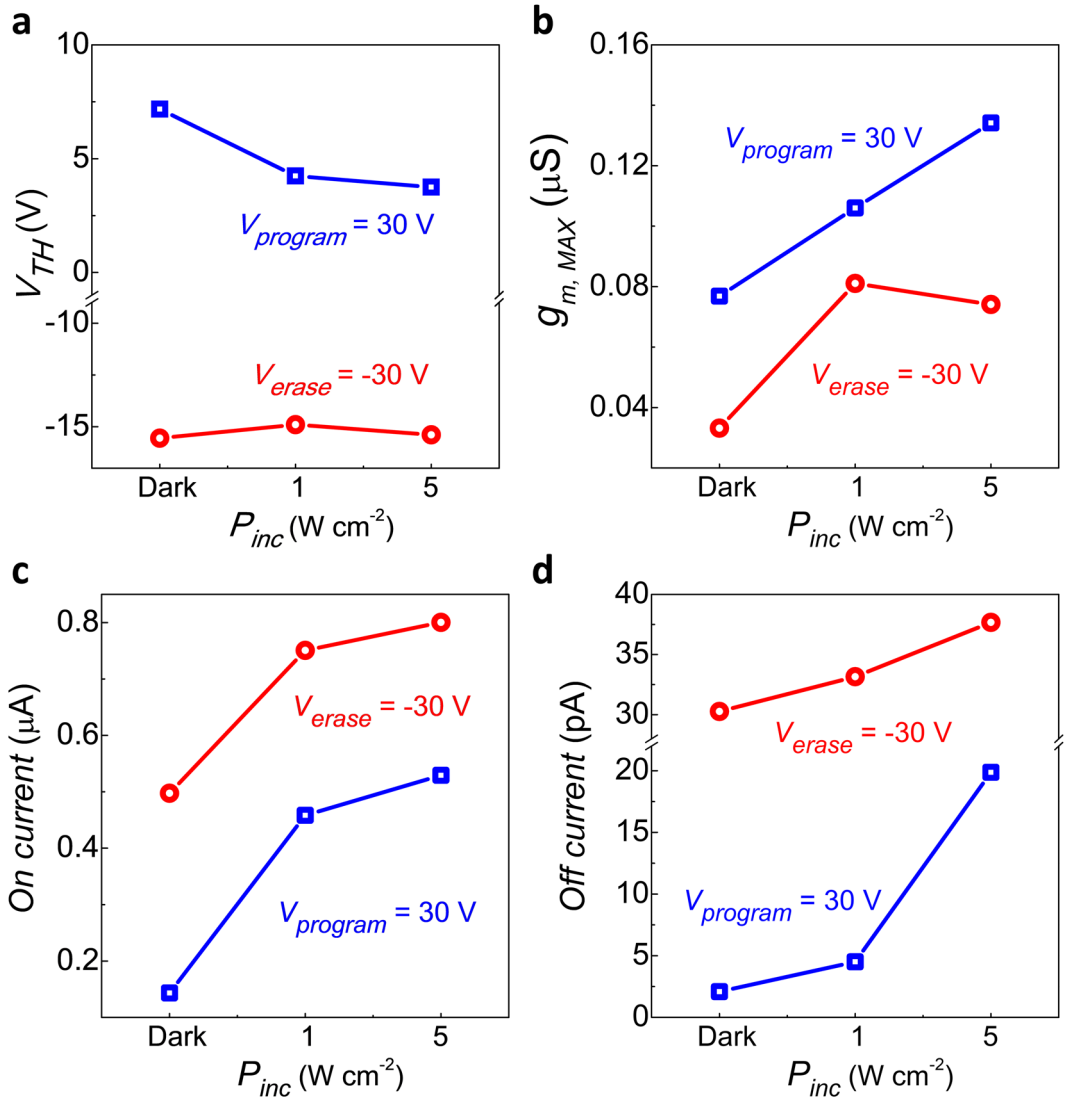

Fig. 4 Parameters extracted from photoinduced memory operation characteristics. Variation of the **a** threshold voltage (V_{TH}), **b** transconductance (g_m), **c** on-current, and **d** off-current of MoS_2 flash memory after various photoinduced programming/erasing operations. Red circles: erasing operation. Blue squares: programming operation.

V_{TH} shift ($V_{TH} = 3.75$ V) was observed compared to that of the programmed state under $P_{inc} = 1$ mW/cm^2 (Fig. 4a). We also investigated the light illumination effects during the erasing operation. Different from the photoinduced programming behavior, there was no V_{TH} change under the photoinduced erasing operation. Rather than a change in the V_{TH} shift, the photoinduced erasing operation resulted in an increase in the on-current in the switching-on region ($V_G > 10$ V). The observed increase in the on-current resulted from the slow decay of the generated photocurrent in the multilayered MoS_2, which supports previously reported phenomena in several studies[35–37]. The photoinduced programming and erasing behaviors under other light illumination ($\lambda_{ex} = 532$ and 638 nm) are shown in Figs. S8–11.

Photosensing memory operation

The photoinduced programming behavior with a change in V_{TH} shift allowed us to demonstrate multilevel photomemory applications that combine photodiodes with memory functions. During the programming operation, the P-memory is programmed differently depending on the presence or absence of light illumination and its light intensity, and thus, the degree of light exposure can be directly stored in the device. We illuminated blue light ($\lambda_{ex} = 405$ nm) onto the P-memory during the programming operation at $V_P = 30$ V, and we

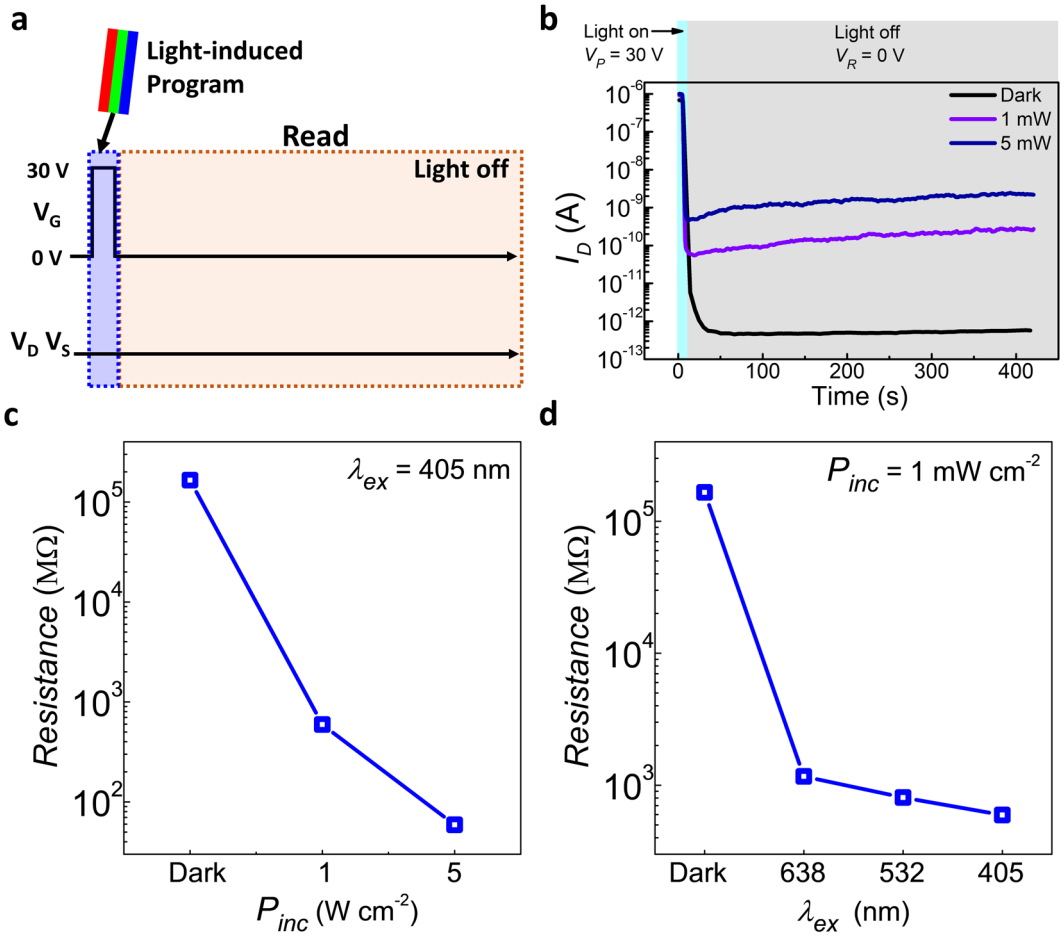

Fig. 5 Multilevel data storage characteristics of MoS2 flash memory under various photoinduced programming conditions. a Schematic diagram of measurement conditions depending on various light illumination under programming operation. **b** Multilevel retention characteristics of blue photoinduced programming with different light intensities at $V_D = 0.1$ V. **c** Average resistance in the retention measurement until 400 s at $V_D = 0.1$ V as a function of the incident power density (P_{inc}). **d** Average resistance in red, green, and blue retention measurements until 400 s at $V_D = 0.1$ V as a function of the excitation wavelength (λ_{ex}).

sequentially measured the read current at $V_R = 0$ V as a function of the photosensing retention time (Fig. 5a). The programming operation at $V_P = 30$ V in the dark resulted in the P-memory exhibiting $V_{TH} = 7.18$ V, which produced a current of 1–2 pA (I_R) at $V_R = 0$ V across the entire range of the photosensing retention time. On the other hand, the programming operation at $V_P = 30$ V under light illumination enabled the P-memory to provide a more than thousandfold higher I_R than that in the programmed state in the dark. The increased I_R with photoactivated programming was unchanged over the entire range of the photosensing retention time test (>400 s) (Fig. 5b). A higher light intensity resulted in a higher I_R with a lower resistance state of the P-memory (Fig. 5c). Under red and green light illumination (λ_{ex} = 532 and 638 nm), we also observed similar I_R increases. As expected, light with a lower wavelength enabled the P-memory to have a greater I_R increase with a lower resistance state, which potentially provides a classification operation according to the wavelength of light (Fig. 5d, Figs. S12 and S13).

Mechanically flexible device manufacturing of the P-memory

As the MoS_2 and PEDOT:PSS layers can be manufactured on top of flexible substrates owing to their excellent thermal budget (<200 °C), we next implemented flexible P-memory. A solution-based PI film was coated on a Si/SiO_2 substrate, and flexible P-memory was fabricated with the same process as for the rigid memory (Scheme 1). For the BDL and the TDL, we deposited 100 nm- and 80 nm-thick Al_2O_3, respectively. By delaminating the P-memory with the PI film from the substrate, we obtained flexible P-memory (Fig. 6a, b). Further details of the flexible P-memory fabrication are given in the Experimental Section. The flexible P-memory

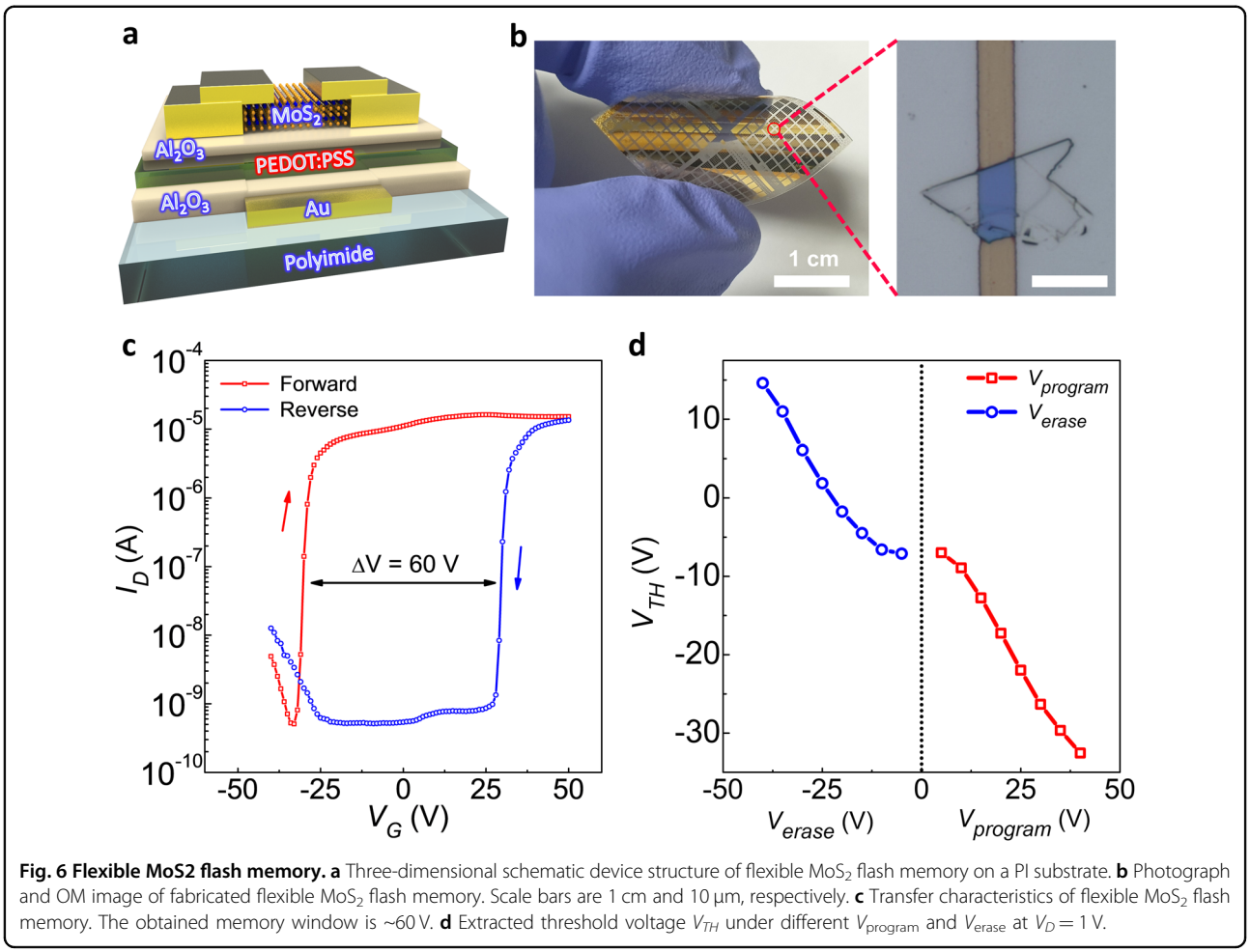

Fig. 6 Flexible MoS2 flash memory. a Three-dimensional schematic device structure of flexible MoS_2 flash memory on a PI substrate. **b** Photograph and OM image of fabricated flexible MoS_2 flash memory. Scale bars are 1 cm and 10 μm, respectively. **c** Transfer characteristics of flexible MoS_2 flash memory. The obtained memory window is ~60 V. **d** Extracted threshold voltage V_{TH} under different $V_{program}$ and V_{erase} at $V_D = 1$ V.

exhibited a large memory window, $\Delta V = 60$ V, obtained by programming/erasing the charges in the PEDOT:PSS floating layer, as we described in the P-memory operation part (Fig. 6c). The amount of V_{TH} shift can be controlled by the applied V_{CG} bias, in which a higher V_{CG} bias results in a larger V_{TH} shift toward the negative or positive side depending on V_{erase} and $V_{program}$, respectively.

To evaluate the mechanical durability of the flexible P-memory, we measured its *I-V* transfer characteristics before and after 1000 bending cycles at a bending radius of curvature $r = 5$ mm (Fig. 7a, Supporting Video 1). Details of the bending test are given in the Experimental Section. The flexible P-memory exhibited the same *I-V* transfer characteristics without any degradation or current change compared to those before the 1000 bending cycles. The observed excellent mechanical durability resulted from the layered structure of MoS_2 and the high flexibility of the PEDOT:PSS layer. To further investigate whether the flexible P-memory operated effectively after 1000 bending cycles, we performed a memory retention test (Fig. 7c). The current ratio of the programmed and erased states was above hundred for 8000 s of the retention measurement time.

Photosensing memory operation of the flexible P-memory

We also tested the photosensing retention time of the flexible P-memory after 1000 bending cycles (Fig. 7d). As expected, lower wavelength light illumination under the programming operation ($V_{program} = 35$ V) allowed the device to exhibit a higher I_R, so the flexible P-memory provided distinguishable resistance states depending on the light exposure properties. The abovementioned comprehensive memory tests confirmed that flexible P-memory exhibited no abnormality in the memory or photoactivated memory operations even after 1000 bending cycles.

Conclusions

In summary, we proposed P-memory that combines a layered MoS_2 thin-film transistor structure with a PEDOT:PSS floating gate. Owing to the virtues of the MoS_2 and PEDOT:PSS combined structure, the P-memory exhibited high performance, including a high switching current ratio $>10^7$, a large memory window >50 V, excellent endurance >1000 cycles, and a long retention time >2000 s. These were confirmed by

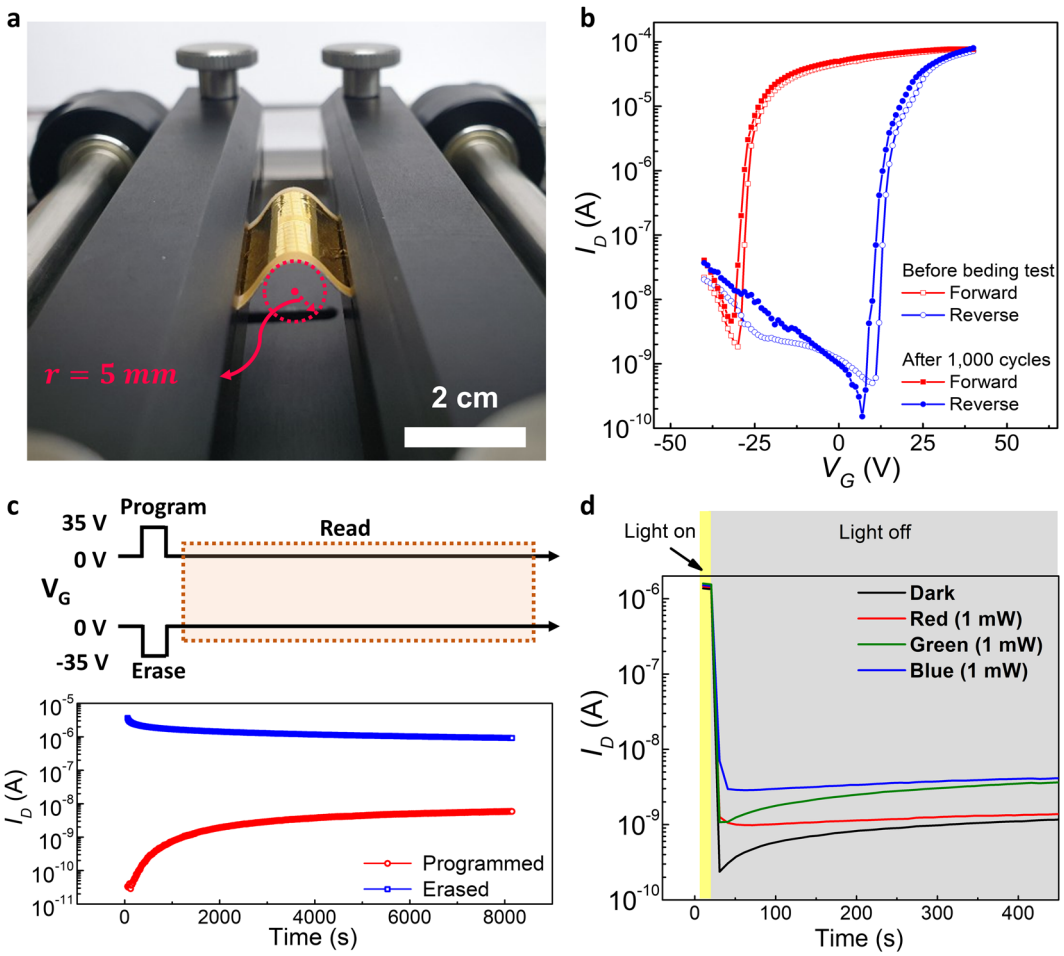

Fig. 7 Bending test and photoinduced operation of flexible MoS2 flash memory. a Photograph of MoS_2 flash memory bent in the bending tester. The bending radius and scale bar are 5 mm and 2 cm, respectively. **b** Comparison of transfer characteristics of MoS_2 flash memory before and after 1000 bending cycles with a 5 mm bending radius. **c** Schematic diagram of the retention measurement conditions and obtained retention characteristics of MoS_2 flash memory under a control gate pulse of ±35 V at $V_D = 0.1$ V for 8000 s after 1000 bending cycles with a 5 mm bending radius. **d** Multilevel retention characteristics of red, green, and blue photoinduced programming (638 nm, 532 nm, and 405 nm, respectively).

multiple device fabrication and characterization to evaluate the reproducibility and uniformity (>30 devices). We also achieved a photoactivated memory operation that combines photodiode and memory functions. Depending on whether light was illuminated, the P-memory provided a different degree of programming, and thus, the degree of light exposure could be stored directly in the device. Furthermore, we demonstrated flexible P-memory by manufacturing the device on a flexible PI substrate. The results indicated that the device maintained its multifunctional memory behavior even after 1000 bending cycles. Through comprehensive experiments, this study showed not only the memory characteristics of conventional floating-gate-based flash memory but also new versatility such as mechanical flexibility and photoactivated memory behavior. These reported results are expected to be useful guidelines in the development of new electronic device features using new nanomaterials.

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Conflict of interest
The authors declare no competing interests.

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References

1. Huang, M. et al. Multifunctional high-performance van der Waals heterostructures. *Nat. Nanotechnol.* **12**, 1148–1154 (2017).
2. Amani, M., Burke, R. A., Proie, R. M. & Dubey, M. Flexible integrated circuits and multifunctional electronics based on single atomic layers of MoS_2 and graphene. *Nanotechnology* **26**, 115202 (2015).
3. Zhao, M. et al. A multifunctional and highly stretchable electronic device based on silver nanowire/wrap yarn composite for a wearable strain sensor and heater. *J. Mater. Chem. C.* **7**, 13468–13476 (2019).
4. Zhang, L.-X. et al. Filter-Free Selective Light Monitoring by Organic Field-Effect Transistor Memories with a Tunable Blend Charge-Trapping Layer. *ACS Appl. Mater. Interfaces* **11**, 40366–40371 (2019).
5. Han, J., Wang, W., Ying, J. & Xie, W. Ambipolar organic thin-film transistor-based nano-floating-gate nonvolatile memory. *Appl. Phys. Lett.* **104**, 2_1 (2014).
6. Kim, J. J., Cho, B., Kim, K. S., Lee, T. & Jung, G. Y. Electrical characterization of unipolar organic resistive memory devices scaled down by a direct metal-transfer method. *Adv. Mater.* **23**, 2104–2107 (2011).
7. Khan, M., Bhansali, U.S. & Alshareef, H. N. High-performance non-volatile organic ferroelectric memory on banknotes. *Adv. Mater.* **24**, 2165–2170 (2012).
8. Cho, B., Song, S., Ji, Y., Kim, T. W. & Lee, T. Organic resistive memory devices: performance enhancement, integration, and advanced architectures. *Adv. Funct. Mater.* **21**, 2806–2829 (2011).
9. Khan, Y. et al. Inkjet-printed flexible gold electrode arrays for bioelectronic interfaces. *Adv. Funct. Mater.* **26**, 1004–1013 (2016).
10. Xu, J. et al. Biodegradable natural pectin-based flexible multilevel resistive switching memory for transient electronics. *Small* **15**, 1803970 (2019).
11. Zhang, P. et al. Structural Phase Transition Effect on Resistive Switching Behavior of MoS_2-Polyvinylpyrrolidone Nanocomposites Films for Flexible Memory Devices. *Small* **12**, 2077–2084 (2016).
12. Boni, G. A. et al. Multiple polarization states in symmetric ferroelectric heterostructures for multi-bit non-volatile memories. *Nanoscale* **9**, 19271–19278 (2017).
13. Lan, Y.-W. et al. Nonvolatile molecular memory with the multilevel states based on MoS_2 nanochannel field effect transistor through tuning gate voltage to control molecular configurations. *Nanotechnology* **31**, 275204 (2020).
14. Cabaret, T. et al. Electro-grafted organic memristors: Properties and prospects for artificial neural networks based on STDP. *14th IEEE Int. Conf. Nanotechnol.* **14**, 499–504 (2014).
15. van de Burgt, Y. et al. A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing. *Nat. Mater.* **16**, 414–418 (2017).
16. Sangwan, V. K. et al. Multi-terminal memtransistors from polycrystalline monolayer molybdenum disulfide. *Nature* **554**, 500–504 (2018).
17. Lu, X. et al. Large-area synthesis of monolayer and few-layer $MoSe_2$ films on SiO_2 substrates. *Nano Lett.* **14**, 2419–2425 (2014).
18. Yoo, H. et al. Chemical doping effects on CVD-grown multilayer $MoSe_2$ transistor. *Adv. Electron. Mater.* **4**, 1700639 (2018).
19. Ahn, C. et al. Low-temperature synthesis of large-scale molybdenum disulfide thin films directly on a plastic substrate using plasma-enhanced chemical vapor deposition. *Adv. Mater.* **27**, 5223–5229 (2015).
20. Kim, H. U. et al. Wafer-Scale and Low-Temperature Growth of 1T-WS_2 Film for Efficient and Stable Hydrogen Evolution Reaction. *Small* **16**, 1905000 (2020).
21. Zhou, J. et al. Synthesis of Co-Doped MoS_2 Monolayers with Enhanced Valley Splitting. *Adv. Mater.* **32**, 1906536 (2020).
22. Hong, X. et al. Ultrafast charge transfer in atomically thin MoS_2/WS_2 heterostructures. *Nat. Nanotechnol.* **9**, 682–686 (2014).
23. Zheng, W. et al. MoS_2 Van der Waals p–n Junctions Enabling Highly Selective Room-Temperature NO_2 Sensor. *Adv. Funct. Mater.* **30**, 2000435 (2020).
24. Safeer, C. et al. Room-temperature spin Hall effect in graphene/MoS_2 van der Waals heterostructures. *Nano Lett.* **19**, 1074–1082 (2019).
25. Feng, Z. et al. Chemical sensing by band modulation of a black phosphorus/molybdenum diselenide van der Waals hetero-structure. *2D Mater.* **3**, 035021 (2016).
26. Choi, S., Shaolin, Z. & Yang, W. Layer-number-dependent work function of MoS_2 nanoflakes. *J. Korean Phys. Soc.* **64**, 1550–1555 (2014).
27. Jadwiszczak, J. et al. MoS_2 Memtransistors Fabricated by Localized Helium Ion Beam Irradiation. *ACS Nano* **13**, 14262–14273 (2019).
28. Wang, C. Y. et al. 2D Layered Materials for Memristive and Neuromorphic Applications. *Adv. Electron. Mater.* **6**, 1901107 (2020).
29. Vélez, S. et al. Gate-tunable diode and photovoltaic effect in an organic–2D layered material p–n junction. *Nanoscale* **7**, 15442–15449 (2015).
30. Huang, Y. et al. Van der Waals coupled organic molecules with monolayer MoS_2 for fast response photodetectors with gate-tunable responsivity. *ACS Nano* **12**, 4062–4073 (2018).
31. Lee, J. J., Lee, S. H., Kim, F. S., Choi, H. H. & Kim, J. H. Simultaneous enhancement of the efficiency and stability of organic solar cells using PEDOT: PSS grafted with a PEGME buffer layer. *Org. Electron.* **26**, 191–199 (2015).
32. Zhang, B. et al. Work function and band alignment of few-layer violet phosphorene. *J. Mater. Chem. A* **8**, 8586–8592 (2020).
33. Cho, Y. et al. Design and Characterization of Semi-Floating-Gate Synaptic Transistor. *Micromachines* **10**, 32 (2019).
34. Jiménez-Molinos, F., Palma, A., Gámiz, F., Banqueri, J. & Lopez-Villanueva, J. Physical model for trap-assisted inelastic tunneling in metal-oxide-semiconductor structures. *J. Appl Phys.* **90**, 3396–3404 (2001).
35. Kufer, D. & Konstantatos, G. Highly sensitive, encapsulated MoS_2 photodetector with gate controllable gain and speed. *Nano Lett.* **15**, 7307–7313 (2015).
36. Zhang, Y. et al. Photothermoelectric and photovoltaic effects both present in MoS_2. *Sci. Rep.* **5**, 7938 (2015).
37. Zhang, W. et al. High-gain phototransistors based on a CVD MoS_2 monolayer. *Adv. Mater.* **25**, 3456–3461 (2013).