Article

Organic thermoelectric device utilizing charge transfer interface as the charge generation by harvesting thermal energy

Shun Kondo[1], Mana Kameyama[1], Kentaro Imaoka[1], Yoko Shimoi[2], Fabrice Mathevet[1,3], Takashi Fujihara[4], Hiroshi Goto[4], Hajime Nakanotani [1,5], Masayuki Yahiro[2] ✉ & Chihaya Adachi [1,5] ✉

We propose an organic thermoelectric device having a new power generation mechanism that extracts small-scale thermal energy, i.e., a few tens of milli-electronvolts, at room temperature without a temperature gradient. We demonstrate a new operating mechanism based on an organic thermoelectric power generation architecture that uses the charge separation capabilities of organic charge transfer (CT) interfaces composed of copper (II) phthalocyanine and copper (II) 1,2,3,4,8,9,10,11,15,16,17,18,22,23,24,25-hexadecafluoro-29H,31H-phthalocyanine as the donor and acceptor, respectively. With the optimized device architecture, values of open-circuit voltage V_{OC} of 384 mV, short-circuit current density J_{SC} of 1.1 μA/cm², and maximum output P_{max} of 94 nW/cm² are obtained. The temperature characteristics of the thermo-electric properties yield activation energy values of approximately 20–60 meV, confirming the low-level thermal energy's contribution to the power generation mechanism. Furthermore, from surface potential analysis using a Kelvin probe, we confirm that charges are generated at the CT interface, and the electrons and holes are diffused to the counter-electrodes with the aid of Fermi-level alignment between adjacent layers.

At present, there is an urgent need to use renewable and previously unused energy sources to realize a decarbonized society. Among these sources, research on thermoelectric devices that use waste heat is attracting growing interest. Normally, thermoelectric power generation[1] using the Seebeck effect assumes device use in high-temperature regions at 100 °C or more in combination with cold regions, i.e., under a temperature gradient condition, thus limiting the locations where these devices can be installed[2]. In particular, because the output improves as the temperature difference increases, it is difficult in principle to harvest energy from a heat source at approximately room temperature[3,4]. Furthermore, devices using inorganic semiconductors, e.g., bismuth telluride (Bi_2Te_3), have problems that

include toxicity and high costs because of their use of precious metals[5]. However, temperature difference-based power generation using organic semiconductors also has fundamental issues that must be resolved, including thicker film formation within array configurations and requirements for stable high-performance n-type semiconductor materials. Moreover, the basic thermoelectric performances of organic semiconductor devices are significantly inferior to those of inorganic semiconductor-based devices[6–8].

Here, we combined the charge separation ability at organic donor/acceptor interfaces, the diffusion ability of organic semi-conductor layers, and the carrier injection capability at organic het-erointerfaces driven by the alignment of the Fermi energy levels to

[1]Center for Organic Photonics and Electronics Research (OPERA), Kyushu University, 744 Motooka, Fukuoka, Japan. [2]Institute of Systems, Information Technologies and Nanotechnologies (ISIT), Materials Open Laboratory (MOL), 4-1 Kyudai-Shinmachi, Fukuoka, Japan. [3]Sorbonne Université, CNRS, Institut Parisien de Chimie Moléculaire (IPCM), Paris, France. [4]GCE Institute Inc., 2-1-6 Sengen, Tsukuba, Japan. [5]International Institute of Carbon Neutral Energy Research Center (I2CNER), Kyushu University, 744 Motooka, Fukuoka, Japan. ✉e-mail: yahiro@isit.or.jp; adachi@opera.kyushu-u.ac.jp

realize an undeveloped mechanism for organic thermoelectric power generators. We propose a device architecture in which charge separation is achieved from the charge-bound state of charge transfer (CT) excitons using low-level thermal energy, and the separated electrons and holes are then diffused and extracted to the opposing electrodes. To date, CT interactions have been studied actively in organic conductors, and high conductivity and superconducting properties have been obtained using various CT types[9–11]. In addition, in recent organic light-emitting diodes (OLEDs) and organic solar cells (OSCs), precise CT interactions at the organic layer interfaces have led to high performance in the charge recombination, exciton generation, and charge separation processes[12–17]. As another versatile CT device, we propose a new thermoelectric device type that harvests room temperature thermal energy, i.e., no temperature difference is required[18].

Results and discussion

Material search

First, we searched for donor and acceptor materials that were suitable for charge separation by low-level room temperature energy at the organic CT interface when using an ITO/donor/acceptor/Al device structure. Figure 1a shows the molecular structures of the materials used here: copper (II) phthalocyanine (CuPc), copper (II) 1,2,3,4,8,9,10,11,15,16,17,18,22,23,24,25-hexadecafluoro-29H,31H-phthalocyanine (F_{16}CuPc), and bisbenzimidazo[2,1-a:1',2-b']anthra[2,1,9-def:6,5,10-d'e'f']diisoguinoline−10,21-dione (PTCBI).

Figure 1b shows the current density–voltage (J–V) characteristics for (1) ITO (100 nm)/CuPc (50 nm)/PTCBI (50 nm)/Al (100 nm) and (2) ITO (100 nm)/CuPc (50 nm)/F_{16}CuPc (50 nm)/Al (100 nm) structures. In the CuPc/PTCBI device case, the current density when a reverse bias was applied was approximately two orders of magnitude lower than that when a forward bias was applied at 2.0 V. In

contrast, in the CuPc/F_{16}CuPc device, the current density under the reverse bias was approximately one order of magnitude higher than that obtained under the forward bias. This can be explained using the relative energy levels of the highest occupied molecular orbitals (HOMOs) and lowest unoccupied molecular orbitals (LUMOs) of the donor and acceptor layers, as shown in Fig. 1c. During forward biasing, charge carriers are injected from the electrodes in both devices, and application of an external electric field causes holes to move through the donor layer and electrons to move through the acceptor layer; this is followed by recombination near the interface between the two layers (①, ③). In contrast, in the CuPc/PTCBI device under reverse bias, charge injection becomes difficult because of the high injection barrier, which limits the current density (②). In the CuPc/F_{16}CuPc device, the HOMO (−5.0 eV) of the CuPc layer and the LUMO (−4.8 eV) of the F_{16}CuPc layer are close together and form a CT state at the interface[19,20]. Therefore, the CT state generated at the junction interface of the CuPc/F_{16}CuPc layers can be charge-separated by an external electric field (i.e., carrier generation occurs at the CT interface), allowing holes to move through the donor layer and electrons to move through the acceptor layer, and resulting in the current observed in the external circuit (④)[15]. This indicates that the CT states at the CuPc/F_{16}CuPc layer interface are capable of inducing high levels of charge generation at low energies. Additionally, we should note that CuPc and F_{16}CuPc are used frequently in OSCs and organic field-effect transistors[21,22]. Because these materials essentially have crystalline textures and form microcrystalline aggregates in their thin films, their relatively strong intermolecular van der Waals forces and the resulting dense intermolecular packing are believed to allow relatively easy charge carrier diffusion. Based on these unique J–V properties in the CuPc/F_{16}CuPc device, the combination of CuPc and F_{16}CuPc suggested that charge separation using low thermal energy is feasible.
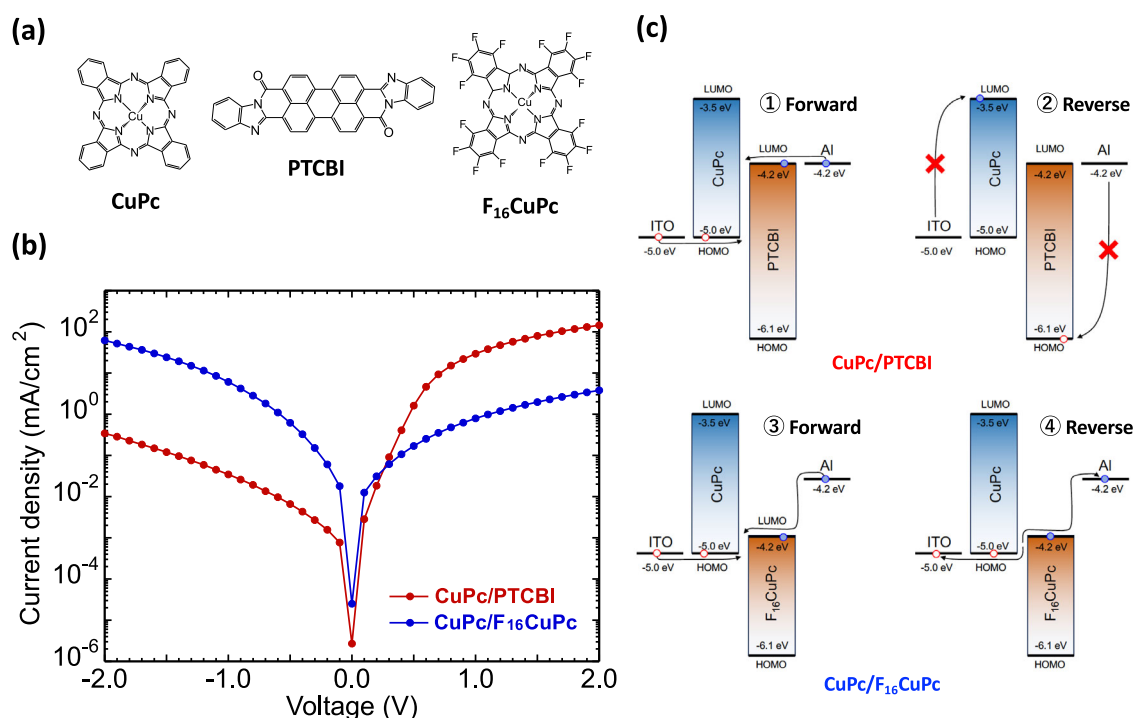

Fig. 1 | Current density–voltage (J–V) characteristics of CuPc/PTCBI and CuPc/F_{16}CuPc-based devices. a Chemical structures of CuPc, PTCBI, and F_{16}CuPc. **b** Current density–voltage (J–V) characteristics (under forward and reverse bias) of the ITO (100 nm)/CuPc (50 nm)/PTCBI (50 nm)/Al (100 nm) device (red) and the ITO (100 nm)/CuPc (50 nm)/F_{16}CuPc (50 nm)/Al (100 nm) device (blue). **c** Schematic energy diagram of the ITO/CuPc/PTCBI/Al device (① forward and ② reverse bias) and the ITO/CuPc/F_{16}CuPc/Al device (③forward and ④ reverse bias).
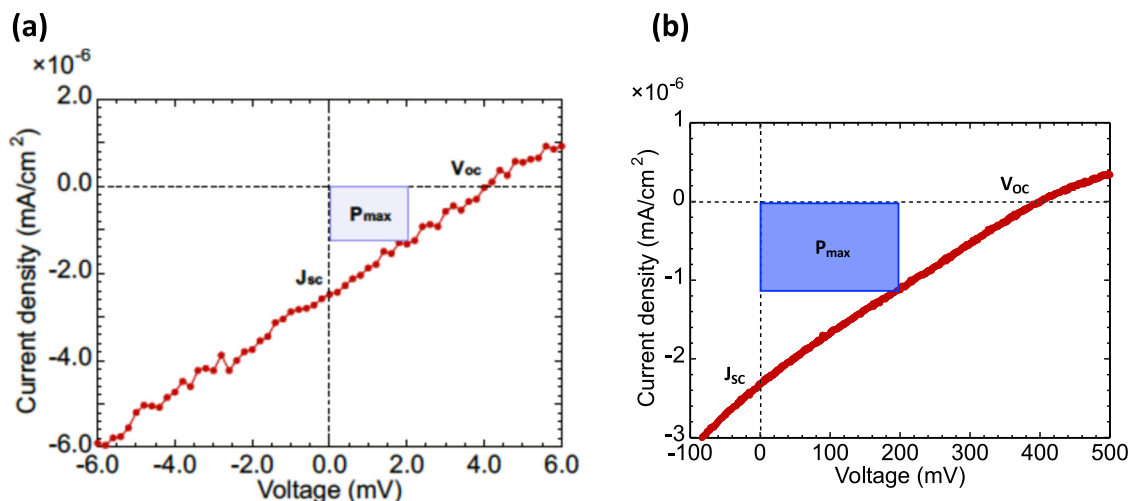
(a)

(b)

Fig. 2 | Thermoelectric behavior of CuPc/F_{16}CuPc-based devices. a Current density–voltage (J–V) characteristics of ITO (100 nm)/CuPc (30 nm)/F_{16}CuPc (70 nm)/Al (100 nm) device. V_{OC}, J_{SC}, and P_{max} correspond to the open-circuit voltage, short-circuit current, and fill factor (FF), respectively. **b** J–V characteristics of ITO (100 nm)/CuPc (30 nm)/F_{16}CuPc (20 nm)/C_{60} (40 nm)/BCP (20 nm)/Al (100 nm) device. Both devices were measured after air exposure.

Thermoelectric properties of a model element using CuPc/F_{16}CuPc

Following the J–V experiment, the thermoelectric properties of ITO (100 nm)/CuPc (30 nm)/F_{16}CuPc (70 nm)/Al (100 nm) structures were evaluated. The experiments were conducted at room temperature (~20 °C) in the dark, and the J–V characteristics were measured before and after atmospheric exposure to ascertain the effects of the atmosphere (Supplementary Fig. S1). After device fabrication, the devices were encapsulated using UV-curing resin in a glove box. When a small hole was made in the encapsulation and the device was exposed to air, its electrical characteristics decreased significantly; the reverse bias current density decreased by an order of magnitude, and the forward bias current density decreased by more than two digits. However, although the device current density was reduced by exposure to air, detailed measurement of the J–V characteristics under application of a more precise step voltage of 0.2 mV confirmed the presence of a very small electromotive force (EMF), as illustrated in Fig. 2a. The measured values were an open-circuit voltage (V_{OC}) of 4.2 mV, a short-circuit current density (J_{SC}) of 2.48×10^{-6} mA/cm², and maximum output (P_{max}) of 2.6 pW/cm², thus confirming that thermoelectric power generation occurred. Here, the significance of exposure to the atmosphere is believed to be that the pinholes (tiny conductive paths formed by Al penetration into organic layers during device fabrication) in the polycrystalline organic thin films become nonconductive because of oxidation or burn-out. Such pinhole issues, which are parasitic in organic thin-film devices, have been widely recognized in OLEDs[23–25].

CuPc/F_{16}CuPc/C_{60}/BCP configuration for higher performance

To improve the output from the thermoelectric device, the charge carriers that are dissociated by the CT complex interface must be transported efficiently through the organic layers and extracted to the electrodes. Therefore, as shown in Fig. 3, a fullerene (C_{60})[26] layer with good electron transport properties was introduced into the device. Note that the energy levels shown in Fig. 3 represent the levels where each layer exists independently without contact. The C_{60} layer LUMO (−4.3 eV) is shallower than that (−4.8 eV) of the F_{16}CuPc layer and was considered to be a barrier to charge transfer. However, given the good electron transport properties of C_{60}, we inserted the layer. Furthermore, 2,9-dimethyl-4,7-diphenyl-1,10-phenanthroline (BCP) was introduced because of the structure's similarity to that of OSCs[27]. Although it remains unclear why a BCP layer with a large energy gap is suitable

for use as an electron transport layer in OSCs, the BCP layer forms a gap state, providing an intermediate energy level between the HOMO and LUMO through which electron transport can occur (Fig. 3)[5,28]. It has been established previously that a BCP layer is effective in extracting electrons to electrodes[29]. Therefore, we fabricated an ITO (100 nm)/CuPc (30 nm)/F_{16}CuPc (20 nm)/C_{60} (40 nm)/BCP (20 nm)/Al (100 nm) device structure by combining the C_{60}/BCP bilayers with the CuPc/F_{16}CuPc layers. Figure 2b shows the resulting electrical characteristics of the device with significant increases in J_{SC} and V_{OC}, where $V_{OC} = 0.40$ V, $J_{SC} = 2.33 \times 10^{-5}$ mA/cm², and $P_{max} = 0.23$ nW/cm². In contrast, almost no power generation characteristics ($V_{OC} = 2$ mV, $J_{SC} = 0.38 \times 10^{-5}$ mA/cm²) were observed in the device with the ITO (100 nm)/CuPc (20 nm)/C_{60} (40 nm)/BCP (10 nm)/Al (100 nm) structure, in which the CuPc and C_{60} layers were attached directly (Supplementary Fig. S2a). Further, to confirm the origin of the electromotive force, we conducted a photo-irradiation experiment under AM1.5 using ITO (100 nm)/CuPc (110 nm)/F_{16}CuPc (45 nm)/C_{60} (40 nm)/BCP (20 nm)/Al (100 nm) as shown in Supplementary Fig. S2b. The V_{OC} did not change largely, i.e., $V_{OC} = 0.44$ V under dark and $V_{OC} = 0.40$ V under light irradiation. The nearly similar V_{OC} indicates that the origin of EMF in this device is located at the CuPc/F_{16}CuPc interface.

The thermoelectric performance is expected to improve with an increase in the environmental temperature. The red line in Fig. 4 shows the temperature variations of V_{OC} within the range from 20 to 90 °C, starting with 0.398 V at 20 °C; V_{OC} then increased with increasing temperature within the range from 20 °C to 70 °C before reaching the saturation characteristic of $V_{OC} = 0.651$ V at 70 °C. Slight jumps in V_{OC} were observed around 44 °C and 52 °C. These jumps may be related to the glass transition temperature of BCP ($T_g = 62$ °C)[30], and it is also possible that changes in the aggregation state of the film morphology may have affected its thermoelectric properties.

Now, we discuss the origin of the maximum value of $V_{OC} = 0.651$ V (at T ~ 70 °C). In this device, the energy difference between the HOMO of the donor layer (CuPc) and the LUMO of the acceptor layer (F_{16}CuPc) is maintained at ~200 meV to ensure that charge separation is possible with the thermal energy at room temperature, based on the Boltzmann distribution. Furthermore, to allow the charge carriers that dissociated from the CT interface to diffuse towards the counter-electrodes with as low a barrier as possible, CuPc, F_{16}CuPc, and C_{60} were selected because of the crystalline aggregation textures of their vacuum-deposited thin films. In addition, BCP, which has been
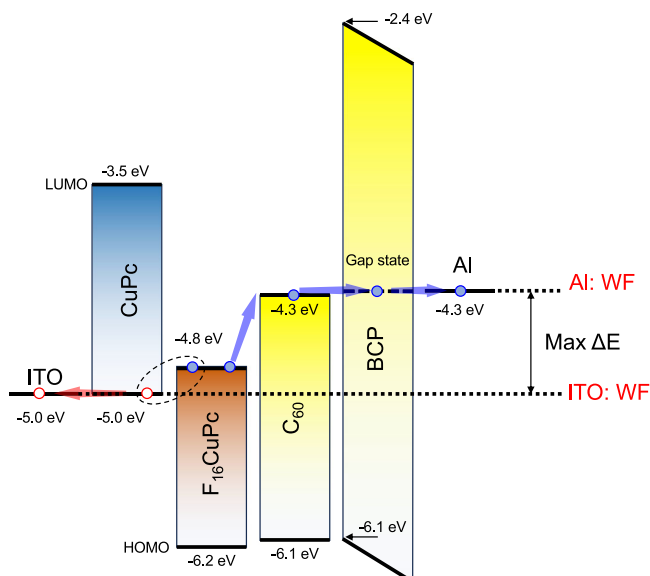
Fig. 3 | Schematic energy diagram of ITO/CuPc/F$_{16}$CuPc/C$_{60}$/BCP/Al device. The energy levels shown represent the levels when each layer exists independently without contact. The values of the HOMO levels of the work function (WF) and organic layers are taken from the literature. Due to the presence of GSP in a BCP layer, the energy levels are tilted.
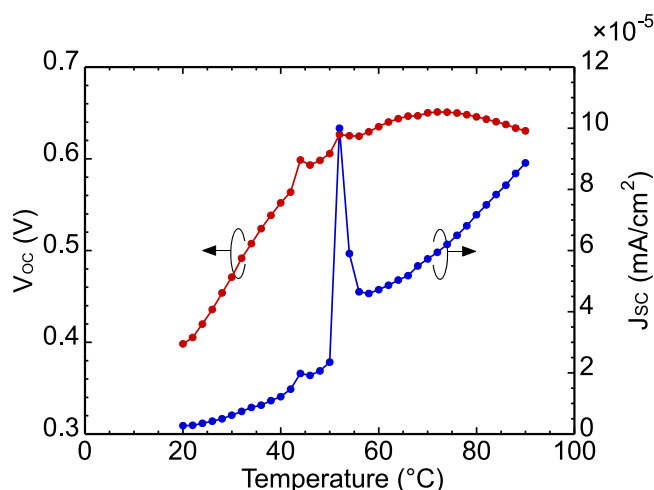

Fig. 4 | Temperature dependence of thermoelectric characteristics. The device is composed of ITO (100 nm)/CuPc (30 nm)/F$_{16}$CuPc (20 nm)/C$_{60}$ (40 nm)/BCP (20 nm)/Al (100 nm) device. Open-circuit voltage V_{OC} and short-circuit current J_{SC} are indicated by red and blue lines, respectively. Some irregular jumps would be ascribed to the glass transition temperature of a BCP layer.

confirmed to extract electrons to cathodes efficiently in OSCs, has been inserted between the C$_{60}$ layer and the Al cathode. Here, a large potential barrier of ~0.5 eV exists between the F$_{16}$CuPc and C$_{60}$ layers, as shown in Fig. 3. The mechanism by which the electrons overcome this barrier and are injected into the LUMO level of C$_{60}$, and then pass through the BCP layer to the Al electrode will be discussed later, based on the surface potential analysis. With this combination of materials, the energy difference between the level at which electrons conduct and the level at which holes conduct is approximately equal to the work function difference between ITO (−5.0 eV) and the Al electrode (−4.3 eV); this shows good agreement with the maximum V_{OC} = 0.651 V observed in the proposed device.

Next, we discuss the temperature variation of J_{SC} over the range from 20 to 90 °C (the blue line in Fig. 4). Similar to V_{OC}, J_{SC} increased

with increasing temperature, with a large spike being observed at ~52 °C, which is close to the glass transition temperature of BCP, and J_{SC} showed a current density that was ~33 times higher at 90 °C than at 20 °C. From this result, the activation energy was obtained from the Arrhenius plot (Supplementary Fig. S3a). Two approximately straight lines were obtained that were roughly bounded by the spike point at 52 °C: E_a = 59.8 meV in the 20–50 °C range and E_a = 20.4 meV in the 56–90 °C range. In contrast, in the CuPc/F$_{16}$CuPC device case (b), the Arrhenius plot was almost linear, and no clear inflection point was observed, resulting in E_a = 33.3 meV.

Here, we discuss the origins of the activation energy obtained in this study. In the proposed device, the following three activation energies can be assumed to form part of the thermoelectric behavior: (1) the energy required to overcome the disordered energy states of the organic layers when charge carriers' hopping occurs[31]; (2) the energy required to de-trap the charge carriers captured at trap sites in the organic thin-film layers; and (3) the energy required for dissociation of the CT-binding energy for free carrier generation[32–34]. Note here that the activation energy required to release and separate the CT states may not be the HOMO-LUMO gap energy between donor and acceptor; instead, it may be the lower-valued charge-pair binding energy. The activation energy values calculated from the results in this study are likely to be a combination of the three factors above. Among them, the first two energies affect the charge transport, while the last affects charge generation, and the charge-pair binding energy is the most noteworthy. According to the literature[32–34], this is the energy required to turn the charge pairs generated from the donor and acceptor into free carriers. In the range from 20 to 90 °C, the 33-fold increase in current density with the temperature change is expected to indicate increases in both charge transport and charge generation. Although it is difficult to assign the three different activation energies to each of the carrier generation and transport processes at present, it was confirmed that the device is driven by activation energies of 20–60 meV.

Tracing charge generation and transport processes by surface potential analysis

The Kelvin probe (KP) method measures the shift in the vacuum level caused by the difference between the work functions of the probe and the sample, and the KP method can be used to measure the potential distribution and charge distribution on a material's surface. In a previous study, Tanaka et al.[35] measured the surface potentials of materials used in OSCs and clarified the details of the carrier dynamics in thin films. In their study, no change was observed in the surface potential when C$_{60}$ was deposited on an ITO layer. However, when C$_{60}$ was deposited on a CuPc layer, a vacuum level shift of 0.3 eV over 50 nm from the CuPc layer was reported under dark conditions at room temperature. This shift was attributed to the diffusion of the charge-separated electrons at the CuPc/C$_{60}$ interface onto the C$_{60}$ surface. This indicates that the electrons in the HOMO of CuPc are thermally excited to the LUMO of C$_{60}$ at the CuPc/C$_{60}$ interface and the electrons then diffuse over 50 nm. However, as shown in Supplementary Fig. S2, because the thermoelectric properties of the device using the CuPc/C$_{60}$ interface are difficult to obtain, the CuPc/F$_{16}$CuPc/C$_{60}$ device configuration is essential. Therefore, we attempted to trace the charge generation and transport processes caused by thermal excitation using the same method for the CuPc/F$_{16}$CuPc/C$_{60}$/BCP layers.

When the data obtained by the KP method are analyzed, it is essential to distinguish whether the surface potential obtained is the result of spontaneous orientation polarization (SOP) or charge carrier diffusion, as depicted in Supplementary Fig. S4[35]. When molecules with an SOP nature are stacked, a giant spontaneous polarization (GSP) is formed at both ends of the film, as shown in Supplementary Fig. S4a. However, if charge injection from the electrode followed by successive charge diffusion to the surface occurs because of the Fermi-level
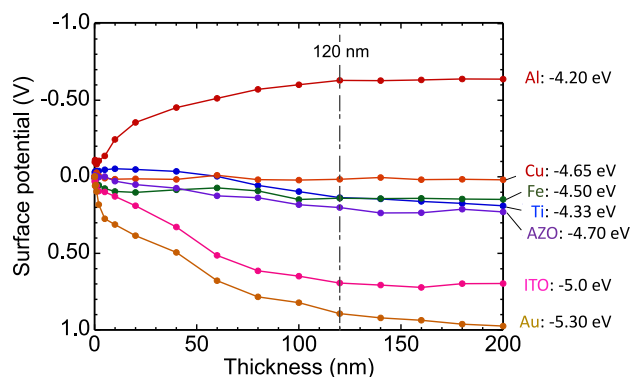
Fig. 5 | Thickness dependence of the surface potential of the CuPc layer (*X* nm) with different bottom electrode layers. The electrode materials of Au, ITO, AZO, Ti, Fe, Cu, and Al were used. When the electrode work function values are closed to the Fermi energy (−4.5 eV) of a CuPc layer, almost no significant change of the surface potentials was observed. On the other hand, Al (−4.20 eV) and ITO (−5.0 eV) and Au (−5.3 eV) resulted in a large appearance of the surface potential shift to negative and positive, respectively, indicating the charge carrier injection for the electrodes into the CuPc layers due to the Fermi energy alignment.
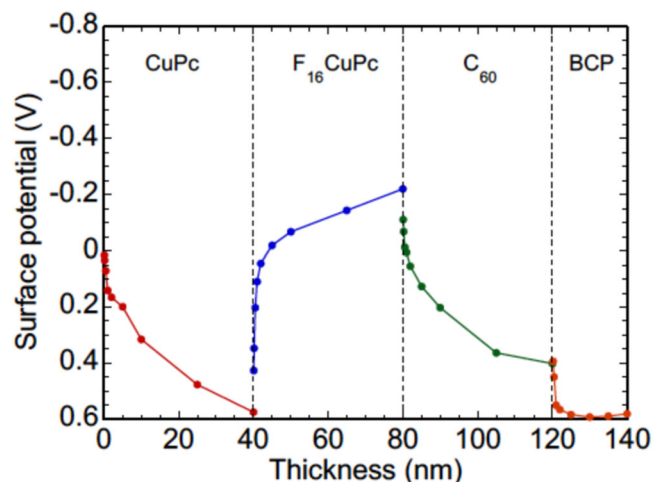

Fig. 6 | Surface potential analysis by Kelvin probe method and the estimated energy-level diagram. Change of surface potential in ITO (100 nm)/CuPc(40 nm)/F_{16}CuPc (40 nm)/C_{60} (40 nm)/BCP (20 nm) layers as measured by the Kelvin probe method. At each data point, after the deposition of the organic layers, the surface potential was measured successively by transferring the substrate from the deposition chamber into a measurement chamber without breaking the vacuum.
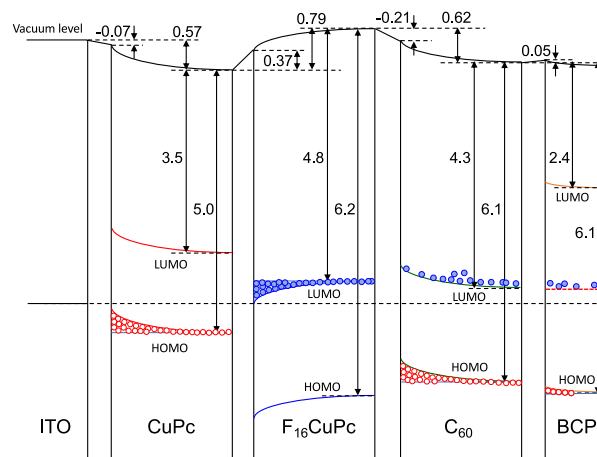
alignment, it provides a similar surface potential gradient, as shown in Supplementary Fig. S4b. Here, the potential difference due to the SOP is characterized by the fact that it increases linearly and without saturation in proportion to the increasing film thickness. However, in the case where the surface potential change is caused by charge injection, there is a limit to the diffusion region, as per the example involving C_{60} reported by Tanaka et al.[35]. Beyond that range, no surface potential change can be observed. After considering the characteristics above, we carefully checked for the presence or absence of SOP in the materials that constitute the device and also observed the charge carrier distribution within the stacked structure.

Figure 5 shows the potential change of the CuPc layer over thicknesses of up to 200 nm when formed on various electrode materials[36–38]. In this experiment, we focused on the correlation between the electrode work function and the potential change on the CuPc layer surface, along with the appearance of the change in surface potential of the CuPc layer in the thickness direction. Interestingly, the CuPc layer's potential change is strongly dependent on the work function of the electrode materials. A deeper electrode work function leads to a larger positive value for the potential change of a CuPc layer, whereas a shallower electrode work function leads to a larger negative value of this change. The boundary at which the positive and negative potential change switches is observed when the Cu, Fe, Ti, and AZO electrodes are used, and the boundary value is close to the Fermi level of a CuPc layer (4.5 eV)[37]. Interestingly, the electron injection also occurs effortlessly, overcoming the Al work function (−4.2 eV) and CuPc LUMO (−3.5 eV) barriers ($\Delta E = 0.7$ eV) to match the Fermi level. This indicates that electrons are injected from the electrode when the electrode's work function is shallower than the CuPc layer Fermi level, and holes are injected from the electrode by thermal excitation when the work function is deeper, as shown in Fig. 5. This means that charge injection occurs on the organic layer side to match the Fermi level at the electrode/CuPc layer interface. Furthermore, the film thickness dependence in Fig. 5 indicates that the range for the surface potential change of the CuPc layer is ~120 nm. This behavior is different from that of the SOP, where the potential gradient varies linearly without saturation in proportion to the film thickness. Therefore, the CuPc layer, similar to the C_{60} layer, does not exhibit SOP, and the charges are injected into the CuPc layer and diffuse over a distance of ~120 nm from the electrode contact interface.

The same idea is also applicable to the nonpolar materials of the F_{16}CuPc and C_{60} layers. Therefore, it was found that no SOPs occurred

in CuPc, F_{16}CuPc, and C_{60}, and that the potential changes appear as a result of charge movement within the thin films. Based on this conclusion, we then analyzed the charge distributions within the stacked structures.

Charge distribution in stacked structures

Figure 6 shows the potential changes on the thin-film surfaces when 40-nm-thick layers of each of CuPc, F_{16}CuPc, and C_{60} and a 20-nm-thick BCP layer are stacked in turn on the ITO substrate, and Fig. 7 shows the energy-level diagram based on the KP method results. The results show that there are positive and negative potential changes in the CuPc, F_{16}CuPc, and C_{60} layers, and there is almost no potential change in the bulk BCP layer.

First, we discuss the movement of the holes. As mentioned earlier, because a junction is formed at the ITO/CuPc interface to match the Fermi levels, a gradual negative potential forms from the CuPc/

Fig. 7 | Estimated energy diagram of the ITO (100 nm)/CuPc (40 nm)/F_{16}CuPc (40 nm)/C_{60} (40 nm)/BCP (20 nm) layers. The vacuum level shift at each layer and interface was carefully depicted with the HOMO and LUMO energy levels. In the case of the BCP layer, the expected mid-gap states were shown as the red dotted line.

F_{16}CuPc interface towards the ITO electrode. Therefore, it is understood that the holes that separated at the CT interface diffuse toward the ITO electrode, as depicted in Fig. 7.

In contrast, the movement of the electrons is rather more complex. First, the negative potential change observed in the F_{16}CuPc layer is not due to SOP, which means that the observed change in surface potential indicates that the electrons that separated at the CT interface have certainly reached the F_{16}CuPc/C_{60} surface. In other words, the electrons that were separated at the CuPc/F_{16}CuPc interface filled the upward potential gradient of the F_{16}CuPc layer and reached the C_{60} layer interface. Second, we explain the potential change in the C_{60} layer. As shown in Supplementary Fig. S5, in the ITO/CuPc/F_{16}CuPc/C_{60} film structure, the first 1 nm region at the C_{60} layer represents the vacuum level shift of the depletion layer at the F_{16}CuPc/C_{60} interface, and if this voltage drop is excluded, then a potential change of +0.45 eV occurs over 40 nm. However, as shown in the ITO/C_{60} film, C_{60} essentially shows no potential change when it is deposited on an ITO electrode, thus indicating zero SOP formation. Therefore, the 0.45 eV energy-level gradient in the C_{60} layer is thought to be induced by the accumulation of electrons localized at the F_{16}CuPc/C_{60} interface (Fig. 7). This is believed to have occurred to match the Fermi level at the F_{16}CuPc/C_{60} interface. In other words, this 0.45 eV change in the potential is considered to correspond to the increase in V_{OC} obtained by the insertion of the C_{60} layer. In fact, V_{OC}, which was 0.004 V at room temperature for the ITO/CuPc/F_{16}CuPc/Al device (Fig. 2a), improved to reach 0.40 V at 20 °C for the ITO/CuPc/F_{16}CuPc/C_{60}/BCP/Al device (Fig. 2b).

Furthermore, in the BCP layer, with the exception of the first vacuum level shift of the depletion layer, almost no potential change was observed in the bulk, whereas an original BCP layer had a GSP of 32 mV/nm. In a previous study, it was reported that the accumulation of photo-induced charge carriers with the opposite sign to the electric field of the GSP will cause the GSP to disappear or decrease[39,40]. Therefore, it would be possible for the GSP to also be canceled in this device if electrons diffuse toward the BCP layer. Based on the discussion above, it can be explained that the electrons generated at the CuPc/F_{16}CuPc interface can diffuse into the C_{60} and BCP layers, as shown in Fig. 7. Further, it has been reported that BCP layers form midgap states between the HOMO and LUMO levels, leading to the extraction of electrons into the electrode[41]. Therefore, it was confirmed that our device architecture outputs an EMF by harvesting ambient heat under dark conditions at room temperature, even without a temperature gradient.

Improvement of device characteristics through film thickness optimization

Analysis using the KP method reveals the following behavior from the carriers in the stacked thin films; thermal charge separation occurs at the CuPc/F_{16}CuPc interface, and holes then drift through the CuPc layer and reach the ITO electrode side. In addition, electrons diffuse in the F_{16}CuPc layer and accumulate at the interface with the C_{60} layer; then, to match the Fermi level, the electrons overcome the potential barrier at the F_{16}CuPc/C_{60} interface and flow further through the C_{60} and BCP layers to reach the Al cathode. Although the mechanism by which the electrons overcome the potential barrier between F_{16}CuPc and C_{60} remains unclear and is debatable, the matching force of the Fermi energies between the F_{16}CuPc and C_{60} layers, where the electron overflow reached the interface, would promote electron injection into the C_{60} layer. However, the decreasing potential curve toward the BCP layer indicates that the electrons injected into the C_{60} layer remain at the F_{16}CuPc/C_{60} interface.

The thickness dependence of the CuPc layer on the KP indicates that the holes can move by up to approximately 120 nm. This implies that the hole diffusion lengths are comparable to this value. Therefore, we examined the CuPc layer's thickness dependence and although some variation was observed, many devices showed their best
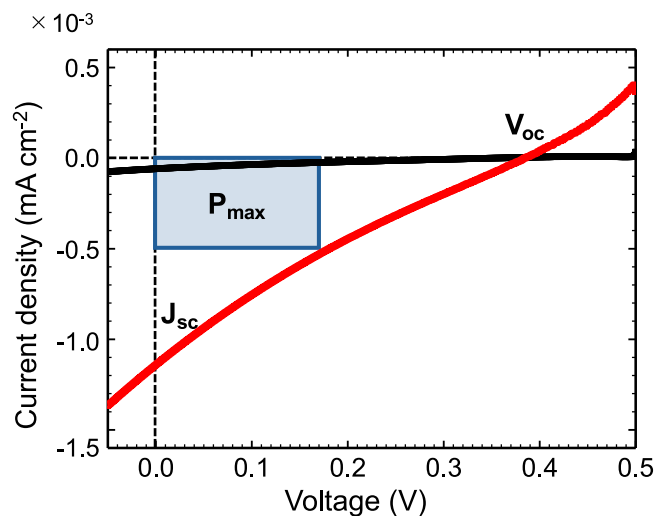

Fig. 8 | Thermoelectric characteristics of ITO/CuPc/F_{16}CuPc/C_{60}/BCP/Al (100 nm) device. Current density–voltage (J–V) characteristics of ITO (100 nm)/CuPc (110 nm)/F_{16}CuPc (320 nm)/C_{60} (20 nm)/BCP (20 nm)/Al (100 nm) device with advanced organic layer thicknesses (red line). The initial device performance of the ITO (100 nm)/CuPc (30 nm)/F_{16}CuPc (20 nm)/C_{60} (40 nm)/BCP (20 nm)/Al (100 nm) structure is also included (black line).

characteristics at -150 nm, which correlated well with the KP results (Supplementary Fig. S6). However, the F_{16}CuPc layer showed a tendency to improve the performance with increasing film thickness, thus indicating that no strong charge traps would be formed in the F_{16}CuPc film and that the electrons diffuse toward the C_{60} interface. In this study, film thicknesses of up to 200 nm were examined, and the maximum value was observed at 200 nm. Furthermore, the 20-nm-thick C_{60} layer showed higher characteristics than the 40-nm-thick film, indicating that the C_{60} layer is not involved in charge separation and that as the film becomes thinner, the resistance to electron transport decreases.

Finally, as shown in Fig. 8, the best thermoelectric performance of $V_{OC} = 384$ mV, $J_{SC} = 1.1$ μA/cm^2, and $P_{max} = 94$ nW/cm^2 was obtained for the CuPc (180 nm)/F_{16}CuPc (320 nm)/C_{60} (20 nm)/BCP (20 nm) device, with results that were more than -100 times better than those of the initial device. Although the device characteristics were improved by film thickness optimization, the fill factor is still insufficient, and an increase in shunt resistance based on pinholes and other factors and reduced series resistance in the carrier path are required to improve it. In addition, suppression of carrier recombination at the p-n junction offers an approach to improve the output performance[42]. Moreover, our device showed an S-shaped J–V curve in the fourth quadrant, as often observed in OSCs, and this curve has been induced by the electric field distribution caused by carrier accumulation on the inside of the device[43]. This curve may be consistent with the fact that the carrier accumulation in each layer, as discussed above, forms space charge, and this results in the S-kink appearance in the J–V characteristics. In addition, we would like to improve the device performance further by controlling the molecular orientation in phthalocyanine layers and also actively controlling the grain boundaries that originate from the polycrystalline nature of these films[44].

In this study, we have constructed a new type of thermoelectric device that does not require a temperature gradient by using an organic CT interface with carrier transport layers. Rather than photoexcitation, which absorbs energies of several electronvolts at the CT interface in OSCs, we have established a mechanism that enables charge separation via thermal excitation with an energy of several 10 meV. As the donors and acceptors enabled charge generation, we observed a primitive small EMF of $P_{max} = 2.6$ pW/cm^2 for the ITO/CuPc/

$F_{16}CuPc$/Al layer combination. Furthermore, by inserting C_{60} and BCP layers into the basic CuPc/$F_{16}CuPc$ structure, P_{max} was improved to -0.23 nW/cm². Finally, by optimizing the thickness for each layer, P_{max} was significantly improved to -100 nW/cm². We believe that a higher current density can be realized easily by increasing the device area, which is an unusual feature of organic materials.

With regard to the device's operating mechanism, to verify the origin of the EMF, we analyzed both the temperature characteristics and the surface potential properties. We found that V_{OC} increased with increasing temperature before finally saturating at 0.65 V, which resulted from the work function difference between the ITO and Al electrode layers. In addition, J_{SC} also improved with increasing temperature, and the current value at 90 °C was found to have increased by a factor of approximately 33 when compared with that at 20 °C. The surface analysis performed by the KP method showed that holes generated at the CuPc/$F_{16}CuPc$ interface diffused through the CuPc layer, while electrons diffused through the $F_{16}CuPc$ layer to overcome the energy barrier at the $F_{16}CuPc$/C_{60} interface, as driven by the Fermi-level alignment, and diffused successively through the C_{60} and BCP layers to the Al cathode. Further investigations of the interface phenomena and optimization of the materials used are expected to improve the thermoelectric performance in future work.

Methods

Device fabrication
In this study, thermoelectric devices with four 2×2 mm² pixel elements with ITO bottom electrodes were fabricated on a glass substrate (Atsugi Micro Co., Ltd., Japan) with outer dimensions of 25×25 mm². They were ultrasonically cleaned using detergent and organic solvents (acetone and ethanol) and dried via exposure to isopropyl alcohol vapor. The devices were then ultraviolet (UV)-treated under an ozone atmosphere and baked on a hot plate at 200 °C. Organic semiconductor thin films and Al for use as the top electrode layer were deposited by resistance heating vacuum evaporation using a vacuum evaporation system (ALS Co., Ltd., Japan) at a rate of 1 Å/s under vacuum conditions of 2.0×10^{-4} Pa or less to fabricate stacked devices. The organic semiconductors and Al top electrodes were patterned using a metal shadow mask. After deposition, the devices were moved into a glove box (MBRAUN Inc.) in which both oxygen and moisture were controlled to less than 0.1 ppm and were then can-sealed with partially engraved glass using UV-curing resin (Nagase Chem-teX Corp.).

Current–voltage characteristic measurement
The current density-voltage (J–V) characteristics of the fabricated devices were measured using a source measurement unit (B2912A, Keysight Technology Inc.). The measurement conditions, e.g., the scan speed, were varied depending on the samples. The typical scan range was from −2 V to 2 V with a voltage step of 0.1 V and a measurement interval of 30 s. The fabricated device, which was sealed in a glove box, was set in a measurement holder installed in a measurement box covered in all directions by a steel plate and electromagnetically shielded, and thus, all measurements were carried out in completely dark room conditions.

Temperature dependence of current density–voltage measurements
The temperature dependence of the thermoelectric characteristics was evaluated using a constant temperature and humidity chamber (LHL-114, Espec Inc.) and a digital multimeter (DMM; 34465 A, Keysight Inc.). The measured elements were placed in element holders (System Engineering Corp.) and were wrapped in aluminum foil to eliminate nonthermal influences, e.g., light and electromagnetic waves, as far as possible. The measurements were conducted from 20 °C to 90 °C with steps of 2 °C.

Surface potential measurement
Unpatterned ITO or glass substrates were used to perform the KP experiment. The KP measurement system was composed of a surface potential measurement room and an organic molecular deposition room, which allowed consistent measurements to be performed in a vacuum environment without exposing the sample to the external atmosphere. The windows of the deposition and measurement sections were covered with aluminum foil to shield the laboratory from external light. A Kelvin probe (UHVKP020, KP Tech. Ltd.) was used as the surface potential measurement instrument, and the deposition and measurement processes were performed after the vacuum was reduced below 2.0×10^{-4} Pa.

Data availability
The data supporting the findings of this study are included within the article and its Supplementary Information.

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Author contributions

C.A. proposed the basic idea and concept. C.A. and M.Y. supervised this project. C.A., M.Y., and S.K. designed the fundamental experiments and provided fundamental contributions. S.K. and M.K. carried out the experiment and contributed to the understanding of the operation mechanism. K.I. and Y. S. also contributed to device fabrication and analysis. F.M., T.F., H.G., and H.N. analyzed the data and contributed to the understanding operation mechanism. C.A., M.Y., and S.K. mainly wrote the manuscript, and all members contributed to writing this manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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Correspondence and requests for materials should be addressed to Masayuki Yahiro or Chihaya Adachi.

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