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High drain field impact ionization transistors as ideal switches

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Baowei Yuan[1,2], Zhibo Chen[1], Yingxin Chen[1], Chengjie Tang[1], Weiao Chen[1], Zengguang Cheng[2], Chunsong Zhao[3], Zhaozhao Hou[3], Qiang Zhang[3], Weizhuo Gan[3], Jiacheng Gao[3], Jiale Wang[3], Jeffrey Xu[3], Guangxi Hu[1], Zhenhua Wu[4], Kun Luo[4], Mingyan Luo[5], Yuanbo Zhang[5], Zengxing Zhang[2], Shisheng Xiong[1], Chunxiao Cong[1], Wenzhong Bao[2], Shunli Ma[2], Jing Wan[1] ✉, Peng Zhou[2] ✉ & Ye Lu[1] ✉

Impact ionization effect has been demonstrated in transistors to enable sub-60 mV dec^{-1} subthreshold swing. However, traditionally, impact ionization in silicon devices requires a high operation voltage due to limited electrical field near the device drain, contradicting the low energy operation purpose. Here, we report a vertical subthreshold swing device composed of a graphene/silicon heterojunction drain and a silicon channel. This structure creates a low voltage avalanche impact ionization phenomenon and leads to steep switching of the silicon-based device. Experimental measurements reveal a small average subthreshold swing of 16 μV dec^{-1} over 6 decades of drain current and nearly hysteresis-free, and the operating voltage at which a vertical subthreshold swing occurs can be as low as 0.4 V at room temperature. Furthermore, a complementary silicon-based logic inverter is experimentally demonstrated to reach a voltage gain of 311 at a supply voltage of 2 V.

To avoid the impact of noises and variations in the real world, an electronic device is typically required to have at least ~4 orders of magnitude on/off ratio to be used as a reliable switch in the modern electronic chips for the Boolean logic computation. This essentially mandates the threshold voltage (V_{TH}) of the field-effect transistors (FETs) device to be at least four times of its subthreshold swing (SS). At the same time, the power consumption of the chip is proportional to the power supply voltage (V_{DD}), a quantity that has to be larger than V_{TH}. Therefore, the ever-increasing demand of the chips' performance improvement and power reduction co-optimization ultimately demands the reduction of V_{TH} at even lower off-state current (I_{off}), i.e., it desires an ideal switch with minimum value of SS. Unfortunately, Boltzmann distribution of carriers in conventional metal-oxide-semiconductor FETs (MOSFETs) sets a thermionic limit of SS to be 60 mV dec^{-1} at room temperature[1], and breaking this limit becomes inevitable for future chip technology development.

Numerous transistor architectures have been proposed at this front. For example, tunneling FETs (T-FETs)[2–4] relying on the quantum tunneling effect instead of thermal emission of carrier is a promising choice. However, the on-state current (I_{on}) of such a device is low due to its band-to-band tunneling mechanism. Negative capacitance FETs (NC-FETs)[5–7] use the dipole effect in ferroelectric material as the gate oxide layer to effectively reduce the gate voltage. However, the ferroelectric material is prone to polarization in the electric field, which restricts the low SS operation only in low-speed applications and not suitable for the gigahertz switching in most of today's computation task. Recently, Dirac-source FETs (DS-FETs)[8,9] have been proposed to achieve both low SS and high I_{on} by source engineering. However, it is noted that all the experimental verifications of this proposal have been

[1]State Key Laboratory of Integrated Chips and Systems, School of Information Science and Technology, Fudan University, Shanghai, China. [2]School of Microelectronics, Fudan University, Shanghai, China. [3]Huawei Technologies Co., LTD., Shenzhen, China. [4]KLMEDIT, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China. [5]State Key Laboratory of Surface Physics and Department of Physics, Fudan University, Shanghai, China. ✉e-mail: jingwan@fudan.edu.cn; pengzhou@fudan.edu.cn; lu_ye@fudan.edu.cn

conducted using low dimensional materials so far, and a demonstration of this technology in the silicon platform is still desired. Silicon-based impact ionization (II) transistors (I-MOS)[10–12] employ the II effect of the drain/channel junction to generate feedback or floating body mechanisms in a silicon channel, and further drastically reduce the SS. However, a large drain voltage is typically required for a high electric field induced II to occur in the traditional silicon-based p-i-n I-MOS[13]. This contradicts the power reduction needs in the first place, and it also damages the gate dielectric and channel materials, which renders it very difficult for practical usage.

Recently, the introduction of heterojunction devices composed of two-dimensional (2D) materials has been shown to resolve some of the aforementioned issues[2–5,8,9,14]. For example, Miao et al. reported a gate-tunable heterojunction tunnel triode based on heterostructures composed of InSe and silicon, which offers an average SS of 34 mV dec^{-1} over four decades of drain current[3]. Gao et al. reported a ballistic I-MOS fabricated by an InSe/BP heterojunction, which has a steep SS (< 0.25 mV dec^{-1}) at low temperatures ($T = 80$ K)[14]. This is mainly attributed to the tunable energy band structure of 2D materials with atomically thin body, and clean vertical van der Waals heterojunctions formed by crystalline surfaces[15]. Since the mainstream chip process technology is still based on silicon platform, this motivates us to explore a silicon-based device architecture with a 2D material/silicon heterostructure drain, to take advantage of both the main complementary metal oxide semiconductor (CMOS) process technology as well as the properties of thin materials.

In this article, we report a vertical subthreshold swing (VS) field-effect transistor (FET) based on silicon MOSFET with graphene/silicon heterojunction (Gr-Si heterojunction) drain, i.e., the device differs from traditional silicon MOSFET only in the drain end, where graphene instead of highly doped silicon is employed to generate a superior potential drop. Gate voltage alters the graphene Fermi level to widen the depletion layer and further strengthen the electric field at this Gr-Si heterojunction. Taking these structural and electrical advantages, the device is demonstrated to achieve an average SS of 16 μV dec^{-1} over 6 orders of current swing and is nearly hysteresis-free at room temperature. The operating voltage at which a VS occurs can be as low as 0.4 V. Additionally, we construct a complementary logic inverter by connecting a steep n-type VSFET in series with a p-type MOSFET, achieving a voltage gain as high as 311 at a supply voltage of 2 V. Finally, the manufacturing process of the devices is largely compatible with the standard silicon process. This work opens up future opportunities for the application of silicon-based heterojunction devices in the field of energy-efficient electronics.

Results and discussion

Device structure and working mechanism

Figure 1a shows a schematic illustration of a n-type VSFET. It is composed of the top p^--doped silicon in the silicon-on-insulator (SOI) as the channel and the monolayer p-type graphene (Supplementary Fig. 4) as the drain. The HfO_2 is used as the gate dielectric and Ti/Au is employed for both gate electrodes and source/drain contacts. The channel width is 5 μm and the channel length is 3 μm. More details about devices fabrication flow are provided in Supplementary Note 1. The device contains a Gr-Si heterojunction drain, a silicon channel and a silicon P-N junction source. The primary mechanism for achieving a VS is believed to be the boosted II process and avalanche phenomenon taking advantage of the strong electrical field in the Gr-Si heterojunction. Schematic diagram of the energy bands of the VSFET is shown in Fig. 1 for the off (Fig. 1b) and on-state (Fig. 1c). In the off-state, the device is biased with negative top-gate voltage (V_{TG}), and the electron injected from the source is suppressed. Graphene is a zero-gap 2D semiconductor, and its Fermi level can be tuned through electrostatic gating[16–18]. As the V_{TG} increases, graphene transitions gradually from p-type doping to n-type doping, leading to the widening of the depletion width in the Gr-Si heterojunction. Simultaneously, the electric field at the Gr-Si heterojunction increases drastically. In addition, the energy band of the silicon channel gradually shifts downward. Electrons are more easily injected from the source into the Gr-Si heterojunction as the injection barrier in the channel decreases, as presented in Fig. 1c. As a result, carriers can obtain sufficient kinetic energy to generate electron-hole pairs within the depletion region under a strong electric field, resulting in avalanche multiplication. This is mainly because the II rate of carriers increases exponentially with the electric field[19]. Further, the holes created by the II accumulate in the SOI body, raising the body potential and further lowering the channel barrier height (Fig. 1c). This induces a feedback loop of more injection of electrons from source electrode and more holes generation from II at the Gr-Si heterojunction. Ultimately, this positive feedback loop helps the abrupt turn on of the device and exhibiting a near VS phenomena.

To confirm the enhanced II located at the Gr-Si heterojunction, the electric field distribution is calculated using density functional theory (DFT)/non-equilibrium Green's function (NEGF). The vertical and lateral electric field contours of the VSFET at a source-drain bias voltage (V_{DS}) of 1 V are displayed in Fig. 1d, e, respectively. Both vertical electric field and lateral electric field are peaked around the graphene and silicon heterojunction drain end. The magnitude of the vertical electric field at the Gr-Si heterojunction reaches 17.6 MV cm^{-1}, more than 4.3 times higher than that close to the source side where no heterojunction exists, as illustrated in Fig. 1f. This enhancement is attributed to the high carrier concentration of graphene and recessed edge[20]. Moreover, the lateral electric field peak in the VSFET occurs within the silicon region of the Gr-Si heterojunction drain and reaches 12.1 MV cm^{-1}, more than 6.5 times higher than that of the normal silicon source P-N junction, as shown in Fig. 1g. And a detailed analysis using DFT/NEGF calculations is presented in Supplementary Note 3. We also use computer-aided design (TCAD) simulations with Synopsys Sentaurus to study the device characteristics. The simulated transfer characteristic curve shows a steep switching characteristic. A detailed TCAD simulation analysis is shown in Supplementary Note 4.

The layout of the device is shown in a false-color scanning electron microscopy (SEM) image (Fig. 1h), illustrating the connection of the graphene drain to both the metal electrode and the silicon channel. A cross-sectional transmission electron microscopy (TEM) image of a typical VSFET is displayed in Fig. 1i. Additionally, a detailed elemental map obtained through energy-dispersive X-ray spectrometry (EDS) reveals a uniform carbon layer along with silicon, confirming the even distribution of graphene on the silicon surface. Cross-sectional TEM images of the magnified dotted rectangle region are presented in Fig. 1j. The interface between graphene and silicon exhibits atomically smooth characteristics, free from impurities and minimizing defects, indicating a high-quality Gr/Si interface with negligible impurities and atomic defects. The VSFET has a steep SS as opposed to Si MOSFET (Fig. 1k) fabricated in similar process conditions, and the I_{on} of both devices reach at the same level at 0.75 V gate bias. The VSFET also exhibits significantly reduced ambipolar characteristics, with a high current on/off ratio of $> 10^6$ at $V_{DS} = 3$ V.

Electrical characterization of VSFET

The electrical characteristics of the device are presented in Fig. 2a–d. Figure 2a shows the transfer characteristic of a n-type VSFET at various back-gate voltages (V_{BG}). The V_{TG} controllability of the device current is improved by increasing the V_{BG} in the negative direction. Additionally, the device electrical characteristics exhibits VS behavior when the V_{BG} is −10 V. These phenomena are mostly attributed to the following mechanism. On the one hand, the increase of V_{BG} in the negative direction raises the barrier height of the bottom silicon channel, making it difficult for the electrons to move across and reach the Gr-Si heterojunction, which reduces the I_{off} of the device. On the other hand,

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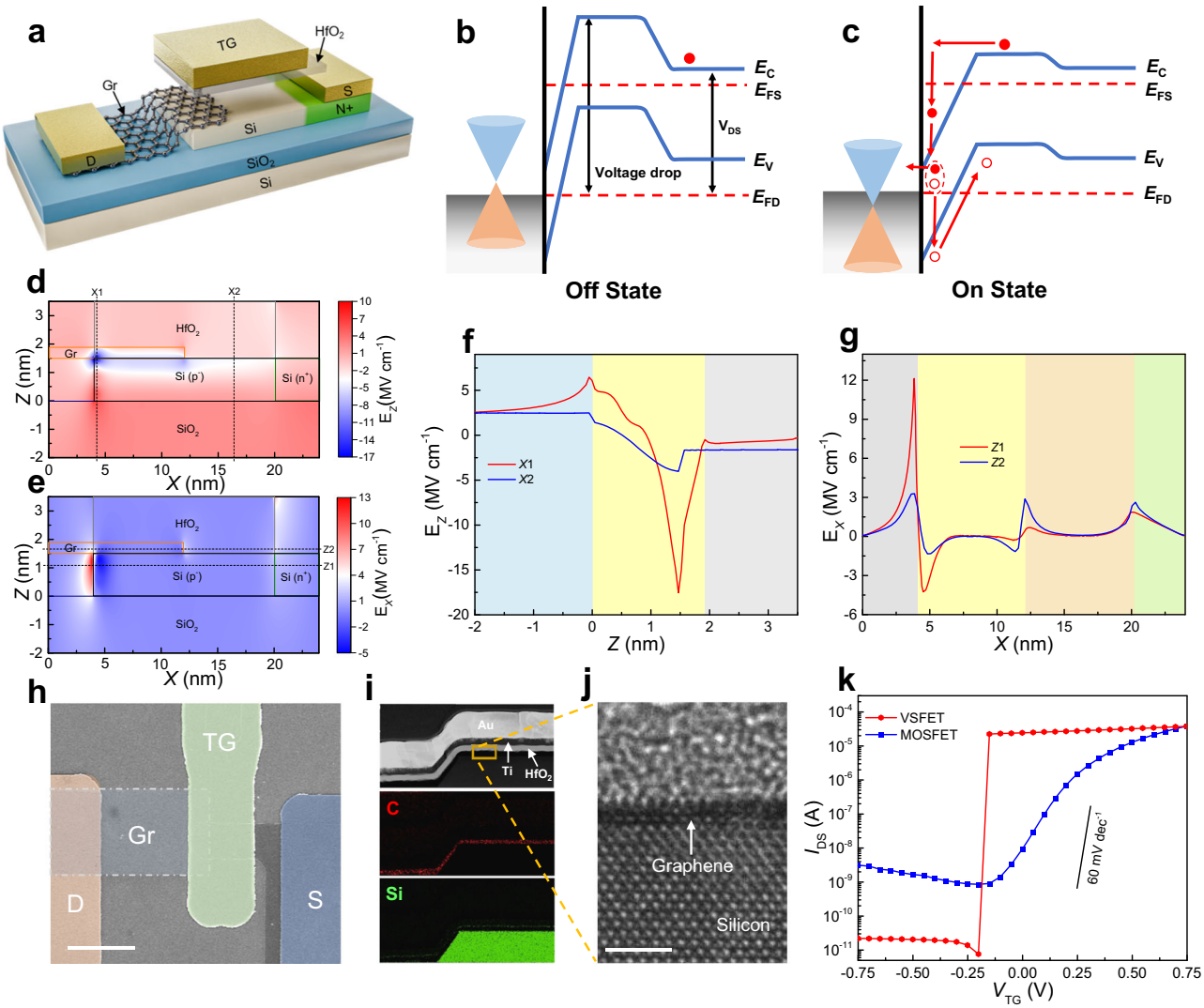

Fig. 1 | Structure and device characterization of the VSFET. a Three-dimensional schematic of the VSFET fabricated on SOI. D, Gr, TG, S, and N + : Drain, graphene, Top-gate, Source, and N-type ion implantation area. Schematic diagram of the energy bands of the VSFET in the off-state (**b**) and on-state (**c**). E_C, E_V, E_{FS}, and E_{FD}: conduction band energy, valence band energy, source fermi level, and drain fermi level, respectively. DFT-simulated electric field contour in vertical (**d**) and lateral (**e**) direction on the VSFET. *X*1, *X*2, *Z*1, *Z*2 are line cuts in (**d**) and (**e**), respectively. **f** Vertical electric field of the VSFET using DFT-simulated. *X*1 represents the vertical electric field near the graphene-silicon heterojunction drain end, and *X*2 represents the vertical electric field in the silicon channel part close to the source. **g** Lateral electric field of the VSFET using DFT-simulated. *Z*1 represents the lateral electric field in the silicon region, and *Z*2 represents the lateral electric field in the graphene layer. **h** Top-view false-color SEM image of a VSFET. Scale bar, 10 μm. **i** Cross-sectional scanning transmission electron microscopy image of the VSFET. Corresponding EDS elemental map showing the distribution of C and Si elements. **j** The zoom-in image in the orange rectangle in (**i**). Scale bar, 2 nm. **k** Comparison of experimentally measured logarithmic-scale transfer characteristics of the fabricated VSFET (red curve) and MOSFET (blue curve) at $V_{DS} = 3$ V.

it strengthens the electric field at the Gr-Si heterojunction, which activates the avalanche multiplication of carriers in the device when the V_{BG} reaches a particular threshold, causing the device to abruptly switch from the off-state to the on-state. It is noted in principle that the device should still be able to produce the VS phenomena by controlling the doping concentration in the silicon channel without applying a V_{BG} (Supplementary Fig. 7). In addition, as the V_{BG} further increases, the I_{off} of the device also rises. This increase can be attributed to the decrease in the depletion width at the Gr-Si heterojunction, which in turn facilitates the diffusion current to easily pass through the heterojunction. When the V_{BG} is fixed at -15 V, sub-60mV dec^{-1} steep slope of SS is consistently observed at various V_{DS}. As V_{DS} increases, the I_{on} gradually increases (Fig. 2b). This superior electric field at the Gr/Si heterojunction enables steep SS even at a low V_{DS} as low as 0.4 V (Fig. 2b inset). And similar results are repeated in multiple devices as shown in Supplementary Fig. 8. Additionally, the gate-leakage current is negligible compared to the drain current (Supplementary Fig. 9). Figure 2c shows the statistical distribution of SS for 30 n-type VSFETs. Note that all devices show SS below 10 mV dec^{-1}, indicating the reproducibility of the fabricated devices. The smallest average SS of our device approaches 16 μV dec^{-1} over 6 orders of magnitude (Fig. 2d), the lowest value among all existing silicon-based FETs. We also study the impact of the scan step size of the top gate voltage on the SS of the device (Supplementary Fig. 10), and it is discovered that the measured SS is still likely to limited by the instrument resolution, i.e., the real SS can be even steeper with a smaller measurement step size. Moreover, multiple devices have also tested similar SS values (Supplementary Fig. 10c). The VSFET clearly exhibits well-behaved rectifying output characteristics, featuring a rectification ratio of approximately 1×10^6 (Supplementary Fig. 11b). A p-type VSFET can be realized by replacing the n-type doping at the ion implantation with p-type doping. The transfer characteristics of the device are presented in Fig. 2e, f.

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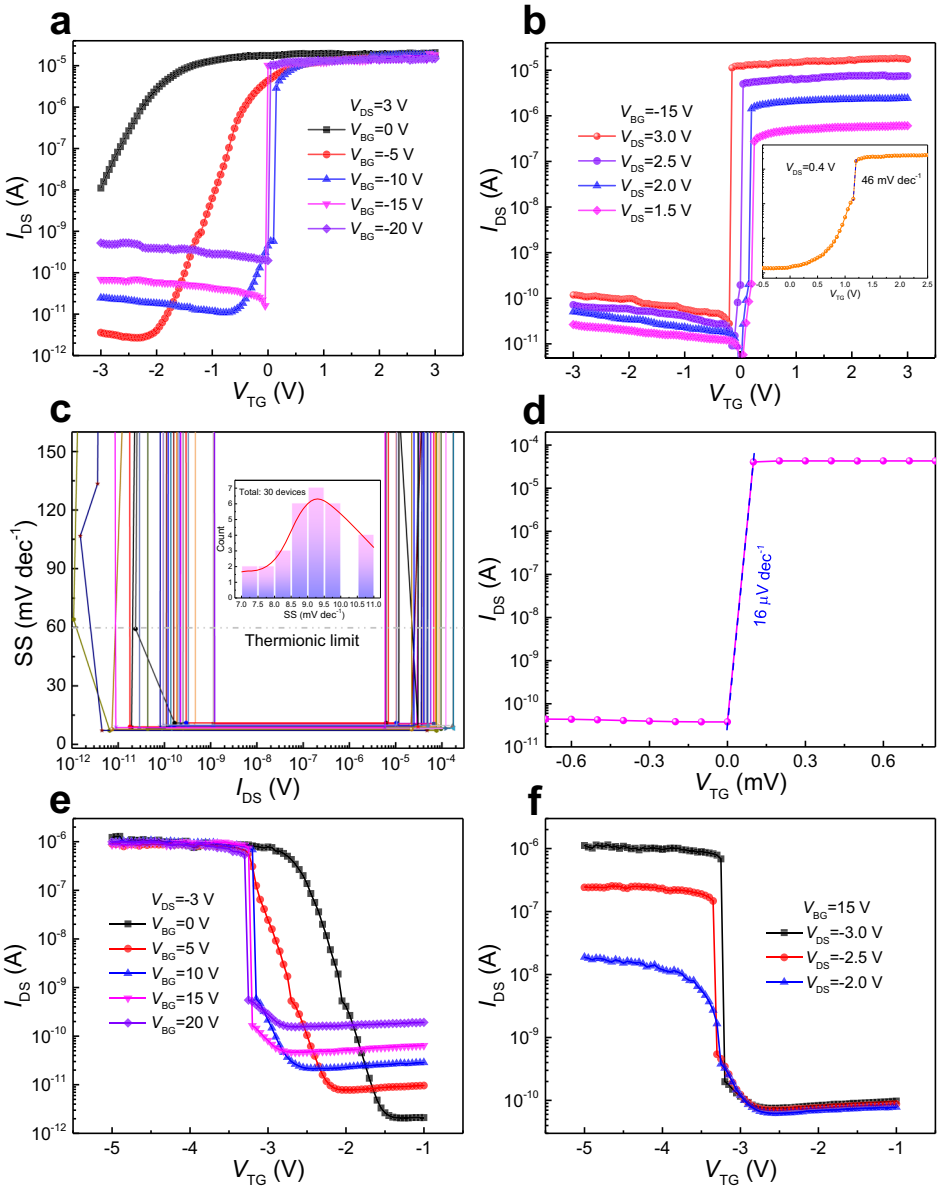

Fig. 2 | Room temperature electrical characterization of the VSFET. a Transfer characteristics of the n-type VSFET with back-gate voltages from 0 V to -20 V with a step of −5 V. **b** Transfer characteristics of the n-type VSFET with bias voltages from 1.5 V to 3 V. The inset is the transfer characteristic curves at V_{DS} = 0.4 V. **c** SS versus output current I_{DS} of 30 representative n-type VSFETs showing reproducibility of the effect at V_{DS} = 3 V. The inset is the statistical distribution of SS for these n-type VSFETs (the voltage scanning step is 50 mV). **d** Transfer characteristics of the n-type VSFET measured with voltage scanning step of 0.1 mV. The bias voltage of V_{DS} is 3 V and the temperature is 300 K. **e** Transfer characteristics of the p-type VSFET with back-gate voltages from 0 V to 20 V. **f** Transfer characteristics of the p-type VSFET with drain bias voltages from −2 V to −3 V.

Compared with the n-type VSFET, the p-type VSFET shows similar electrical characteristics except the I_{on} is relatively weaker, which could possibly be attributed to the lower carrier mobility of holes and/or the unoptimized fabrication process for p-type device.

To further verify the transport mechanism of the VSFET, we conduct temperature-varying tests on the steep transfer characteristics (Supplementary Fig. 12), and the extracted SS is shown in Fig. 3a. In contrast to typical MOSFET, which exhibits a linear temperature relationship due to the Boltzmann distribution (2.3 $kT\,q^{-1}$, blue line), the SS of the VSFET is rather insensitive to temperature variations (red line), confirming the subthreshold transport is not from thermionic emission. In addition, the current noise density spectra are measured under various V_{TG} from −3 V to 3 V, and the normalized noise power spectral density, $S(f)/I^2$ is shown in Fig. 3b. All the spectral density exhibits typical $1/f$ behavior. It is also discovered that the normalized noise power density in the on-state is lower than that in the off-state. The device rapidly turns on as an avalanche of carriers is activated, creating a significant amount of current. After the device is turned on, its normalized noise power density tends to saturate and remains constant regardless of the change in the V_{TG}. This indicates that the carriers inside the device have stabilized and are no longer impacted by the carrier multiplication, which is advantageous for the reliability of the device. This is further demonstrated by the detailed repeatability tests exhibited in Supplementary Fig. 13. Figure 3c displays the forward and reverse transfer characteristic curves of one device and it shows a very small hysteresis window (approximately 50 μV), benefiting from the high-quality interface between the graphene and silicon. The fact that our device exhibits a hysteresis-free window suggests that its working principle goes beyond a pure feedback device mechanism[21], and this makes VSFET more feasible for low-power logic systems. Figure 3d benchmarks the SS

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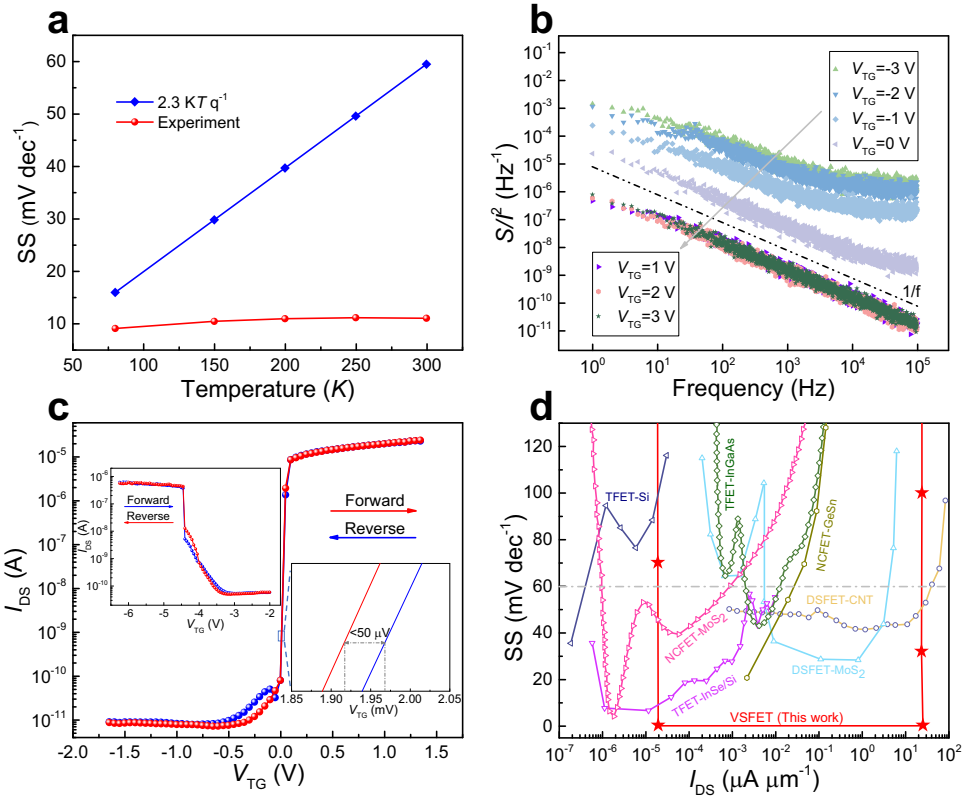

Fig. 3 | Performance of the VSFET. a The SS as the function of temperature. Blue curve is theoretical value which follows the Boltzmann limitation (2.3 kT q^{-1}), and the red curve is the experimentally measured results of the n-type VSFET. **b** Normal noise power spectral density versus frequency for different top gate voltages at room temperature. The tilted black dashed line is the standard 1/f noise guideline. **c** Forward and reverse transfer characteristic curves of VSFETs. The inset-left is the corresponding transfer characteristic curves of p-type VSFET. The inset-right is the transfer characteristic curves of I_{DS} from 10^{-10} to 10^{-9} A, showing that the device exhibits a nearly free hysteresis of 50 μV. **d** Benchmarking of the n-type VSFET with other state-of-the-art steep-slope transistor technologies[3,8,9,22–25]. Subthreshold swing as a function of drain current for various types of sub-thermionic FET. The gray dashed line represents the SS = 60 mV dec^{-1} limit.

as a function of normalized drain current for a VSFET and various types of existing sub-thermionic FETs, including T-FETs[3,22,23], NC-FETs[24,25] and DS-FETs[8,9] at room temperature. Where the SS versus I_{DS} for the VSFET is extracted from the transfer curves (Supplementary Fig. 10b). The average SS of VSFET remains significantly low (« 1 mV dec^{-1}) over 6 orders of magnitude, and the steepest range exists in the entire subthreshold region, exhibiting an ideal current switching behavior. Furthermore, the VSFET shows a superior I_{60} current (the current when the subthreshold SS is equal to 60 mV dec^{-1}) density (~26 μA μm^{-1}), higher than any TFET technologies reported.

Complementary inverter composed of the VSFET

The characterization of a complementary inverter utilizing a combination of p-type MOSFET and n-type VSFET are accomplished. The corresponding circuit diagram is depicted in Fig. 4a. Transfer characteristics of the p-type MOSFET and n-type VSFET are illustrated in Fig. 4b. Additionally, Fig. 4c represents the voltage transfer characteristics of the inverter, along with the voltage gain (V_{gain}) exhibiting the input voltage (V_{IN}) under supply voltages (V_{DD}) of 1.5 V and 2 V, respectively. The output voltage (V_{OUT}) is high (logic "1") when the input voltage (V_{IN}) is low (logic "0"). As V_{IN} increases (logic "1"), V_{OUT} is pulled down to a low level (logic "0"). This illustrates the logic operation of this inverter. High V_{OUT} values are close to V_{DD} and low V_{OUT} values are close to 0.1 V, indicating a good V_{TH} match between these two devices. The V_{gain} increases as V_{DD} increases, reaching a peak value of 311 when V_{DD} is 2 V, and this is considerably higher in comparison with any existing silicon-based MOSFET inverters. In addition, with the increase of the V_{DD}, the transition voltage (V_M) exhibits a right-shifting tendency toward positive V_{IN}. We also analyze the effect of the SS of the steeper device on the V_{gain} of the complementary inverter. The calculation results show that the inverter's V_{gain} increases with decreasing SS (Supplementary Note 11). Figure 4d is the benchmark of the V_{gain} as a function of V_{DD}, it is not only higher than another steep switching devices[26–30], but also advantageous compared to reported 2D semiconductor-based CFETs[31–35], and silicon-based CFETs[36–38].

In summary, we have successfully demonstrated a silicon-based VSFET with nearly vertical subthreshold swing. Thanks to the Gr-Si heterojunction drain, the electric field in the silicon close to the drain end is significantly enhanced and this drastically boosts the II rate. Taking this major advantage, sharp switching behavior can be observed under supply voltage as low as 0.4 V, and the device exhibits an average SS of 16 μV dec^{-1} over 6 decades of drain current and nearly hysteresis-free (<50 μV) at room temperature. Furthermore, we experimentally demonstrate a high-performance complementary FET inverter composed of traditional MOSFET and VSFET. This inverter exhibits a voltage gain as high as 311 at a supply voltage of 2 V. This research paves the way for developing silicon-based devices in energy-efficient electronics.

Methods

Device fabrication

The VSFET was formed by transferring chemical vapor deposition (CVD) grown graphene onto pre-patterned SOI substrates. The pre-patterned was carried out on an SOI substrate. The mesa isolation was formed by photolithography followed by wet etching. Photolithography was then used to define the silicon channel and ion implantation regions. Then, ion implantation of Arsenic ions was used to form n$^+$ doping for the ion implantation regions. Multiple Ti/Au electrodes were patterned and

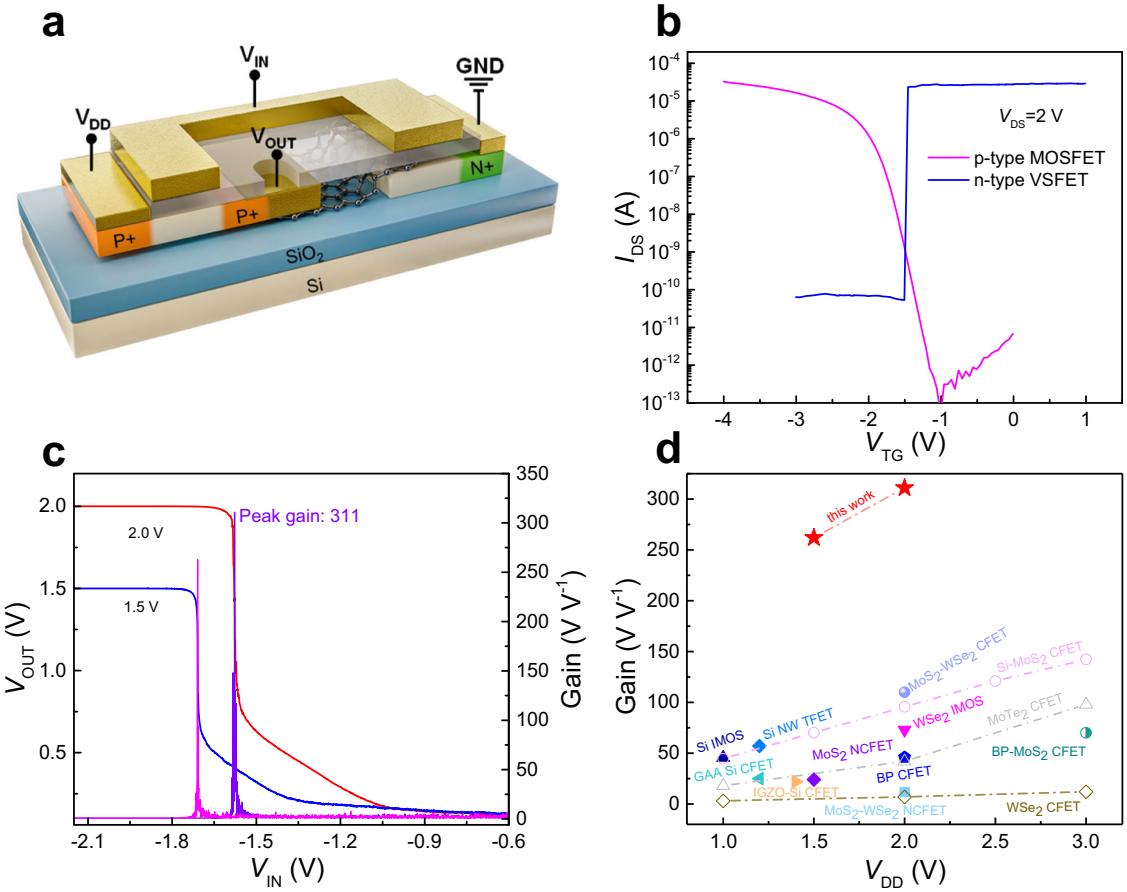

Fig. 4 | Complementary inverter fabricated with VSFET as n-type FET and conventional MOSFET as p-type FET. a Three-dimensional schematic, and circuit configuration of the inverter. **b** Transfer characteristics of n-type VSFET and p-type MOSFET (blue and pink curves, respectively). **c** The voltage transfer characteristics and gains of the inverter under V_{DD} = 1.5 and 2.0 V. **d** Benchmark of inverter gain as a function of V_{DD} for inverters based on steep switching devices[26–30], 2D semiconductor-based CFETs[31–35], silicon-based CFETs[36–38] and VSFET in this work.

deposited using photolithography and electronic beam evaporation, acting as the source and drain. The CVD grown graphene purchased from ACS Material, LLC. was transferred from a copper substrate to a pre-patterned SOI substrate and then patterned as drains of the device by photolithography and O_2 reactive ion etching (RIE). Since there are no dangling bonds on the surface of the graphene, it is difficult to grow HfO_2 directly through atomic-layer deposition (ALD) technology, so ~2 nm SiO_2 was deposited as a seed layer before growing HfO_2. The HfO_2 layer was grown by ALD technology as a high-*k* dielectric layer. The top gate was patterned and deposited using photolithography and E-beam evaporation of Ti/Au films.

Material characterization and electrical measurement

The structure of the device was confirmed through cross-sectional high-resolution transmission electron microscopy using an FEI Titan3 G2 60-300, coupled with energy dispersive X-ray spectroscopy. The scanning electron microscopy image was obtained using a Zeiss Sigma 300. Electrical measurements were conducted using Keithley 2636B and 2612B source/meters. All electrical measurements were carried out in a vacuum probe station under dark conditions at room temperature, except for specific variable temperature tests. The noise was assessed using a noise measurement system (PDA NC300L).

Data availability

The data that supports the findings of this study are available at https://zenodo.org/records/13756121. All other data are available from the corresponding authors upon request.

Code availability

The codes used for simulation and data plotting are available from the corresponding authors upon request.

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Author contributions

Y.L., J.Wan, and J.X. conceived and supervised the project. B.Y. wrote the manuscript, and Y.L., J.Wan, and P.Z. revised the manuscript. B.Y., Z.C., and Y.C. fabricated the devices. B.Y. performed the electrical measurements and data processing with assistance from C.T. and W.C. C.Z., Z.H., Q.Z., and J.Wang contributed to the working mechanism analysis. Z.H. and W.G. contributed to the TCAD simulation analysis. Q.Z. and J.G. contributed to the DFE/NEGF simulation analysis. M.L. and Y.Z. contributed to the temperature-varying tests. Y.L., Z.C., G.H., Z.W., K.L., Z.Z., S.X., C.C., W.B., and S.M discussed the results. All authors commented on the paper.

Competing interests

The authors declare no competing interests.

Additional information

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Correspondence and requests for materials should be addressed to Jing Wan, Peng Zhou or Ye Lu.

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