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# Cryogenic in situ fabrication of reversible direct write logic circuits and devices

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Signal transmission across cryogenic and room-temperature environments remains a significant bottleneck in superconducting quantum computing and classical circuit integration. Furthermore, interactions among cryogenic devices often require room-temperature interfacing, driving substantial demand for data read/write interfaces, which in turn increases interconnect complexity and constrains scalability. In situ fabrication of cryogenic, high-performance logic circuits and devices presents a promising solution to address this "wiring bottleneck". Here, we demonstrated interfacial two-dimensional electron gas devices with reversible interface states that can be directly modulated at operating temperatures while achieving an unprecedented ultrahigh on/off ratio. Remarkably, these devices can be patterned using a "light pencil" and erased with a pulsed electric field, enabling resist free, in situ direct writing and electrical erasure of the interface state.

Cryogenic circuits and devices are essential to advancing understanding of superconducting mechanisms[1,2], spintronics[3,4], and the development of scalable superconducting quantum computers[5,6]. However, their interconnections and control typically depend on room-temperature interfaces, which introduce unavoidable challenges such as noise and thermal conduction[7–9]. As the number of cryogenic devices continues to grow, the "wiring bottleneck" has emerged as a critical barrier to scalability[8,10,11]. Addressing this limitation requires innovative strategies, with one of the most promising being the in situ, repeatable fabrication of high-performance cryogenic logic circuits and devices, including field-effect transistors (FETs)[12,13]. In parallel, field-induced metal-insulator transitions (MIT) offer an intriguing route for the in situ realization of such devices. However, existing approaches for reversible MIT, such as those using conductive atomic force probes[1,14] based on the "water cycle" mechanism[15], electric field induced hydrogenation[16], and hydrogen ion liquid gating technique[17], are largely confined to room temperature. The complexity and scalability challenges associated with these techniques further limit their applicability in large-scale device fabrication. While X-ray irradiation has been shown to induce MIT under cryogenic conditions, reversing the transition necessitates thermal annealing[18], which not only risks damaging other delicate cryogenic chips but also incurs prohibitive costs, further limiting its practical applicability. Consequently, there is a pressing need to develop a simpler, more cost-effective approach for the repeatable and in situ fabrication of cryogenic logic circuits and devices.

Our study aims to develop a low-cost method for reconfigurable, in situ direct-writing of low-power logic circuits and devices at the interface under cryogenic conditions, without photoresist. Over the past two decades, the correlated two-dimensional electron gas (C-2DEG) generated at the interface between two insulating oxides[19], $LaAlO_3$ (LAO) and $SrTiO_3$ (STO), has garnered widespread attention. This interface exhibits plentiful physical phenomena, including superconductivity[20,21], magnetism[22,23], Rashba spin-orbit coupling[24], and quantum oscillations[25–27]. Furthermore, the C-2DEG interface can be well controlled through various means, such as optical[28], electric[29], and magnetic fields[30], and possesses excellent chemical stability[31], interference resistance, and high mobility[19], making it an ideal platform for developing oxide functional devices[14,32,33]. The metallic nature of this interface eliminates high Schottky barriers, facilitating near-

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perfect ohmic contact between the channel and electrodes. Additionally, the single crystal STO substrate boasts an extremely high relative dielectric constant ($\kappa$ ~ 20,000)[1,34], remaining above 3000 even in an electric field of 5 kV/cm[35,36]. Numerous studies have demonstrated that a high quality single crystal STO film can be integrated on a single-crystal silicon surface[37,38], positioning it as one of the ideal candidates for the next generation of cryogenic, low-power oxide functional devices integrated on silicon[39]. However, the excessively high interface carrier concentration poses challenges in controlling the electric field over the C-2DEG, because C-2DEG interfaces beyond the critical thickness are very conductive and, under normal circumstances, cannot be non-volatilely transformed into an insulating state. Therefore, discovering a non-volatile method to deplete interface carriers is essential for high performance cryogenic devices.

In this study, we present a heterostructure of $LaFeO_3$ (LFO) delta-doped at LAO/STO interfaces to reduce the carrier concentration of the C-2DEG (see Fig. 1a). Using two straightforward examples, we demonstrate in situ construction of two types of cryogenic devices. The first one is a cryogenic FET with ohmic contacts controlled by a back-gate, where the C-2DEG channel is primarily concentrated at the interface to the substrate side, with the thickness as thin as 1 nm or even a mono layer[40]. This cryogenic FET exhibits a high carrier mobility of up to 2300 $cm^2V^{-1}s^{-1}$, an ultra-low off-state current ($I_{off}$) around $10^{-12}$ A, a remarkably low supply voltage ($V_{DS}$) of 5 mV enabled by barrier-free contacts, a high on/off current ratio ($I_{on}/I_{off}$) approaching $10^9$, and excellent electrical durability and performance, on par with the most advanced cryogenic FETs reported to date[41]. The second one is a laser direct-writing technology where a laser can produce localized conductive pathways. Furthermore, these pathways are reversible and can be erased using a pulsed back-gate voltage, allowing the conductive pattern to be redefined. This approach, leveraging a "light pencil" for writing and an "electric field eraser" for resetting, provides a versatile and repeatable method for in situ fabricating reversible cryogenic circuits and devices.

## Results

### Back-gate induced metal-insulator transition: fabrication of normally-off channels

The resistance-temperature (R-T) curve serves a clear method for assessing the conductive behavior of the C-2DEG interface. As shown in Fig. 1b, measurements were performed using the two-wire method and the Van der Pauw method respectively. Since the Van der Pauw method can eliminate the contribution of contact resistance[42], the measured resistance is solely contributed by the C-2DEG interface. The R-T curve confirms that the C-2DEG interface exhibits metallic behavior. Its carrier concentration extracted from the Hall effect is approximately $1.93 \times 10^{13}$ $cm^{-2}$, and the calculated mobility exceeds 2300 $cm^2V^{-1}s^{-1}$ at 2 K. In contrast, the resistance measured from the two-wire method is a sum of the interface C-2DEG and contact resistances. Interestingly, the R-T curve from the two-wire method exhibits similar behavior to that from the Van der Pauw method. This fact indicates a typical metallic ohmic contact between the metal electrodes and C-2DEG surface. Simultaneously, the Current-Voltage (I-V) characteristics of both methods at 2 K are linear and exhibit no threshold voltage (see Fig. S1), indicating the successful achievement of a barrier-free metal-channel contact.

According to our previous work[43], this system undergoes a non-volatile transition from normal-on to normal-off state (i.e., MIT) at 2 K after applying a pulsed back-gate voltage of 210 V. With a $V_{DS}$ = 0.5 V, Fig. 1c shows the variations in interface resistance resulting from the non-volatile MIT induced by 1 ms pulses $V_{BG}$ of 100 V, 150 V, 175 V, and 210 V, respectively. For the case of $V_{BG}$ = 210 V, the resistance exceeds the measurement limit of $10^{10}$ Ohms, so the $I_{on}/I_{off}$ ratio will be greater than $10^8$, indicating that the channel is cut off at this point.

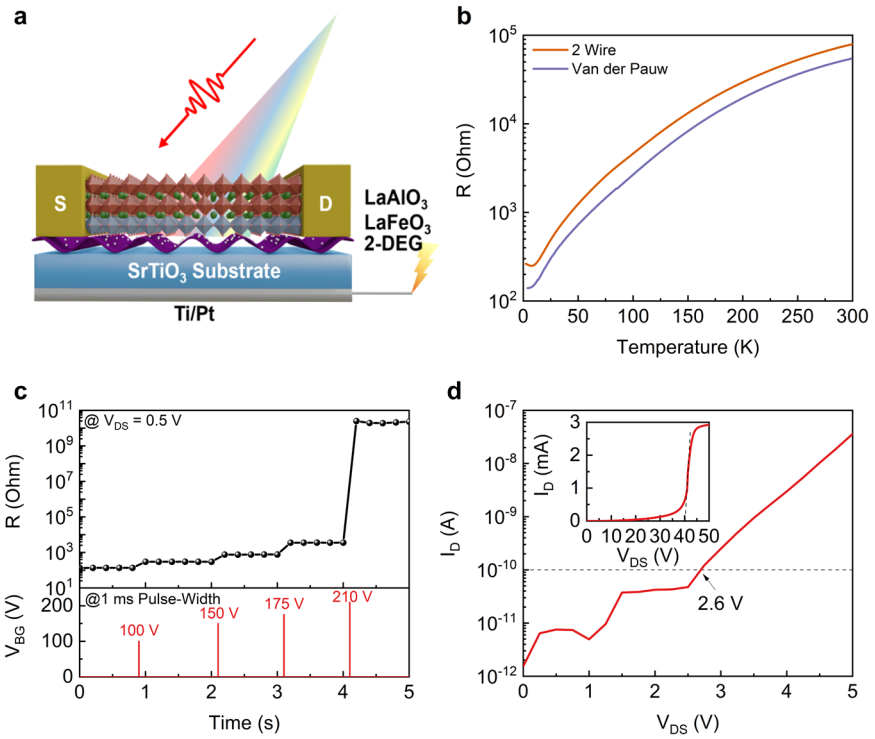


**Fig. 1 | Description of the C-2DEG FET technology platform and fabrication of insulation channels. a** A schematic of optical-electric C-2DEG field-effect transistor. **b** Two-wire method and Van der Pauw method were employed to measure the resistance-temperature curves of the C-2DEG interface, respectively. **c** Pulsed back-gate voltages ranging from 100 to 210 V with a pulse width of 1 ms were applied to achieve different resistance states of the C-2DEG interface under $V_{DS}$ = 0.5 V. **d** The $I_D$-$V_{DS}$ curve of normal-off interface exhibits an onset voltage of approximately 2.6 V. The illustration indicates that the interface experiences breakdown at a $V_{DS}$ of around 40 V.

To prove that the switching can be faster, we developed a homemade pulse generator to apply 50 µs pulses of gate voltage and observed comparable switching behavior, as shown in Fig. S2a. To further estimate the gate response time, we adopt the conventional RC charging–discharging framework. Within this model, the characteristic timescale for a full cycle is approximately given by $2 \times 5\ R_{eff}C$, where $R_{eff}$ is the effective series resistance. For our cryogenic FET, this model implies a theoretical temporal resolution of $2 \times 5\ R_{eff}C$, which is directly determined by the gate capacitance and thus depends on gate area and dielectric thickness. With our current gate design (area: 25 mm2, thickness: 0.5 mm), resolution can be expressed as $10R_{eff}\ \varepsilon S/d$, yielding a value of ~4 µs under our current device geometry. If the gate dimensions are scaled down to match those used in advanced CMOS technologies (a gate area of 150 $nm^2$ and a thickness of 12 nm) the theoretical time resolution could be reduced to ~1 ps. This straightforward method for modulating the MIT at the C-2DEG interface via a back-gate in cryogenic conditions presents a promising avenue for the advancement of cryogenic electronics. Furthermore, Fig. 1d shows the I-V characteristics when the channel is completely cut off ($V_{BG} = 0$). Drain-source breakdown voltages ($V_{DSS}$, according to $I_D \geq 10^{-10}$ A) is approximately 2.6 V, followed by a linear ohmic region (2.6–7 V). As $V_{DS}$ increases further, the channel undergoes avalanche breakdown at $V_{DS} \geq 40$ V. This value is significantly higher than the $V_{DSS}$, indicating that the channel demonstrates exceptional stability.

## Parallel-plate capacitor series model

Our prior research proposed a plausible model to elucidate the non-volatile MIT[43]. At lower temperatures, the majority of gases solidify and deposit as a layer on the surface of the thin film. Under these conditions, the environmental pressure is minimal, and a strong electric field, induced by a 210 V back-gate voltage, penetrates the sparse gaseous medium, facilitating the generation of electrons. In the presence of this electric field, electrons adhere to the solidified gas layer (referred to as the gas ice layer) on the thin film surface. This system can be approximated as two parallel-plate capacitors arranged in series (see Fig. 2). In this configuration, the upper parallel-plate capacitor consists of the charged gas ice layer and the C-2DEG interface, with the epitaxial thin films as thin as 6 nm acting as the dielectric layer. The lower parallel-plate capacitor comprises the C-2DEG interface and the bottom electrode, with the STO substrate serving as the dielectric medium. Upon removal of the back-gate voltage, the C-2DEG interface induces positive charges corresponding to the number of electrons in the gas ice layer, depleting the interface carriers.

To further substantiate the validity of this model, Fig. 1c demonstrates that varying the back-gate voltage results in distinct resistance states at the interface. Using the previously determined dielectric constant of the single-crystal STO substrate[43], we calculated the charge density in the gas ice layer under different back-gate voltages. Assuming that the carrier mobility at the C-2DEG interface remains constant before and after charging the gas ice layer, we computed theoretical resistance values (see Table S1). Notably, these theoretical resistance values exhibit excellent agreement with the experimentally measured values, further corroborating the accuracy of the series-connected parallel-plate capacitor model. Furthermore, reapplying the back-gate voltage again results in the bottom electrode acquiring positive charges, which in turn induces electrons at the C-2DEG interface. Leveraging this principle, we can construct a single cryogenic FET cell based on the described mechanism.

## Cryogenic FET with ultra-high on/off ratio

Figure 3b presents a comparative analysis of transfer characteristics ($I_D$-$V_{BG}$) under various $V_{DS}$ at 2 K. Remarkably, the channel can be efficiently driven with a minimal $V_{DS}$ of 0.5 mV, which is two orders of magnitude smaller than traditional 2D FETs[44–46], while boasting an $I_{on}/I_{off}$ ratio beyond $10^5$. Therefore, it can be foreseen that such a small $V_{DS}$ can reduce power consumption by approximately four orders of magnitude. As $V_{DS}$ gradually increases from 1 mV to 1 V, the channel maintains a low $I_{off}$ (~ $10^{-12}$ A), with occasional discontinuities attributed to exceeding the electronic measurement range. With the rise in $V_{DS}$, the $V_{BG\text{-}on}$ significantly decreases from 70.5 V to 55.5 V, and for $V_{DS} \geq 500$ mV, the $I_{on}/I_{off}$ ratio is close to $10^9$. Cyclic characteristics reveal that the leakage current after channel closure is less than 1 nA, and the $V_{BG\text{-}off}$ is less than the $V_{BG\text{-}on}$ but greater than 0, signifying that channel closure does not necessitate applying a negative $V_{BG}$.

However, the application of $V_{BG}$ exceeding 50 V presents a challenge in application. Consequently, we addressed this challenge by mechanically thinning the STO substrate thickness from 0.5 mm to 0.2 mm (see Fig. S4). Furthermore, Fig. 3c compares the transmission characteristics of the FET at 2 K with STO thicknesses of 0.5 mm and 0.2 mm. Notably, at a $V_{DS}$ of 50 mV, the turn-on voltage significantly decreases from 70.5 V to 17 V, while the $I_{on}/I_{off}$ ratio remains relatively unchanged, indicating potential for practical application scenarios. However, to ensure that the power supply voltage can effectively drive the subsequent gate stage, it is necessary to reduce the thickness of the STO gate layer to approximately 14 nm in order to achieve millivolt-level operation. This dimensional scaling could be realized through water-assisted transfer of freestanding membranes or by growing high-

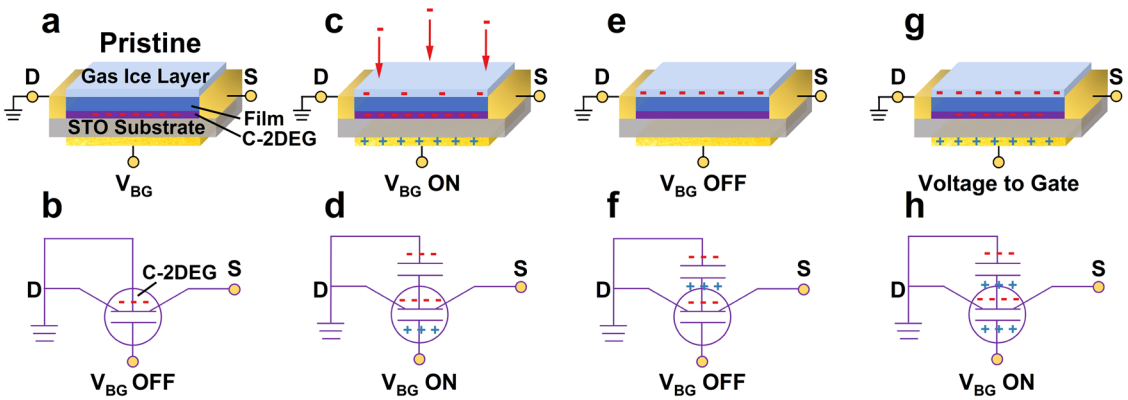


**Fig. 2 | Schematic model of C-2DEG FET. a, b** The C-2DEG interface is conductive in the pristine state. **c, d** When $V_{BG}$ is applied, the C-2DEG interface induces more carriers. At the same time, the strong electric field ionizes the gas molecules under low gas pressure, and the charges are attracted to the surface of the gas ice layer by the electric field. **e, f** When the $V_{BG}$ is turned off, charges are absorbed in the insulating gas ice layer, but the bottom electrode is no longer charged. Therefore, positive charges are induced at the C-2DEG interface to neutralize the carriers, and the interface becomes an insulating state. **g, h** When $V_{BG}$ is applied again, carriers are induced at the C-2DEG interface and the interface is switched to conductive state.

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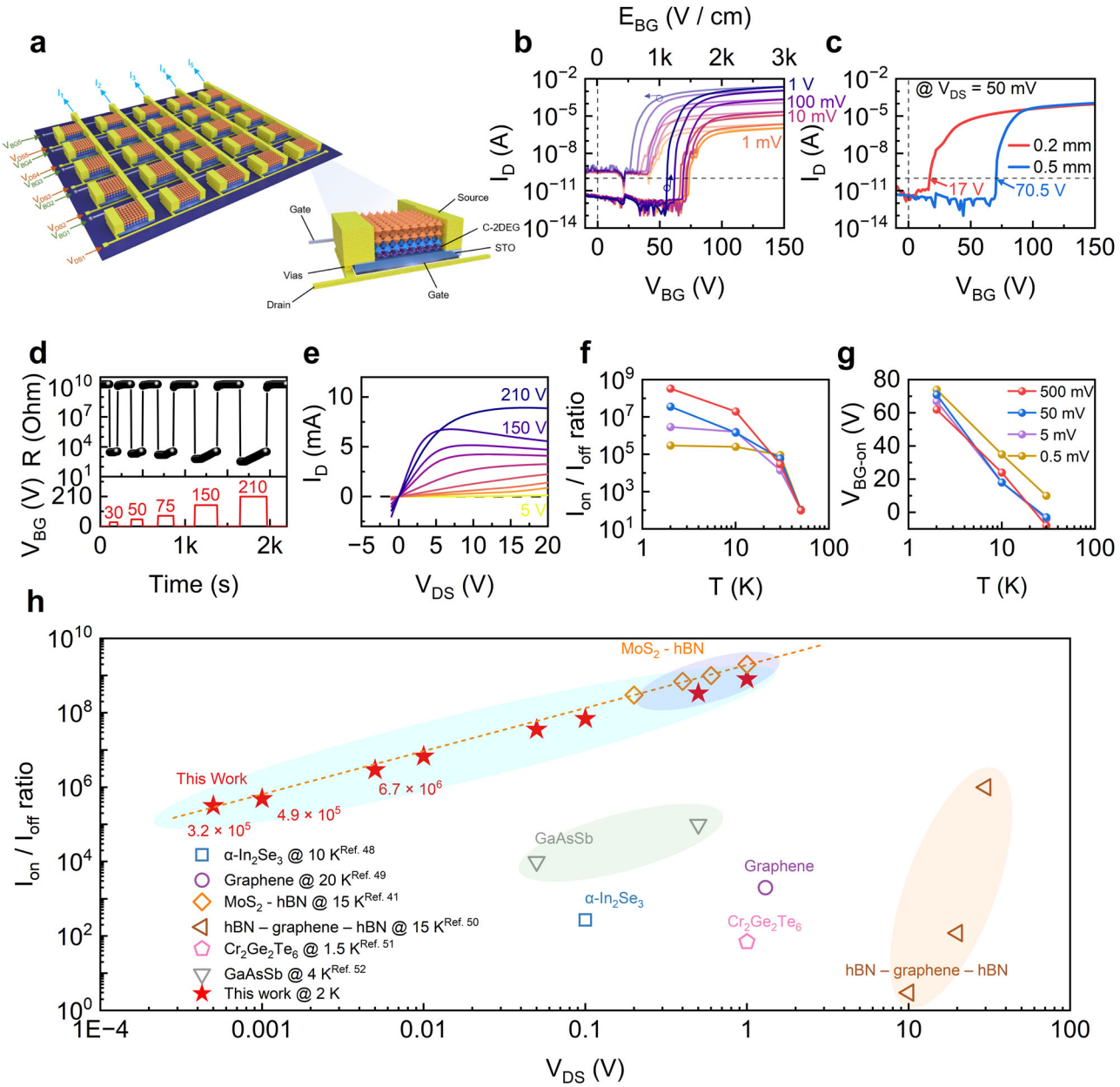


**Fig. 3 | Cryogenic direct-current characterization of C-2DEG FET. a** Conceptual diagram of constructing cryogenic FET array. **b** The $I_D$-$V_{BG}$ cyclic curve spanning a supply voltage range from 1 mV to 1000 mV. The $V_{BG\text{-}on}$ and $V_{BG\text{-}off}$ decrease significantly as $V_{BG}$ increases. **c** Comparison of $I_D$-$V_{BG}$ curves of samples with substrate thicknesses of 0.2 mm and 0.5 mm respectively. $V_{BG\text{-}on}$ was significantly reduced from 70.5 V to 17 V due to the reduction of STO gate thickness under $V_{DS}$ = 50 mV. **d** Different $V_{BG}$ (from 30 V to 210 V) inject carriers to produce different conductive states under $V_{DS}$ = 0.5 V. **e** $I_D$-$V_{DS}$ characteristics of C-2DEG interface under different $V_{BG}$ (from 5 V to 210 V). **f** $I_{on}/I_{off}$ ratio as a function with different $V_{DS}$ (from 0.5 mV to 500 mV). **g** $V_{BG\text{-}on}$ as a function with different $V_{DS}$ (from 0.5 mV to 500 mV). **h** $I_{on}/I_{off}$ ratio versus $V_{DS}$ in C-2DEG FET compared to other FETs with typical semiconductor channel materials. The orange dashed line represents the expected fit as reported in the ref. 41.

quality ultrathin STO films via molecular beam epitaxy[47,48]. Such an approach would lower $V_{BG\text{–}on}$ to around 4.7 mV and is expected to result in a steeper inverse subthreshold slope.

To intuitively assess the response speed and stability of resistance switching, a wider $V_{BG}$ pulse was applied to the sample with an STO thickness of 0.2 mm, using a $V_{DS}$ of 0.5 V (see Fig. 3d). At this juncture, a $V_{BG}$ of only 30 V can lead to an $I_{on}/I_{off}$ ratio exceeding $10^7$, and the response time of the MIT is lower than 1 ms. Here, 1 ms is our digital measurement lower limit. As $V_{BG}$ gradually increases, the $I_{on}/I_{off}$ ratio also significantly increases. The metallic-state resistance exhibits a slow relaxation after maintaining a high $V_{BG}$ for ~1 min, due to the reduced $\kappa$ value of the STO substrate under strong electric fields. In fact, this change is too weak to affect the normal operation of the FET, and 1 min far exceeds practical device operation times. Moreover, our FET works very well without breakdown under a continuous $V_{BG}$ of 210 V for 5 min, further confirming the stability of the C-2DEG interface.

Furthermore, Fig. 3e depicts the typical output curve of the FET with an STO thickness of 0.2 mm when temperatures as low as 2 K. A linear ohmic I-V relationship is observed at $V_{BG}$ = 20 V, and when $V_{BG}$ < 20 V, the I-V characteristics of channel closure, similar to Fig. 1d, are exhibited in Fig. S6. As $V_{BG}$ gradually increases, the saturation leakage current rises, and the variable resistance region gradually narrows, exhibiting typical N-type channel enhancement FET output

characteristics. In addition, A negative resistance effect is observed at very high $V_{DS}$ (above 7.5 V). At such high electric fields, the probability of carrier collisions increases significantly, and carriers may also be captured by local traps, leading to a decrease in $I_{DS}$. However, when $V_{BG}$ exceeds 150 V, the carrier concentration induced by the back-gate surpasses the initial concentration, resulting in a transition to an N-depletion-type FET[49]. Consequently, FET achieved from $V_{BG} = 210$ V exhibits a larger saturation leakage current and a wider variable resistance region.

Temperature stability stands as a critical parameter for evaluating device performance. Despite our field-effect transistor can be operated with a drain–source voltage as low as 0.5 mV, as previously demonstrated, prolonged continuous operation will induce non-negligible Joule heating. To underscore the influence of temperature on the turn-on voltage, we conducted temperature-dependent tests on the sample with STO substrate thicknesses of 0.5 mm within the 2–50 K range. Figure 3f, g (Extracted from Fig. S3) delineates the relationship between $I_{on}/I_{off}$ ratio, $V_{BG\text{-}on}$, and temperature under different $V_{DS}$ drives. Visually discernible from the Fig. S3 is the fact that the reduction in $I_{on}/I_{off}$ ratio primarily stems from the increase in off-state current as the temperature rises. However, at the ultra-low $V_{DS}$ of 0.5 mV, the $I_{on}/I_{off}$ ratio remains almost unchanged and maintains a high level of $10^5$ when the temperature rises to 30 K. This indicates that even if Joule heating causes the FET temperature to rise by 30 K, its performance is scarcely affected. Subsequently, with warming to 50 K, all $I_{on}/I_{off}$ ratios decrease to approximately 100. Nevertheless, the $V_{BG\text{-}on}$ is notably affected by temperature, dropping to around 20 V at 10 K and further diminishing to 0.

Figure 3h compares our FET alongside and some typical 2D semiconductor channel materials including α-$In_2Se_3$[50], Graphene[51], $MoS_2$–hBN[41], hBN–graphene–hBN[52], $Cr_2Ge_2Te_6$[53] and GaAsSb[54]. This analysis focuses on $I_{on}/I_{off}$ ratio and supply voltage at cryogenic environment. Evidently, the supply voltage exerts a significant impact on the $I_{on}/I_{off}$ ratio, exhibiting a decrease as the supply voltage diminishes. Our FET, crafted through a simpler fabrication method, attains an $I_{on}/I_{off}$ ratio comparable to the most promising cryogenic FETs reported to date, particularly at lower temperatures. Remarkably, at the lowest $V_{DS}$ ~ 0.5 mV, the $I_{on}/I_{off}$ ratio reaches an impressive $10^5$, a value surpassing the performance of most FETs operating at higher supply voltages. Consequently, the C-2DEG interface can be acknowledged as the one of the most energy-efficient cryogenic 2D channel available.

Based on the schematic diagram in Fig. 2, we observe that, owing to the insulating state of the gas ice layer, the upper layer, resembling a parallel-plate capacitor, will not discharge as long as the adsorbed charge reaches saturation and the temperature remains constant. Consequently, the energy required for writing and reading one bit in a C-2DEG FET logic unit is respectively determined by the energy consumed for charging the lower parallel plate capacitor by the external gate voltage, denoted as $E_{PPC}$, and the Joule heating, denoted as $E_{OMH}$, generated by driving the internal C-2DEG and the contact resistance of the metal state[55]:

$$E_{PPC} = V_{BG}\int_0^\infty idt = \frac{V_{BG}^2}{R}\int_0^\infty e^{-\frac{t}{RC}}dt = CV_{BG}^2 = \varepsilon_r\varepsilon_0 E_{BG}^2 Sd \propto \mathrm{S}\cdot\mathrm{d} \quad (1)$$

$$E_{OHM} = E_{C-2DEG} + E_{con} = \frac{V_{DS}^2 t}{R_{OHM}} \propto V_{DS}^2 \cdot t \quad (2)$$

Here, $\varepsilon_r$ represents the relative dielectric constant, $\varepsilon_0$ is the vacuum permittivity, $E_{BG}$ is the back gate electric field strength, S is the area of the STO gate, d is the thickness of the STO gate, t is the pulse width, and $R_{OHM}$ is the sum of the C-2DEG interface resistance and contact resistance.

However, it is worth noting that the interface resistance of the C-2DEG,denoted as $R_{C-2DEG} = \rho_S \frac{W}{L}$, where $\rho_S$ is surface resistivity, $W$ represents the channel width and $L$ denotes the channel length. Thus, its numerical value solely depends on the ratio of channel width to length, independent on the actual channel area. Consequently, if the channel is proportionally scaled down to the nanometer level, its $R_{C\text{-}2DEG}$ remains unchanged, implying constant reading power consumption $E_{OHM}$. Presently, we have achieved a $V_{DS}$ of ~0.5 mV, and the energy required for reading 1-bit of computation will be below $10^{-18}$ J for a pulse width t of 1 ns, which is six orders of magnitude lower than traditional 2D FETs (~pJ/bit)[52].

It is evident that the $E_{PPC}$ is directly proportional to the volume of the STO gate. However, with the present large gate dimensions, the $E_{PPC}$ reaches a significant value of $10^{-11}$J/bit, and other performance parameters, such as the inverse subthreshold slope, of the FET are not directly comparable to those of advanced nanoscale-gate FETs[56]. Future efforts could employ self-supporting techniques to reduce gate thickness to the micrometer scale and apply patterning to minimize gate area (see Fig. 2a), potentially lowering the $E_{PPC}$ well below the $E_{OHM}$. Furthermore, as shown in Fig. S7, the gate leakage current for the 0.2 mm-thick gate remains negligible near the $V_{BG\text{-}on}$, with a typical value around $10^{-11}$A. This fact indicates that the power dissipation associated with gate leakage is negligible. Nevertheless, an alternative ultra-low-power method for channel activation is still needed given the current size of gate layer.

## Optical pencil & electric eraser: reversible in situ laser direct-writing

Previous discussions revealed that carrier depletion in the C-2DEG interface arises from charge accumulation within the gas ice layer. Developing a low-power approach to remove this charge could locally restore the conductivity of channels. Photonic devices, known for their ultra-low power requirements, represent a promising solution. To evaluate this potential, we constructed a tunable light source covering wavelengths from 200 to 1100 nm using a xenon lamp coupled with a monochromator, directing the output into cryogenic environments via an optical fiber.

A typical Hall bar pattern was defined over a $1 \times 1\,mm^2$ region on the sample surface using a mask (Fig. 4a). As shown in Fig. 4b, an initial pulsed back-gate voltage of 210 V was applied in darkness, inducing the MIT. Subsequently, the Hall bar region was exposed to infrared light (wavelength $\lambda$ of 900 nm) and ultraviolet light ($\lambda$ of 300 nm), both of which triggered a transition from the insulating to the metallic state. Following exposure, the interfacial resistance stabilized in the metallic state, affirming the non-volatile nature of the transition. In the metallic state, the Hall resistance ($R_{xy}$) exhibited a linear dependence on the external magnetic field ($\mu_0$H, see Fig. 4c), with a carrier concentration of $n_H = 2.23 \times 10^{13}\,cm^{-2}$ extracted via the Hall effect. This value is in close agreement with the carrier concentration $n_V = 1.93 \times 10^{13}\,cm^{-2}$, previously measured by the van der Pauw method over a $5 \times 5\,mm^2$ region. Additional pulsed back-gate voltage induced the further non-volatile MIT, demonstrating that conductive pathways written via light pencil can be effectively erased by a pulsed electric field.

Given that both infrared and ultraviolet light produced comparable modulation of the interfacial resistance within the exposed region, we explored the wavelength dependence of this phenomenon. Figure 4d presents the interfacial resistance response across the infrared, visible, and ultraviolet spectral ranges. A sharp decline in interfacial resistance was observed near 1000 nm, indicating a complete recovery of metallic conductivity. A kink around 360 nm corresponds to the bandgap of the STO substrate (~3.4 eV)[19]. Notably, cyclic testing revealed that upon returning to a wavelength of 1100 nm, the interfacial resistance did not revert to the insulating state, further substantiating the non-volatile nature of the transition.

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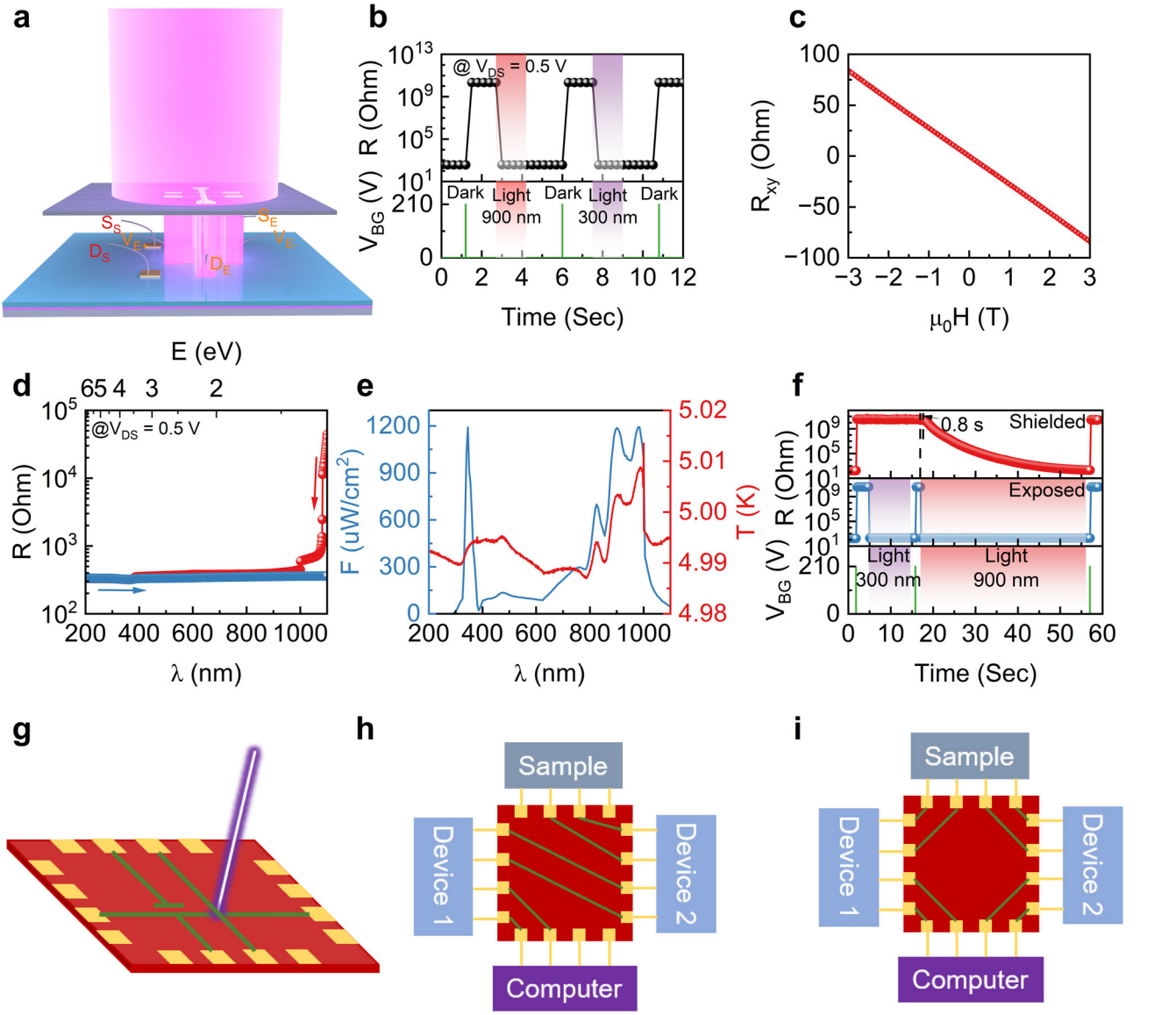


**Fig. 4 | Cryogenic reversible in situ direct-writing logic circuits. a** Schematic of light exposure on the sample surface with a hall bar patterned mask. The left side is shielded, and the right side forms a Hall bar pattern. **b** Modulation of the C-2DEG interface state. A 210 V back-gate pulse (1 ms) induces an insulating state, which transitions to a persistent conductive state after exposure to infrared (900 nm, 1.2 s) or ultraviolet light (300 nm, 1.2 s). **c** Hall resistance as a function of the external magnetic field measured in darkness following Hall bar pattern exposure. **d** Resistance of the insulating C-2DEG interface as a function of wavelength. Red and blue curves represent measurements for decreasing (1100–200 nm) and increasing (200–1100 nm) wavelengths, respectively. **e** Light flux (blue) and thermocouple temperature (red) versus wavelength (290–1100 nm). Temperature closely tracks light flux, suggesting thermal effects. **f** Source-drain current response in shielded and exposed regions. Ultraviolet light causes a localized non-volatile transition in the exposed region, while infrared light induces a gradual conductive transition in shielded areas due to thermal effects. **g** Conceptual illustration of ultraviolet laser direct-writing for creating conductive pathways. Schematic representations of serial (**h**) and parallel (**i**) logic circuit switching between cryogenic devices using "optical pencil" and "electric eraser" technology.

The potential contribution of thermal effects associated with laser exposure warranted further investigation. To assess this, temperature variations induced by the laser were measured using a thermocouple (see Fig. 4e). The thermocouple response closely followed the light flux distribution, showing a pronounced increase near 1000 nm, which coincided with the steep decline in interfacial resistance. This finding suggests that thermal effects, arising from laser exposure, promoted evaporation of the gas ice layer, thereby restoring the interfacial metallic state.

In contrast, the ultraviolet light of 300 nm, characterized by a significantly lower light flux, elicited no discernible thermocouple response, indicating a non-thermal mechanism. To verify this, two additional electrodes were introduced in the shaded region adjacent to the Hall bar (see Fig. 4a), enabling a comparative study of electrical transport properties in both shaded and exposed regions. Following the application of a back-gate voltage pulse, both regions exhibited the non-volatile MIT. Under ultraviolet light exposure ($\lambda$ of 300 nm), only the patterned region transitioned to the metallic state, while the shaded region remained insulating (see Fig. 4f). This localized response confirmed the non-thermal nature of the ultraviolet-induced transition. The metallic state in the exposed region persisted post-exposure, and the transition was reversible through the application of a pulse back-gate voltage, demonstrating repeatability.

Under infrared light ($\lambda$ of 900 nm), both the patterned and shaded regions transitioned to the metallic state. However, the shaded region required approximately 40 s to fully recover its metallic state, indicative of a thermally driven process. Prolonged infrared exposure caused thermal diffusion, leading to evaporation of the charged gas ice layer in

the surrounding areas and gradual restoration of conductivity. These findings highlight that low-flux ultraviolet light enables localized, non-volatile insulator-to-metal transitions with ultra-low switching power, whereas infrared light induces broader, thermally driven transitions. These findings enable laser-based direct-writing of conductive pathways (see Fig. 4g) and erasure via back-gate control, facilitating parallel (see Fig. 4h) and serial (see Fig. 4i) switching of cryogenic devices. As illustrated in Fig. S9, localized erasure can also be achieved by tailoring the geometry of the back-gate electrode. Therefore, this approach offers a scalable platform for in situ, large-scale fabrication of integrated circuits and devices in cryogenic environments, particularly when extended beyond gas ice layer techniques in future studies.

In summary, we demonstrated two in situ fabrication approaches for cryogenic devices based on the C-2DEG interface. First, by using a fully metallic C-2DEG interface as the channel, we successfully eliminated the Schottky barrier at metal-semiconductor contacts, significantly reducing $V_{DS}$ and enabling a FET with low contact resistance and a high $I_{on}/I_{off}$ ratio in cryogenic environments. Additionally, we confirmed that reducing the thickness of the single-crystal STO dielectric layer can significantly lower $V_{BG}$-on. This finding suggests that, in the future, techniques such as water-assisted transfer of freestanding membranes may allow for downsizing gate dimensions, potentially enabling large-scale, ultra-low-power silicon-integrated FET arrays.

However, with the current gate dimensions, the power consumption required for channel activation remains non-negligible. To address this, we developed an alternative method of channel activation based on low-flux ultraviolet laser excitation, enabling localized activation without affecting the interface states in adjacent regions. This approach introduces a cryogenic, in situ, reversible direct-writing technique. By controlling the laser scanning paths and shapes, this method could facilitate the in situ laser direct-writing fabrication of devices and logic circuits in cryogenic environments in the future.

## Methods

### Sample growth

$LaAlO_3/LaFeO_3/SrTiO_3$ samples are epitaxially grown on a (001)-oriented $TiO_2$-terminated $SrTiO_3$ substrate using pulsed laser deposition (PLD, KrF, $\lambda = 248$ nm) at 700 °C. The fluence ranges from 1 to 1.5 J/cm$^2$, and deposition frequency is 2 Hz, and the oxygen pressure is maintained between $2 \times 10^{-5}$ to $1 \times 10^{-4}$ mbar. 5-u.c. of LFO followed by 10-u.c. of LAO thin films were grown sequentially. The growth was monitored by Reflection High-Energy Electron Diffraction (RHEED). The as grown samples were gradually cooled down to room temperature at a rate of 30 °C/min while maintaining constant oxygen pressure. Ti adhesive layers and Au electrodes were deposited using magnetron sputtering.

### Transport measurement

The top electrode penetrates the LAO and LFO films by a wire bonder, creating a connection to the two-dimensional electron gas interface. The sample size constructed in this work was $5 \times 5 \times 0.5$ mm and $5 \times 5 \times 0.2$ mm. Cryogenic environments were obtained through a PPMS setup (Quantum Design DynaCool system). Wires and optical fiber with a diameter of 600 µm were integrated using a home-made multifunction probe. The self-constructed wavelength continuously variable light source system comprises a xenon lamp source (PF300-T8 300 W) and a monochromator (CEAULIGHT CEL-IS151), and current and pulse voltage were read and output by the Keithley digital source meter group (6517A, 2613B, 2450 & 2400). The Hall bar channels defined by the employed shadow mask have a width of approximately 50 µm.

## Data availability

The data that support the findings of this study are available from the corresponding author upon request. Source data are provided with this paper.

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## Author contributions

Z.L. directed the project, supervised sample growth and reviewed the manuscript. Y.H. and L. Wang contributed equally to this work. Y.H. did most of the design and fabrication of the devices, performed the experiments and wrote the manuscript. L. Wang did the mask experiment and contributed to manuscript writing. T.L., L. Wei, S.H., J.L., W.X., L.L., and M.H. contributed to measurements and data analysis. Z.S. contributed to manuscript writing. K.C., Y.G., G.R. and G.K. reviewed the manuscript. All the authors discussed the results and commented on the paper.

## Competing interests

The authors declare no competing interests.

## Additional information

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