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Tunable flexible artificial synapses: a new path toward a wearable electronic system

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The flexible electronics has been deemed to be a promising approach to the wearable electronic systems. However, the mismatching between the existing flexible deices and the conventional computing paradigm results an impasse in this field. In this work, a new way to access to this goal is proposed by combining flexible devices and the neuromorphic architecture together. To achieve that, a high-performance flexible artificial synapse is created based on a carefully designed and optimized memristive transistor. The device exhibits high-performance which has near-linear non-volatile resistance change under 10,000 identical pulse signals within the 515% dynamic range, and has the energy consumption as low as 45 fJ per pulse. It also displays multiple synaptic plasticity features, which demonstrates its potential for real-time online learning. Besides, the adaptability by virtue of its three-terminal structure specifically contributes its improved uniformity, repeatability, and reduced power consumption. This work offers a very viable solution for the future wearable computing.

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INTRODUCTION

The flexible electronics has become a very attractive field. Tons of flexible devices have been reported during the past decades, with different device structures and materials, working as sensors,[1–3] computing blocks,[4] or display units.[5,6] For noncomputing components, the achievements are very satisfactory. Lots of devices step toward practical use, for example, the electronic skins[3,7,8] and the wearable sensors.[1] However, when it comes to the computing component, the situation is not comforting. The existing flexible transistors are still difficult to have comparable performance to silicon devices. Although there were some demonstrations for flexible circuit[4,9] based on the conventional computing architectures, e.g., *von Neumann and Modified Harvard*, the functions and performance were very limited and clearly insufficient for processing those numerous less structured[10] information receiving from the environment and the human body. Without a powerful flexible computing block, the final goal of having a full-wearable electronic system is far beyond our reach.

In recent years, the brain-inspired computing has been proved to have the features of high parallelism, energy efficiency and fault tolerance,[11] which would enhance the performance dramatically. As a proof-of-concept, the artificial neural network has already achieved a success on software level using the and central processing unit (CPU) and graphics processing unit (GPU) on conventional computers and proved its effectiveness on cognitive computing.[11] With the help of this new approach, we will have much better chance to deal with the numerous and abstract information processing tasks, which is the main role for the wearable systems. But a direct transplant of that way into the flexible computers is hard, the same dilemma still exists because of the unsatisfied flexible device performance.

The new neuromorphic architecture can be a better solution. On one hand, it has the merged computing and memory blocks, which have not only the features of the brain-like computing, but also no bottle-neck of conventional computing architecture.[12,13] On the other hand, the characteristics of brain-like computers which is fault-tolerant and highly parallel lower the requirements on device performance (such as speed and yield) significantly, thus offers a new chance for flexible device-based computers. By having a flexible hardware implementation of the neuromorphic system, the neuromorphic computing and the flexible electronics could achieve a mutual promotion thus lead to a high-performance wearable computing system.

For a flexible neuromorphic system, the key element is the flexible artificial synapse which exhibits synaptic plasticity—i.e., *the values of weights are adaptable to the stimulating history*.[14] Nowadays, more and more works about memristor-based synaptic devices are emerging because of the bright future for their using in neuromorphic computers.[15,16] For example, a multiplier and memory array need hundreds of transistors in a CPU-/GPU-based artificial neural network, while in a neuromorphic system, only one synaptic device will be sufficient to achieve the same function. This further facilitates the realize of flexible neuromorphic system by decreasing the required flexible device number. However, the artificial synapses with physical flexibility are rare. Up to date, there are only few published works achieved flexible artificial synapse,[17–19] but most of them have the same or even worse problems as rigid synaptic devices, which suffered from low multilevel states number, high energy consumption, poor

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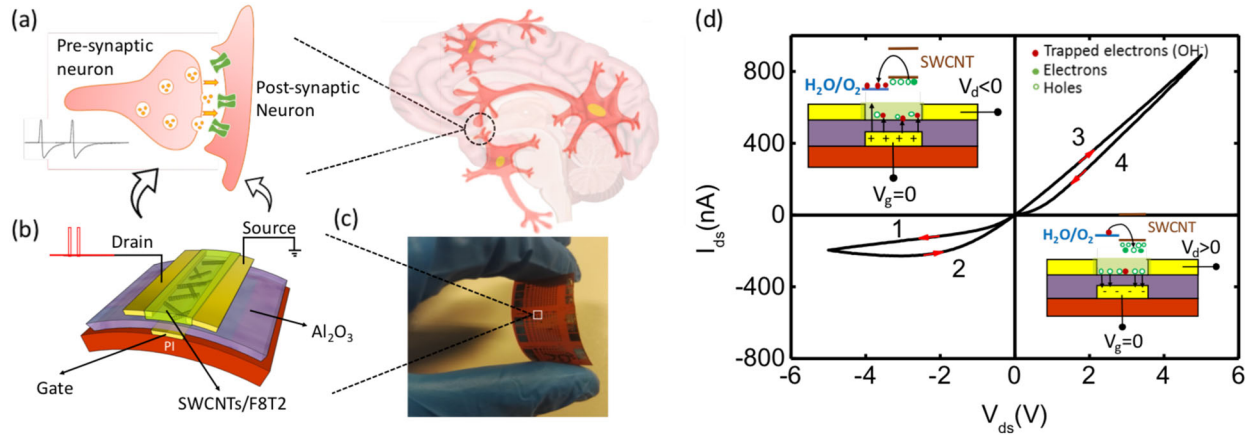

Fig. 1 Schematics and working mechanism. Schematics of (**a**) a biological synapse and (**b**) artificial synapse. **c** Photograph of flexible artificial synapses. **d** Pinched $I_{ds}-V_{ds}$ curve with V_g set as 0 V (L = 20 μm, W = 50 μm), and the insets indicate the mechanism of the memristive feature

repeatability and uniformity, etc., thus are still obstructing their practical use. This is mainly caused by the unsatisfied working mechanism, such as less-controlled forming and rupture of conductive filaments.[20,21] Although some efforts already have been done to overcome these shortcomings, the best choice of working mechanism, materials and device configuration is still under investigation.

Hysteresis during electrical characterization is a well-known effect in electronic devices.[22,23]Commonly this effect is believed to be a weakness because it increases the instability. However, since hysteresis always bonds with the stimulation-history-related current, it can actually work as the source of synaptic behavior. In regard to its application as an artificial synapse, the source of hysteresis should induce prominent hysteresis, stably exist, and have a simple fabrication process. There were evidences showed that the H_2O/O_2 redox couples near the dielectric–channel interface in the organic transistors trap electrons through electrochemical reactions, causing an prominent hysteresis behavior.[24,25] The reaction occurs throughout the channel area, working as an average effect, which means that its reliability is higher than that of the randomly-formed filament mechanism. Also, the H_2O/O_2 redox couples are unlimited in nature, offering a near-intrinsic large hysteresis in the device, and this feature provides a simple fabrication process and broad option of materials. Among all the alternative materials, single-wall-carbon-nanotube's (SWCNTs) exceptional stability in various environments and mature production technology further ensure its potential for mass production. More importantly, a new device configuration instead of the commonly used real or *pseudo* two-terminal devices[26] can be adopted to optimize the device performance by taking full use of the three terminals in a field-effect transistor structure. This configuration minimizes power consumption (both static and dynamic power consumption) and offers a chance to effectively modulate the device after its fabrication, improving the device functionality, uniformity and repeatability.

In this work, by setting the drain and source of a field-effect transistor as presynaptic and postsynaptic neurons (the source terminal was always connected to the ground) and using the gate as a tuning terminal (Fig. 1a, b), an artificial synapse based on a gate-tunable flexible memristive transistor (FMT) was fabricated using a convenient processes based on SWCNT and polymer composite on a hydrophilic dielectric layer. The implemented prototype devices have memristive features that are comparable to those of state-of-the-art inflexible and flexible synaptic devices,[16,17,27] which has the near-linear nonvolatile resistance change under 10,000 identical pulse signals over a wide range (515% of the lowest current), with a power consumption as low as 45 fJ. Furthermore, the gate-tunable behavior helps improve the uniformity, repeatability, and even power consumption of the devices. Various synaptic plasticity were also demonstrated, such as paired-pulse facilitation (PPF), long-term potentiation (LTP), and spike-timing-dependent plasticity (STDP). The artificial synapse can either be excitatory or inhibitory, depending on the gate modulation. The device could keep functioning under bending conditions thus strengthened its potential in wearable applications. Our FMT showed superiority than the existing flexible artificial synapses on various aspects, such as the energy consumption, device dimension, states capacity, states linearity,[17,19] and showed more kinds of synaptic plasticity.[17–19] To further illustrate its applicability, a simulated neuromorphic computing network was implemented in a single-layer modeled with the governing function extracted from the implemented flexible artificial synapse.

RESULTS

Working mechanism

A FMT was fabricated using a SWCNT network/polymer composite combined with a Al_2O_3 dielectric. The schematic structure and photograph of the FMT are shown in Fig. 1b, c. A hydrophilic Al_2O_3 dielectric was used to induce more H_2O/O_2 redox couples as trap states. SWCNTs and a poly(9,9-dioctylfluorene-co-bithio-phene) (F8T2) blend were dip-coated in the channel area (see Methods section). The entire process adopted the simplest field-effect transistor fabricating process, and the polymer was mainly used for better dispersion and film formation of SWCNTs. In addition, it offered visible light absorption for further photoelectrical application potential.

A prominent anticlockwise shaped hysteresis in the transfer characteristic curve was observed in our devices (Fig. S1, supplementary information). The chemical potential of the H_2O/O_2 redox couple (−5.3 eV when pH = 6)[24] lies near the top of SWCNTs' valance band (−4.9 eV),[28] which enables electrons to easily transfer from SWCNTs to H_2O/O_2 redox couples via the electrochemical reaction indicated in the following equation[24]:

$$2H_2O + O_2 + 4e^- \leftrightarrows 4OH^-.$$

The electrochemical potential difference between the SWCNT and H_2O/O_2 redox couples can be controlled by the applied gate electrical field.[24,25,29] This reaction traps electrons as immobile negative centers (OH^-) near the dielectric–channel interface, leading to an electrostatic screening of the gate field, which affects the channel current I_{ds}. Because this reaction requires a long time to achieve an equilibrium state, the population of

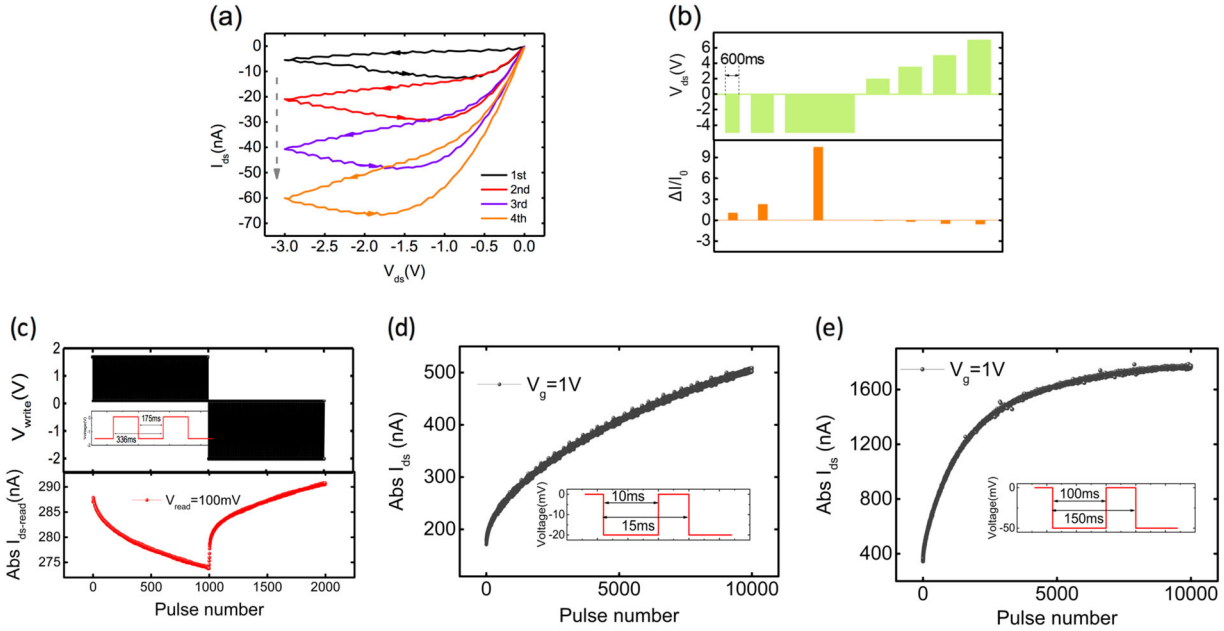

Fig. 2 Memristive features of the FMT. **a** Consecutive *I–V* scanning at a negative V_{ds}. **b** Responses to pulses with different intensities and durations. **c** Read current for 1000 identical positive pulses ($V_d = 1.7$ V, 175 ms pulse width, 336 ms period) followed by 1000 identical negative pulses ($V_d = -2$ V, 175 ms) with $V_g = 0$ V. After each pulse, the read current was measured at $V_d = 0.1$ V (small enough at $V_g = 0$ V to eliminate the effect of the reading process) to show the current change induced by the previous pulse. The interval between two writing pulses was 161 ms. **d** Response to 10,000 pulses (−20 mV, 10 ms pulse width, 15 ms period) at $V_g = 1$ V. **e** Response to 10,000 pulses (−20 mV, 100 ms pulse width, 150 ms period) at $V_g = 1$ V. **a, b** were tested on a device with L = 20 μm and W = 50 μm, (**c**) was tested on a device with L = 80 μm and W = 100 μm, (**d, e**) were tested on a device with L = 30 μm and W = 200 μm

electrons trapped near the interface is different according to the stimulate history; thus, stimulation-history-related states show up. It is worth mentioning that the hydrophilic dielectric (not restricted to Al_2O_3) is important for the existence of abundant trap states. For comparison, smaller hysteresis and less remarkable memristive functions have been observed in hydrophobic polymer dielectric transistors (Figs. S2, S3). This means that hydrophobic dielectric layers were not good-enough candidates for implementation in memristive devices. Also, we think the hydrophilic dielectric layers can provide adequate H_2O/O_2 redox couples under normal environment, so the relative humidity change in the atmosphere would not change the device performance dramatically. Figure S4 indicates that the hysteresis gaps of the FMT are nearly the same under different relative humidity, which further strengthens our assumption. Then, the fabricated FMTs were characterized electrically to test their properties as artificial synapses.

Memristive features

Figure 1d shows the typical current–voltage characteristics of FMT. V_s and V_g were set to 0 V, and the insets illustrate the working mechanism. The pinched hysteresis loop across points $I = 0$ and $V = 0$, a fingerprint of a memristor, indicates the memristive characteristic of the device.[30] We can divide the process into four stages. At stage 1, the electrochemical potential of the SWCNTs was pushed higher than that of the H_2O/O_2 redox couples thus more electrons were trapped and accumulated near the dielectric layer. And at stage 2, most of the previously trapped electrons were still there due to the slow equilibrium speed, and the continued trapping process created new states different from those in stage 1. When V_d was positive ($V_{gd} < 0$) (stage 3 and 4), the trapped electrons were gradually extracted. Less trapped electrons in stage 4 compared with stage 3 led to a smaller I_{ds}. Figure 2a shows four consecutive sweeps, which were measured across the device. For consecutive negative V_d sweeps, I_{ds} increased compared with the previous sweeps (also backward sweep exceeded its forward sweep). This behavior specifically indicated the time-and-voltage-related resistance,[30] which fits the definition of a memristor. Figure S5 (supplementary information) shows the consecutive sweep for positive voltage.

In neuromorphic computing, pulsed signals are more expected to occur. The response to V_d pulses with different amplitude values and durations is demonstrated in Fig. 2b. The I_{ds} change over the initial current ($\Delta I/I_0$) after each pulse was used to indicate the degree of responses to different V_d pulses. Generally speaking, the higher and longer the positive/negative voltage pulse, the more significantly I_{ds} decreased/increased. FMTs showed a bidirectional response to the inputs. The results in Fig. 2c show the I_{ds} of 1000 identical positive V_d pulses and 1000 identical negative V_d pulses. With same input pulses, the device conductivity gradually changed, which is the key feature of a memristive device.

A series of characterizations was performed to demonstrate the key metrics of FMTs, such as the ability of continues resistance change, energy consumption, dynamic range and linearity. We measured the response to 10,000 V_d pulses with a 10 ms width and 20 mV amplitude at $V_g = 1$ V. From Fig. 2d, we observe that the memristive feature was maintained with good linearity during the entire test, which provided a large amount of states. To reduce energy consumption, a V_d pulse with a low amplitude was applied, which led to a relatively small I_{ds}, as well as gate leakage (~1 nA). The total energy consumption per spike was as low as 45 fJ, which was comparable or even lower than a biological synapse.[10] As shown in Fig. 2d, I_{ds} did not saturate. To obtain the full dynamic range, pulses with longer widths were used. Figure 2e demonstrates that I_{ds} changed by 515% compared with the initial current, which indicates its large dynamic range. The large amount of resistance states with low energy consumption was crucial for neuromorphic computing, which however has not been successfully reported yet. The demonstrated minimal resistance changes were large which reflected the less-controllable working

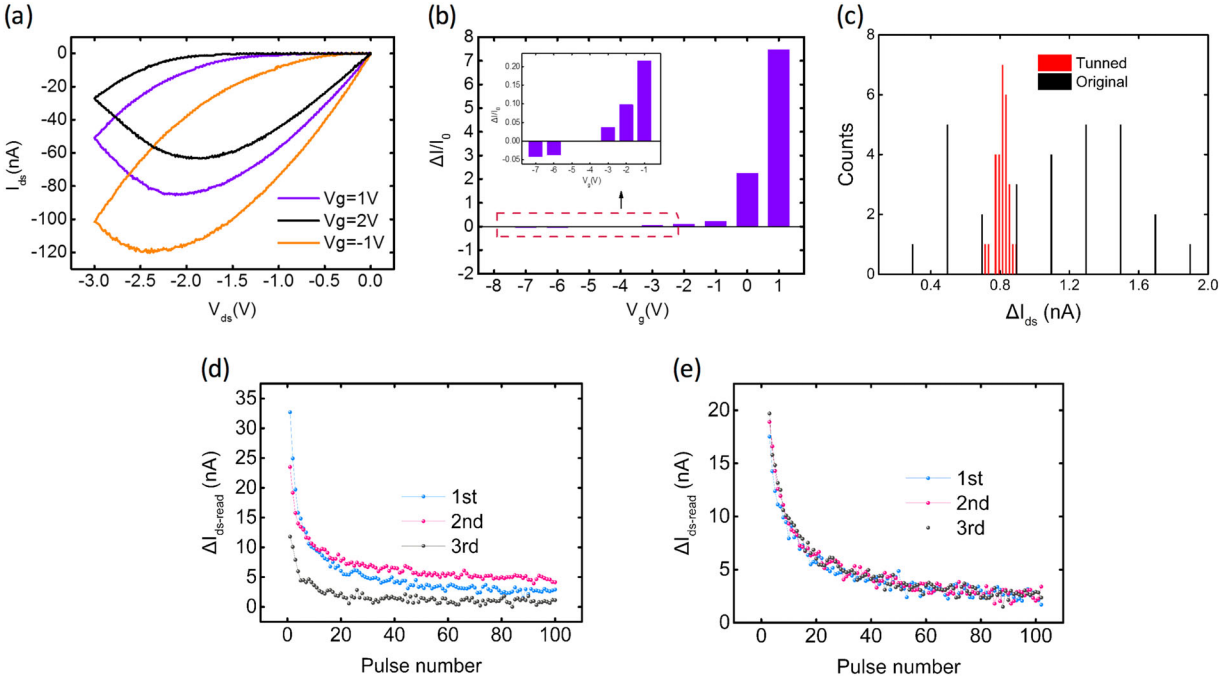

Fig. 3 Gate-tuning function of the FMT. **a** *I–V* scanning at different V_g biases. **b** Responses to identical V_{ds} pulses (−5 V, 1 s) at different V_g. **a, b** were tested on a device with L = 20 μm and W = 50 μm. **c** The current change per pulse at $V_{ds} = -4$ V 10 ms for 28 devices at the same V_g = 0 V (original) and different V_g (tuned). **d** Three tests without gate initialization. **e** Three tests with V_g from −2 V to 2 V, $V_{ds} = 0.1$ V *IV*-scanning initialization. **c–e** were tested on a device with L = 60 μm and W = 100 μm

mechanism. To achieve a resistance change, high-intensity voltage signals were needed, and that would increase the current thus lead to a high energy consumption. What was worse, the dynamic ranges of those devices were small so that resistance change saturated quickly, and this was also a reason of the limited resistance state number. In our FMT, the required input voltage across the presynaptic and postsynaptic terminals was successfully compromised by the gate terminal, thus showed an improved performance. The gate terminal benefited the FMT in various aspects, and we will discuss more in the next section.

Gate-tuning function

Due to the structure and working mechanism, the functions of this FMT can be extended using the third terminal, the gate, which benefits device performance. Figure 3a shows that with different gate voltages V_g, the *I–V* curves are different, suggesting a gate tuning possibility. This behavior is further illustrated in Fig. 3b, where the amplitude and sign of the current change $\Delta I/I_0$, which is caused by a single V_d pulse (−5 V, 1 s), can be modulated according to the voltage value V_g at the gate terminal as follows: a positive V_{gd} ($V_{gd} = V_g - V_d$) increases I_{ds} after a V_d pulse, while a negative V_{gd} decreases I_{ds} after a V_d pulse. In other words, while keeping V_d fixed, the amplification/attenuation function of the memristor can be tuned using V_g by changing the sign of V_{gd}. Moreover, it was observed that the magnitude of amplification and attenuation was positively correlated with the value of V_{gd}.

There were three aspects by which the gate tuning function benefited device performance. First, the fabrication process introduces variation between devices and decreases uniformity. Unfortunately, the widely used conductive filament memristors' uncontrollable working mechanism has made this issue more severe and hard to be fixed because of the two-terminal nature.[18,31] Using the gate tuning function, the device variation could be compensated by applying an extra adjusting voltage on the gate terminal. As a proof-of-concept, Fig. 3c demonstrates a uniformity improvement by the gate tuning function. In a lot of applications which use paired-memristors as a single synapse (as the case will be shown in simulation section), the difference in current Δ*I* over each input pulse matters most instead of the current value itself.[11] And since the linear region was more favorable, we here used the average Δ*I* in the linear region (which can be roughly calculated by dividing the total current change by the pulse number in the linear region) as an indicator of the device feature. It is obvious that the tuned devices showed obvious narrower distribution range comparing to the original devices thus improved the uniformity.

Repeatability in a device is also of paramount importance. Gate tuning can be used to increase the performance repeatability of a FMT. The same characterization was performed on one device for several times. For each test, the Δ*I*-pulse relationships were inconsistent (see Fig. 3d). However, by initializing the device with V_g scanning, the Δ*I*–pulse relationships on one device were nearly identical, as shown in Fig. 3e. This valid method, which was provided by the gate terminal, not only ameliorated repeatability but also avoided extra initializing operations on working terminals (source and drain), which was always difficult in real fabricated circuits. A more detailed discussion of the gate tuning function can be found in the supplementary information.

Finally, gate tuning can decrease energy consumption. The device had zero static power consumption since the input voltage and the output current were synchronized which means if there were no input spikes, there were no energy consumption. While applying input signals, the key parameter V_{gd} was the potential difference between V_g and V_d, which means that either V_g or V_d provide equivalent contributions to V_{gd}. Since the trapping and detrapping of electrons was mainly controlled by the amplitude and sign of V_{gd}, the current change Δ*I* over each input pulse could be controlled by either V_g or V_d. To obtain a greater Δ*I*, the amplitude of V_{gd} needed to be larger. However, application of a large voltage V_d to the drain would eventually increase I_{ds} and, consequently, increase energy consumption. Instead, keeping the gate voltage V_g at a high amplitude and the drain voltage V_d at low amplitude, made the device more energy-efficient and

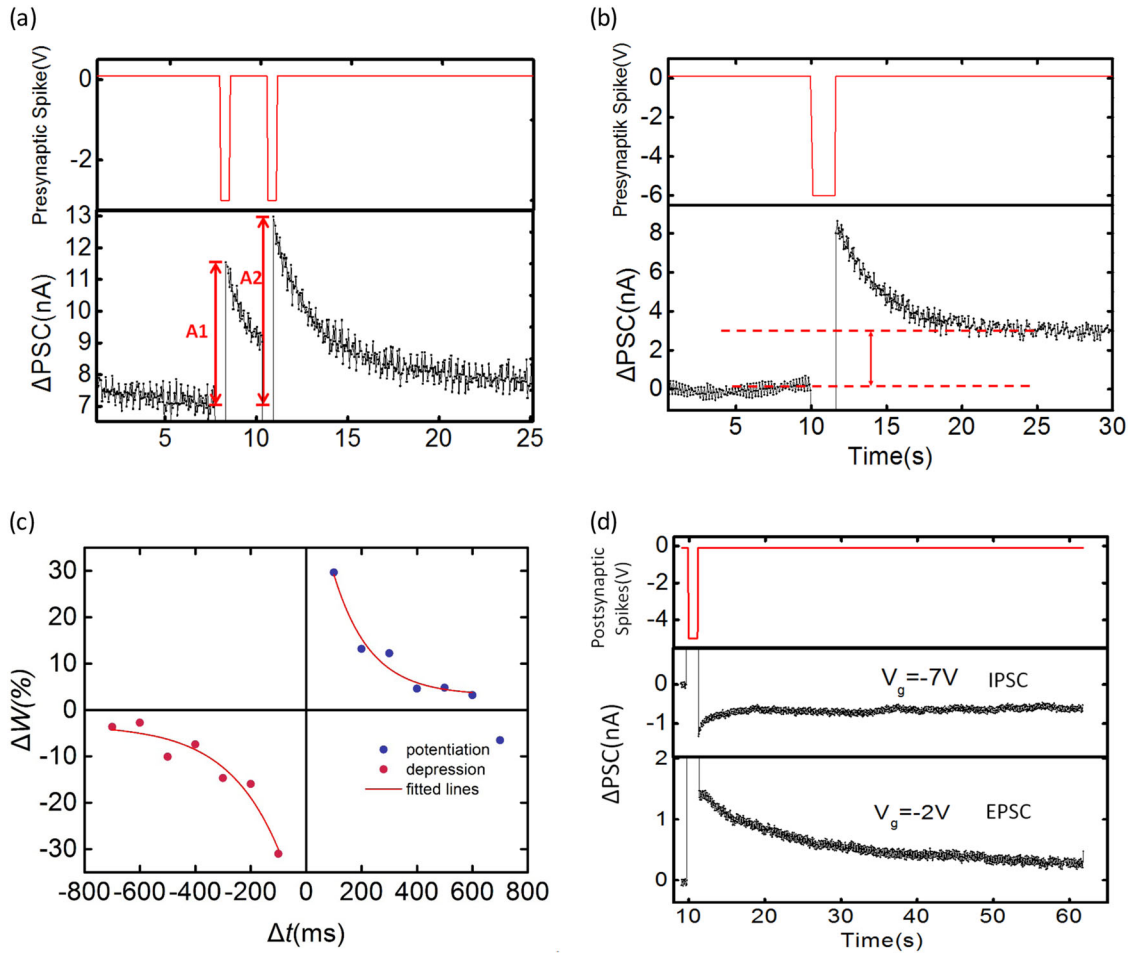

Fig. 4 Synaptic plasticity of the FMT. **a** PPF and **(b)** LTP in an artificial synapse. A 100-mV reading voltage was applied before and after the spike to monitor the current change ΔPSC with the minimized effect induced by the reading voltage. **c** STDP follows the asymmetric Hebbian rule. **d** Excitatory synapses were achieved for $V_g = -2$ V, inducing an excitatory postsynaptic current (EPSC), while $V_g = -7$ V, inducing an inhibitory postsynaptic current (IPSC). Both ΔPSCs were induced by a presynaptic spike with −5 V, 1 s. All data were tested on a device with L = 20 μm and W = 50 μm

avoided performance loss. The previously shown energy consumption, low to 45 fJ per pulse, which is demonstrated in Fig. 2d, was obtained in this type of scenario, and Fig. S6 further illustrates this low-power contribution.

Synaptic plasticity

Synapse plasticity is believed to be the biological foundation of learning and memory.[32] Here, different modes of synaptic plasticity were realized in FMTs. Voltage spikes on two terminals of the memristor represented the presynaptic and postsynaptic spikes and triggered I_{ds} as a postsynaptic current (PSC), which in this case represented the synaptic weight (Fig. 1a, b).

For a synapse, STP refers to the strengthening or weakening of the synaptic weight over a short period of time, normally from tens of milliseconds to a few minutes,[32] and is involved in important brain functions, such as learning and attention.[33] PPF is a type of STP that deals with two close successive spikes on a synapse. PSC, which is evoked by the second spike, is enlarged compared with the former spike. Figure 4a shows the PPF effect in our artificial synapse. Two identical presynaptic spikes (−3 V for 450 ms with a 2-s interval) were applied to the presynaptic neuron, and the later spike induced a larger PSC. Compared with the previous spike, ΔPSC, which was induced by the second spike, increased by 12%.

Unlike STP, LTP normally lasts for minutes or more. In the human brain, LTP forms the basis of memory and learning.[34,35] To obtain LTP, a spike with a −6 V amplitude and 1450 ms duration was used as the presynaptic spike (with the same reading voltages as in the PPF testing), as shown in Fig. 4b. PSC increased with the spike and then decayed after it was over, but to a higher level than the initial state, for tens of seconds to minutes. This long-term facilitation of synaptic weight is similar to the LTP in a biological synapse. As a contrast, a spike with a low amplitude and short duration (−3 V, 450 ms) was applied to the artificial synapse, and PSC decayed to the initial state immediately after the spike passed (Fig. S7). These results indicate that stronger stimulation leads to a longer modification, similarly to the corresponding physiological process in the human brain. In Fig. 3b, we have already seen that the gate terminal could modulate the degree of the resistance change. The testing process was similar with that of the STP and LTP. So, it is natural to believe that the intensity of STP and LTP would be related to the gate voltage.

Among synaptic plasticity, STDP has been widely studied and used in both biological and artificial neuron networks.[36] With the development of neuromorphic engineering, the STDP mechanism has been studied further and used in various applications.[37,38] Taking the most commonly used asymmetric Hebbian learning rule as an example, if a presynaptic spike precedes a postsynaptic spike, the synaptic weight will be strengthened. By contrast, if the presynaptic spike arrives later than the postsynaptic spike, the

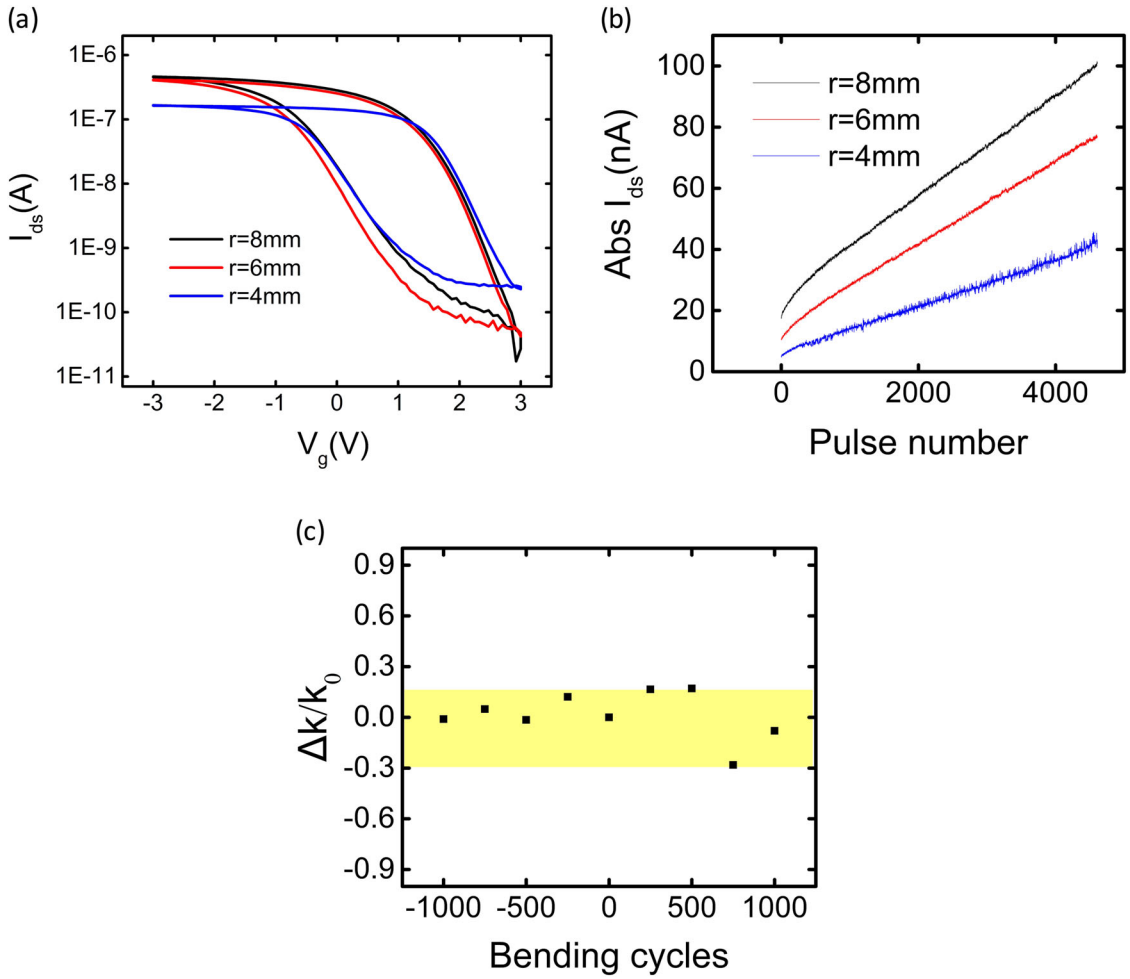

Fig. 5 Bending tests of the FMT. **a** I_{ds}–V_{gs} curve under different bending radiuses. **b** Response to consecutive identical pulses (−1 V, 10 ms pulse width, 15 ms period) at $V_g = 0.5$ V. **c** Variation of the ΔI per pulse under repeated bending actions

synaptic weight will be depressed. The spike interval between the presynaptic and postsynaptic neurons was $\Delta t = t_{post} - t_{pre}$, and the synaptic weight change from one spike was calculated as $\Delta W = I_{post} - I_{pre}/I_{pre}$. The result is plotted in Fig. 4c. The proposed artificial synapse in our study clearly exhibited the STDP. The larger Δt, the smaller the change observed in the synaptic weight. The data obtained can be fitted with a simple exponential curve:

$$W = A * e^{-(\Delta t/\tau)} + B$$

where $\tau_1 = 132$ ms and $\tau_2 = 186$ ms. In addition, the SRDP, which is another important feature in the human brain[39]; the relation between synaptic weight change ΔW; and the spike intervals are shown in Fig. S8. The SRDP was another feature of a biological synapse, which always indicated a different response to different frequent spikes. The SRDP feature of the FMT was measured and shown in Fig. S9.

Typically, in the human brain, a neuron is either excitatory or inhibitory. It is the role of specific neurotransmitters to determine the type of neuron, while the neural spikes are always the same. In such a case, when we try to mimic an excitatory or inhibitory neuron or synapse, it is important to keep the input, namely, the presynaptic spikes, the same. For an artificial synapse with only two terminals, it is rather difficult to modulate its type without changing the applied signals or device configuration (the conventional way of achieving the transformation was to use a reversed input signal). Our artificial synapse, due to the gate tuning function, allowed us to modify the synapse type during operation once the network was established. Specifically, the type of function, an excitatory or inhibitory synapse, can be achieved in one device with the same input (Fig. 4d). This feature allows for a more flexible network structure and paves the way to new algorithms and system architectures.

Physical flexibility

Physical flexibility was one of the key feature of the FMT. The functioning and endurance of the FMT under bending conditions were thus useful to evaluate its feasibility as a building block of the flexible computer. We tested the transfer characteristic curves and the pulse signal responses of a FMT under different bending radius. Figure 5a shows the comparison of the transfer characteristic curves under 4 mm, 6 mm, 8 mm bending radius, respectively. With the bending radiuses was larger than 6 mm, the current decrease was negligible. But for the bending radius below 6 mm, then the current decreased about 60%. The pulse tests also reflect this trend. From Fig. 5b, we can see with bending radius smaller than 4 mm, the ΔI per pulse (can be seen as the slope k) was decreased. Both the hysteresis and the memristive features were sustained under bending. The test setup is shown in Fig. S10.

The endurance after repeated bending operations was also tested. From Fig. 5b, we can see the current–pulse relationship has good linearity, we here use the slope k as an indicator of the ΔI per pulse. The slope without bending was k_0, after every 250 bending, the same device was characterized with the same pulse test in Fig. 5b and extracted the slope k. We here use k–k_0/k_0 to indicate the

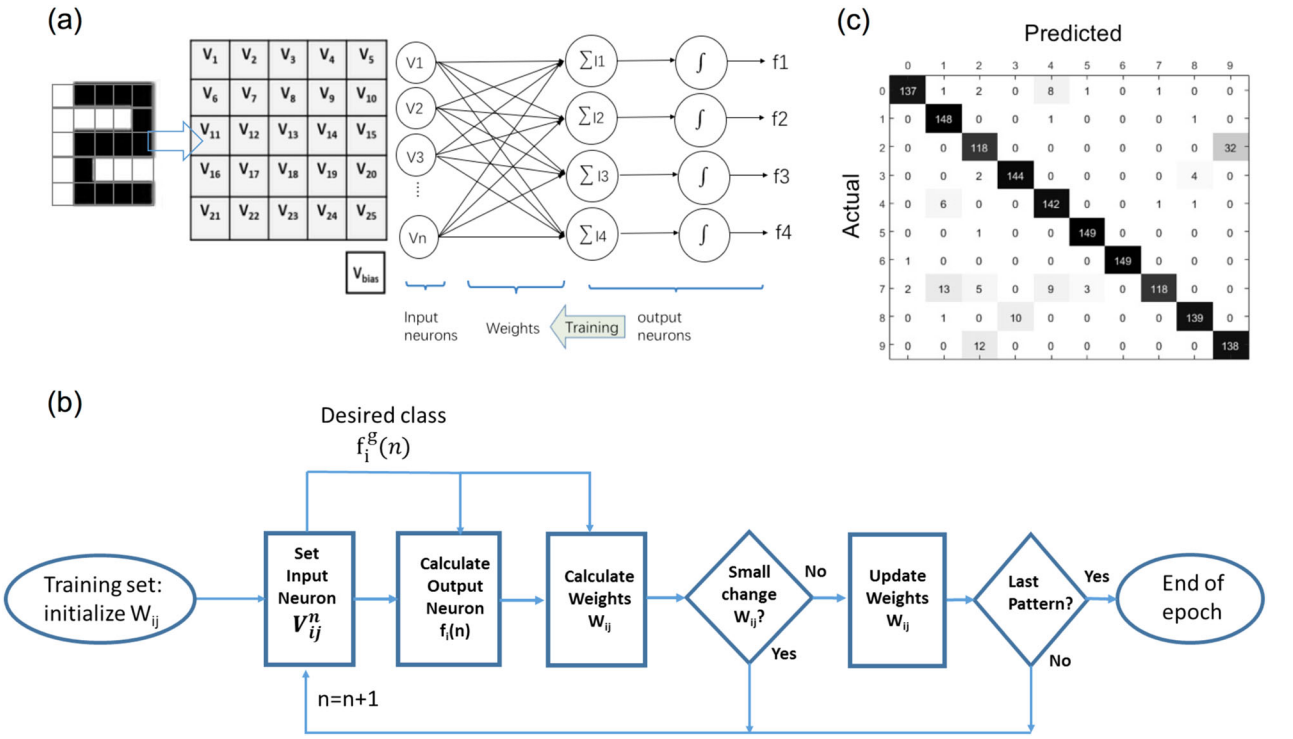

Fig. 6 Simulated neuromorphic network using FMT data. **a** Single-layer perceptron to classify 5*5 binary images. **b** Flow chart of the training algorithm. **c** Classification results, shown as a confusion matrix

variation caused by the bending operations. The bending was performed in two directions; the negative bending numbers corresponds to the negative radius bending. The bending radius was ±6 mm. The result is shown in Fig. 5c. The variation within 1000 bending operations shows not obvious trend. The average variation was about +1.3%, and was about 9.9% if we consider the absolute variation. This result also indicated that the change was reversible. The performance would get back to the initial level if the substrate was released back to flat. So, the current decrease shown in Fig. 5a, b was assumed to be cause by the extended channel length while bending.

Simulated neuromorphic network

To demonstrate the capabilities of the implemented artificial synapses as building blocks of a neural network, a simple single-layer perceptron[12] was simulated using the operational model obtained from the experimental characterization of the implemented artificial synapse. The learning task required the neural network to identify 10 numbers, 0–9, defined by 10 different patterns and represented by 25 elements in a 5*5 black-white matrix, see Fig. 6a. The function was implemented by training and processing a neuromorphic network with 26 inputs, V_j, with $j = 1, 2, \ldots 25$, for pixel input and V_{26} for constant bias, as shown in Fig. 6a. Four outputs of f_i, ($i = 1, 2, 3, 4$) were calculated from:

$$f_i = \tanh\left(a * \sum_{j=1}^{26} W_{ij} V_j\right)$$

These outputs were used to show the results of learning and processing. Thus, 4*26 synapses with trainable synaptic weights W_{ij} were used to build the neural network, and each synapse consisted of a differential pair (two memristors, one for potentiation and the other for depression) to make the synaptic weights be approxiemately zero. In this type of neuromorphic network, the Manhattan update rule,[40] which is shown in the supplementary information, was chosen to train the system and update the synapses weights. The flow chart of the training algorithm is shown in Fig. 6b. The four outputs were encoded to represent ten different patterns, as indicated in Table S1. In total, 1500 different patterns containing 150 noisy versions of each target pattern were used for training, and another 1510 patterns were used for testing. The training and testing pattern sets are shown in Fig. S10. The average accuracy was 92.13%, and all the testing results are shown in the confusion matrix in Fig. 6c. The matrix was filled with the number of results that correspond to different conditions. If the predicted pattern (the input pattern) was the same as the target pattern (the pattern evaluated by the system), then the recognition was correct, which lies on the diagonal of the matrix. This demonstration shows the feasibility of our artificial synapse for neuromorphic implementation.

DISCUSSION

In conclusion, a new approach of wearable electronic system was proposed by combining flexible devices and the neuromorphic system. And the key element for this new architecture, a high-performance flexible artificial synapse, was demonstrated based on FMT. By transforming the undesired H_2O/O_2 redox couple induced hysteresis in transistors into a remarkable origin of memristive features, FMT was fabricated and its performance was characterized. Thanks to its reliable working mechanism and the unique gate tuning function, the artificial synapse has the advantages of its number of states, dynamic range, repeatability, uniformity, energy and cost efficiency, thus was very competitive among the existing artificial synapses (both inflexible and flexible). In addition, a series of synaptic plasticity, such as PPF, LTP, STDP, and SRDP, was demonstrated, and even a transition between excitatory and inhibitory PSC was revealed. The FMT could work under bended states and showed good endurance for multiple bending operations, thus makes it qualified for using in wearable applications. Finally, as a proof-of-practicability, a simulated neuromorphic network using the parameter extracted from the

artificial synapse was realized and achieved pattern recognition and classification. This high-performance flexible artificial synapse paves the new way toward the wearable electronic system.

METHODS

Device fabrication

The transistor was fabricated on a cleaned polyimide film (DuPont Kapton, thickness 75 μm). First, the gate electrode was defined using photolithography. Then, 8 nm of Cr and 50 nm of Au were deposited via thermal evaporation followed by a lift-off process. An Al_2O_3 dielectric layer was grown using ALD under 200 °C. The source and drain were fabricated on top of the dielectric layer using the same method. Channel area was defined by opening a window on the photoresist using photolithography. Various channel area sizes were defined for investigating the performance. The SWCNT/F8T2 composite was prepared by dispersing SWCNTs (NanoIntegris, 99% semiconducting) in the F8T2 (Lumtec) solution in toluene (Sigma-Aldrich) (0.2 mg/mL). The prepared architectures were immersed in the composite solution for 7.5 h to deposit the SWCNT network embedded in the F8T2 thin film.

Characterization

Electrical characterization was performed using a Keysight B1500A Semiconductor Device Parameter Analyzer. The pulse and wave signals were generated by programming the input manually using the listed IV-scanning function except the 10,000 short pulse tests, which were obtained from the pulse-mode of the Source/Measure Unit module.

Data availability

The data that support the findings of this study are available from the corresponding author on request.

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AUTHOR CONTRIBUTIONS

K. Yang designed, fabricated, and characterized all the devices. S. Yuan developed the simulation work, involved in experiments and data analysis. L. Tu and J. Wang helped with experiments. Y. Huan, J. Xu, and Z. Zou helped with system design and simulation. J. Wang, Y. Zhan, L. Zheng, and F. Seoane helped to analyzed the data and provided guidance on researches. K. Yang and S. Yuan together wrote the manuscript, which all authors discussed and contributed. Y. Zhan, L. Zheng, and F. Seoane supervised the work.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj Flexible Electronics* website (https://doi.org/10.1038/s41528-018-0033-1).

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