PERSPECTIVE

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Van der Waals integration before and beyond two-dimensional materials

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Material integration strategies, such as epitaxial growth, usually involve strong chemical bonds and are typically limited to materials with strict structure matching and processing compatibility. Van der Waals integration, in which pre-fabricated building blocks are physically assembled together through weak van der Waals interactions, offers an alternative bond-free integration strategy without lattice and processing limitations, as exemplified by two-dimensional van der Waals heterostructures. Here we review the development, challenges and opportunities of this emerging approach, generalizing it for flexible integration of diverse material systems beyond two dimensions, and discuss its potential for creating artificial heterostructures or superlattices beyond the reach of existing materials.

Semiconductor heterostructures and superlattices represent the essential material foundation for all modern electronics and optoelectronics. Integrating dissimilar materials with pristine interfaces is essential for creating functional devices by design and has long been a pursuit of the materials science community. The current strategy for hetero-material integration generally relies on chemical epitaxial growth or physical vapour deposition (PVD). Chemical epitaxial growth methods, such as molecular beam epitaxy (MBE) and metal–organic chemical vapour deposition (MOCVD), have provided the highest-quality heterostructures for a wide range of state-of-the-art devices, including high–electron-mobility transistors, light-emitting diodes (LEDs) and quantum cascade lasers[1]. However, such integration relies on one-to-one chemical bonds and is usually limited to materials with highly similar lattice symmetry and lattice constants, and thus similar electronic properties, which often require similar processing conditions (Fig. 1a, b)[2–4]. Materials with substantially different lattice structures or processing conditions cannot be epitaxially grown together without generating too much interface disorder, which could severely alter their intrinsic properties (Fig. 1a, lower panel). For example, MBE involves strict constraints on the lattice constant or film thickness of the epitaxial layer, where the lattice mismatch f should typically be smaller than 5% to prevent polycrystalline phase formation, and the epitaxial layer needs to be thinner than a critical thickness d_c (about 10 nm for $f = 1\%$) to prevent the formation of misfit dislocations[5]. Even with these requirements met, the resulting interface is still plagued by strain in both lattices, as can be observed in a typical two-dimensional electron gas superlattice[6] (Fig. 1c). For thicker epitaxial layers, slight mismatching normally leads to misfit dislocations at the interface[7] (Fig. 1d), which could propagate well beyond the interfaces and result in extensive threading dislocations when the mismatch increases[8] (Fig. 1e). These constraints imposed by MBE are also valid for other chemical integration techniques, such as MOCVD or atomic layer deposition (ALD). For example, owing to substantial lattice structure differences, a high-quality dielectric thin film cannot be easily integrated on top of a crystalline semiconductor with pristine surface (for example, silicon or graphene). Such striking lattice differences often result in island formation during the nucleation stage and prevent uniform thin-film deposition (Fig. 1f)[9,10].

On the other hand, conventional physical vapour deposition relying on high-energy vaporization of precursor materials is more flexible on material types and lattice structures, and is thus widely used for integrating highly disparate materials to create functional interfaces. However, the deposited materials are typically amorphous or polycrystalline and the resulting heterostructure interfaces are usually plagued by unavoidable deposition-induced defects and rich chemical disorders that dictate the interface properties. For example, vacuum evaporation and sputtering are standard processes used for depositing metal contacts on various semiconductors. Although widely used, such high-energy integration processes involve continuous bombardment of the contact region by high-energy metal atoms and clusters and strong local heating, typically producing a disordered glassy layer at the metal/semiconductor interface[11] (Fig. 1g) and leading to the Fermi level pinning (FLP) effect and incontrollable Schottky barriers in semiconductor devices[12].

Van der Waals integration

Alternatively, van der Waals (vdW) integration, in which pre-fabricated building blocks are physically assembled together through weak vdW interactions, offers an alternative low-energy material-integration approach. Such a physical assembly method does not rely on one-to-one chemical bonds and does not involve direct chemical processing on existing materials; thus, it is not limited to materials that have similar lattice structures or require compatible synthetic conditions. It has therefore attracted considerable interest for integrating diverse two-dimensional (2D) atomic crystals with highly distinct lattice structures yet little chemical disorder at the interface[13–16] (Fig. 2a). Although vdW integration has been well recognized and intensively explored in 2D devices, its applicability to other material systems (beyond 2D materials) and its prospects for scalable integration and practical applications have not been fully appreciated.

In principle, without the requirements of lattice matching and processing compatibility, such a bond-free integration strategy is not limited to a particular material dimension and could be generally applicable for flexible integration of radically different materials with distinct crystal structures (crystallinity, lattice symmetry, lattice constant), electronic properties (metals, semiconductors, insulators

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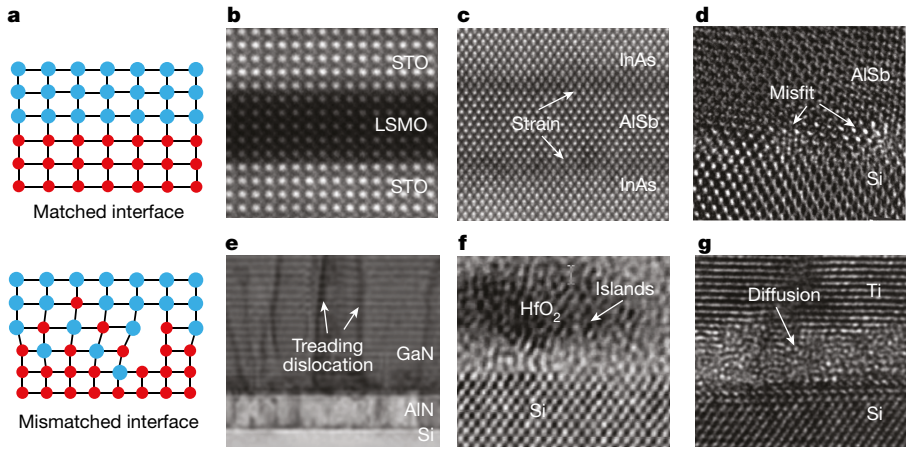


Fig. 1 | Structural characteristics of conventional bonded heterostructure interfaces. a, Schematic illustrations of bonded heterostructure interfaces: a lattice-matched interface (top) and a lattice-mismatched interface (bottom). **b**, Cross-sectional image of a lattice-matched interface (STO/LSMO; STO, $SrTiO_3$; LSMO, $La_{0.7}Sr_{0.3}MnO_3$) grown using pulsed laser deposition, with low interfacial strain and one-to-one chemical bonds. Image adapted from ref. [4] with permission from PNAS. **c**, Cross-sectional image of InAs/AlSb interfaces grown using MBE, with clear interface strains. Image adapted from ref. [6] with the permission of AIP Publishing. **d**, Cross-sectional image of a III-Sb/Si interface grown using MBE. Misfit dislocations are observed owning to the lattice mismatch. Image adapted from ref. [7] with permission from Elsevier. **e**, Cross-sectional image of GaN(AlN)/AlN/Si superlattice grown by MOCVD. Threading dislocations are observed owing to large lattice mismatch. Image adapted from ref. [8] with permission from IOP Publishing. **f**, Cross-sectional image of a HfO_2/Si interface fabricated using ALD. Poor nucleation is observed on the H-terminated silicon surface with discontinuous HfO_2 islands. Image adapted from ref. [9] with permission from Elsevier. **g**, Cross-sectional image of Ti/Si interface fabricated using high vacuum deposition, with a glassy interfacial layer. Image adapted from ref. [11] with permission from Elsevier.

and superconductors) or material dimensions[17–20] (zero-dimensional, 0D; one-dimensional, 1D; 2D; and three-dimensional, 3D) (Fig. 2b). Without direct chemical bonding (Fig. 2c), vdW integration could enable the creation of a series of artificial heterostructures and superlattices with atomically clean and electronically sharp interfaces between highly disparate materials, as exemplified in various vdW interfaces demonstrated recently (for example, Bi_2Te_3/FeTe, graphene/Al_2O_3, MoS_2/Au, phosphorene/molecules)[15,18–20] (Fig. 2d–g).

In this Perspective, we start with the fundamental concepts of the vdW distance, vdW interaction and vdW gap to generalize the definitions and requirements for vdW integration, and summarize current vdW building blocks. Next, we outline the historical background and highlight state-of-the-art vdW heterostructures with various material dimensions, including 1D/1D, 0D/2D, 1D/2D, 2D/2D, 2D/3D and 3D/3D, and then discuss potential opportunities and challenges arising in these defect-free and pinning-free vdW interfaces. Overall, we hope to highlight the bond-free vdW integration as a general low-energy integration approach (as opposed to conventional high-energy chemical integration) that can impart unparalleled freedom to integrate distinct materials beyond the limits of traditional integration approaches, opening up new opportunities for fundamental studies and enabling unprecedented device functions and performance beyond the reach of existing materials.

Bonded versus vdW-gapped interfaces

The vdW interaction[21,22], named after Dutch scientist Johannes Diderik van der Waals, generally includes three different types of intermolecular interactions: dipole–dipole interaction (Keesom force), dipole-induced dipole interaction (Debye force) and instantaneous dipole-induced dipole interaction (London force) (Fig. 3a). The vdW interaction has been simply modelled and approximated using a Lennard–Jones potential[23,24], which dates back to 1924, with the lowest potential at an equilibrium centre-to-centre distance between two vdW-interacting atoms or molecules (for example, 0.38 nm for an argon dimer) (Fig. 3b) that is often referred to as the vdW distance (d_{vdW}) (Fig. 3c).

The vdW interaction strength is typically of the order of 0.1–10 kJ mol^{-1}, about 2–3 orders of magnitude smaller than that of ionic or covalent bonds (about 100–1,000 kJ mol^{-1}). Although being the weakest interaction, the vdW force ($>10^{-12}$ N per atom pair or >10 N cm^{-2}) within an intimate-contact interface is in fact much larger than the gravity force of typical integrated structures[25,26] and is strong enough to hold bulk materials (about 1–10 N cm^{-2} for 1-m-thick material) together against gravitational movement. Nonetheless, owing to their finite surface roughness, most interfaces between two rigid 3D bulk materials do not exhibit intimate contact to reach the vdW distance and fully activate the vdW interaction. Therefore, flexible low-dimensional materials or thin films are usually more likely to reach the vdW distance and activate the vdW interaction, and thus are more suitable for vdW integration.

The vdW gap, although frequently used in 2D materials research, does not have a clear definition and is often mixed with the 2D layer thickness or the 2D layer-to-layer distance. To ensure consistency and avoid confusion, here we define the vdW gap as the difference between the vdW distance and the covalent bond length (as labelled in Fig. 3c, d). Hence, the vdW gap (g_{vdW}) could be approximated using:

$$g_{vdW} \approx d_{vdW} - r_a - r_b \quad (1)$$

where r_a and r_b are the covalent radii of individual atoms. Using this equation, the g_{vdW} value of argon dimers can be calculated as 0.23 nm. From this point of view, the vdW gap in layered materials is much smaller than their layer-to-layer spacing. As shown in Fig. 3d, the interlayer spacing of graphite is 0.34 nm and the calculated g_{vdW} is about 0.2 nm using equation (1). For other layered materials with different interlayer spacings ranging from about 0.3 nm to about 0.8 nm (Fig. 3e), the calculated g_{vdW} exhibits a similar value of around 0.2 nm, comparable to that of argon dimer or graphite layers. Additionally, the g_{vdW} value between artificially assembled vdW interfaces[19,27,28] (for example, Au/MoS_2, BN/graphene and WSe_2/Bi_2Se_3) is also around 0.2 nm.

vdW devices before and beyond two dimensions

Early examples of vdW integration date back to the early 2000s, when various synthetic nanostructures were integrated into functional devices using simple physical-assembly approaches (such as drop-casting, rubbing and stamping). This enabled the early blossoming of nanoscale electronic and optoelectronic devices assembled from carbon nanotubes[29,30] or semiconducting nanowires[31,32]. These pioneering efforts have shown the unique opportunities of vdW integration to

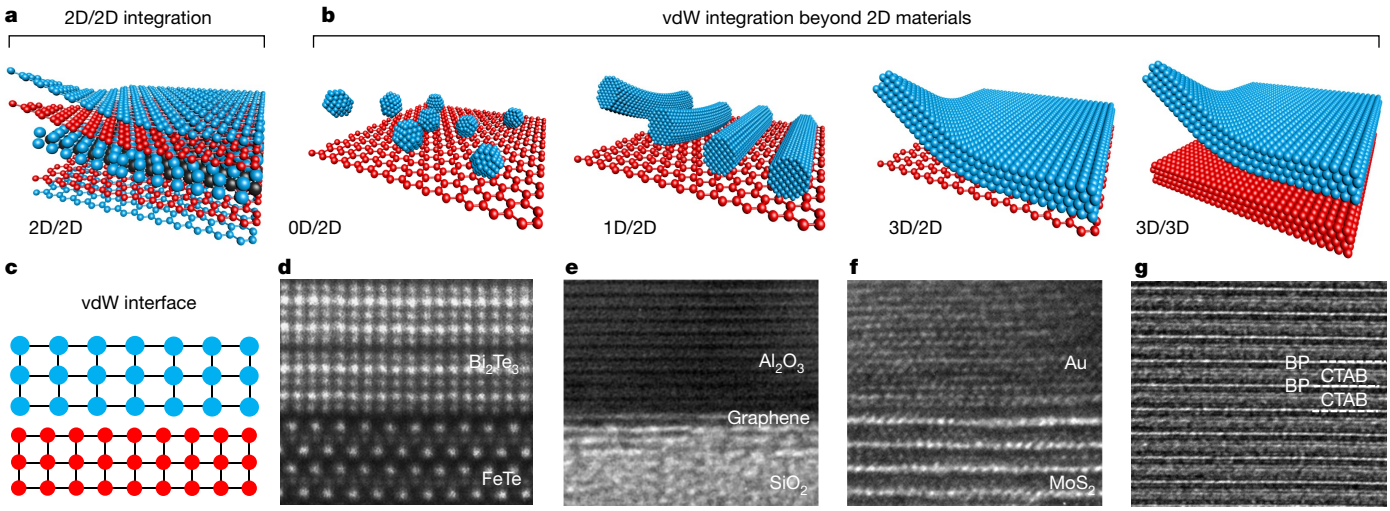
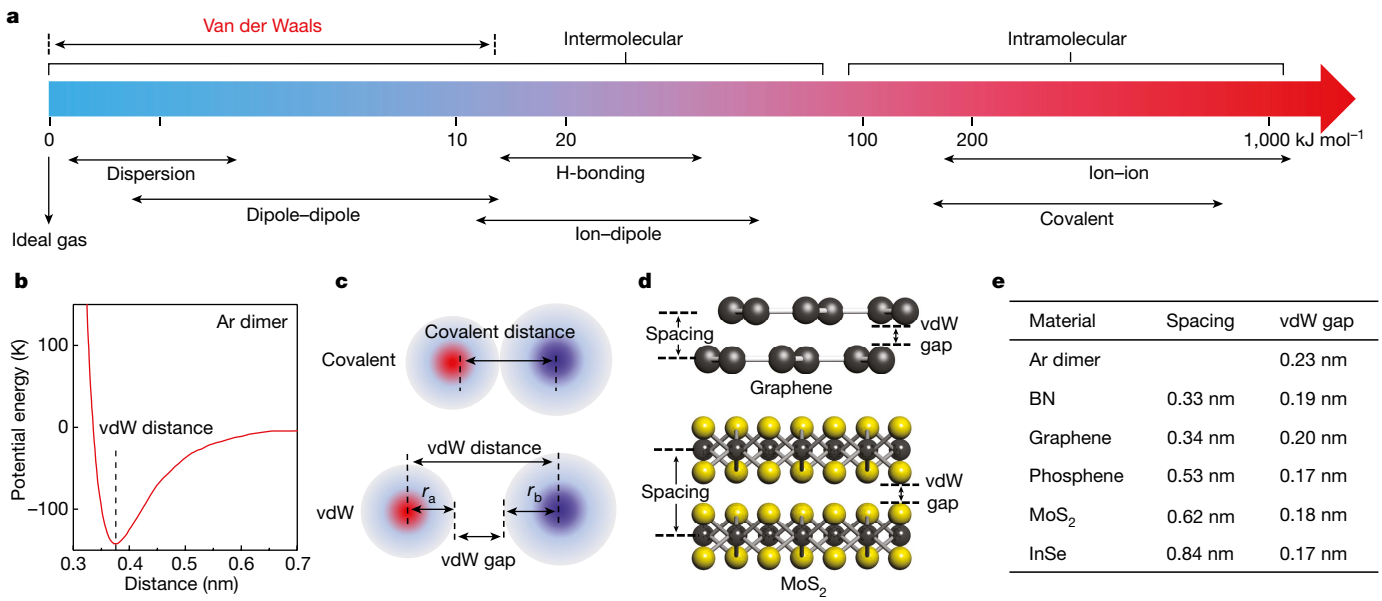


Fig. 2 | Illustration and structural characteristics of vdW-integrated interfaces. a, **b**, Schematic illustrations of 2D/2D integration (**a**) and vdW integration beyond 2D materials (**b**). Blue and red spheres represent atoms of the integrated and the host material, respectively. **c**, Bonding-free atomic structure at a vdW interface. **d**–**g**, Cross-sectional images of vdW-contacting interfaces with various material dimensions: Bi_2Se_3/FeTe (**d**; adapted from ref. [15], Springer Nature); Al_2O_3/graphene (**e**; adapted from ref. [18] with permission from PNAS); Au/MoS_2 (**f**; adapted from ref. [19], Springer Nature); a high-order BP/CTAB superlattice (BP, black phosphorus; CTAB, cetyl-trimethylammonium bromide) (**g**; adapted from ref. [20], Springer Nature). These weakly interacting vdW interfaces feature atomically clean and electronically sharp interfaces without apparent strain or disorder beyond the interface.

overcome the limitations of conventional epitaxial approaches to seamlessly combine highly disparate materials that are otherwise incompatible (for example, GaN, CdS or CdSe on Si)[32–34] and thus enable the creation of vdW devices with unprecedented functions and performance.

With the isolation of graphene[35] and diverse 2D atomic crystals[36] with dangling-bond free surfaces, vdW integration has gained tremendous momentum for creating a wide range of heterostructures with atomically clean and electronically sharp interfaces, offering a rich playground for both fundamental studies as well as novel device concepts[14,16,17,37] (Fig. 4). In fact, one of the primary engines for the recent blossoming of 2D device research is the vdW integration itself, which makes the highest-quality heterostructures readily available to physicists and electrical engineers, without the need of the expensive facilities and lengthy development processes that are necessary for high-quality heterostructure growth.

2D/2D vdW heterostructures with an atomically clean, electronically sharp interface offer a rich system for fundamental studies and electronic device demonstrations[27,38–53]. For example, by encapsulating graphene in a BN/graphene/BN vdW heterostructure, an ultrahigh carrier mobility of 140,000 $cm^2\ V^{-1}\ s^{-1}$ and up to 1,000,000 $cm^2\ V^{-1}\ s^{-1}$ can be achieved at room temperature and cryogenic temperature,



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Material	Spacing	vdW gap
Ar dimer		0.23 nm
BN	0.33 nm	0.19 nm
Graphene	0.34 nm	0.20 nm
Phosphene	0.53 nm	0.17 nm
MoS_2	0.62 nm	0.18 nm
InSe	0.84 nm	0.17 nm

Fig. 3 | Definition of vdW interaction, vdW distance and vdW gap. a, Energies of various molecular interactions. vdW interaction is the weakest intermolecular interaction (also termed physical interaction), much smaller than typical intramolecular interactions (also termed chemical interactions). **b**, Potential energy versus distance for an Ar dimer system, with a vdW distance of about 0.38 nm (lowest potential point) and a vdW gap of about 0.23 nm (difference between vdW distance and covalent radius). Image adapted from ref. [24] with the permission of AIP Publishing. **c**, Schematic illustration of the vdW gap and the vdW distance in a covalent-bonded system and a vdW system. **d**, **e**, Comparison between layer spacing and calculated vdW gap in various layered 2D materials. The calculated vdW gap is around 0.2 nm, comparable to that of the Ar dimer.

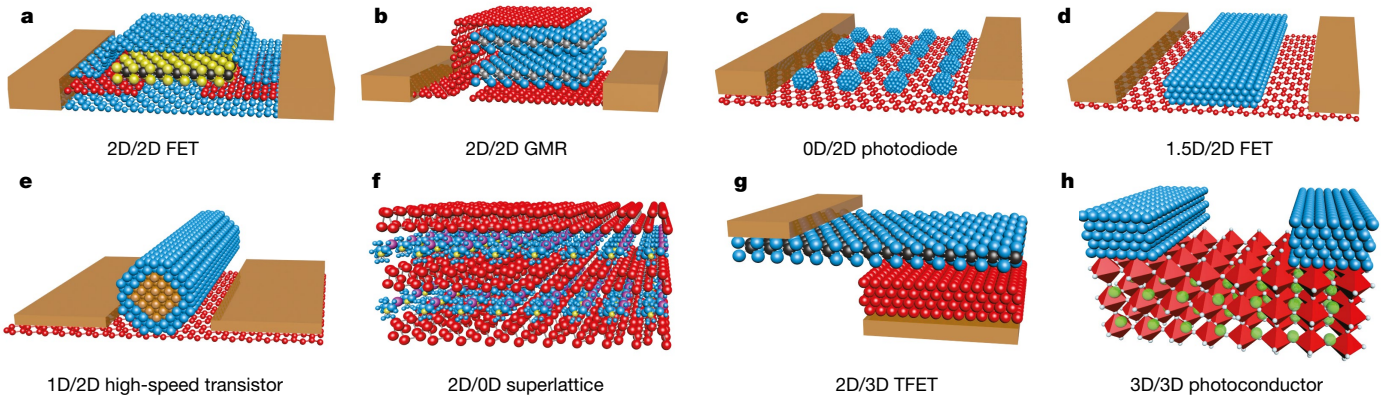


Fig. 4 | Schematics of state-of-the-art vdW-integrated electronic and optoelectronic devices. a, 2D/2D planar transistor with a 2D semiconductor as the channel (MoS_2, yellow and black), a 2D dielectric (BN, blue) as the encapsulation layer and a 2D metallic material (graphene, red) as the contact electrodes. **b**, 2D/2D vdW magnetic vertical tunnelling junctions, with atomically thin CrI_3 (blue) as a spin-filter tunnel barrier and graphene (red colour) as the contact electrodes. GMR, giant magnetoresistance. **c**, 0D/2D photodiode created by vdW integration of quantum dots or plasmonic nanoparticles (blue) on top of graphene (red) without damaging the pristine graphene lattice, thus providing greatly enhanced photocurrent. **d**, 1.5D/2D top-gate FET based on the vdW integration of a 1.5D Al_2O_3 nanoribbon (as the dielectric; blue) on top of graphene (red) without damage in its pristine lattice. **e**, 1D/2D high-speed transistor obtained by vdW-integrating a 1D core–shell nanowire (as a self-aligned mask, blue) to enable the construction of 2D transistors (graphene, red) with high cut-off frequency. **f**, 2D/0D high-order superlattice obtained by intercalating 0D molecules (blue) into a 2D material (phosphorene, red), resulting in a stable superlattice with radically different constituents and tunable interlayer distances or band offset. **g**, 2D/3D tunnelling transistor constructed using 2D MoS_2 (blue and black) and 3D Ge (red). The vdW integration of MoS_2 enables the creation of an electronically abrupt junction for high-efficiency electron tunnelling, and 3D germanium provides well controlled doping density and the desired electron affinity for ultra-small subthreshold swing. **h**, 3D/3D vdW integration enables the creation of damage-free metal contacts (blue) on delicate perovskite (red), with much more efficient charge transport than that achieved with deposited contacts.

respectively[13,27,54]. Similar vdW structures can be created by vdW-integrating a 2D semiconducting channel, a 2D insulating dielectric and 2D metallic contacts (Fig. 4a), enabling the realization of quantum oscillation and the highest carrier mobility in various 2D semiconductors[55–59]. Besides conventional planar structures, another key development in 2D vdW devices is the demonstration of vertical transistors by sandwiching a 2D insulator or semiconductor channel between graphene electrodes, enabling a switchable vertical transport mechanism based on a tunable tunnelling or thermionic barrier[39,41,42,44,60]. Similarly, vertical graphene/MoS_2 junctions have enabled the construction of unique gate-tunable photodiodes[42,44,46], and a MoS_2/BN quantum well structure has been used to create LEDs[49].

Besides high-performance devices, vdW heterostructures have also provided an ideal platform for fundamental studies. For example, vdW-assembled hetero-bilayers host electrically tunable interlayer excitons with electrons and holes localized in different layers[61–64], inheriting novel valley-contrasting physics from their monolayers but with much longer exciton lifetimes. vdW heterostructures of 2D magnetic materials have allowed probing intrinsic 2D magnetism (for example, CrI_3) and realizing giant tunnelling magnetoresistance[65–70] endowed by the multiple spin-filtering effect (Fig. 4b). In addition, the discovery of 2D magnetic materials could enable the creation of vdW magnetic heterostructures through the proximity effect[71], which is expected to be strong in 2D materials, for exploring a variety of novel phenomena and functionalities. Beyond the chemical composition of the constituent layers, the twist angles between different layers offer another degree of freedom to tailor their electronic properties for exotic physics, as highlighted by the recent observation of correlated insulator behaviour and superconductivity in magic-angled bilayer graphene homostructures[72,73].

Beyond 2D materials, the vdW integration of 2D atomic layers with other dimensional material components, such as 0D, 1D or 3D bulk materials, is essential for integrating 2D materials into functional devices; the related integrating approaches are summarized in Box 1. The previous PVD integration can usually damage underlying monolayer atomic lattices and degrade their electronic properties[74]; hence, the development of a damage-free vdW integration approach is essential for capturing the intrinsic merits of 2D materials in functional devices. For example, damage-free vdW integration of 0D plasmonic nanostructures[75] (Au) or quantum dots[76] (PbS) on graphene has enabled the fabrication of graphene photodetectors with greatly enhanced photocurrent (Fig. 4c). vdW integration of 1.5-dimensional (referred to as nanoribbon) Al_2O_3 on graphene opens a bond- and damage-free dielectric integration pathway to high-mobility top-gated graphene transistors and predates 2D/2D vdW integration (Fig. 4d)[18]. Similar approaches were also used to integrate nanowire gates with graphene nanoribbons to ensure high performance in graphene nanoribbon transistors[77,78]. Furthermore, vdW-integrating a metal oxide core–shell nanowire or a 1D metal/oxide gate stack on 2D materials defines a self-aligned ultrashort channel length without damaging the underlying 2D semiconductors (Fig. 4e), enabling the realization of the fastest so far transistors from graphene and MoS_2, with an intrinsic cut-off frequency of 420 GHz and 42 GHz, respectively[79–82]. In particular, the physical assembly of lithographically defined gate arrays on large-area 2D atomic layers opens a pathway to scalable vdW integration[81,82]. Beyond low-dimensional nanostructures, molecules or ions can be chemically absorbed onto 2D materials to form self-assembled monolayers (SAM) and 2D/SAM vdW heterostructures[83,84], or intercalated into layered crystals or 2D/2D vdW heterostructures[20,85], generating high-order bond-free vdW superlattices between radically different constituents with highly tunable interlayer distances and tailored electronic properties (Figs. 2h, 4f).

vdW-integrated devices can also be extended to 3D materials. This approach combines the atomically sharp interfaces provided by vdW integration with well developed 3D systems with rich material choices and designable properties. One interesting example is the creation of a tunnelling transistor with ultralow sub-threshold swing from a 2D/3D MoS_2/Ge vdW heterostructure (Fig. 4g)[86]. The vdW integration of 2D MoS_2 enables the creation of an electronically abrupt junction, which is critical for efficient electron tunnelling (not easily achievable within ion-implanted heterostructures), whereas the use of 3D germanium provides a well controlled doping density and the desired electron affinity (difficult to achieve using 2D semiconductors) to maximize the ON-state current while retaining low OFF-state current and small sub-threshold swing. Another recent example is the demonstration of vdW-integrated metal/semiconductor junctions (3D/2D) with highly

Box 1

Building blocks for vdW integration

A variety of materials can function as the building blocks for vdW integration (Figure). Although integration methods may vary, they all share similar integration processes, with three essential steps: (1) pre-fabrication of the vdW building blocks, (2) isolation from the sacrificial substrate and (3) physical assembly (or lamination) on the target material.

Molecules, 0D and 1D materials

Molecules and 0D and 1D materials are generally produced by bottom-up chemical synthesis as freestanding objects in solution or with low bonding forces to a growth substrate[111]. They can function as vdW building blocks and be directly integrated on the target material using simple surface adsorption, dip-coating, drop-casting or physical rubbing processes, as shown in Figure. Scalable integration may also be achieved by assembling these nanostructures (using fluid[112], electrical[113] or magnetic-field-guided[114] assembly) directly on the target material, or by first creating them on a sacrificial substrate using advanced lithography and then transferring them onto the target material ('assemble-peeling' in Figure)[75,81].

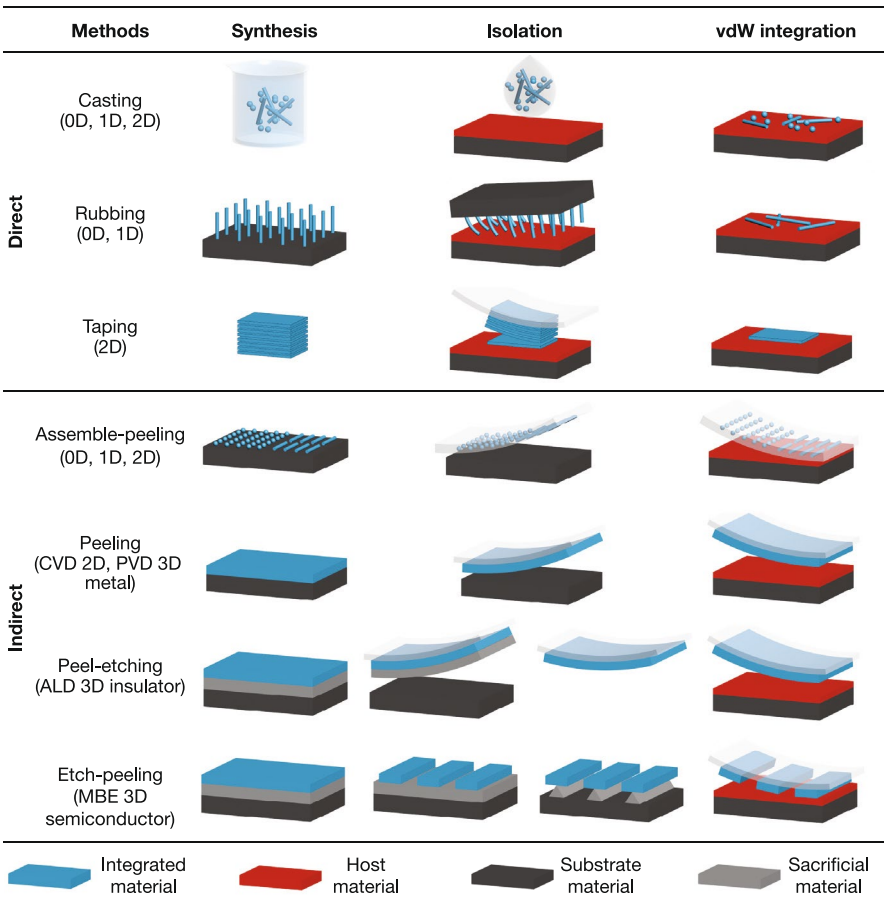
2D materials

Most 2D layered materials (for example, graphite and MoS_2) can be directly integrated on the target material using top-down methods, such as rubbing or mechanically exfoliation[115]. On the other hand, 2D building blocks and more complicated heterostructures can be synthesized using various bottom-up approaches (such as CVD) on a sacrificial substrate, then isolated using mechanical peeling (dry transfer)[116], solution-assisted peeling[117,118], metal-assisted transfer[119–123] or an etching process (wet transfer)[124], and then laminated onto the target material. Large-scale 2D vdW thin films are also achieved through solution assembly of colloidal 2D nanosheets, featuring broad-area dangling-bond-free 2D/2D contacts (between nanosheets) with few interfacial trapping states[125,126].

3D materials

The key challenge for vdW integration of 3D materials is their rigidity and relatively large surface roughness, leading to a partially contacting interface, which is undesirable for stable vdW integration and charge transport. 3D metals pre-deposited using PVD or 3D polymers pre-fabricated using solution coating typically demonstrate weak bonding with the substrate and can be mechanically isolated[19] using a 'peeling' method similar to that used for 2D building blocks. The back surface of these 3D materials replicates that of the sacrificial substrate and can be atomically flat for effective vdW integration. However, the top surface of PVD metals typically exhibits nanometre-scale roughness[127] and may not be optimal for vdW integration[128,129].

For 3D semiconductors pre-fabricated using chemical approaches (such as MOCVD and MBE) with strong interface bonds, selective etching of the sacrificial layer is necessary for their isolation. For example, single-crystal silicon with a smooth surface can be isolated from a silicon-on-insulator structure[105]. For high-quality III–V semiconductors, a pre-patterning process (into stripes; 'etch-peeling' in Figure) can help reduce the etching time and provide improved surface flatness and mechanical flexibility; the isolation and integration of InAs (from AlSb), GaAs (from AlAs) and GaN (from AlN) have been demonstrated[93,97,99]. Additional functional or passivation layers may also be deposited on the isolated building blocks before vdW integration for further tailoring of the interface properties.



Box Fig. 1 | 0D, 1D, 2D and 3D building blocks for vdW integration. Blue colour represents the integrated material, red colour represents the host material, dark grey and light grey represent the substrate material and sacrificial layer, respectively. The host material is involved in the isolation process for direct integration, but not involved in the isolation process of indirect integration. Details are provided in Box 1.

tunable barrier height approaching the Schottky–Mott limit[19]. The use of a dangling-bond-free 2D semiconductor is essential for avoiding Schottky–Taam surface states (not easily achievable in covalent-bonded 3D semiconductors), and the use of a 3D metal provides a rich material library with proper work functions for the designed band alignments (not yet available in 2D metals). In optoelectronics, various devices are also demonstrated by vdW-integrating 2D graphene with a 3D Si waveguide, a SiN_x ring resonator or optical fibre, allowing the realization of a unique gate-tunable optical modulator[87], frequency combs[88] and a Q-switched laser[89,90], respectively. Besides electron transport and electron–photon interaction, the recently emerged strong electron–phonon coupling in a 2D/3D vdW structure could also offer a rich system for exploring new physics and devices, such as strong Raman scattering (WSe_2/SiO_2)[91] and high-critical-temperature superconductivity ($FeSe/SrTiO_3$)[92].

3D/3D vdW heterostructures may also be created with unique attributes[93–95]. For example, 3D metal thin films can be vdW-integrated onto 3D semiconductors as contact electrodes with minimum interfacial disorder, greatly reducing the interface states and pinning effects in typical metal/semiconductor junctions and allowing the generation of a highly tunable Schottky barrier largely dictated by the metal work function[19]. This low-energy metal integration is crucial for forming 3D/3D vdW metal/semiconductor contacts from delicate materials, such as organic polymer[96] or hybrid perovskites (Fig. 4h), where the contact area could be severely damaged by the conventional high-energy metal deposition process. Our preliminary studies show that a vdW metal/perovskite contact features a damage-free and atomically clean interface, allowing much more efficient charge transport and achieving a highest optical gain of over 10^9. Additionally, distinct 3D semiconductor membranes may be separated from their epitaxial growth substrates[97–99] and physically assembled to enable the creation of new-generation 3D/3D semiconductor heterostructures or superlattices beyond the limits of traditional material-growth approaches.

Integration by design

The initial studies of vdW integration and vdW heterostructures revealed many exciting opportunities. By further extending vdW integration to include the well developed 3D materials and other low-dimensional materials, a much broader range of material components can be isolated, mixed, matched and combined to create highly engineered heterostructures and enable the construction of a new class of electronic, optoelectronic or magnetic devices with unprecedented performance or entirely new functions beyond the reach of the existing materials. Here we discuss some unique opportunities arising from vdW-integrated heterostructures.

Tunable vdW metal/semiconductor junctions

In vdW metal–semiconductor (MS) junctions, a metal thin film is pre-fabricated and physically laminated onto the semiconductor surface with little integration-induced damage and minimized FLP effect, thus ensuring a highly tunable barrier height by design[19]. Therefore, Ohmic contacts to various 2D semiconductors may be realized by vdW-integrating specific metals with proper work functions matching the respective semiconductor band edges. In this way, the majority-carrier type can be tailored from electrons to holes by tuning the work function of the contact metals, and complementary metal–oxide–semiconductor (CMOS) circuits could be created with the same 2D channel material by simply integrating metals with work functions matching the conduction- or valence-band position. We note that CMOS integration using a single 2D semiconductor is a key challenge for the 2D device community because there is little physical space for impurity dopants in such atomically thin semiconductors.

vdW metal integration may also be explored for improving the contacts to various 3D semiconductors; however, the effect may not be as straightforward as in 2D semiconductors. Typical 3D semiconductors could suffer from surface dangling bonds owing to the crystal lattice termination at the surface, leading to unavoidable interface states. Specifically, for a covalent semiconductor (such as Si and GaAs) with little electronegativity difference, dangling bonds result in a large number of gap states that serve as reservoirs for carriers to pin the Fermi level. In this case, vdW integration may achieve limited improvement, but could still be observable once the surface dangling bonds are passivated (for example, H-termination or thin oxide passivation)[40,100]. On the other hand, for covalent semiconductors with large electronegativity difference (for example, SiC or GaN) or ionic semiconductors, a minimized FLP effect with improved contact behaviour is expected. This could be particularly useful for large-bandgap III–V semiconductors (for example, GaN), where the optimized p-type contact is difficult to achieve using a conventional doping approach.

Besides enhancing carrier transport efficiency, vdW-integrated MS junctions could also benefit devices requiring a high Schottky barrier to hinder charge transport. For example, in metal–semiconductor field-effect transistors (MESFETs), the MS Schottky barrier is used as the gate to modulate carrier concentration inside the channel[1]. In this case, a large Schottky barrier is desired for the gate to ensure smaller gate leakage and larger gate voltage operation range, but is hard to control using a conventional deposited MS junction owing to the FLP effect. With the ability to create vdW MS junctions with tunable barrier height, optimized Ohmic contacts and Schottky gate could be achieved at the same time by integrating metals with work functions matching either the band edges (small barrier for contacts) or the middle of the forbidden gap (large barrier for the gate) (Fig. 5a). Furthermore, designable Schottky barriers at the vdW MS interfaces could also enable the construction of novel devices, such as hot-electron photodetectors with tunable and designable detection edge or multi-level memory cells.

Pinning-free interfaces for coherent transport

Coherent charge injection is critical for various quantum electronic devices that require phase coherence, but is often plagued by interface scattering due to structural disorder at the electrode interfaces. For example, in magnetoresistance and spintronic devices based on polarized carrier transport across various heterostructure interfaces, such as ferromagnetic/conductor/ferromagnetic (giant magnetoresistance), ferromagnetic/insulator/ferromagnetic (tunnel magnetoresistance) or ferromagnetic/semiconductor/ferromagnetic (spin transistor), the spin-injection efficiency is dictated by the interface quality and largely suppressed by interfacial roughness, impurities and other types of interface disorder. For instance, in a deposited Fe/Si magnetic junction, high-energy Fe atoms (during vacuum deposition) tend to diffuse into the Si lattice and lead to randomly oriented local magnetic moments[101], severely scattering the injected spin-polarized electrons and degrading overall spin polarization. By contrast, within vdW magnetic junctions, the interface states and the atom interdiffusion-induced scattering effects could be minimized by physically integrating various functional components (ferromagnetic metal, insulator, semiconductor) with atomically clean and magnetically sharp interfaces, enabling efficient coherent spin injection[96] (Fig. 5b). Beyond magnetic junctions, the vdW integration approach may also be extended to create other functional junctions that were previously plagued by interface disorder. Possible directions include vdW superconductor/semiconductor junctions, Josephson tunnelling junctions (Fig. 5c) and metal/insulator tunnelling junctions.

Heterogeneous-layer assembly by design

One of the most attracting attributes of vdW integration is the freedom of 'assembly-by-design'. A possible playground for vdW integration, therefore, would be stacks of III–V semiconductor-based devices that could not be previously grown (through MBE or MOCVD). For instance, a heterojunction bipolar transistor based on the wide-bandgap GaN is commercially important for high-frequency, high-power amplification[102], but its overall performance is severely limited by the low conductivity of MOCVD-grown p-type GaN base region[103]. Using vdW layer-by-layer integration, one could take a 'transplant surgery'

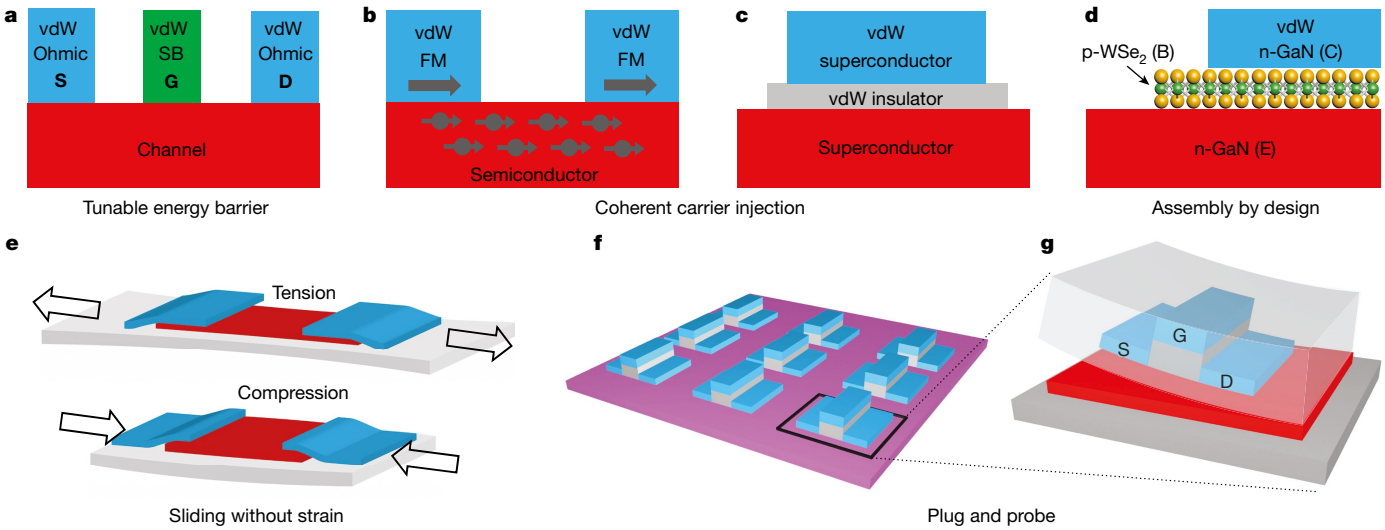


Fig. 5 | New opportunities in vdW-integrated heterostructures and superlattices beyond 2D materials. a, A MESFET structure using one-step vdW integration of pre-fabricated metal electrodes with distinct work functions, resulting in a low Schottky barrier (SB) (source, S, and drain, D) and a large Schottky barrier (gate, G) through a single integration step. **b**, **c**, Schematic illustration of a vdW-integrated ferromagnetic (FM)/semiconductor junction (**b**) and a superconductor/insulator/superconductor junction (**c**) for coherent charge injection in quantum electronic devices. The defect- and pinning-free interface could considerably reduce interface disorder and the associated scattering that plague such devices. **d**, Heterostructure integration of n-GaN/p-WSe_2/n-GaN vdW structure (B, base; C, collector; E, emitter) for high performance heterojunction bipolar transistor by replacing p-GaN with p-type WSe_2. **e**, Schematic illustration of a vdW heterostructure (vdW metal, blue; stretchable semiconductor, red) with distinct stiffness under mechanical compression (bottom) and tension (top). The bonding-free vdW interaction allows two contacting materials to slide against each other and effectively release the local strain at the interface. **f**, **g**, Plug-and-probe vdW integration, where a complex structure (for example, source drain contacts and a gate stack) is pre-fabricated on wafer scales. Every time used, one piece of the structure is cut from the mother wafer and laminated on the target material within a few seconds for directly probing its intrinsic properties.

approach to replace the poor p-type GaN layer with other materials of better p-type conductivity (for example, p-type WSe_2 or p-type Si), leading to a novel heterogeneous n-GaN/p-WSe_2/n-GaN (or n-GaN/p-Si/n-GaN) structure (Fig. 5d). Similarly, vdW stacking could also play an important role in organic polymer stacks that typically share similar material solubilities[104] and are hard to be integrated without dissolving others, or amorphous oxide stacks that share similar etchants and are limited by the lack of selective etching process. Possible applications include vdW vertical memories, vdW tandem photovoltaics, vdW OLEDs (organic LEDs), bipolar OFETs (organic field-effect transistors) and organic CMOS circuits.

vdW sliding interface

Flexibility and stretchability are important features for future wearable electronic devices, but are difficult to achieve in typical silicon or III–V semiconductor wafers. Previous approaches to this challenge include two conceptually different methods. One relies on the use of new structures (such as wavy silicon membranes)[105] and the other relies on new materials that are intrinsically flexible (such as organic polymers). Although these approaches have successfully improved the flexibility of individual building blocks, interface strain in heterostructures, which could dictate the overall device flexibility, has been insufficiently addressed until now. When a chemically bonded heterostructure is stretched, large internal strains are usually built up at the interface between two dissimilar materials (for example, semiconductor/dielectric, semiconductor/metal), which typically have distinct Young's moduli, where the failure often occurs first. By contrast, within vdW-integrated devices, constituent components with distinct mechanical properties could slide over each other when compressed or stretched (Fig. 5e) while retaining clean and sharp vdW interfaces with optimized charge transport. Such a sliding junction can effectively release the local strain at the interface and therefore overcome the fundamental mechanical mismatch in functional systems. Other sliding-related effects, such as the triboelectric effect or frictional heat generation, are also interesting to investigate.

Plug-and-probe intrinsic material properties

vdW integration could also be extended to integrate multiple functional components through a 'one-step' assembly process without additional lithography. For example, all essential components of a typical MOSFET (gate metal, dielectric insulator, contact metal and encapsulation polymer, as shown in Fig. 5f, g) could be pre-fabricated in a large scale and directly laminated on the targeted semiconductor surface. Besides enabling optimized contact and dielectric interfaces, such vdW integration offers an effective 'plug-and-probe' approach for investigating intrinsic material properties. The top gate and contact structures could be integrated on the target material without any conventional fabrication steps or exposure to solvents and, more importantly, the entire pre-fabricated structures could be integrated within a few seconds at room temperature, which would be crucial for many unstable materials (such as silicene or germanene[106,107]) that rapidly degrade with time or fabrication steps. Besides these exotic 2D materials, the relatively 'old' 2D materials (such as graphene and transition metal dichalcogenides) also deserve a re-visit through this simple plug-and-probe approach. Our preliminary results demonstrate that the effective field-effect mobility of CVD-grown monolayer WSe_2 could be substantially improved (up to about 200 $cm^2\ V^{-1}\ s^{-1}$) by an immediate plug-and-probe operation, suggesting that the performance of other 2D materials may be largely underestimated owing to unnoticed time-related or fabrication-induced degradations.

Beyond 2D materials, this low-temperature, solvent-free and low-energy integration strategy could be useful for other delicate materials, including molecular monolayers, organic thin films or crystals, and metal halide perovskites. Such materials are usually not stable under high temperature, not compatible with traditional micro-fabrication processes (for example, they are soluble in various solvents) or are highly prone to metal-deposition-induced degradation. Importantly, the plug-and-probe approach offers a lithography-free, solvent-free and damage-free pathway to rapid device prototyping using these delicate materials, which is essential for investigating their intrinsic properties and pushing the performance limit of various devices (OFETs, OLEDs,

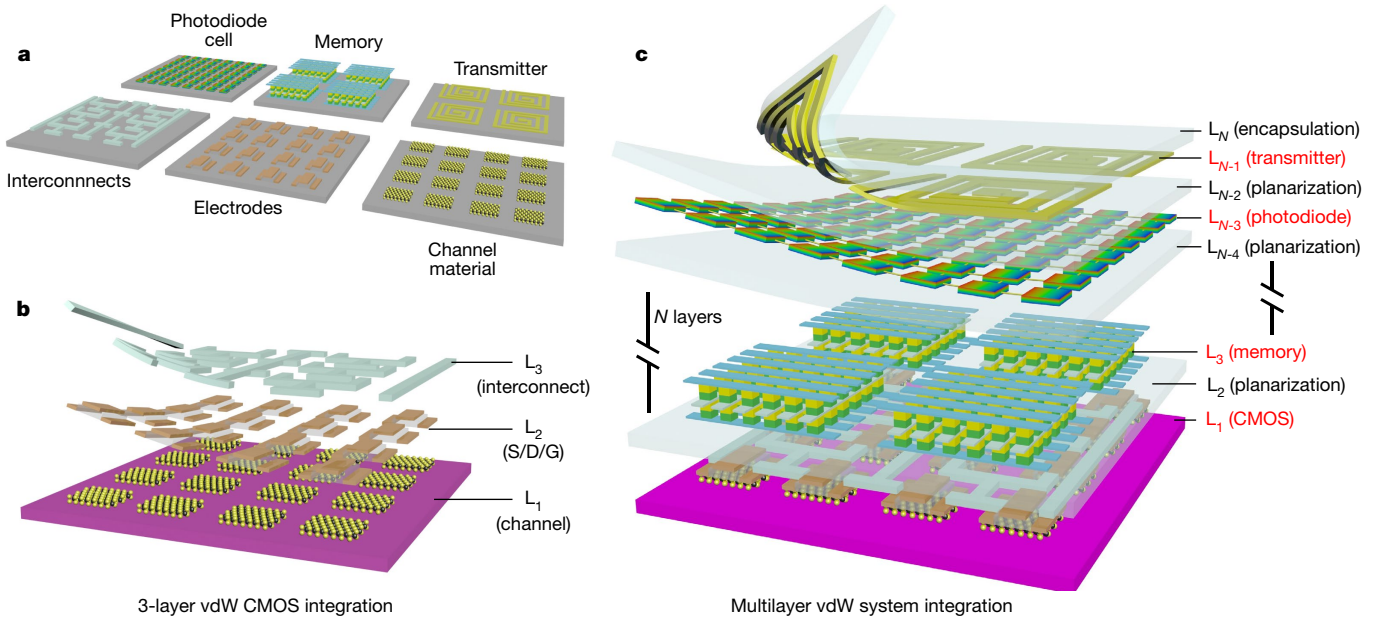


Fig. 6 | Potential layer-by-layer vdW assembly of a 3D electronic system. **a**, Schematics of the essential building blocks for vdW device integration and the essential device layers for vdW system integration. **b**, Schematic illustration of circuit-level (CMOS circuit) vdW integration by assembling various building blocks, including channel material (L_1), electrodes and dielectrics (L_2) and interconnects (L_3) on a target semiconductor layer. **c**, Schematic illustration of high-order system-level integration by vdW-stacking multiple active functional layers with low-temperature planarization layers (passive layers; translucent in the schematic) in between.

organic photovoltaics and perovskite FETs, photovoltaics and LEDs) previously plagued by fabrication-induced degradations.

Another advantage of the plug-and-probe approach is its energy and cost efficiency. In conventional micro- and nano-electronics research, device fabrication involves time-consuming, expensive lithography and vacuum deposition processes that may not be easily accessible in many laboratories. Furthermore, precious metals (for example, Au and Pt) have to be deposited uniformly across a metre-scale vacuum chamber, even when only a few micrometre-scale devices are fabricated each time. In contrast, using the plug-and-probe approach, a large array of standard device structures could be batch-processed on the wafer scale using conventional lithography with high throughput. When needed, a small area of the device structure is isolated from the mother wafer (Fig. 5f, g) and laminated onto the target material like a 'tattoo tape', with greatly reduced time and cost. This is especially desired for structures involving more sophisticated processes, such as extreme ultraviolet photolithography-processed ultrashort gates, ultrathin dielectrics or special structures (for example, optical metamaterials and T-gates). We therefore anticipate that these complex pre-fabricated wafers could be the first products using plug-and-probe commercialization and standardization, which may further lower the entry barrier for the broader research community, greatly accelerate device prototyping from new materials and create new opportunities in nanoelectronics and nanophotonics.

Outlook

After nearly two decades of expanding efforts in vdW integration of various material systems, questions are frequently raised on whether this is purely an academic game or it could offer some practical technological potential. The recent demonstrations of vdW integration of large arrays of lithographically defined microstructures of 3D materials[79,81,82] could alter the landscape and offer a promising outlet by combining the advantages of vdW integration (for example, atomically clean and electronically sharp interfaces) with more scalable and reliable 3D materials and conventional fabrication techniques. For example, the vdW-integrated 3D metal/MoS_2 interface has enabled the creation of a nearly ideal pinning-free MS interface, which is difficult to achieve with conventional fabrication approaches[19], allowing the experimental validation of the Schottky–Mott limit predicted many decades ago. The creation of such high-performance devices with simple vdW integration highlights the robustness of this approach and its unique merits for creating pristine interfaces that are not otherwise readily accessible.

vdW integration can be further extended for scalable system-level integration. Various active or passive device layers can be assembled by repeatedly laminating pre-fabricated vdW building blocks (for example, semiconductors, gate dielectrics and contacts) or pre-assembled device layers (such as CMOS circuits, flash memories and photodiode cells) using a layer-by-layer stacking process (Fig. 6). Each active device layer could be separated by a passive planarization layer and may be further connected with other layers using vertical interconnect access holes. Within this heterogeneous stacking geometry, function layers are vdW integrated without the limits set by lattice-matching or process-compatibility requirements, which could enable 3D electronic integration with much reduced process cost and device footprint. Hence, such a combination of vdW integration with more mature and more reliable 3D materials and devices could bridge the gaps between academic research and industrial applications.

Despite the extraordinary potential and many exciting demonstrations of proof-of-concept devices, the challenges of turning them into practical technologies should not be understated. Sustained investment is imperative, not only for pushing the limit of individual devices but also for improving their integration yield, processability, stability and scalability. Although the ability to physically assemble individual building blocks into vdW heterostructure has offered vast flexibility for heterogeneous material integration and has considerably accelerated both fundamental studies and proof-of-concept demonstrations, scalable vdW integration of heterostructure device arrays with high yield and throughput remains a major challenge. For example, the state-of-the-art vdW stacking process still largely relies on a manual alignment–transfer technique using a soft stamp (for example, silicone polymer), which typically has a large mechanical expansion coefficient and could limit the alignment resolution in large-scale integration. Additionally, for most vdW interfaces, the size, uniformity, wrinkles, surface contamination and interfacial air bubbles represent notable technical challenges that could severely limit the device yield, whereas these difficulties grow exponentially with increasing integration areas or integration steps[108]. These technical challenges require unified efforts from multiple

disciplines, particularly chemistry and materials science, for the synthesis and fabrication of vdW building blocks with high uniformity, atomic flatness and elaborate structure design[52,109,110], as well as engineering, for the development of an automatic stamping machine with appropriate mechanical design, which would be critical for reducing defects, improving the integration yield and achieving better alignment resolution over a large scale.

Another potential challenge is the reliability and stability of the weakly bonded vdW heterostructures. As noted, the vdW interactions between two fully contacting surfaces are strong enough to hold bulk materials together against gravitational movement or disintegration. Therefore, the instability or delamination of two fully vdW-interacting materials is unlikely, unless there is a strong enough external force or interfacial strain. On a related matter, thermal expansion and contraction of the individual vdW building blocks should not be overlooked, because mismatched thermal properties could lead to interfacial strain and interfacial sliding when the temperature changes. In this regard, the mild vdW integration process is advantageous because it normally does not require a large temperature swing, which is typically inevitable in conventional integration processes. However, such a thermal effect should still be considered during device operation, and strain-releasing structures or a heat-dissipation layer could be integrated to prevent accumulated strain in large-area integration. Despite these and other challenges, the bond-free vdW integration opens a new dimension for material integration, with unparalleled freedom to integrate materials that could not be previously combined, opening up new possibilities to approach physical limits previously inaccessible and to enable the development of novel devices with unprecedented performance or entirely new functions beyond the reach of existing materials and systems. Such exciting prospects and the associated new challenges call for more efforts to fully unlock the potential of vdW integration for future technologies.

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