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A new extended single-switch high gain DC–DC boost converter for renewable energy applications

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High-gain DC/DC converters are considered one of the most important components of green energy systems. Large numbers of these converters are used for increasing the voltage gain by using an extreme duty cycle. However, it increases losses and the cost, degrades the system performance, and hence obtains a low efficiency. In this article, a new design of a high-gain DC/DC boost converter is proposed. This converter has the potential to be used in low input voltage applications that need a high voltage gain such as systems powered by solar photovoltaic panels and fuel cells. The new topology is characterized by its simplicity of operation, high voltage gain, better efficiency, continuity of the input current, reduced number of inductors and capacitors, and can be extended to get higher gains. The converter structure, principle of operation, and design consideration of inductors and capacitors are presented in detail. Derivation of power losses and efficiency is presented. A laboratory prototype is implemented, and various experimental tests are given. The achievement of the suggested design is confirmed and compared with other recent high-gain converters.

The usage of renewable energy sources (RESs) is becoming more common and crucial as a result of the fast-rising demand for electrical energy and the expanding use and higher production costs of fossil fuel-based energy resources. One of the renewable energy sources, photovoltaic (PV) energy, has experienced rapid development during the past few decades. PV sources' output power and voltage are variable, nonlinear, and dependent on the surrounding temperature, solar radiation levels, and load values¹. To connect the PV sources to the electricity grid and obtain the maximum energy possible from these sources under different operating conditions, high step-up voltage DC/DC converters with greater efficiency are used to emphasize the right tracking of the maximum power and lift the low PV voltage level to proper DC levels needed for inverters². DC/DC boost converters are used for a variety of practical applications, which require high levels of DC voltage with small input current ripples³. One of the most important of these applications is RESs. The traditional DC/DC boost converter includes four components: a power switch, diode, input inductor, and output capacitor. It has a simple structure with a low price, and it is characterized by a non-pulsating input current in the continuous conduction mode (CCM) operation⁴. Nevertheless, the main disadvantages of this converter are extreme conduction losses, severe switching stresses, excessive input current ripples, and rising electromagnetic interference (EMI). Additionally, it is improper for applications that need raising voltage gains.

Many research efforts have been done to get further voltage gain without working at an extreme duty ratio and to remedy the abovementioned issues⁵. An interleaved DC/DC boost converter was introduced in⁶. It used two standard boost converters connected in parallel. The reliability of the interleaved converter based on the Markov standard was presented in⁷. To minimize the ripples of the input current, the switching losses and EMI levels, different PWM control schemes were introduced in⁸, and another control structure based on a look-up table was stated in⁹. However, they have problems with isolating gate signals and increasing the cost. Moreover, the voltage gain was identical to the conventional converters¹⁰. Interleaved boost converter based on a voltage doubler was used¹¹. Another control method by combining alternating phase shift control and customary interleaving PWM control for the interleaved converter was proposed in¹². A six-phase interleaved DC/DC converter with switched capacitor voltage multiplier cells was listed in¹³. These structures confirmed low current ripples, large voltage gain, and balancing of voltage capacitors. However, the main issues were the duty cycle restriction and rising cost. An assortment of DC/DC boost converters based on a switched capacitor was suggested in¹⁴ and a switched capacitor/inductor was hired in¹⁵. High voltage gain was satisfied, but they have large conduction losses, serious switching stresses, and circuit complexity. In¹⁶, a cascaded boost converter was used with high-voltage gain,

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and low switching losses, and current ripples. However, shortcomings were noted such as rising cost, decreased efficiency, and complexity of the control system.

Different topologies in the literature were introduced for realizing high-voltage gain such as coupled inductor/capacitor converter¹⁷, voltage-clamped coupled inductor converter¹⁸, a standard boost in series with flyback converter¹⁹, and classic converter with a coupled inductor and a voltage lift cell²⁰. Nevertheless, several issues like lowest efficiency, adding EMI levels, pulsing input current, high price, and complexity of the drive circuit are noted. To decrease the output diode voltage stress of the flyback cell and improve the efficacy, a coupled inductor boost combined flyback converter was suggested in²¹. However, a snubber circuit is needed to absorb the surges across the main power switch. A DC/DC converter that used voltage multiplier cells of capacitor-inductor-diode with a voltage lift circuit to boost the voltage gain was introduced in²². High voltage gain and low switches voltage stresses were accomplished. Unfortunately, because the main switch is connected in series with the input DC source, the input current is discontinuous. Therefore, the circuit is not appropriate for renewable energy applications such as PV applications. The converter efficiency decreased as the number of cells increased because each cell is made up of four components, making it suitable only for low-power applications. Quasi Z-source converters²³, quasi-Y-source converters²⁴, and hybrid Z-source boost converters²⁵ were also founded. Two cascaded Z-source boost converters were proposed in²⁶, which took the advantage of cascaded technique and impedance source converters. These topologies attained high voltage gain at a small duty ratio and continual input current. But they have a limited duty cycle, excessive stresses on the active switch, and complex drive circuit. A hybrid topology was presented in^{27,28} integrated the coupled inductor and switched capacitor to achieve higher voltage gain. Nonetheless, the copper loss and the main switch voltage stress were raised by rising the turns ratio of the coupled inductor. A DC/DC converter based on quad switched inductor was studied in²⁹ to accomplish high voltage gain. However, this converter has a lot of components, which reduces the efficiency, and raises the cost and the size of the circuit. Another DC/DC converter based on the voltage multiplier structure was introduced in³⁰. High voltage gain and high efficiency can be achieved, but the converter has some drawbacks for example high voltage stress on the main switch, and is suitable only for low voltage low power applications.

This article offers a new high voltage gain non-isolated DC/DC boost converter to improve the abovementioned problems. This converter uses a reduced number of passive components. It has the following features: control simplicity, high output voltage gain, and small voltage stress across the power switch and diodes. Furthermore, cascading additional cells can be offered to have a very high voltage gain. The circuit description and modes of operation are described in detail. The steady-state process of the proposed converter is studied. The voltage gain derivation in CCM is evaluated. The voltage stresses across the power switch, diodes, and capacitors are derived. Power losses and efficiency are derived based on the equivalent model for the suggested topology circuit with parasitic elements. The experimental results and comparative analysis are given to confirm the success of the proposed converter.

The proposed topology in this paper differs from the circuit in²², which uses the main switch connected in series with the input DC source. Consequently, the input current is discontinuous which causes constraints for PV applications. Also, each cell of this circuit in²² consists of four components, then, the converter efficiency decreased as the number of cells increases. So, it is suitable only for low-power applications. The current work also differs from the circuits in^{23–26} which employ Quasi Z-source, quasi-Y-source, hybrid Z-source, and two cascaded Z-source boost converters, respectively. Although these topologies attain high voltage gain with a low duty ratio and continuous input current. However, they have a limited duty cycle, high stresses on the active switch, and complex drive circuits.

The proposed converter and its steady-state investigation

Circuit description and modes of operation. The offered multi-cells DC/DC boost converter is shown in Fig. 1. To understand the operation of the proposed DC-DC boost converter, the circuit with two cells ($n=2$) shown in Fig. 2 is analyzed. Each cell contains two passive elements (one inductor and one capacitor), and one diode.

The proposed circuit composes of one active power switch, four diodes, and five passive components. Under assumptions of the ideal power switch and diodes, and pure inductive and capacitive elements, steady state analysis of the two operation modes is discussed. The key waveforms of the two cells of the suggested converter are displayed in Fig. 3.

Mode 1 ($0 \leq t \leq DT$). Figure 4 shows the equivalent circuit during mode 1. As obvious SW, D_1 , D_2 , and D_3 are ON, and D_0 is OFF. The currents (i_{L1} , i_{L2}) of the inductors (L_1 and L_2) increase linearly. The inductor's voltage opposes the input dc voltage V_{in} . The capacitors C_1 and C_2 charge with a voltage nearly the same as V_{in} . The saved energy in the capacitor C_0 supplies the load. The equations of mode 1 can be obtained from Fig. 4b by applying KVL and KCL as follow:

$$V_{L1-on} = V_{L2-on} = V_{C1-on} = V_{C2-on} = V_{in} \quad (1)$$

The supply current during the switching-on period (i_{s-on}) is given by;

$$\left. \begin{aligned} i_{s-on} &= i_{L1-on} + i_{C1-on} + i_{L2-on} + i_{C2-on} \\ i_{C0} &= i_o \end{aligned} \right\} \quad (2)$$

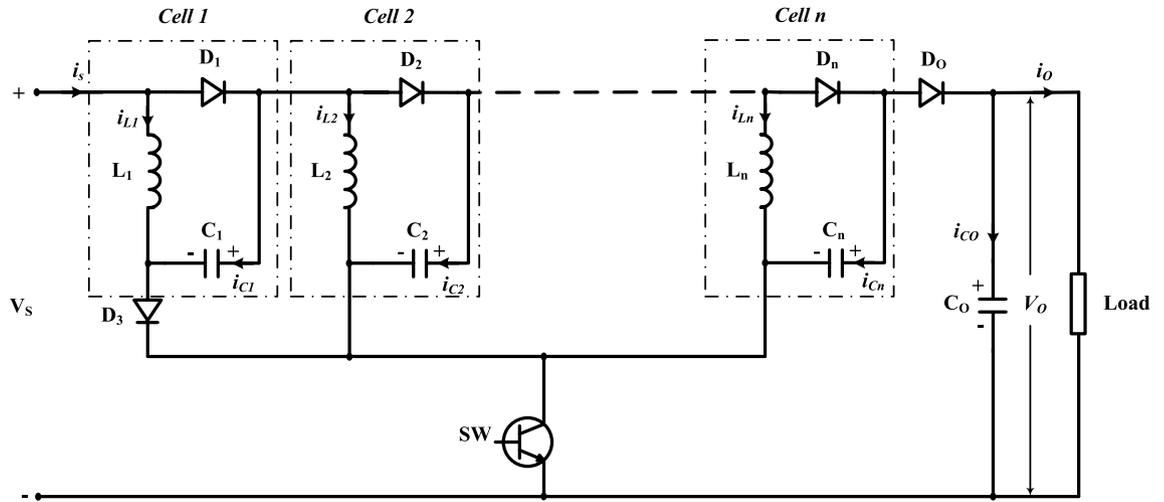


Figure 1. The multi-cells proposed DC-DC boost converter.

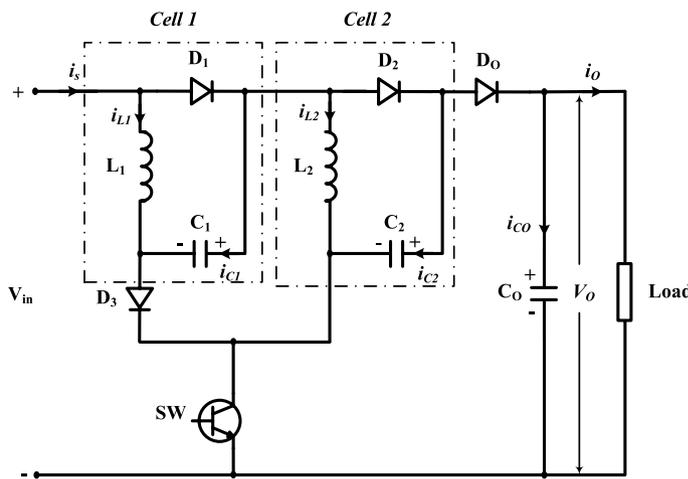


Figure 2. The two cells proposed DC-DC boost converter.

Mode 2 ($DT \leq t \leq T$). Figure 5 displays the equivalent circuit during mode 2. It is noted that SW, D_1 , D_2 , and D_3 are OFF, and D_o is ON. The inductors' voltages V_{L1} and V_{L2} are inverted, and the saved energy in the passive components L_1 , L_2 , C_1 , and C_2 is transmitted to the load and C_o . The equations of mode 2 can be obtained from Fig. 5b by applying KVL and KCL as follow:

$$V_{in} + V_{L1-off} + V_{C1-off} + V_{L2-off} + V_{C2-off} = V_o \tag{3}$$

The supply current during the switching-off period (i_{s-off}) is given by;

$$\left. \begin{aligned} i_{s-off} &= i_{L1-off} = i_{C1-off} = i_{L2-off} = i_{C2-off} \\ i_{s-off} &= i_{C_o} + i_o \end{aligned} \right\} \tag{4}$$

Voltage gain derivation and voltage stresses across the switch, diodes, and capacitors. The ripple of the inductor current i_{L1} during the switching-on interval is:

$$\Delta i_{L1-on} = \frac{V_{in} DT}{L_1} \tag{5}$$

where D is the duty ratio.

The ripple of the inductor current i_{L2} during the switching-on interval is:

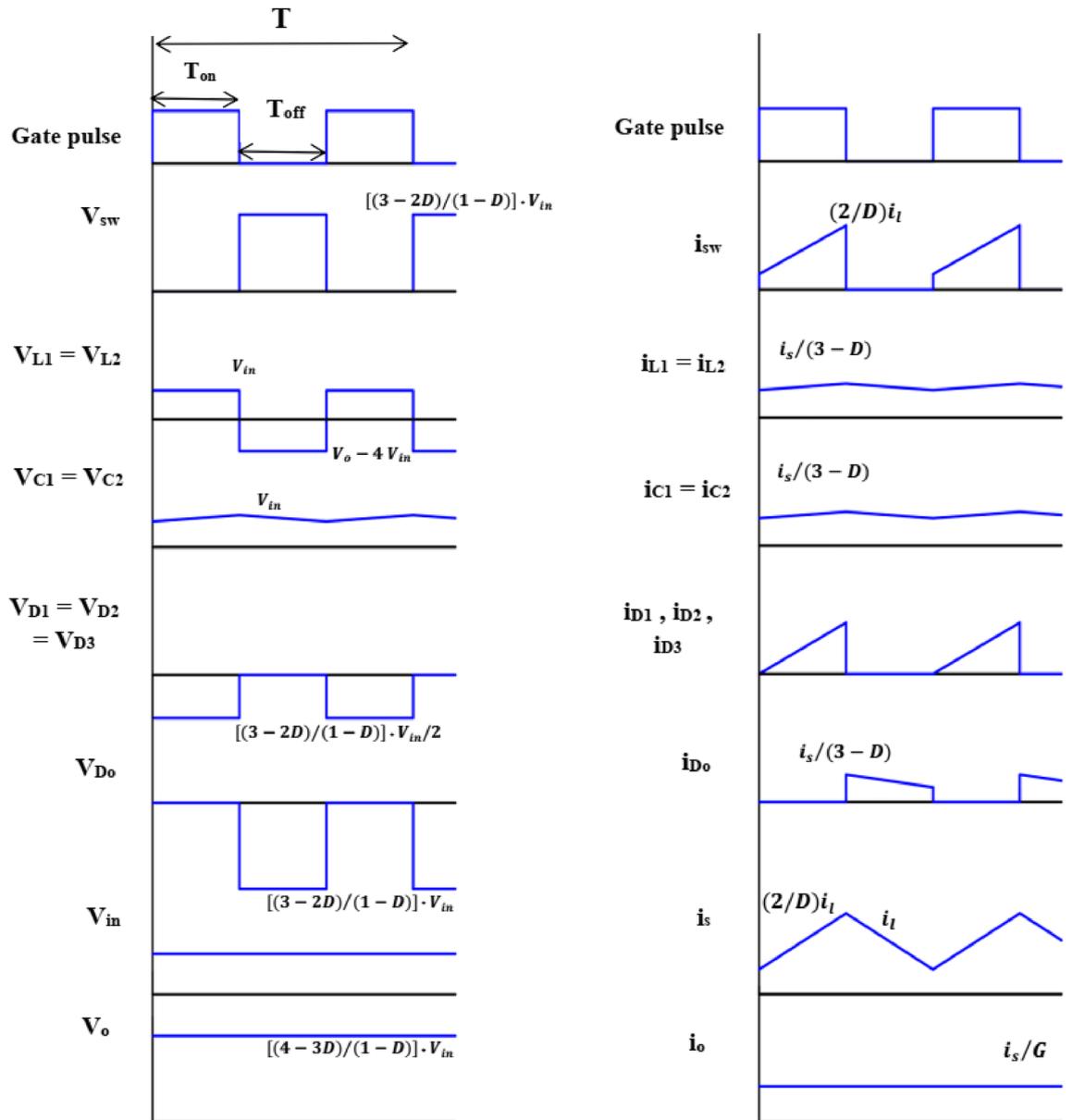


Figure 3. Operating modes of proposed converter.

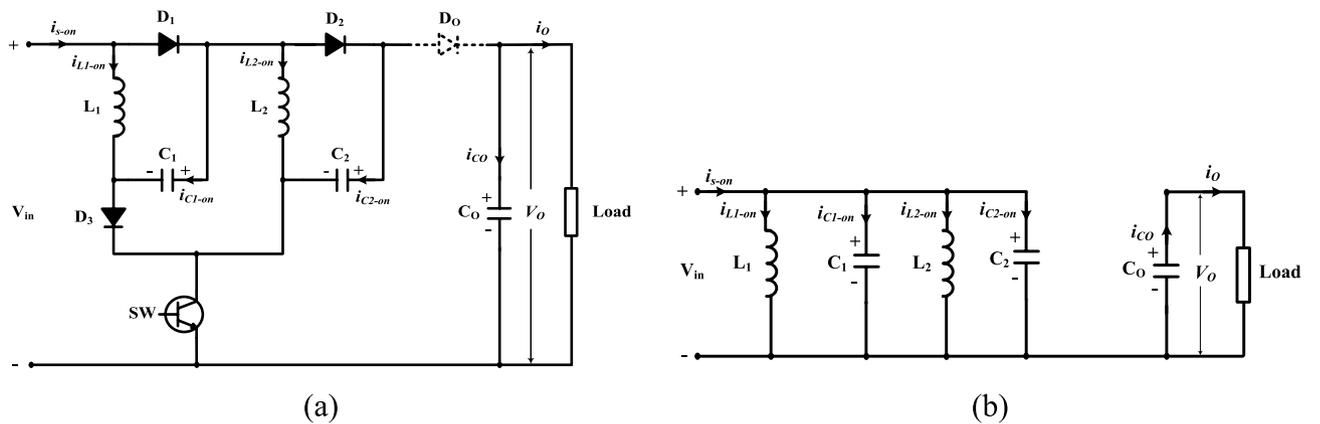


Figure 4. Equivalent circuit of Mode 1: (a) active and inactive elements, and (b) equivalent electrical circuit.

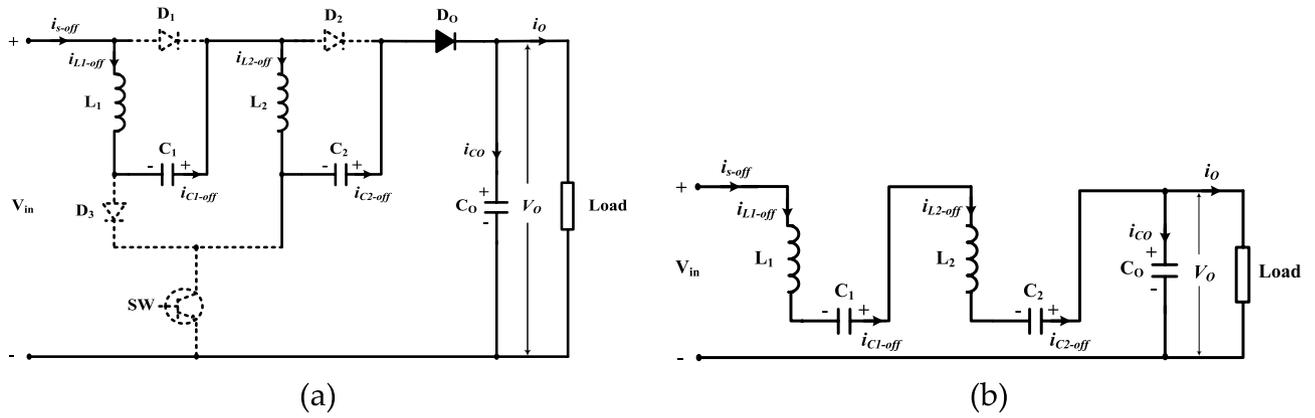


Figure 5. Equivalent circuit of Mode 2: (a) active and inactive elements, and (b) equivalent electrical circuit.

$$\Delta i_{L2-on} = \frac{V_{in}}{L_2}DT \tag{6}$$

The ripple of the inductor current i_{L1} during the switching-off interval is:

$$\Delta i_{L1-off} = \frac{(V_o - 4V_{in})}{L_1}(1 - D)T \tag{7}$$

The ripple of the inductor current i_{L2} during this mode is:

$$\Delta i_{L2-off} = \frac{(V_o - 4V_{in})}{L_2}(1 - D)T \tag{8}$$

By using the volt-sec balance through the inductors L_1 and L_2 , and from Eqs. (5) and (7);

$$\Delta i_{L1} = \frac{V_{in}}{L_1}DT = \frac{(V_o - 4V_{in})}{L_1}(1 - D)T \tag{9}$$

Also, Eqs. (6) and (8) yield;

$$\Delta i_{L2} = \frac{V_{in}}{L_2}DT = \frac{(V_o - 4V_{in})}{L_2}(1 - D)T \tag{10}$$

By solving Eqs. (9) or (10), the voltage gain can be found as follow:

$$\frac{V_o}{V_{in}} = \frac{(4 - 3D)}{(1 - D)} \tag{11}$$

For steady-state operation, the charge on capacitors C_1 and C_2 should not change;

$$DTi_{C1-on} = (1 - D)Ti_{C1-off} \tag{12}$$

and

$$DTi_{C2-on} = (1 - D)Ti_{C2-off} \tag{13}$$

If each of the inductances L_1 and L_2 is large enough, I_{L1} is nearly equal to its average current I_{L1} and also, I_{L2} is nearly equal to its average current I_{L2} .

For $L_1 = L_2$;

$$I_{L1} = I_{L2} = I_L \tag{14}$$

Then, from Eq. (4), we obtain

$$i_{s-off} = I_L \tag{15}$$

Also, by substituting from Eqs. (12), (13), and (14) into Eq. (2), one can obtain:

$$i_{s-on} = I_L + \frac{1 - D}{D}I_L + I_L + \frac{1 - D}{D}I_L = \frac{2}{D}I_L \tag{16}$$

The average supply current can be given as:

$$I_s = Di_{s-on} + (1 - D)i_{s-off} \tag{17}$$

$$I_s = 2I_L + (1 - D)I_L = (3 - D)I_L \tag{18}$$

The voltage stresses across the switch, diodes, and capacitors respectively can be expressed as:

$$V_{SW} = \frac{(3 - 2D)}{(1 - D)} V_{in} \tag{19}$$

$$\left. \begin{aligned} V_{D1} = V_{D2} = V_{D3} &= \frac{(3 - 2D)}{2(1 - D)} V_{in} \\ V_{Do} &= \frac{(3 - 2D)}{(1 - D)} V_{in} \end{aligned} \right\} \tag{20}$$

$$\left. \begin{aligned} V_{C1} = V_{C2} &= V_{in} \\ V_{Co} &= \frac{(4 - 3D)}{(1 - D)} V_{in} \end{aligned} \right\} \tag{21}$$

From this analysis, we can summarize the following:
For $n = 1$;

$$G_1 = \frac{(2 - D)}{(1 - D)} \tag{22}$$

where G_1 is the voltage gain at number of cells (n) = 1.
For $n = 2$;

$$G_2 = \frac{(4 - 3D)}{(1 - D)} \tag{23}$$

This equation can be written as;

$$G_2 = \frac{(2 - D)}{(1 - D)} + 2 \tag{24}$$

where G_2 is the voltage gain at number of cells (n) = 2.
For $n = 3$;

$$G_3 = \frac{(6 - 5D)}{(1 - D)} \tag{25}$$

This equation can be written as:

$$G_3 = \frac{(2 - D)}{(1 - D)} + 4 \tag{26}$$

where G_3 is the voltage gain at number of cells (n) = 3.

To generalize the formula based on number of cells (n), the voltage gain can be obtained according to the following formula for $n \geq 1$.

$$G_n = \frac{(2 - D)}{(1 - D)} + 2(n - 1) \tag{27}$$

and the average supply current for any number of cells can be given as following:

$$I_s = (n + 1 - D)I_L \tag{28}$$

The voltage gain of the proposed converter at different number of cells ($n = 1, 2, \text{ and } 3$) is displayed in Fig. 6. It is obvious that the voltage gain has a higher value in comparison to the conventional DC-DC boost converter. Moreover, the proposed converter can be extended to get higher voltage gains by increasing the cascading additional cells.

Also, the voltage stresses across the switch, diodes, and capacitors for any number of cells can be expressed as:

$$V_{SW} = (G_n - 1)V_{in} \tag{29}$$

$$\left. \begin{aligned} V_{D1} = V_{D2} = V_{D3} &= \frac{(G_n - 1)}{2} V_{in} \\ V_{Do} &= (G_n - 1)V_{in} \end{aligned} \right\} \tag{30}$$

$$\left. \begin{aligned} V_{C1} = V_{C2} &= V_{in} \\ V_{Co} &= G_n V_{in} \end{aligned} \right\} \tag{31}$$

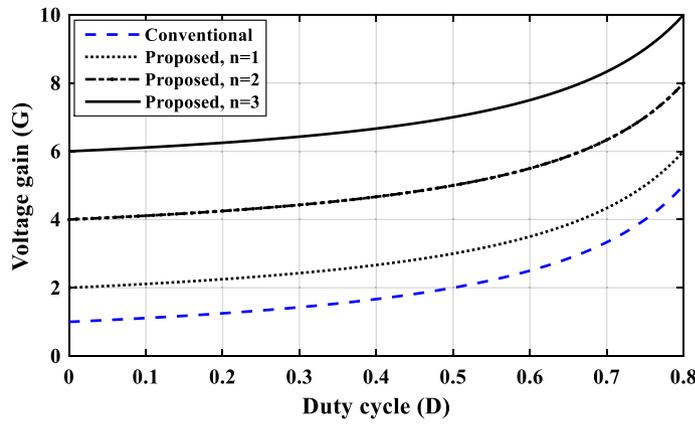


Figure 6. Voltage gain of the proposed boost converter at different number of cells ($n = 1, 2$ and 3) and the conventional one.

Design consideration. The design of inductors and capacitors is considered an important issue to guarantee the operation of the suggested circuit in CCM. Therefore, this part is presented to describe the design of these passive elements.

Inductor design. During Mode 1, the voltage across the inductor is provided by:

$$V_L = L \frac{di}{dt} = L \frac{\Delta I_L}{\Delta t_{on}} \tag{32}$$

The voltage across the inductor is the same as the input voltage. The inductance is defined by:

$$L = \frac{V_{in}}{\Delta I_L} DT = \frac{V_{in}}{(\%r_i)I_L} DT \tag{33}$$

where $\%r_i$ is the percent inductor current ripple allowed. The average value of the inductor current I_L can be obtained from Eq. (18), then, substituting into Eq. (33), one obtains:

$$L = \frac{D(3 - D)}{(\%r_i)G_2^2} R_L T \tag{34}$$

where R_L is the load value. Then, the inductance value for any number of cells can be given from the following equation,

$$L = \frac{D(n + 1 - D)}{(\%r_i)G_n^2} R_L T \tag{35}$$

Capacitor design. The current flowing through the capacitor C_1 in $0 \leq t \leq DT$ period can be obtained from Eqs. (12) and (15) as $((1-D)/D)I_L$. Then, the capacitance value C_1 can be derived as:

$$C_1 \frac{\Delta V_C}{DT} = C_1 \frac{(\%r_v)V_{in}}{DT} = \frac{(1 - D)}{D} I_L \tag{36}$$

where $\%r_v$ is the percent capacitor voltage ripple allowed in C_1 .

By substituting from Eq. (18) into Eq. (36), the capacitance value C_1 can be obtained. In the same way, the capacitance value C_2 can be derived. Hence,

$$C_1 = C_2 = \frac{G_2^2 T}{(\%r_v)R_L} * \frac{(1 - D)}{(3 - D)} \tag{37}$$

For any number of cells, the capacitance value of C_1 and C_2 can be given from the following relation:

$$C_1 = C_2 = \frac{G_n^2 T}{(\%r_v)R_L} * \frac{(1 - D)}{(n + 1 - D)} \tag{38}$$

The capacitor C_o is charged in the period $DT \leq t \leq T$, hence,

$$C_o = \frac{(1 - D)T}{\Delta V_{C_o}} * I_{C_o} = \frac{(1 - D)T}{(\%r_v)V_{C_o}} * (I_L - I_o) \tag{39}$$

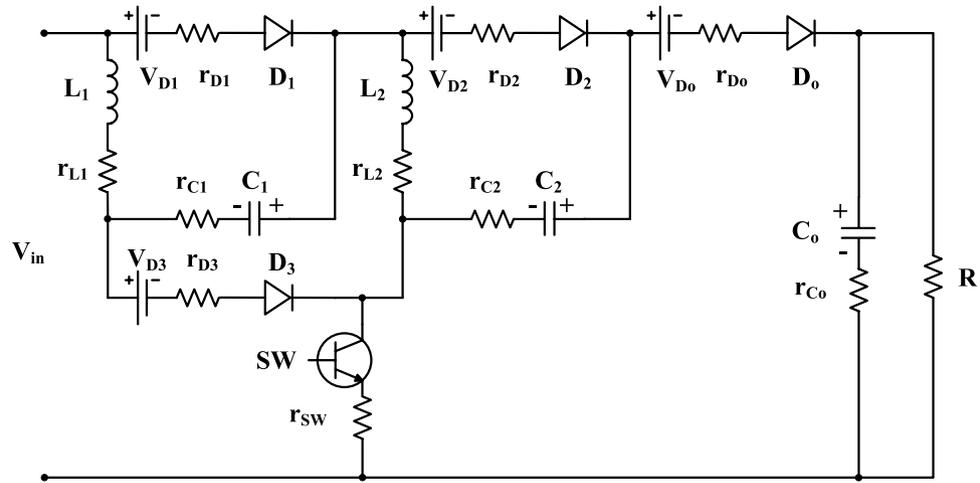


Figure 7. Equivalent model for the proposed circuit with parasitic elements.

By substituting from Eq. (18) into Eq. (39), the capacitance value C_o can be obtained.

$$C_o = \frac{(1 - D)T}{(\%r_v)R_L} * \left(\frac{G_2}{(3 - D)} - 1 \right) \tag{40}$$

For any number of cells, the capacitance value of C_o can be given from the following relation,

$$C_o = \frac{(1 - D)T}{(\%r_v)R_L} * \left(\frac{G_n}{(n + 1 - D)} - 1 \right) \tag{41}$$

Power losses and efficiency

The power losses of the two-cell for the proposed topology are estimated by calculating the switching losses and conduction losses. The power loss of each component is determined, then, the converter power losses can be investigated by summing all these parts. Also, the converter efficiency can be determined based on the power losses. The converter model with the parasitic elements is displayed in Fig. 7.

For the computation of conduction losses in the converter, all diodes are considered with cut in voltages V_{D1} , V_{D2} , V_{D3} , and V_{D_o} . Also, the internal resistances are r_{D1} , r_{D2} , r_{D3} , and r_{D_o} . Each inductor L_1 and L_2 has a lumped DC resistance r_{L1} and r_{L2} , respectively, and each capacitor C_1 , C_2 and C_o has an equivalent series resistance r_{C1} , r_{C2} , and r_{C_o} , respectively. Both conduction and switching losses are considered for the main switch with on-state resistance occupied as r_{sw} .

The power switch losses. The practical power switch has conduction and switching losses. The switching loss is the sum of the conduction and switching losses and it can be written as:

$$P_{loss(SW)} = P_{loss-conduction(SW)} + P_{loss-switching(SW)} \tag{42}$$

where the conduction loss of SW can be stated as:

$$P_{loss-conduction(SW)} = i_{SWrms}^2 * r_{SW} \tag{43}$$

The switch current can be obtained from Mode 1 and Eq. (16), then the *rms* value of the switch current can be established as:

$$i_{SWrms} = \frac{2V_oG}{R\sqrt{D}(3 - D)} \tag{44}$$

Substituting from (44) into (43), then the power conduction loss can be determined by:

$$P_{loss-conduction(SW)} = \frac{4V_o^2G^2}{R^2D(3 - D)^2} r_{SW} \tag{45}$$

The switching loss ($P_{loss-switching}$) of the power switch SW can be determined by:

$$\begin{aligned}
 P_{loss-switching(SW)} &= P_{loss-switching(SW)-on} + P_{loss-switching(SW)-off} \\
 P_{loss-switching(SW)} &= \frac{t_{on} * V_{SW} * i_{SW-on} * fs}{2} + \frac{t_{off} * V_{SW} * i_{SW-off} * fs}{2} \\
 P_{loss-switching(SW)} &= \frac{(t_{rt} + t_{ft}) * V_{SW} * i_{SW-avg} * fs}{2}
 \end{aligned} \tag{46}$$

where t_{rt} and t_{ft} is the rise time and fall time of the switch, respectively.

The average current of the switch current can be found as:

$$i_{SW-avg} = \frac{2GV_o}{R(3 - D)} \tag{47}$$

Substituting from (19) and (47) into (46), then the power switching loss can be determined by:

$$P_{loss-switching(SW)} = \frac{(t_{rt} + t_{ft}) * V_o^2 * (3 - 2D) * fs}{R(3 - D)(1 - D)} \tag{48}$$

Then the switching loss of SW can be investigated by:

$$\left. \begin{aligned}
 P_{loss-total(SW)} &= \frac{4G^2V_o^2}{R^2D(3 - D)^2} r_{SW} \\
 &+ \frac{(t_{rt} + t_{ft}) * V_o^2 * (3 - 2D) * fs}{R(3 - D)(1 - D)}
 \end{aligned} \right\} \tag{49}$$

The diodes losses. The diodes are supposed to have the same cut in voltages and equivalent series resistance, $V_{D1} = V_{D2} = V_{D3} = V_{Do} = V_D$; $r_{D1} = r_{D2} = r_{D3} = r_{Do} = r_D$.

The total diodes losses can be stated as:

$$\left. \begin{aligned}
 P_{loss-total(Diodes)} &= P_{loss-D1} + P_{loss-D2} \\
 &+ P_{loss-D3} + P_{loss-Do}
 \end{aligned} \right\} \tag{50}$$

where, the power loss of each diode can be determined by;

$$\begin{aligned}
 P_{loss-D1} &= V_D * i_{D1avg} + i_{D1rms}^2 * r_D \\
 P_{loss-D1} &= (2 - D)V_D * i_L + \frac{(2 - D)^2}{D} * i_L^2 * r_D \\
 P_{loss-D1} &= \frac{(2 - D)GV_oV_D}{R(3 - D)} + \frac{(2 - D)^2G^2V_o^2}{R^2(3 - D)^2D} * r_D
 \end{aligned} \tag{51}$$

$$\begin{aligned}
 P_{loss-D2} &= V_D * i_{D2avg} + i_{D2rms}^2 * r_D \\
 P_{loss-D2} &= (1 - D)V_D * i_L + \frac{(1 - D)^2}{D} * i_L^2 * r_D \\
 P_{loss-D2} &= \frac{(1 - D)GV_oV_D}{R(3 - D)} + \frac{(1 - D)^2G^2V_o^2}{R^2(3 - D)^2D} * r_D
 \end{aligned} \tag{52}$$

$$\begin{aligned}
 P_{loss-D3} &= V_D * i_{D3avg} + i_{D3rms}^2 * r_D \\
 P_{loss-D3} &= V_D * i_L + \frac{1}{D} * i_L^2 * r_D \\
 P_{loss-D3} &= \frac{GV_oV_D}{R(3 - D)} + \frac{G^2V_o^2}{R^2(3 - D)^2D} * r_D
 \end{aligned} \tag{53}$$

$$\begin{aligned}
 P_{loss-Do} &= V_D * i_{Doavg} + i_{Dorms}^2 * r_D \\
 P_{loss-Do} &= (1 - D)V_D * i_L + (1 - D) * i_L^2 * r_D \\
 P_{loss-Do} &= \frac{(1 - D)GV_oV_D}{R(3 - D)} + \frac{(1 - D)G^2V_o^2}{R^2(3 - D)^2D} * r_D
 \end{aligned} \tag{54}$$

Then, the total power loss in the diodes can be determined by substituting from (51), (52), (53), and (54) into (50) as:

$$P_{loss-total(Diodes)} = \left. \begin{aligned} & \frac{(5 - 3D)GV_oV_D}{R(3 - D)} \\ & + \frac{(2 - D)G^2V_o^2}{R^2(3 - D)D} * r_D \end{aligned} \right\} \tag{55}$$

The capacitors losses. There are three capacitors are shown in the proposed topology. The total power loss due to the capacitors is given by:

$$P_{loss-total(Capacitors)} = \left. \begin{aligned} & i_{C1rms}^2 * r_{C1} + i_{C2rms}^2 * r_{C2} \\ & + i_{Corms}^2 * r_{Co} \end{aligned} \right\} \tag{56}$$

The three capacitors are assumed to has the same equivalent series resistance, $r_{C1} = r_{C2} = r_{Co} = r_C$. The *rms* value of current through the capacitors and the power loss of each capacitor can be estimated using the expressions:

$$\left. \begin{aligned} i_{C1rms} &= i_{C2rms} = \sqrt{\frac{(1 - D)}{D}} I_L \\ i_{Corms} &= \sqrt{\frac{D}{(1 - D)}} I_o \end{aligned} \right\} \tag{57}$$

Then,

$$\left. \begin{aligned} P_{loss-C1} &= P_{loss-C2} = \frac{(1 - D)}{D} I_L^2 * r_C = \frac{(1 - D)}{D} \frac{G^2V_o^2}{R^2(3 - D)^2} * r_C \\ P_{loss-Co} &= \frac{D}{(1 - D)} I_o^2 * r_C = \frac{DV_o^2}{R^2(1 - D)} * r_C \end{aligned} \right\} \tag{58}$$

Substituting from (58) into (56), the total power loss due to the capacitors can be given by:

$$P_{loss-total(Capacitors)} = \left. \begin{aligned} & \frac{2(1 - D)}{D} \frac{G^2V_o^2}{R^2(3 - D)^2} * r_C \\ & + \frac{DV_o^2}{R^2(1 - D)} * r_C \end{aligned} \right\} \tag{59}$$

The inductors losses. The inductors loss can be expressed as:

$$P_{loss-total(Inductors)} = i_{L1rms}^2 * r_{L1} + i_{L2rms}^2 * r_{L2}$$

Assuming the inductors have the same internal resistance $r_{L1} = r_{L2} = r_L$ and have the same *rms* value of the inductor currents $i_{L1rms} = i_{L2rms} = i_{Lrms}$. Then, the inductors losses can be determined as:

$$P_{loss-total(Inductors)} = 2i_{Lrms}^2 * r_L \tag{60}$$

Using (18), the *rms* value of the inductor current can be established, then the total power loss in the inductors can be expressed as;

$$P_{loss-total(Inductors)} = \frac{2G^2V_o^2}{R^2(3 - D)^2} * r_L \tag{61}$$

Substituting from Eqs. (49), (55), (59), and (61) into the below equation, the total converter loss can be obtained.

$$\left. \begin{aligned} P_{loss-total} &= P_{loss-total(Switches)} + P_{loss-total(Diodes)} \\ &+ P_{loss-total(Capacitors)} + P_{loss-total(Inductors)} \end{aligned} \right\} \tag{62}$$

The expression for total losses is as follows:

$$\left. \begin{aligned} P_{loss-total} &= \left[a \left(4 \frac{r_{SW}}{R} + b \frac{r_D}{R} \right) + c \frac{r_C}{R} + d \frac{r_L}{R} \right] \\ &+ e \frac{V_D}{V_o} + f((t_{rt} + t_{ft})f_s) P_o \end{aligned} \right\} \tag{63}$$

where

Devices	Value
Inductances (L_1, L_2, L_3, L_4)	9.3 mH
Input voltage (V_{in})	24 V
Output voltage (V_o)	107 V
Output power (P_o)	52 W
Load (R)	220 Ω
Inductances (L_1 and L_2)	3 mH
Capacitances (C_1, C_2)	4.7 μ F
Diodes (D_1, D_2, D_3 , and D_o)	MUR1560
Main switch (SW)	FGH40N60UFD
Switching frequency (f_s)	5 kHz

Table 1. Parameters of the suggested DC–DC boost converter.

$$\left. \begin{aligned} a &= \frac{G^2}{D(3-D)^2}, b = (2-D)(3-D) \\ c &= \frac{2G^2(1-D)}{D(3-D)^2} + \frac{D}{(1-D)}, d = \frac{2G^2}{(3-D)^2} \\ e &= \frac{(5-3D)G}{(3-D)}, f = \frac{(3-2D)}{(3-D)(1-D)} \end{aligned} \right\} \quad (64)$$

Finally, the efficiency (η) of the suggested topology can be determined as:

$$\eta = \frac{P_o}{P_o + P_{loss-total}} \quad (65)$$

where, P_o is the output power. Substituting from (63) into (65), the proposed converter efficiency (η) can be defined as:

$$\eta = \frac{1}{1 + a\left(4\frac{r_{SW}}{R} + b\frac{r_D}{R}\right) + c\frac{r_C}{R} + d\frac{r_L}{R} + e\frac{V_D}{V_o} + f(t_{rt} + t_{ft})f_s} \quad (66)$$

Experimental results

To authorize the efficacy of the proposed DC-DC boost converter, a prototype has been built in the laboratory. The parameters of the suggested converter are given in Table 1. A photograph of the experimental setup system is shown in Fig. 8, and a schematic drawing for the test system is shown in Fig. 9. The results are captured using an oscilloscope during open-loop and closed-loop control.

Open loop results. Figures 10, 11, 12 and 13 show the experimental results when the suggested DC-DC boost topology operates at $D=0.4$. Fig. 10a shows the gate-emitter switch voltage waveform with duty cycle 40%. Fig. 10b shows the input and output voltage waveforms of the proposed converter. It is observed that the output DC voltage at this duty cycle equal to about 107 V obtained from input voltage equal to 24 V, that represents 4.46 times of the input voltage. Also, the output voltage ripple is equal to 4 V that represents 3.7% from the output voltage.

It can be noticed from Fig. 10c that the input current is continuous with average value equal to about 2.36 A. The voltages of the capacitors C_1 and C_2 are shown in Fig. 10d and e, respectively. The voltages across the capacitors C_1 and C_2 are equal with value 21 V across each capacitor, which validates Eq. (21). The experimental waveforms of voltages and currents for L_1 and L_2 are captured in Fig. 11a and b, respectively. It can be noticed that i_{L1} and i_{L2} are continuous signals. This ensures that the converter operates in CCM. The average current value passes through L_1 or L_2 is found to be 1 A that confirms Eq. (18). The voltage across L_1 or L_2 is almost equal to the input voltage (24 V) during the mode 1, and their values are -14 V during mode 2 that confirm the analysis. Figure 11c displays the voltage across the main switch (SW) with a value of 76 V.

The experimental waveforms of voltages across D_1, D_2, D_3 , and D_o are shown in Fig. 12 with values of 36.1 V, 35.9 V, 36 V and 76 V, respectively. It can be seen that the voltage across the diodes D_1, D_2 , and D_3 is almost equal with a value equal to the half value of the voltage across the diode D_o that confirms Eq. (20). Furthermore, Eq. (19) is validated from Figs. 11c and 12d. These figures show that the voltage through the switch equals to the diode D_o voltage.

To present the voltage gain against the duty cycle, the waveforms of Fig. 13 are plotted for derived and experimental results. It can be observed that the experimental and the theoretical curves have a good convergence. However, the slight variations between the theoretical and experimental results are due to the influence of parasitic elements.



Figure 8. The experimental setup system.

The converter efficiency against the output power at different values of the input voltage and at $D=0.4$ is given in Fig. 14. The maximum measured efficiency at $V_{in}=24$ V and $D=0.4$ is 92.6% and increases to 93.7% if the input voltage increases to 48 V. Also, it can be seen that the efficiency is enhanced with raising the input voltage. Furthermore, the measured efficiency at $V_{in}=24$ V and output power $P_o=52$ W is 91.2%. In this case, the total power losses equal 5 W that represents 9.6% from the output power. Also, Fig. 14 shows the theoretical efficiency curve at $V_{in}=24$ V that calculated from Eq. (66). The great convergence between the theoretical and measured efficiency curves proves the validity of the analysis. Table 2 shows the measured efficiency of the suggested converter and other similar works at the same output power, $P_o=52$ W. It is clear from Table 2 that the suggested converter has the highest efficiency compared to the other related topologies.

Figure 15a illustrates the power losses division and the ratio of power losses for each component from the total power losses. The switch loss, the inductors losses, the capacitors losses, and the diodes losses represents 4%, 19%, 29%, and 48% of the total power losses, respectively. Figure 15b illustrates the efficiency pie chart at this experimental case. Hence, the converter efficiency can be enhanced by choosing low voltage/current rating of its components and the production of final converter fabrication.

Closed loop results. The experimental prototype is also examined during a closed loop control. A schematic diagram of the circuit that is utilized to control the output voltage of the proposed converter is shown in Fig. 16. A PI controller is applied to regulate the output voltage. The parameters of the PI controller are $K_p=100$ and $K_i=200$.

Figure 17 shows the output voltage response with changing the reference voltage (V_{ref}) at input dc voltage equal to 24 V and a full load value. A step change in the reference voltage from 125 to 105 V (decrease) and from

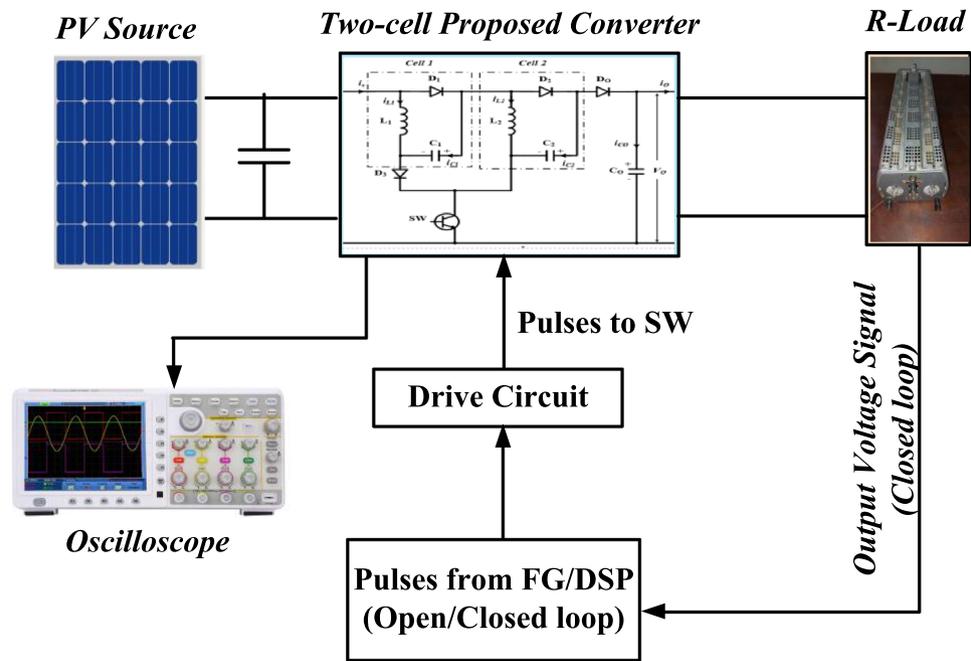


Figure 9. The schematic drawing for the test system.

105 to 125 V again (increase). It is noted that the output voltage tracks the reference voltage smoothly. Figure 18 shows the output voltage response with changing the input voltage at $V_{ref}=140$ V. A step change (decrease/increase/decrease) in the input voltage from 30 to 24 V is applied. This step change represents 25% change of the input voltage. It is observed that the output voltage maintains its value under reference voltage change. Figure 19 shows the output voltage response with changing the load resistance value at $V_{ref}=115$ V. A step change (increase/decrease) in the load resistance value from about 30% of the full load to full load value is applied. The output voltage remains constant under load changes. This proves the effectiveness of the closed loop control of the proposed converter.

Discussion

In this part, a comparison between the two-cell proposed converter and other recent boost topologies is presented. Table 3 shows the comparison results according to the number of components, ideal voltage gain, and maximum voltage stresses through the main switch, output diode, and the output capacitors. The waveforms, which summarize the comparison, are plotted as shown in Figs. 20, 21 and 22.

Figure 20 illustrates the variation of voltage gain when the duty cycle is varied, the proposed converter has the highest voltage gain for $D \leq 0.5$. For $D > 0.5$, the converter in²⁹ has the highest voltage gain value. However, the proposed topology has a total number of components of 10 components, but the converter in²⁹ has 16 components which increases the cost and complexity of the system and decreases the efficiency. Also, the proposed converter has higher voltage gain for duty cycle varies from 0.5 to 0.67 than converters in^{31–33}, and the conventional one. The normalized maximum switch voltage stress for each converter is recorded in Table 3 and shown in Fig. 21. Converter in³¹ has the highest normalized switch voltage stress, while converter in²⁹ has the lowest normalized voltage stress, and approximately constant for all voltage gain values. The introduced converter has modest normalized voltage stress across the main switch. The normalized maximum output diode voltage stress for each converter is documented in Table 3 and shown in Fig. 22. The suggested converter has the lower normalized output diode voltage stress except the converter in³² that has the lowest value. However, the converter in³² has total number of components of 14 components which greater than the proposed converter that decreases the efficiency and increases the cost and the volume of the converter. From this comparative analysis, it is proved that the suggested converter has significant features in comparison to the modern topologies.

Conclusion

A new design of compact circuit that converts a low-level dc voltage to a high-level dc voltage has been proposed in this paper. It has a single switch and fewer passive components compared with recent boost converters. The new converter gets a high voltage gain at modest duty cycle, low switching losses, good efficiency, and it can be extended to get higher voltage gains by increasing the cascading additional cells. The suggested converter has been examined during open and closed loop process, and ensures a good control performance under reference voltage, input voltage, and load changes. Experimental results under different operating situations prove the usefulness of the new converter. In addition, the comparison between the new two-cell boost converter and

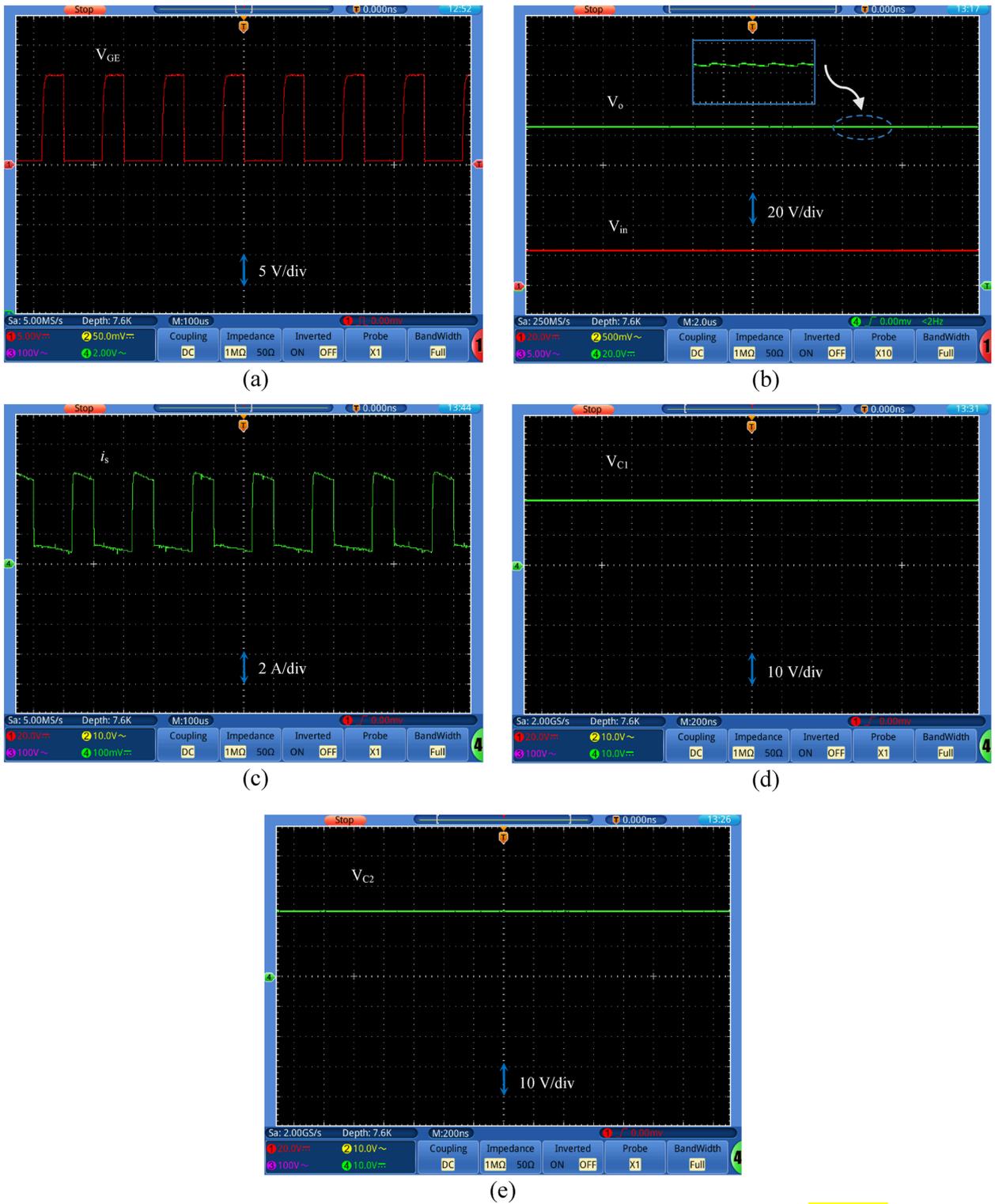
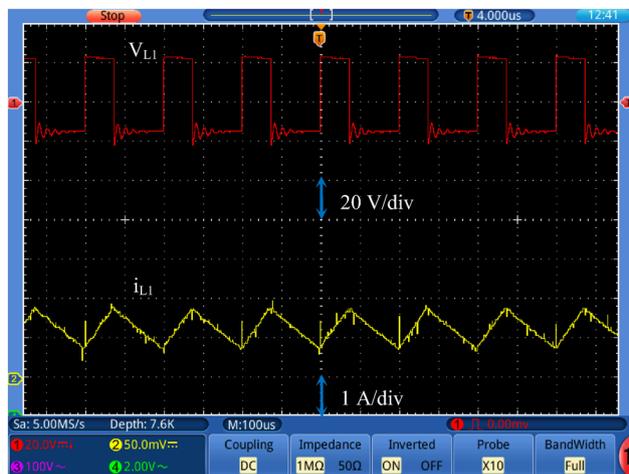
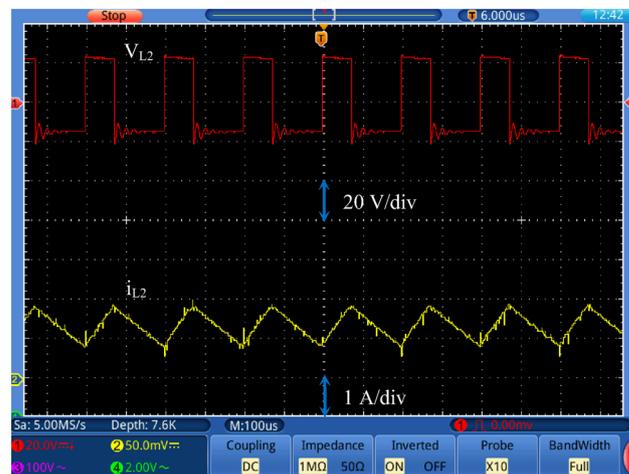


Figure 10. Experimental waveforms of (a) gate-emitter voltage, (b) input and output voltage, (c) input current, (d) capacitor C_1 voltage, and (e) capacitor C_2 voltage.

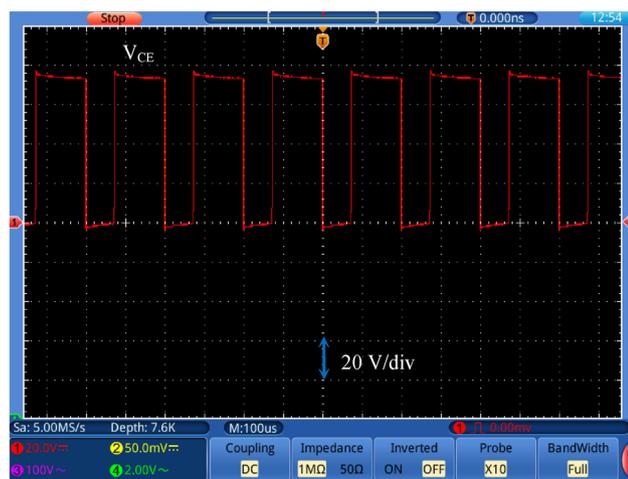
other recent topologies has been presented. The proposed converter has the greatest voltage gain for duty cycle values $D \leq 0.5$ with a total number of 10 components, which decreases the cost and complexity of the converter and increases the efficiency.



(a)



(b)



(c)

Figure 11. Experimental waveforms of (a) inductor L_1 voltage and current, (b) inductor L_2 voltage and current, and (c) SW voltage.

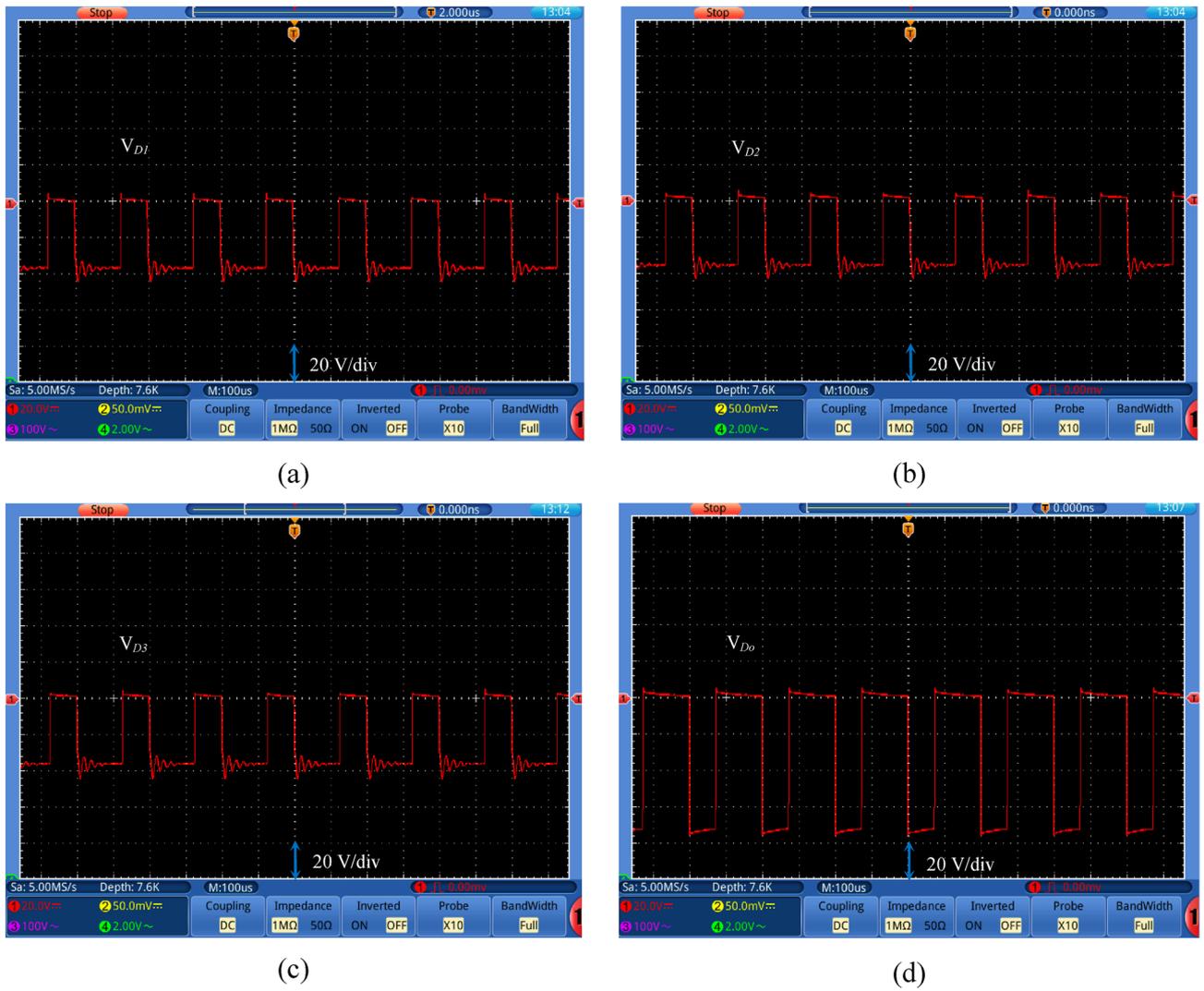


Figure 12. Experimental waveforms of (a) diode D_1 voltage, (b) diode D_2 voltage, (c) diode D_3 voltage, and (d) diode D_0 voltage.

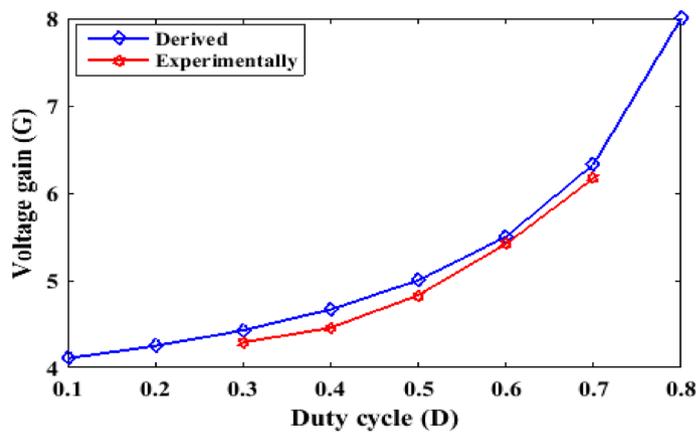


Figure 13. Voltage gain versus duty cycle: derived and experimentally.

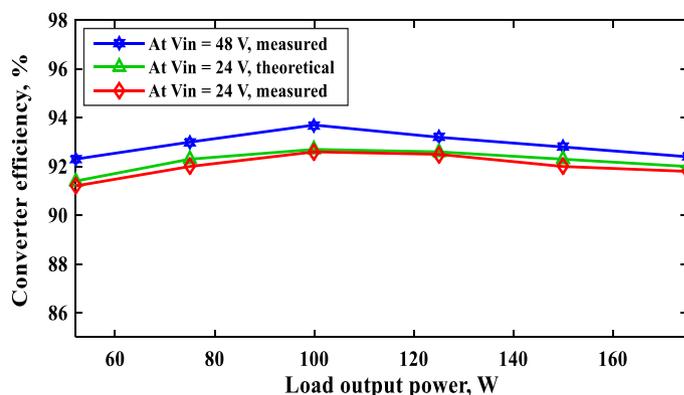


Figure 14. Converter efficiency versus output power at different values of the input voltage and $D=0.4$.

Type of converter	Measured efficiency (%)
Conventional converter	87.3
A converter in ³	90.8
A converter in ¹⁵	90
A converter in ²²	88.2
A converter in ²³	88
A converter in ²⁴	83.5
Proposed converter	91.2

Table 2. Measured efficiency of the proposed circuit and other related topologies.

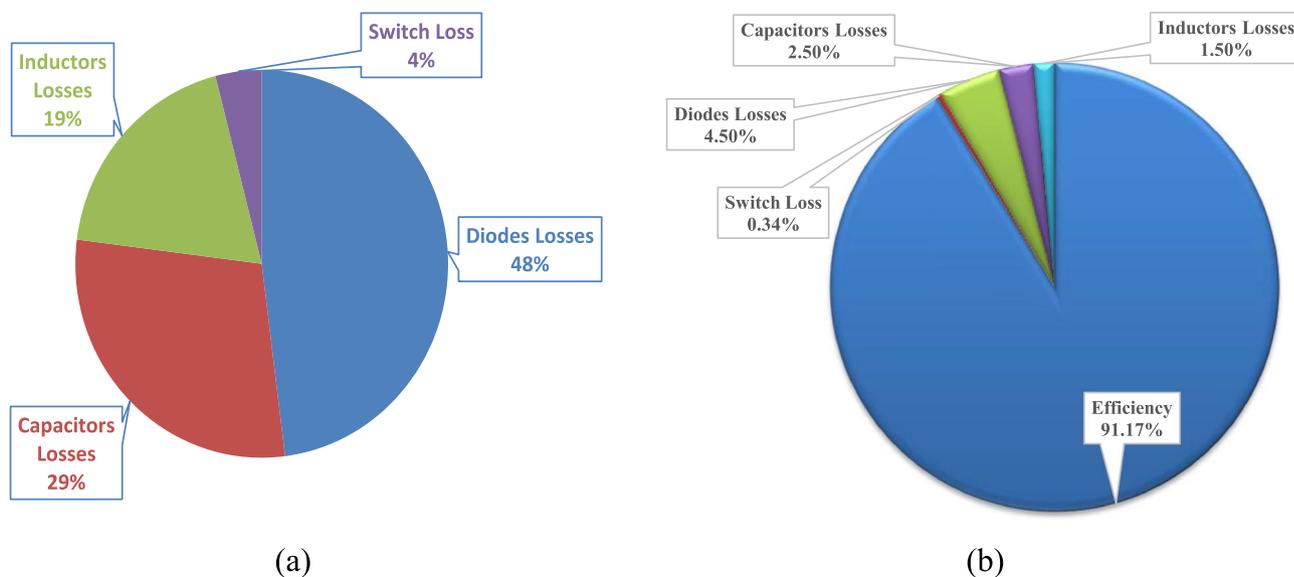


Figure 15. (a) Power loss distribution, and (b) the efficiency pie chart at a duty cycle of 40%, $V_{in}=24$ V and $P_o=52$ W for converter components.

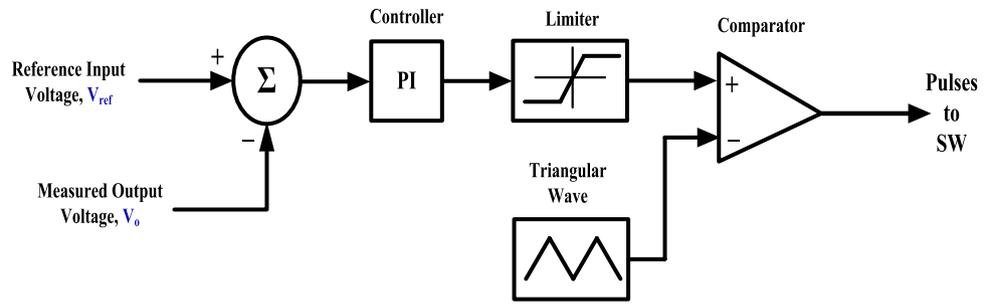


Figure 16. A schematic diagram of closed loop control circuit.

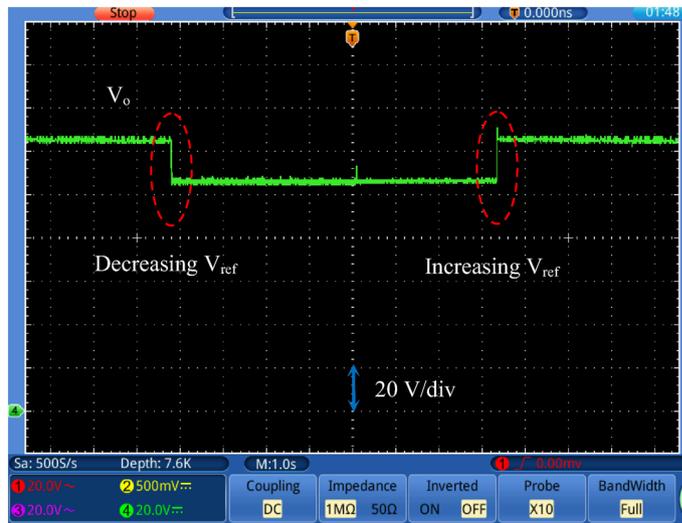


Figure 17. Output voltage with changing the reference voltage (V_{ref}) at $V_{in} = 24$ V.

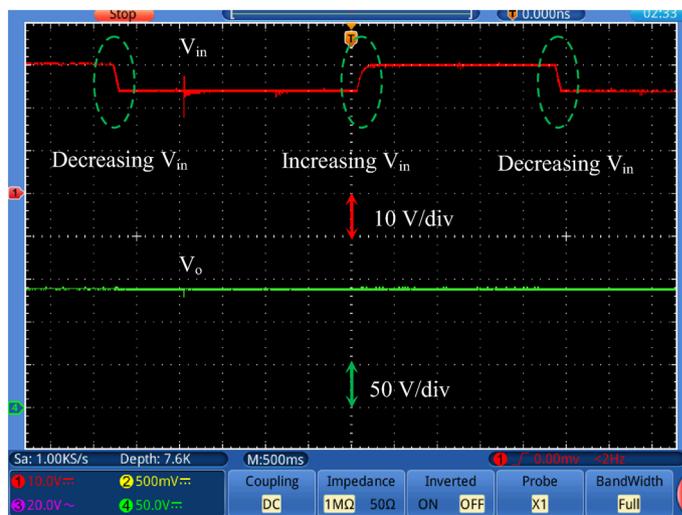


Figure 18. Output voltage response with changing the input voltage (V_{in}) at $V_{ref} = 140$ V.

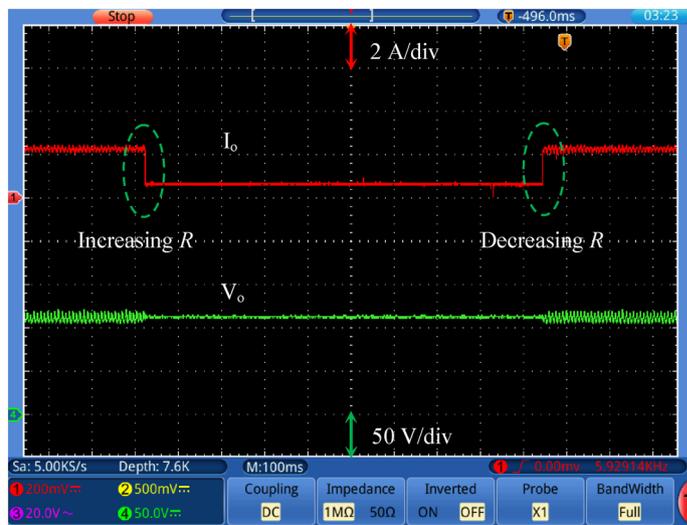


Figure 19. Output voltage response with changing the load value at $V_{ref}=115\text{ V}$.

Converter	Number of					Voltage gain (G)	Maximum switch voltage stress	Output diode voltage	Output capacitor voltage
	Switches	Inductors	Diodes	Capacitors	All components				
Conventional	1	1	1	1	4	$\frac{1}{(1-D)}$	GV_{in}	GV_{in}	GV_{in}
Ref. ²⁹	2	4	9	1	16	$\frac{1+3D}{(1-D)}$	$\frac{(G+1)}{2G} V_{in}$	GV_{in}	GV_{in}
Ref. ³¹	2	3	2	3	10	$\frac{D}{(1-D)^2}$	$\frac{G}{D} V_{in}$	$\frac{G}{D} V_{in}$	GV_{in}
Ref. ³²	1	4	3	6	14	$\frac{3D}{(1-D)}$	$\frac{(G+3)}{3} V_{in}$	$\frac{(G+3)}{3} V_{in}$	GV_{in}
Ref. ³³	2	2	2	2	8	$\frac{2}{(1-D)}$	$\frac{G}{2} V_{in}$	GV_{in}	GV_{in}
Two cells proposed	1	2	4	3	10	$\frac{(4-3D)}{(1-D)}$	$(G-1)V_{in}$	$(G-1)V_{in}$	GV_{in}

Table 3. Comparison between the proposed converter and recent converter topologies.

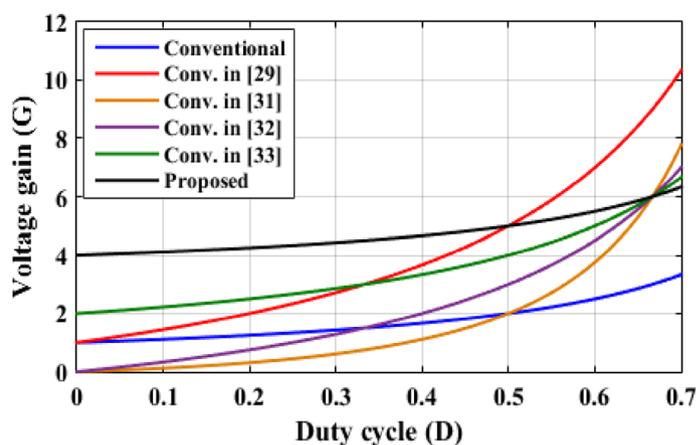


Figure 20. Voltage gain versus duty cycle.

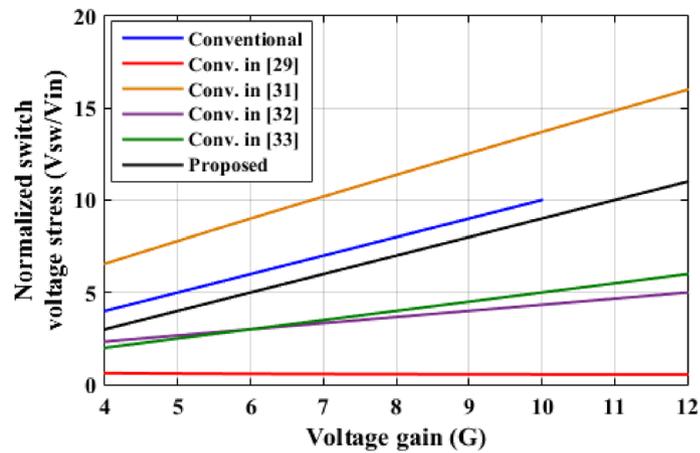


Figure 21. Normalized switch voltage stress with voltage gain variation.

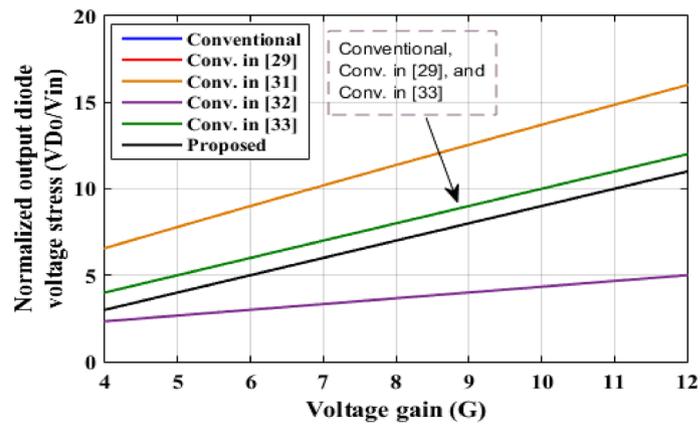


Figure 22. Normalized output diode voltage stress with voltage gain variation.

Data availability

All data generated or analyzed during this study are included in this published article.

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Competing interests

The authors declare no competing interests.

Additional information

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