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## Stabilized voltage source inverter for sensitive loads in nuclear installations

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The present paper proposes a novel design of a stabilized single-phase voltage-source inverter with pure sinusoidal output voltage for photovoltaic systems employed for feeding sensitive loads in nuclear installations. Such types of loads require a voltage source with quite stabilized magnitude and frequency and pure sinusoidal shape that is free from higher-order harmonics. The inverter is based on an H-bridge four insulated gate bipolar transistors (IGBTs) with gate drivers and optocoupler isolators. A control system based on a fast DSP unit and a microcontroller is designed for cancelation of the higher-order harmonics to produce a pure sinusoidal output with almost zero total harmonic distortion (THD). The sinusoidal purity, frequency and magnitude stabilization are achieved through pulse width modulation (PWM) controlled by a fast-response feedback system that measures the time wave form of the output voltage applied to the load and then calculates the THD, frequency and amplitude. The sinusoidal shaping is performed with aid of a sinusoidal shaping filter (SSF) to fasten the operation of higher-order harmonic cancellation. The frequency measurement is achieved through a frequency counter whereas the amplitude measurement is carried out through a differential amplifier that amplifies the difference between the output voltage of the inverter (while being applied to the load) and reference voltage that determines the desired amplitude. A prototype of the entire system of the proposed voltage-source inverter is fabricated for experimental evaluation of its performance. It is shown through simulation and experimental work that the proposed control system of the inverter output voltage is able to stabilize both the amplitude and frequency of the voltage applied to the load irrespective of the load impedance. Also, it is shown that the THD of the output voltage is  $-57$  dB (0.00025%), which is almost zero. Moreover, the switching losses are considerably reduced and can be negligible owing to the use of the appropriate IGBTs. The efficiency of the proposed inverter is obtained by simulation taking into account all types of losses. Also, the dependence of the inverter efficiency on the load current is investigated. The average efficiency of the proposed voltage-source inverter is shown to be higher than 97%.

Some AC-powered equipment utilized in nuclear installations are sensitive to the instabilities of the amplitude and frequency of the AC power system. The critical functions of such equipment in the nuclear installations may be badly affected by the instabilities caused by fluctuations of the amplitude and/or frequency<sup>1,2</sup>. Also, the higher-order harmonics imposed in the electric power system may be dangerous to such AC-powered equipment in the nuclear installations. It often happens that an additional load is added (in parallel) to the loads being energized at the inverter output resulting in a sudden drop in the output voltage. Also, when an energized load is disconnected from the inverter output, a sudden increase in the amplitude of the output voltage may occur. Furthermore, some loads may inject currents with higher order harmonics that may be harmful to such sensitive loads connected to the output of the same inverter. Nevertheless, the stability of the inverter output voltage is vital to electrical power systems in such nuclear installations. For this reason the safe operation of such critical equipment require high-quality voltage source with highly stabilized amplitude and frequency, pure sinusoidal waveform, and high efficiency. The inverter proposed in the present work is a high-quality single-phase voltage source (220 V, 50 Hz), for supplying the vital equipment in nuclear installations as mentioned above.

A stand-alone inverter obtains the DC power from batteries that can be charged by photo voltaic (PV) arrays or by another available source. Those batteries may have built-in battery chargers that can be used to charge the batteries when an AC source is available. One of the most critical issues of the voltage-source inverter design

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is the control system that realizes the amplitude and frequency stabilization and the sinusoidal purity of the output waveform<sup>3</sup>.

Recently, a lot of research work has been focused on the stabilization of the inverter output voltage as a crucial requirement of the inverters used for photovoltaic systems. In 2018, Diouri et al. simulated a voltage-source inverter model with varying load and tested it by Simulink. Proportional-Integral-Derivative (PID) controller was for correcting the voltage drop leading to good regulation of the output voltage of the inverter<sup>4</sup>. In 2019, Wang et al. proposed a novel combined centralized/decentralized method to achieve voltage regulation by overcoming the challenge of PV power imbalance. The response of the reactive inverter power to PV power changes is adaptively scheduled to overcome the negative effect on the voltage regulation caused by voltage/reactive power interaction<sup>5</sup>. In 2020, Ersan Kabalc conducted a survey on single-phase grid-connected voltage-source inverters regarding their enhancements in circuit design and mechanisms of control<sup>6</sup>. In 2021, Dhanamjayulu et al. suggested a novel 15-level single-phase voltage-source inverter. This inverter helps generate 15 levels of stepped voltage with low total harmonic distortion (THD) and thereby improving the efficiency and reducing the cost and system complexity<sup>7</sup>. In 2022, Lulbadda et al. presented the operation of a voltage-source inverter in reactive power-injection mode in the absence of solar energy. The main concern was the design of the control system of the inverter. The suggested method enabled the injection of the amount of reactive power needed for output voltage regulation<sup>8</sup>. In 2023, C. Choeung et al. demonstrated a control system based on linear matrix inequality (LMI) for a voltage-source inverter with LC filter<sup>9</sup>.

In the present work, a new design of a stand-alone stabilized voltage-source inverter for energizing sensitive equipment in the nuclear installation. This inverter depends on an H-bridge of four insulated gate bipolar transistors (IGBTs) for voltage inversion. Also, it depends on a robust control system to produce pure sinusoidal voltage with stabilized amplitude and frequency. The present work proposes new methods for frequency stabilization, voltage regulation and reduction of the THD of the inverter output voltage, especially while being applied to the sensitive load loads of the nuclear installations as mentioned above. These methods are combined in a control system of fast response. A sinusoidal shaping filter (SSF), which is an LC filter, is connected to the output of the H-bridge to enable producing a sinusoidal waveform of the inverter output voltage through the processes of the control system. The main components of the proposed control system are a microcontroller, a digital signal processing (DSP) unit, and the feedback circuits. The microcontroller is dedicated for switching the H-bridge to produce a square-wave AC voltage with the required duty cycle. The function of the DSP unit is to handle the feedback signals and to issue the proper commands to the microcontroller. One of the feedback signals is generated by direct conversion of the output voltage to DC signal and then input to an analog-to-digital converter (ADC) for fast amplitude regulation. Another feedback signal is a scaled rectified version of the inverter output voltage. After rectification, this signal is subjected to sampling and input to another ADC. From this signal, the actual waveform of the inverter output voltage can be reconstructed by the DSP unit to measure the amplitude, frequency, and THD. By proper switching of the IGBTs of the H-bridge and by setting the appropriate value of the duty cycle, the amplitude, frequency and THD of the inverter output voltage can be accurately adjusted irrespective of the load impedance. Moreover, the proposed control system enables the suppression of any higher-order harmonics caused by some types of loads. In the control system of the proposed Voltage-source inverter, the Arduino Uno microcontroller is used for direct switching of the H-bridge and the Espressif ESP32-wroom-32 microcontroller with the Espressif DSP library (ESP-DSP) is used to implement the DSP unit for harmonic analysis of the time waveform of the output voltage. The central unit of the control system is the ESP32 DSP whose commands are issued to the Arduino Uno microcontroller through serial communication.

## Methods and results

### Design requirements of the voltage-source inverter

The inverter is proposed as a single-phase 220 V, 50 Hz, voltage source for vital equipment that play critical roles in nuclear installations. These devices must remain in excellent working condition at all times without interruption. They are very sensitive to any variations of the amplitude and frequency of the power source. Such instabilities of the voltage source may lead to malfunction, temporary, or permanent failure during operation of these equipment thereby resulting in dangerous consequences. For this reason the safe operation of such critical equipment require high-quality voltage source with highly stabilized amplitude and frequency, very low THD, and high efficiency.

### Stability requirements of the voltage source

#### *Amplitude stability*

The amplitude stability of the required voltage source can be realized by minimizing the change of the amplitude from the desired value by minimizing the following errors.

- The amplitude error (AE) is defined as the percent ratio of the mean amplitude error to the desired amplitude.
- The amplitude fluctuation rate (AFR) is defined as the percent ratio of the rms value of the amplitude variation to the rms value of the voltage

#### *Frequency stability*

The frequency stability of the required voltage source can be realized by minimizing the frequency deviation from the desired frequency by minimizing the following errors.

- The frequency error (FE), which is defined as the percent ratio of the mean frequency error to the desired frequency.
- The frequency fluctuation rate (FFR), which is defined as the percent ratio of the rms value of the frequency variation to the mean value of the frequency.

*Sinusoidal purity*

The sinusoidal purity of the output voltage is crucial for excellent operational conditions the equipment mentioned above. It can be realized by minimizing the THD.

- The THD is defined as the percent ratio of the square root of the total power of the higher-order harmonics to the power of the fundamental harmonics.

*High Efficiency*

To optimize the operation and minimize the need for battery replacement, the inverter efficiency should be maximized.

- The inverter efficiency ( $\eta$ ) is defined as the percent ratio of the power consumed by the load to the power input to the inverter (i.e. the power output from the battery).

Quantitatively, the required performance metrics of the proposed voltage-source inverter are summarized in Table 1. It should be noted that these quantitative requirements were determined based on analytical and experimental studies carried out by the work team charged with implementing safety and efficiency procedures of the equipment in the previously mentioned nuclear facilities.

**Design of the inverter switching circuit**

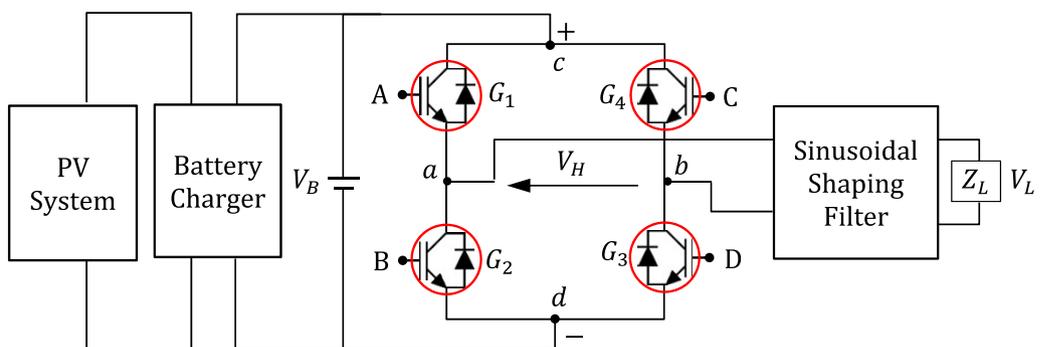
As mentioned in the introduction, the proposed voltage-source inverter belongs to the category of stand-alone inverters that obtain the DC input from batteries that can be charged with the PV array or by an AC source if present and usable. The design of the proposed voltage-source inverter includes the basic IGBT circuit, the IGBT gate driver and the optocoupler isolator.

*Basic IGBT circuit for voltage inversion*

The basic IGBT H-bridge circuit designed for the proposed voltage-source inverter is presented in Fig. 1. The positive terminal of the battery is connected to the point *c* of the H-bridge whereas the point *d* is connected to the negative terminal. The output voltage of the bridge is the voltage between the points *a* and *b*,  $V_H = V_a - V_b$ . If  $V_{Aa} > V_{Th}$  and  $V_{Dd} > V_{Th}$ , whereas  $V_{Cb} = 0$  and  $V_{Bd} = 0$ , then the output voltage,  $V_H$  is positive ( $V_H \approx +V_B$ ). If  $V_{Cb} > V_{Th}$  and  $V_{Bd} > V_{Th}$ , whereas  $V_{Aa} = 0$  and  $V_{Dd} = 0$ , then the output voltage,  $V_H$  is negative ( $V_H \approx -V_B$ ).

| Quality issue       | Condition         |
|---------------------|-------------------|
| Amplitude stability | $AE \leq 2\%$     |
|                     | $AFR \leq 1\%$    |
| Frequency stability | $FE \leq 0.5\%$   |
|                     | $FFR \leq 0.25\%$ |
| Sinusoidal purity   | $THD \leq 1\%$    |
| High efficiency     | $\eta \geq 95\%$  |

**Table 1.** Required performance metrics of the proposed voltage-source inverter.



**Figure 1.** The basic IGBT H-bridge circuit of the proposed inverter.

Thus,  $V_H$  is, primarily, a square-wave with zero-mean (i.e. zero DC component). The H-bridge shown in Fig. 1 is controlled through a fast digital controller that is responsible for generating the control signals at A, B, C and D.

#### IGBT gate driver

Bipolar junction transistors (BJTs) are inserted between the digital controller and the H-bridge to play the dual role of protecting the digital controller and amplifying the current supplied to the gates of the IGBTs of the H-bridge. For example, a BJT current buffer is used as shown in Fig. 2. Note that the BJT  $T_1$  is biased to operate in the active region. It can be shown that the base current  $I_B$  drawn from the microcontroller is given as follows.

$$I_B = \frac{V_C - V_\gamma}{(1 + \beta)R_G} \quad (1)$$

where  $V_\gamma \approx 0.7$  V,  $\beta \approx 300$  is the current amplification for the BJT model 2N3904. If these values are used in (1), one gets  $I_B \approx 0.3$  mA, which is very low current that can be drawn from the digital controller without causing harmful load.

#### Optical isolation of the IGBT circuit

For more protection of the digital controller and for more reduction of the current drawn from the digital controller, an optocoupler isolator can be used as shown in Fig. 3. Active-low control logic is used such that the digital controller sinks the current to turn on the IGBT.

#### Complete design of the inverter switching circuit

The complete circuit diagram of the IGBT H-bridge designed for the proposed voltage-source inverter including the interface circuit between the microcontroller and the H-bridge is presented in Fig. 4. This interface protects the microcontroller from possible high currents that can be drawn from it during operation. The protective interface circuit includes the IGBT gate drivers and the optocoupler isolators as presented in Fig. 4.

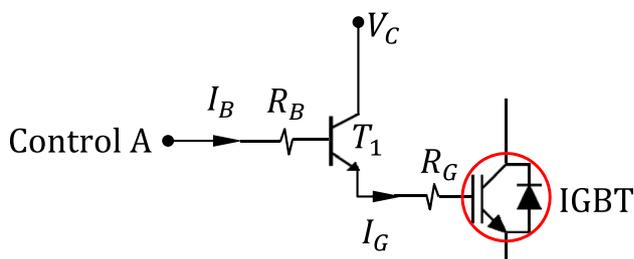
### Analysis of the output voltage of the IGBT H-bridge

#### Time waveforms of switching the H-bridge for efficient voltage inversion

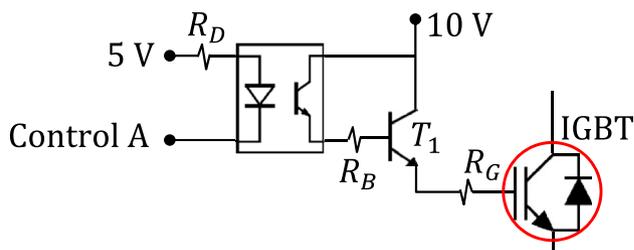
The time waveforms of the input control signals A and B of the IGBT H-bridge and the corresponding output voltage,  $V_H$ , can be sketched as shown in Fig. 5. When the inputs A, D are logically “Low” whereas the logic inputs B, C are logically “High”, the transistors  $G_1$  and  $G_3$  are saturated and the transistors  $G_2$  and  $G_4$  are off. In this case, the H-bridge output voltage,  $V_H$ , is positive and almost equal to the battery voltage,  $V_B$ . In a similar way, when the inputs B, C are logically “Low” whereas the inputs A, D are logically “High”, the inverter output voltage,  $V_H$ , is almost equal to  $-V_B$ . The frequency of the H-bridge output signal,  $f_H$ , can be determined as follows.

$$f_H = \frac{1}{T_L + T_H} \quad (2)$$

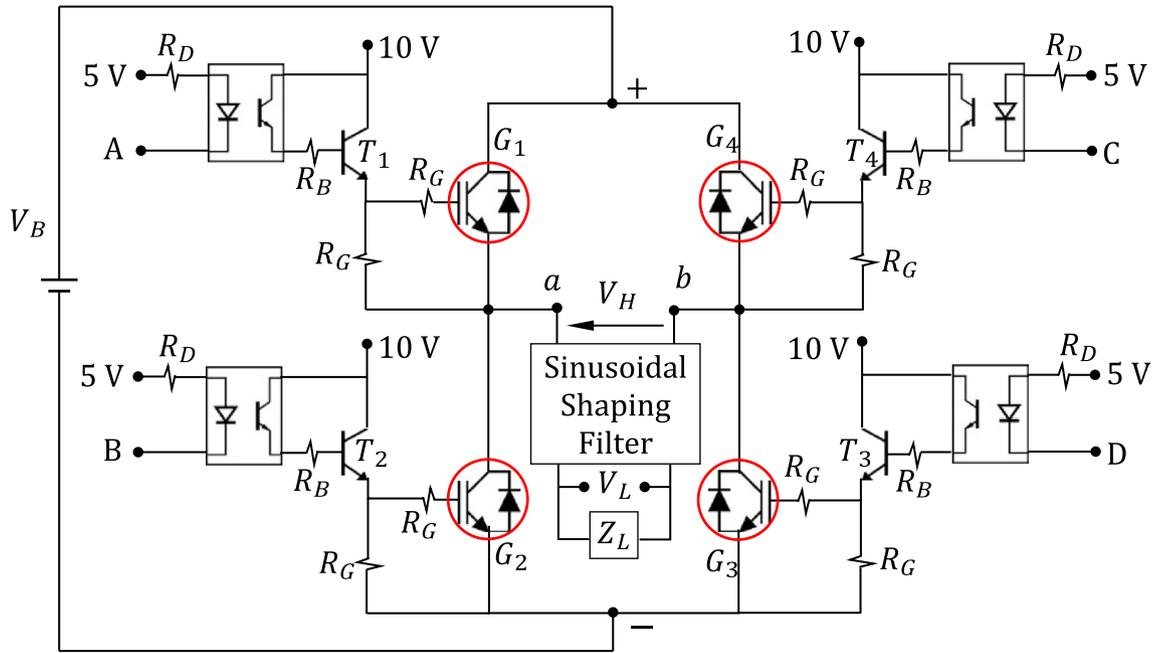
Let us define the ratios  $R$  and  $D$  as follows.



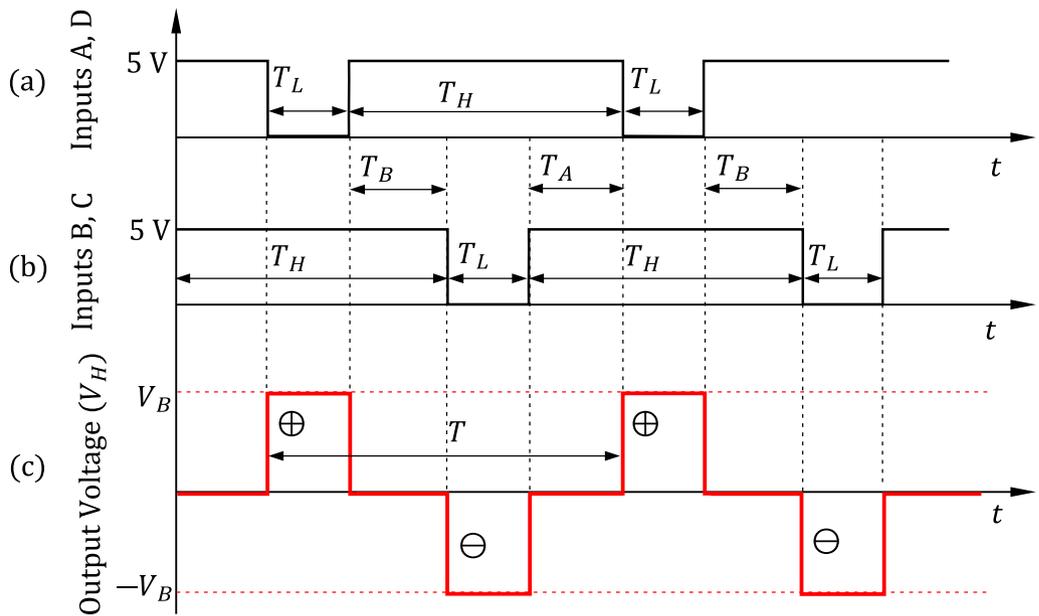
**Figure 2.** IGBT gate driver without optocoupler isolator.



**Figure 3.** Optocoupler isolator is connected for protection of the control circuit.



**Figure 4.** Circuit diagram of the IGBT H-bridge for the proposed voltage-source inverter, the IGBT gate drivers and optoisolators.



**Figure 5.** Sketched time waveforms of the IGBT H-bridge input control signals (A, D) and (B, C) and the corresponding inverter output voltage,  $V_H$ , at no-load.

$$R = \frac{T_H}{T_L}, D = \frac{2T_L}{T_H + T_L} = \frac{2}{R + 1} \tag{3}$$

Note that  $D$  is the duty cycle of the output square wave of the H-bridge. The root-mean-squared (rms) value of the H-bridge output voltage,  $V_{Hrms}$ , can be expressed in terms of the battery voltage and the duty cycle as follows.

$$V_{Hrms} = V_B \sqrt{\frac{2}{R + 1}} = V_B \sqrt{D} \tag{4}$$

Setting  $T = T_H + T_L = 0.02$  s results in a square wave with frequency 50 Hz. In this case, the principal harmonic of the Fourier series expansion will be at 50 Hz.

*Total harmonic distortion of the H-bridge output voltage*

The time waveform of the output voltage of the H-bridge can be expressed in a Fourier series as follows.

$$v_H(t) = \sum_{n=1}^{\infty} a_{Hn} \cos(\omega_n t) = \sum_{n=1}^{\infty} a_{Hn} \cos(n\omega_r t) \tag{5}$$

where,  $\omega_r = 2\pi f_r$  and  $f_r = 50$  Hz is the fundamental harmonic frequency.

Let  $H_H$  be the total harmonic distortion (THD) of the square wave at the H-bridge output; this can be expressed as follows.

$$H_H = \frac{1}{a_{H1}} \sqrt{\sum_{n=2}^{\infty} a_{Hn}^2} \tag{6}$$

where  $a_{Hn}$  is the magnitude of the  $n$ th-order harmonic of the Fourier expansion. As the frequency of the square wave is 50 Hz, the magnitude of the 1st-order harmonic,  $a_{H1}$ , will be much greater than the higher-order harmonics ( $a_{H1} \gg a_{Hn}, n \geq 2$ ). However, the Fourier series of the square wave is slowly convergent as it has very slowly decaying magnitudes and, hence, large number of terms is required for accurate calculation of the series in (5). The rms value of the H-bridge output voltage,  $V_{Hrms}$ , can be expressed in terms of the principal harmonic magnitude,  $a_{H1}$ , and the THD as follows.

$$V_{Hrms} = a_{H1} \sqrt{\frac{1 + H_H^2}{2}} \tag{7}$$

Comparing the expression (7) to (4), it can be shown that,

$$a_{H1} = V_B \sqrt{\frac{2D}{1 + H_H^2}} \tag{8}$$

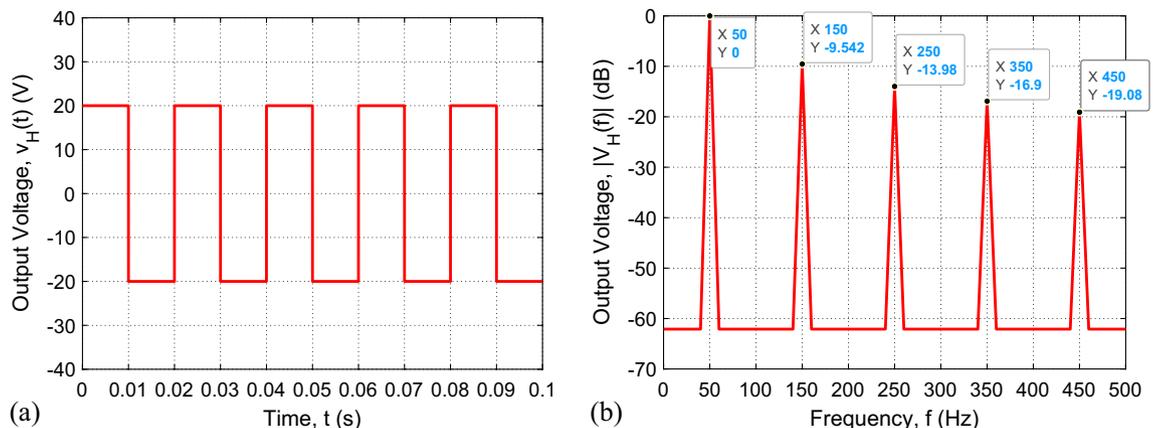
The normalized power of the battery voltage is  $V_B^2$  (i.e. when applied to one- $\Omega$  resistive load), whereas the normalized power of the 1st-order harmonic is  $a_{H1}^2/2$ . Thus,  $H_H$  can be expressed as follows.

$$H_H = \sqrt{\frac{DV_B^2 - \frac{1}{2}a_{H1}^2}{\frac{1}{2}a_{H1}^2}} = \sqrt{\frac{2DV_B^2}{a_{H1}^2} - 1} \tag{9}$$

The last equation means that to calculate the THD of the square wave voltage at the H-bridge output, it is enough to get the magnitude of the first harmonic,  $a_{H1}$ .

**Simulation results for the H-bridge output voltage**

To test the functionality of the IGBT H-bridge, the Proteus simulator is employed and the schematic diagram shown in Fig. 4 is used to monitor the time waveform of the output voltage at the indicated test points *a* and *b*. It should be noted that the model of the Arduino Uno™ microcontroller is used in the Proteus simulator to generate the control signals (A, B, C, and D shown in Fig. 4). The time waveform of the H-bridge output voltage,  $v_H(t)$ , (voltage difference between *a* and *b*) obtained by simulation, is presented in Fig. 6a. The corresponding spectrum magnitude,  $|V_H(\omega)|$ , obtained by applying the fast Fourier transform (FFT), is presented in Fig. 6b. It is shown that only the odd-order harmonics exist where the 1st-order harmonic is exactly at 50 Hz and its magnitude is about three times the magnitude of the 3rd-order harmonic, which is the maximum magnitude among those of the higher-order harmonics. The THD calculated using expression (9) gives  $THD_H \approx 50\%$  (−3 dB), which



**Figure 6.** The output voltage of the H-bridge: (a) Time waveform,  $v_H(t)$ . (b) Normalized frequency spectrum magnitude,  $|V_H(\omega)|$ .  $T = 0.02$  s and duty cycle,  $D = 1$ .

means that the power of the 1st-order harmonic is almost equal to twice the power the of all the other (higher-order) harmonics.

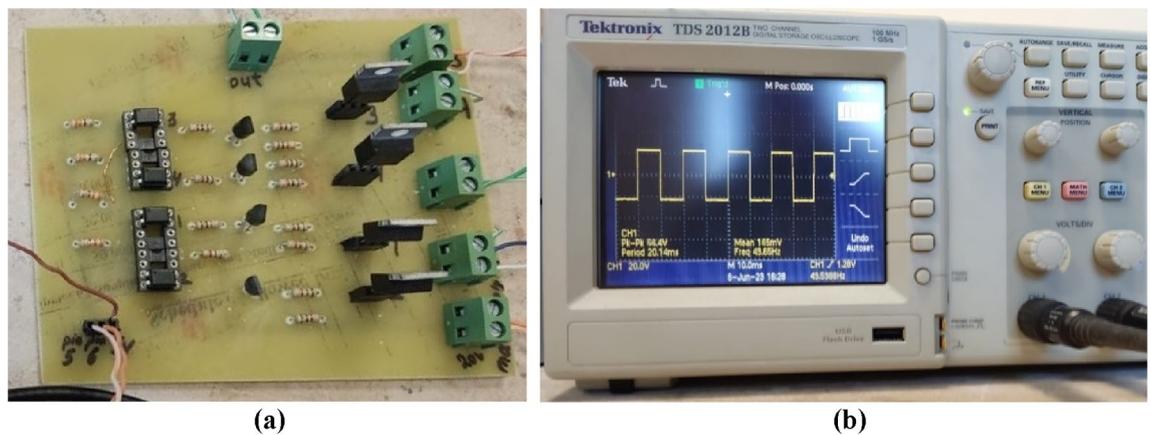
### Experimental measurement of the H-bridge output voltage

For experimental testing of the switching IGBT H-bridge, the circuit prototype shown in Fig. 7a is fabricated. The AC square-wave voltage at the output of the H-bridge is measured using Tektronix oscilloscope model TDS 2012B as shown in Fig. 7b. This model of the oscilloscope has the capability of spectral analysis through the built-in FFT option.

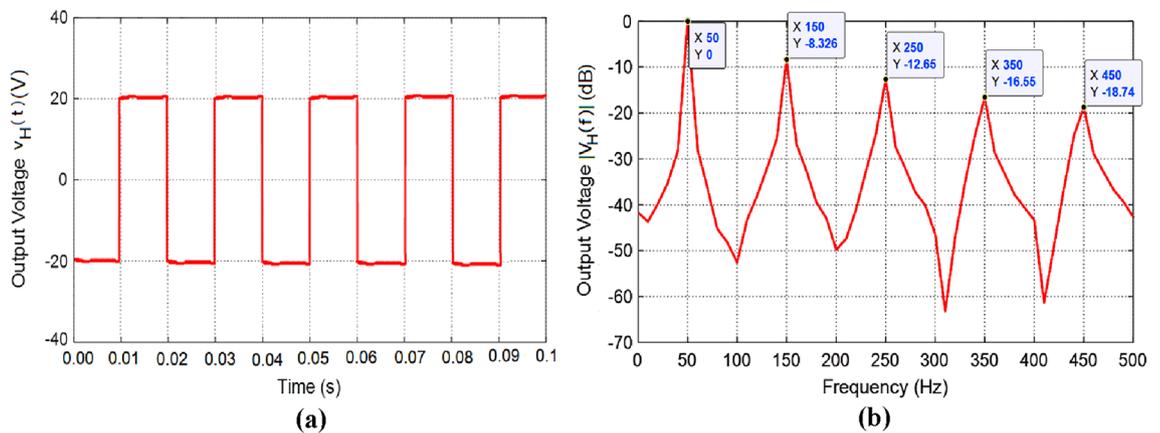
The results of experimental measurements of the AC voltage at the output of the fabricated prototype of the IGBT H-bridge are presented in Fig. 8. These experimental results correspond to the simulation results presented in Fig. 6. The AC square-wave voltage at the output of the fabricated H-bridge is measured using Tektronix oscilloscope model TDS 2012B where the measured waveform is presented in Fig. 8a. This oscilloscope has the capability of spectral analysis through the application of the built-in FFT option. The measured spectrum of the of the H-bridge output voltage is presented in Fig. 8b. It is shown that the simulation and measurement results shown in Figs. 6 and 8, respectively, come in good agreement with each other.

### Sinusoidal shaping of the inverter output Voltage

A fast-response control system is designed to achieve the objectives of the proposed voltage-source inverter including voltage regulation, frequency stabilization, and minimization of THD. This control system requires a SSF at the output of the H-bridge. In the present section, an LC filter resonating at the desired frequency,  $f_r$ , of the output voltage (usually 50 Hz) is proposed.



**Figure 7.** The fabricated IGBT H-bridge circuit produces a square-wave output voltage of frequency 50 Hz when the duty cycle is set to  $D = 1$ . (a) Fabricated H-bridge circuit of the schematic shown in Fig. 4. (b) The output square wave is displayed by the Tektronix oscilloscope model TDS2012B.



**Figure 8.** Output voltage of the IGBT H-bridge (without applying the SSF), as measured by Tektronix oscilloscope model TDS2012B for duty cycle  $D = 1$ . (a) Time waveform,  $v_H(t)$ . (b) Normalized spectrum magnitude,  $|V_H(f)|$ , obtained by the FFT option of the oscilloscope.

*LC Filter for sinusoidal shaping of the H-bridge output*

The objective of the voltage-source inverter design is to achieve a pure sinusoidal time waveform of the AC voltage with the desired frequency at the inverter output. Therefore, it is proposed to suppress the higher-order harmonics of the square-wave H-bridge output voltage using the LC-filter as shown in Fig. 9. The proposed LC filter is constructed of a series coil and shunt capacitor inserted between the H-bridge and the load as shown in the figure. By setting the appropriate values of the inductance and capacitance, such LC filter can be proposed for sinusoidal shaping of the square-wave output voltage. The coil has an inductance  $L_F$  and an (unavoidable) internal resistance  $r_F$  that is usually very small for high-quality wire-wound coil. Thus, the resistance  $r_F$  is proportional to the length of the coil wire, i.e. the number of turns. Also, the coil inductance,  $L_F$ , is proportional to the number of coil turns as explained in Appendix B. Also,  $r_F$  is proportional to  $L_F$ , and one can write the following expression.

$$r_F = \alpha L_F \tag{10}$$

where  $\alpha$  is the constant of proportionality (defined in Appendix B) and has the units  $\Omega/H$ .

The filter output can be expressed as Fourier series expansions with frequency harmonics that are integer multiples of the fundamental frequency 50 Hz.

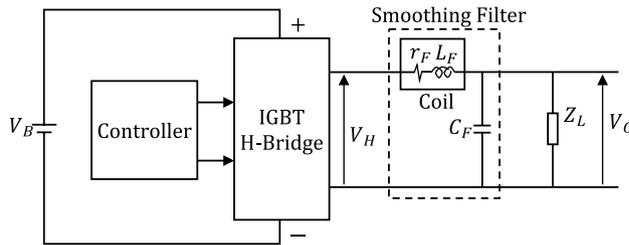
$$v_O(t) = \sum_{n=1}^{\infty} a_{On} \cos(n\omega_r t) \tag{11}$$

Consider that the output impedance of the H-bridge is much smaller than the input impedance of the SSF while the load is being connected in parallel with the filter capacitor as shown in Fig. 10. Thus, the following expression can be obtained for the transfer function of the filter/load combination, which is the relation between the inverter output voltage,  $V_o(\omega)$ , and the output voltage of the H-bridge,  $V_H(\omega)$ .

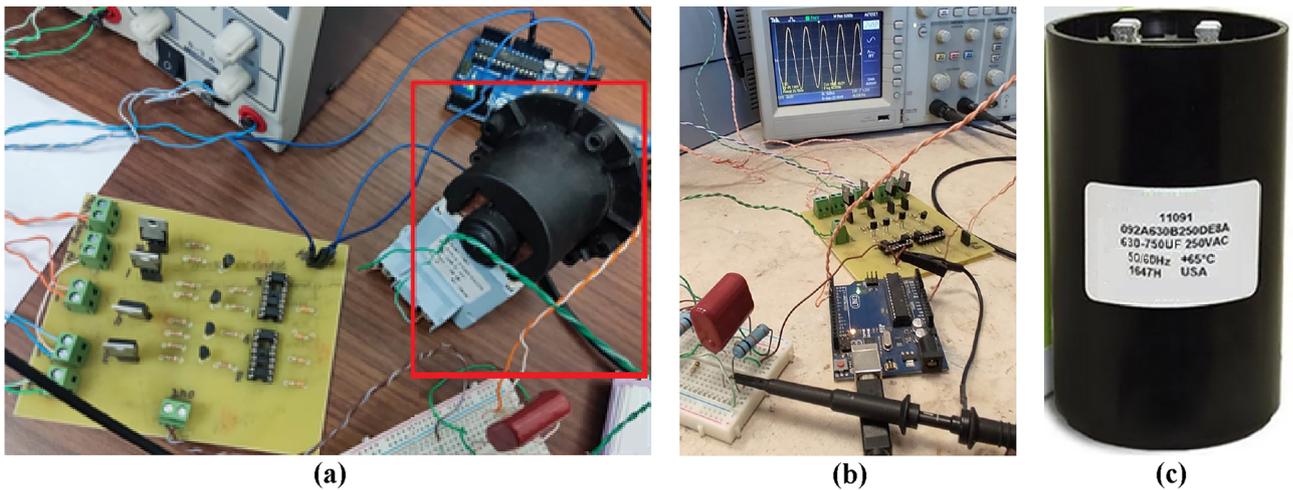
$$G_F(\omega) = \frac{V_o(\omega)}{V_H(\omega)} = \frac{Z_L}{Z_L(1 - \omega^2 L_F C_F) + r_F + j\omega(L_F + C_F r_F Z_L)} \tag{12}$$

where  $Z_L$  is the load impedance connected at the inverter output.

To filter out all the frequency harmonics except for that with  $f = f_r$ , it is required that  $G_F(\omega)$  has a sharp maximum at  $f_r$ . This can be achieved if  $\omega_r^2 L_F C_F = 1$ , where  $\omega_r = 2\pi f_r$ . This requires that  $C_F$  and  $L_F$  are related to each other through the following expression.



**Figure 9.** Sinusoidal shaping of the inverter output voltage using an LC filter resonant at 50 Hz.



**Figure 10.** Experimental evaluation of the effect of the SSF. (a) The fabricated inverter with the SSF and the controller. The coil of the SSF is bounded by a red frame. (b) The time waveform of the voltage at the output of the SSF is displayed by the Tektronix oscilloscope model TDS2012B. (c) The 750  $\mu$ F, 250 VAC capacitor from BMI (Airstar Supply) manufacturer.

$$C_F = \frac{1}{\omega_r^2 L_F} \quad (13)$$

At resonance ( $\omega = \omega_r$ ), condition (13) is satisfied and expression (12) can be reduced to get the following expression.

$$G_F(\omega) = \frac{Z_L}{r_F + j\omega_r(L_F + C_F r_F Z_L)} \quad (14)$$

The filter gain,  $\mathcal{G}_F$ , is the magnitude of  $G_F(\omega)$  at resonance.

$$\mathcal{G}_F \stackrel{\text{def}}{=} |G_F(\omega_r)| \quad (15)$$

For well-designed wire-wound coil on MnZn ferrite core (see Appendix B),  $r_F$  is very small and can be neglected. Hence, the filter gain can be expressed as follows.

$$\mathcal{G}_F = \frac{|Z_L|}{\omega_r L_F} \quad (16)$$

This means that decreasing the filter coil inductance,  $L_F$ , increases the filter gain and, hence, increases the amplitude of the amplitude of the inverter output voltage. Moreover, since the coil resistance,  $r_F$ , is proportional to the coil inductance,  $L_F$ , it is recommended to decrease  $L_F$  to reduce the voltage drop across  $r_F$  and to reduce the power dissipated in the SSF.

Since the relation (13) is satisfied, the THD of the output voltage is very small and the output of the filter is almost sinusoidal and can be approximated as follows.

$$v_O(t) \approx A_O \sin(\omega_r t) \quad (17)$$

where  $A_O$  is the amplitude of the sinusoidal voltage applied to the load at the SSF output and can be expressed as follows.

$$A_O \approx a_{O1} = \sqrt{2} |V_O(\omega_r)| \quad (18)$$

Replacing  $V_O(\omega_r)$  by  $G_F(\omega_r) V_H(\omega_r)$  in (18), the amplitude  $A_O$  can be expressed as follows.

$$A_O = \sqrt{2} |G_F(\omega_r) V_H(\omega_r)| \quad (19)$$

From the harmonic analysis of the H-bridge output voltage detailed above, it can be shown that, if  $f_r = 1/T$ , then,

$$|V_H(\omega_r)| = \frac{a_{1H}}{\sqrt{2}} \quad (20)$$

Substituting from (20) into (19) and making use of (15), the flowing expression is obtained for  $A_O$ .

$$A_O = \mathcal{G}_F V_B \sqrt{\frac{2D}{1 + H_H^2}} \quad (21)$$

Substituting for  $\mathcal{G}_F$  from (16) into (21), gives the following

$$A_O = \frac{|Z_L|}{\omega_r L_F} V_B \sqrt{\frac{2D}{1 + H_H^2}} \quad (22)$$

Substituting for  $A_0$  from (22) into (17), the following approximation is obtained.

$$v_O(t) \approx \frac{|Z_L|}{\omega_r L_F} \sqrt{\frac{2D}{1 + H_H^2}} V_B \sin(\omega_r t) \quad (23)$$

As mentioned above, for well-designed SSF,  $H_H$  is very small and can be neglected in (21) and (22). By setting  $D = 1$  and  $H_H = 0$  in (22), the following expression is obtained for  $A_0$ .

$$A_O \approx \sqrt{2} \frac{|Z_L|}{\omega_r L_F} V_B, \text{ for } D = 1 \quad (24)$$

Substituting for  $A_0$  from (24) into (17), the following approximate expression is obtained for the time waveform of the inverter output voltage,  $v_O(t)$ , when applied to load of arbitrary impedance  $Z_L$ .

$$v_O(t) \approx \sqrt{2} \frac{|Z_L|}{\omega_r L_F} V_B \sin(\omega_r t), \text{ for } D = 1 \quad (25)$$

### Experimental measurement of the voltage at the output of the SSF

For experimental measurement of the inverter output voltage, the SSF is fabricated and connected to the output of the IGBT H-bridge as shown in Fig. 10a. The coil is fabricated as a copper wire of diameter 2 mm wound around a cylindrical MnZn ferrite core of diameter 3 cm and length 1.2 cm. The number of turns is 6 to produce coil inductance  $L_F = 13.5$  mH and coil resistance  $r_F = 3.1$  m $\Omega$ . This type of coil is described in-detail in Appendix B. For resonance of the SSF the capacitance of the non-polar capacitor is  $C_F = 750$   $\mu$ F. The AC voltage at the output of the SSF is measured using Tektronix oscilloscope model TDS 2012B as shown in Fig. 10b.

The spectrum of the output voltage is measured through the built-in FFT option of the oscilloscope. The measured time waveform and spectrum of the voltage at the output of the SSF are presented in Fig. 11a and b, respectively, where the load impedance is  $Z_L = 55\Omega$  and the duty cycle is set to  $D = 1$ . Owing to the SSF, the measured time waveform of the output voltage is almost pure sinusoidal as shown in Fig. 11a, where the amplitude  $A_0$  is about 311 V (220 V rms). Also, Fig. 11b shows that the higher-order harmonics have very low magnitudes relative to the fundamental harmonic. This results in a very low value of the THD that is less than  $-37$  dB (0.02%).

### Characteristics of the inverter output without voltage regulation

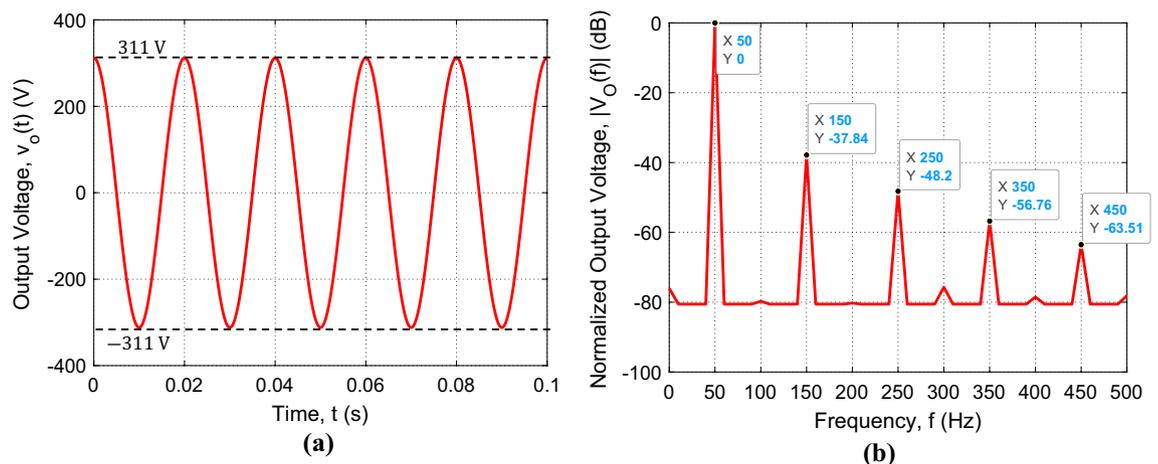
The voltage at the output of the SSF can be expressed as Fourier series expansion with frequency harmonics that are multiples of  $f_r$  as given by (11). As explained in Appendix A, the THD of  $v_O(t)$  can be calculated as follows.

$$H_O = \frac{1}{a_{O1}} \sqrt{\sum_{n>1} a_{On}^2} \quad (26)$$

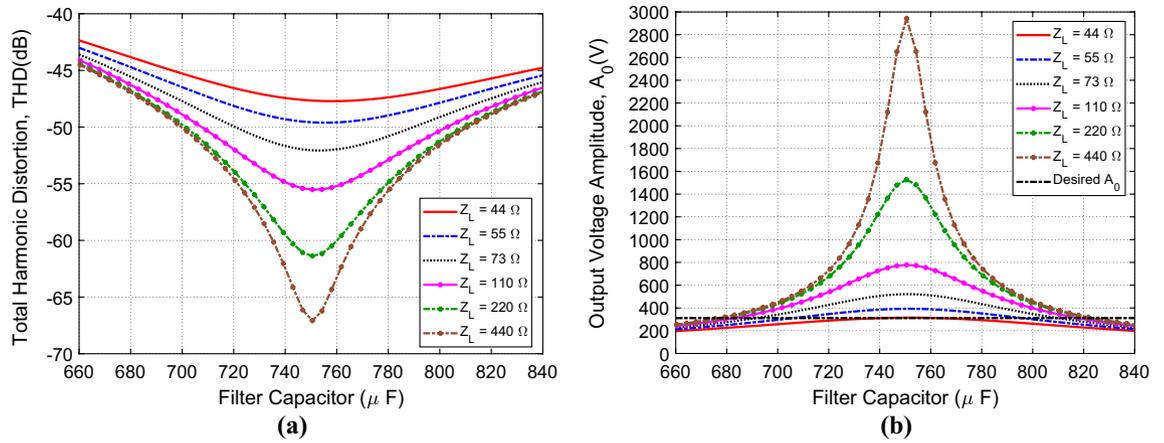
The Proteus simulator is used to obtain the time waveform of the output voltage  $v_O(t)$  for  $T = 0.02$  s to get the fundamental harmonic  $f_r = 50$  Hz. The duty cycle is set to  $D = 1$ , the coil inductance is  $L_F = 13.5$  mH, and the coil resistance is  $r_F = 1.6$  m $\Omega$ . The coil is wire wound on a cylindrical core of MnZn ferrite material with  $\mu_r = 5000$  as described in Appendix B. The THD is then obtained by harmonic analysis using (11) and (26). Figure 12a shows the dependence of the THD on the filter capacitance  $C_F$  for different values of the load impedance,  $Z_L$ . It is shown that the THD is decreased with increasing  $Z_L$ . However, the THD is below  $-40$  dB (0.01%) for all the indicated values of the load impedance ( $Z_L \geq 44\Omega$ ). Also, it is shown that the minimum values (local minima) of the THD is achieved at the resonance of the SSF, i.e. at  $C_F = \omega_r^2/L_F = 750$   $\mu$ F. Figure 12b presents the simulation results to show the dependence of the amplitude,  $A_0$ , of  $v_O(t)$  for  $f_r = 50$  Hz, on the filter capacitance  $C_F$  for different values of the load impedance,  $Z_L$ . It is shown that  $A_0$  increases with increasing the load impedance. Also, it is shown that the maximum values of the  $A_0$  (local maxima) are achieved at the resonance of the SSF, i.e. at  $C_F = \omega_r^2/L_F = 750$   $\mu$ F. It should be noted that it is required to get  $A_0 = 311$  V to get 220 V rms AC voltage at the inverter output. From the curves presented in Fig. 12, it is shown that a control system is necessary to regulate the output voltage so as to keep  $A_0 = 311$  V irrespective of the load variations. The control system proposed for voltage regulation is explained in-detail later on.

### V-Z and V-I characteristic curves of the inverter output without voltage regulation

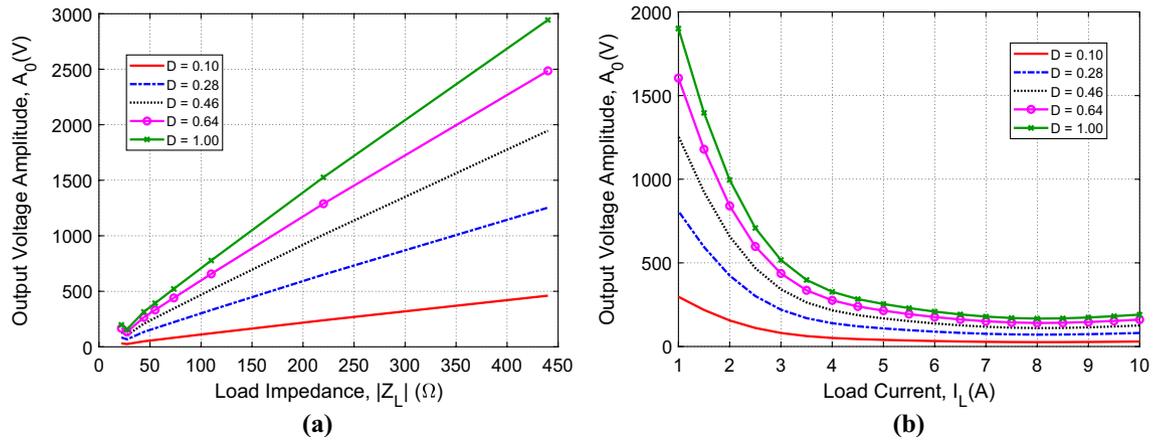
For establishing a robust regulation mechanism of the inverter output voltage when applied to arbitrarily load impedance, it may be necessary to investigate the variation of the inverter voltage with varying the load impedance or, alternatively, with varying the load current. The  $V_L$ - $Z_L$  characteristic curves of the inverter without voltage regulation are presented in Fig. 13a. It is shown that the load voltage decays with decreasing the load



**Figure 11.** The sinusoidal voltage measured by Tektronix oscilloscope model TDS 2012B at the output of the SSF of the proposed inverter for load impedance  $Z_L = 55\Omega$  with periodic time  $T = 0.02$  s and duty cycle  $D = 1$ ; the SSF parameters are  $C_F = 750$   $\mu$ F,  $L_F = 13.5$  mH, and  $r_F = 3.1$  m $\Omega$ . (a) Time-waveform of the SSF output voltage. (b) The corresponding normalized spectrum magnitude,  $|V_O(f)|$ , obtained by the built-in FFT option of the oscilloscope.



**Figure 12.** Dependence of (a) the THD and (b) the amplitude of the inverter output voltage (applied to  $Z_L$ ) on the SSF capacitance,  $C_F$ , for different values of the load impedance,  $Z_L$ ;  $L_F = 13.5 \text{ mH}$ ;  $r_F = 3.1 \text{ m}\Omega$ ;  $D = 1$ .



**Figure 13.** Dependence of the amplitude,  $A_0$ , of the output voltage,  $v_0(t)$ , on (a) the load impedance,  $Z_L$ , and (b) the load current,  $I_L$ , for different values of the duty cycle,  $D$ , without applying the voltage regulation scheme. The period  $T = 0.02 \text{ s}$  ( $f_r = 50 \text{ Hz}$ ) and the SSF parameters are  $C_F = 750 \mu\text{F}$ ,  $L_F = 13.5 \text{ mH}$ , and  $r_F = 3.1 \text{ m}\Omega$ .

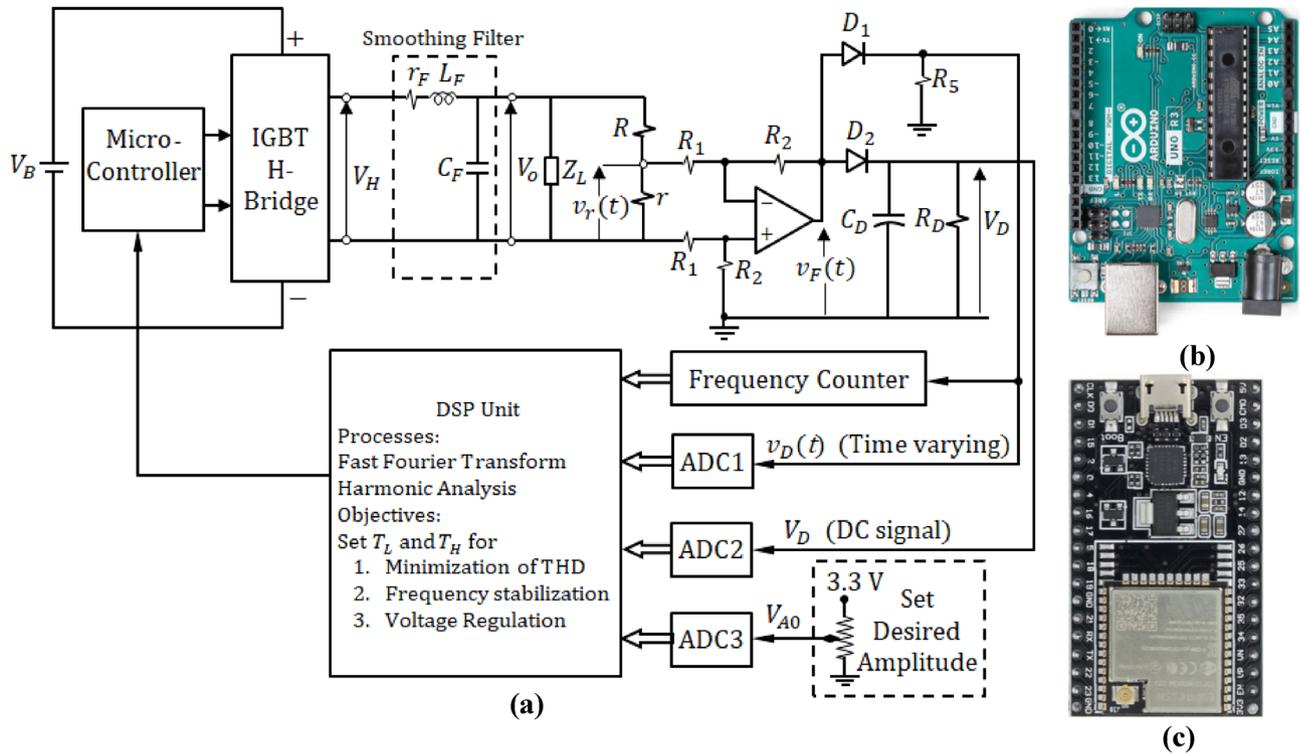
impedance. Also, for a specific value of the load current, the load voltage depends on the value of the duty cycle,  $D$ , defined by the expression (3). The corresponding  $V_L$ - $I_L$  characteristic curves are presented in Fig. 13b. These curves are equivalent to the  $V_L$ - $Z_L$  characteristic curves presented in Fig. 13a. It is shown that the load voltage decays with increasing the load current. Also, for a specific value of the load current, the load voltage depends on the value of the duty cycle,  $D$ . From these characteristic curves, it is shown that a control system is necessary to regulate the output voltage so as to keep  $A_0 = 311 \text{ V}$  irrespective of the load variations. The control system proposed for voltage regulation is explained in-detail later on.

### Control system for voltage regulation, frequency stabilization, and THD Improvement

As discussed in the previous section, it has been shown that the amplitude of the load voltage  $V_L$  is dependent on the load impedance,  $Z_L$ , or, equivalently, the load current,  $I_L$ . According to the load-dependent curves describing the dependence of the THD of the inverter output voltage on the duty cycle,  $D$ , that are presented in Fig. 13a, the value of  $D$  can be determined to keep the THD below a pre-specified maximum allowable value. On the other hand, the dependence of the amplitude of the sinusoidal output on  $D$  is described by the load-dependent curves presented in Fig. 13b. Thus, to stabilize the amplitude of the inverter output voltage, the value of  $D$  can be changed by a regulation mechanism to compensate the change of the load impedance so as to stabilize the amplitude of the output voltage. In the meantime, it can be ensured that the selected value of  $D$  satisfies the required value of the maximum allowable THD. Thus, a control system can be designed to ensure pure sinusoidal output voltage with regulated and stabilized amplitude. Moreover, this control system can stabilize the frequency by controlling the value of  $T$  so as to get the output frequency exactly equal to 50 Hz.

#### Block diagram of the proposed control system

The closed-loop control system shown in Fig. 14a is designed to achieve three main objectives: (i) regulation of the inverter output voltage to have a desired amplitude and stabilization of this amplitude even under impedance



**Figure 14.** Control system for frequency stabilization, amplitude regulation and minimization of the THD of the output voltage. (a) Block diagram. (b) Arduino Uno microcontroller. (c) Espressif ESP32-Wroom-32 DSP unit.

load variation, (ii) stabilization of the output voltage frequency at 50 Hz by controlling the value of  $T$  (equivalently,  $T_L + T_H$ ), and (iii) minimization of the THD of the output voltage. For fast response of the control system to the variation of the load voltage amplitude, the rectified voltage  $V_D$  is used. This voltage is a DC voltage signal that is proportional to the amplitude of the sinusoidal voltage applied to the load. The frequency stabilization and the reduction of the THD require sampling of the actual time waveform of the voltage applied to the load. This can be achieved through the processing of the feedback signal  $v_D(t)$ . This signal is a scaled rectified version of the load voltage  $v_o(t)$ . Using reasonable sampling rate, the FFT of  $v_o(t)$  can be obtained and, hence, the frequency of the principal harmonic can be accurately retrieved and the THD can be calculated. It should be noted that the amplitude of  $v_o(t)$  can, also, be measured by the amplitude of the feedback signal  $v_D(t)$ . However, the measurement of the amplitude by  $V_D$  is faster as there is no processing required like the case in which the amplitude of  $v_o(t)$  is retrieved by processing the signal  $v_D(t)$ . Nevertheless, the amplitude calculated by processing the feedback signal  $v_D(t)$  can be used to confirm the amplitude retrieved directly by reading  $V_D$  through ADC2.

In the proposed control system, the Arduino Uno microcontroller, shown in Fig. 14b, is used for direct switching of the H-bridge, and the Espressif ESP32-wroom-32 microcontroller, shown in Fig. 14c, with the Espressif DSP library (ESP-DSP) is used to implement the DSP unit for harmonic analysis of the time waveform of the output voltage. Thus, the central unit of the control system is the ESP32 DSP whose commands are issued to the Arduino Uno microcontroller through serial communication as described by the block diagram shown in Fig. 14a.

*Generation of the feedback signals required for the control system*

The method proposed for load voltage regulation of the inverter output voltage depends on a feedback system for stabilization of the inverter output amplitude,  $A_o$ . The proposed feedback system is presented in Fig. 14a. A potential divider is connected in-parallel with the load impedance,  $Z_L$ . This potential divider is composed of a small resistance,  $r$ , in series with a high resistance  $R$  as shown in Fig. 14a. The voltage  $V_r$  is proportional to the voltage applied to the load current.

Under the assumption that  $R + r \gg |Z_L|$ , one can write.

$$V_r = V_o \frac{r}{R + r} \tag{27}$$

The output voltage of the differential amplifier can be expressed as follows.

$$V_D = \frac{R_2}{R_1} V_r = V_o \frac{R_2 r}{R_1 (R + r)} \tag{28}$$

*Generation of the feedback signal for frequency stabilization and minimization of THD*

To facilitate harmonic analysis of the inverter output voltage for the purpose of stabilizing the frequency and minimizing the THD, the voltage signal  $v_D(t)$  is generated as a scaled half-wave rectified version of  $v_o(t)$ . The feedback signal,  $v_D(t)$ , can be expressed as follows.

$$v_D(t) = \frac{R_2 r}{R_1(R+r)} \bar{v}_o(t) - V_\gamma \quad (29)$$

where  $\bar{v}_o$  is the half-wave rectified version of  $v_o(t)$ .

**Feedback signal for frequency stabilization.** Measuring the frequency of the inverter output signal doesn't require applying FFT. The control system measures the frequency of  $v_D(t)$  immediately by the frequency counter hardware module shown in Fig. 14a without the need for harmonic analysis. The frequency of the inverter output voltage,  $v_o(t)$ , is the same as the frequency of  $v_D(t)$ . Thus, the output of the frequency counter module is a digital value indicating the frequency of the inverter output. This allows the DSP program to take a fast response and can immediately adjust the frequency of the inverter output voltage. This is performed by setting the correct value of  $T$  and issuing this as a command to the microcontroller program.

**Feedback signal for minimization of THD.** The calculation of the THD of the inverter output voltage requires the application of harmonic analysis to the time waveform  $v_o(t)$ . This is simply achieved in the DSP module by constructing this waveform from the feedback signal  $v_D(t)$ . The Espressif ESP32-wroom-32 microcontroller, used as the DSP module for the proposed inverter, has the ability to perform FFT and IFFT functions, required for harmonic analysis, through the Espressif DSP library<sup>10,11</sup>.

*Generation of the feedback signal for amplitude regulation*

Initially, the operator can set the desired amplitude of the inverter output voltage,  $v_o(t)$ , by setting the value of the analog input  $V_{A0}$  using a precise, high-resolution potentiometer. This signal is fed-back to the control system (input to the DSP) through ADC3 as shown in Fig. 14a. For fast control regarding the voltage amplitude regulation, it is recommended to generate a DC signal that is directly proportional to amplitude of the inverter output voltage. For this purpose, the voltage signal  $V_D$  is generated as a DC voltage proportional to the amplitude of the inverter output voltage,  $A_o$ , and can be expressed as follows.

$$V_D = V_{FM} - V_\gamma \quad (30)$$

where,

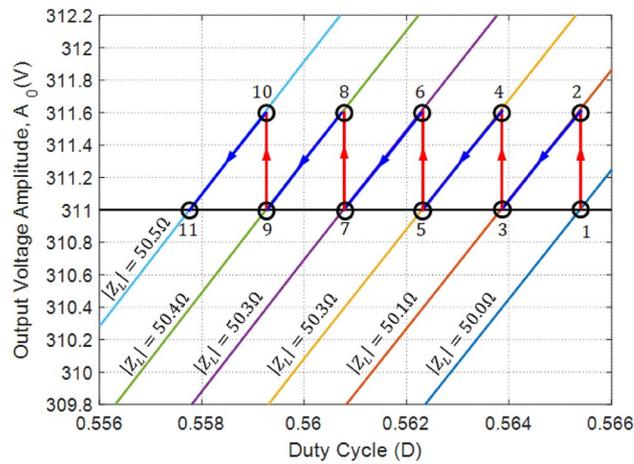
$$V_F = \max(v_F(t)) = \frac{R_2 r}{R_1(R+r)} A_o \quad (31)$$

This signal can be fed-back to the voltage regulation system through ADC2, as shown in Fig. 14a, without the need for any signal processing to get fast response of voltage regulation. A comparison between the DC input voltages  $V_D$  and  $V_{A0}$  is used by the control system to regulate the amplitude of the output voltage to satisfy the requirement that  $V_D = V_{A0}$ .

*Example scenario for applying the amplitude regulation procedure*

As given by (24) and explained through numerical results presented in the previous section, the amplitude,  $A_o$ , of the inverter output voltage is strongly dependent on the magnitude of the load impedance,  $|Z_L|$  and on the duty cycle,  $D$ , of the square-wave voltage at the output of the H-bridge. Thus, an amplitude regulation system is essentially required for the proposed voltage-source inverter to keep the amplitude constant irrespective of the load impedance. The idea of proposed amplitude regulation, proposed in the present work, is based on changing the value of  $D$  to compensate the change of  $|Z_L|$  so as to keep  $A_o$  constant at the desired value. The feedback DC voltage signal  $V_D$  can read by the DSP through ADC2 with 10-bit resolution and sampling rate of 1 MSPS. This enables the DSP to acquire the amplitude of the output voltage with high accuracy and fast rate as explained above.

To demonstrate an example scenario of amplitude regulation, Fig. 15 presents a plot for the curves describing the dependence of  $A_o$  on  $D$  and for different values of  $|Z_L|$ . Consider the case of a sensitive load in a nuclear installation with varying impedance. It is required to energize this load with stabilized output voltage of 220 V (i.e.  $A_o = 311$  V). Consider that the inverter is initially at the operating point 1 as shown in Fig. 15 where  $Z_L = 50\Omega$ ,  $D = 0.5655$ , and  $A_o = 311$  V. At this point,  $Z_L$  starts to gradually increase leading to increase  $A_o$ . Since the minimum detectable change of  $A_o = 0.6$  V (as determined by the resolution of the ADC), the DSP can detect the change of  $A_o$  when it reaches 311.6 V and  $Z_L$  reaches  $50.1\Omega$ . This means that the inverter is moved to operating point 2. To decrease  $A_o$  back to the desired value, the DSP starts to reduce  $D$  gradually (with a much faster rate than that of the load impedance change), which leads to decrease  $A_o$  until the inverter reaches the operating point 3, at which  $A_o = 311$  V,  $D = 0.5639$ , and  $Z_L = 50.1\Omega$ . However, the load impedance continues increasing leading the move the inverter to the operating point 4 at which  $Z_L = 50.2\Omega$ , at which the DSP detects that  $A_o = 311.6$  V. To restore  $A_o$  back to the desired value, the DSP reduces the value of  $D$ , until the inverter reaches the operating point 5, at which  $D = 0.5623$ ,  $Z_L = 50.2\Omega$ , and  $A_o = 311$  V. This process is repeated leading to very low level of amplitude variations around the desired value as shown in Fig. 15 that presents one of the worst case scenarios of the load impedance change. The maximum percentage amplitude fluctuation ratio



**Figure 15.** An example scenario for the amplitude regulation when the load impedance magnitude changes gradually from  $50\Omega$  to  $50.5\Omega$ . The control system continuously changes the value of  $D$  to keep the amplitude the inverter output voltage as close as possible to the desired value.

(% $AFR_{max}$ ) is the percentage ratio between the peak-to-peak voltage (PPV) of the amplitude variation to the mean value of the amplitude. During the worst-case process of voltage amplitude regulation, the % $AFR_{max}$  can be evaluated as follows.

$$\%AFR_{max} = \frac{\text{rms of amplitude variation}}{\text{rms of the output voltage}} \times 100\% = \frac{0.85}{220} \times 100\% = 0.4\% \quad (32)$$

### Simulation and experimental assessment of the voltage-source inverter with applying the control system

The complete voltage source inverter includes the switching IGBT H-bridge, the SSF, and the control system that is constructed by the circuits generating the feedback signals, the microcontroller and the DSP unit. The programs of the Arduino Uno™ microcontroller and the Espressif ESP32-wroom-32™ microcontroller with the Espressif DSP library (ESP-DSP) are developed to perform the function of the control system as described in previous section.

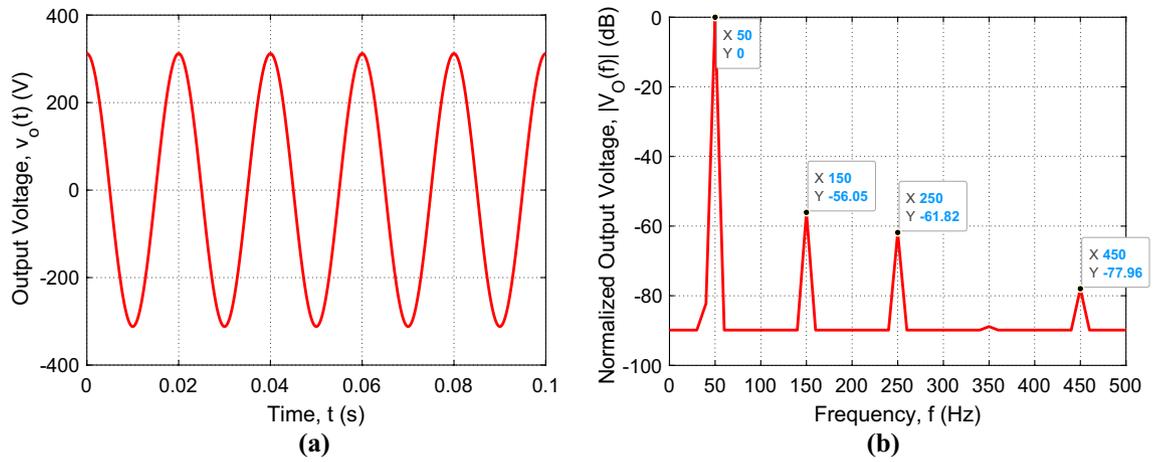
#### Simulation results of the inverter output voltage under the control system

The Proteus simulator is used to simulate the complete design of the proposed voltage source inverter that is presented in Fig. 14a. The entire system including the programs of the Arduino Uno and the ESP32-wroom-32 microcontrollers is subjected to simulation for examining the inverter operation. When the operation of the complete system including the IGBT H-bridge, the SSF, the feedback circuit, the DSP unit, and the microcontroller is simulated in the Proteus simulator, the time waveform and the spectrum of the inverter output voltage are presented in Fig. 16, where the load impedance varies from  $Z_L = 11\Omega$  ( $I_L = 20\text{ A}$ ) to  $Z_L = 440\Omega$  ( $I_L = 0.5\text{ A}$ ). To get the amplitude,  $A_0$  stabilized at  $311\text{ V}$  ( $220\text{ V rms}$ ), the DSP varies the duty cycle  $D$  to compensate the change of  $A_0$  due to the variation of  $Z_L$  as described before. Owing to the application of the control procedure described in the previous section, the time waveform of the inverter voltage is pure sinusoidal as shown in Fig. 16a. It is shown that the amplitude  $A_0$  is stable at, exactly,  $311\text{ V}$  for load impedances varying from  $11\Omega$  to  $440\Omega$ . Also, it is shown in Fig. 16b that the higher-order harmonics are depressed as they have very low magnitudes relative to the fundamental harmonic. This results in a very low value of the THD that is less than  $-57\text{ dB}$  ( $0.0002\%$ ).

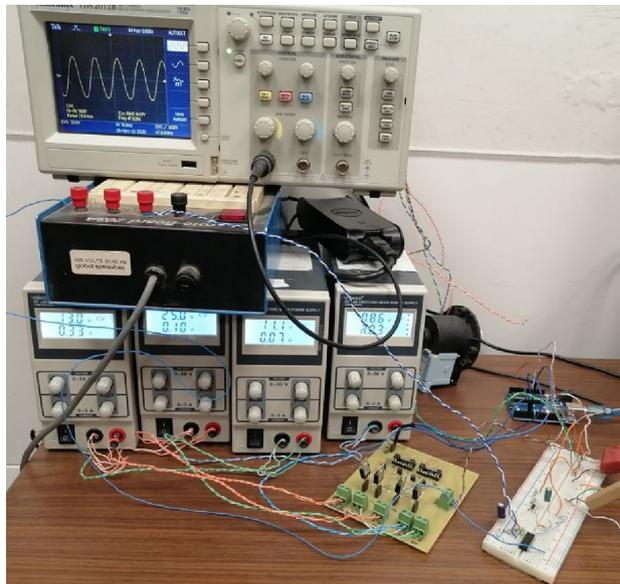
#### Experimental measurement of the inverter output voltage under the control system

The complete circuits of the inverter with the proposed control system are fabricated and subjected to experimental measurements. The fabricated prototype of the voltage-source inverter includes the IGBT H-bridge, the sinusoidal shaping SSF, the Arduino Uno™ microcontroller, and the Espressif ESP32-wroom-32 microcontroller with the Espressif DSP library (ESP-DSP). The experimental measurements are performed by the Tektronix oscilloscope model TDS 2012B as shown in Fig. 17. The built-in FFT facility of the oscilloscope is used to measure the spectrum of the output voltage.

The measured time waveform and the corresponding spectrum of the inverter output voltage are presented in Fig. 18a and b, respectively, for load impedances varying from  $Z_L = 11\Omega$  ( $I_L = 20\text{ A}$ ) to  $Z_L = 440\Omega$  ( $I_L = 0.5\text{ A}$ ). Owing to the application of the control procedure described in the previous section, the measured time waveform of the inverter voltage is pure sinusoidal as shown in Fig. 18a, where the amplitude  $A_0$  is shown to be stable at, exactly,  $311\text{ V}$ . Also, Fig. 18b shows that the higher-order harmonics are depressed as they have very low magnitudes relative to the fundamental harmonic. This results in a very low value of the THD that is less than  $-57\text{ dB}$  ( $0.00025\%$ ). Comparing the results shown in Fig. 16 to those shown in Fig. 18, it becomes clear that the simulation results and experimental measurements of the proposed voltage source inverter agree well with each other.



**Figure 16.** Simulation results of the sinusoidal voltage at the output of the SSF of the proposed inverter for load impedances varying from  $Z_L = 11\Omega$  ( $I_L = 20$  A) to  $Z_L = 440\Omega$  ( $I_L = 0.5$  A) with periodic time  $T = 0.02$  s; the SSF parameters are  $C_F = 750\ \mu\text{F}$ ,  $L_F = 13.5$  mH, and  $r_F = 3.1$  m $\Omega$ . (a) Time-waveform of the inverter output voltage,  $v_o(t)$ . (b) The corresponding normalized spectrum magnitude,  $|V_O(f)|$ , obtained by FFT.



**Figure 17.** Experimental testing of the fabricated prototype of the complete voltage-source inverter including the control system described in the previous section.

### Power loss and efficiency of the voltage-source inverter

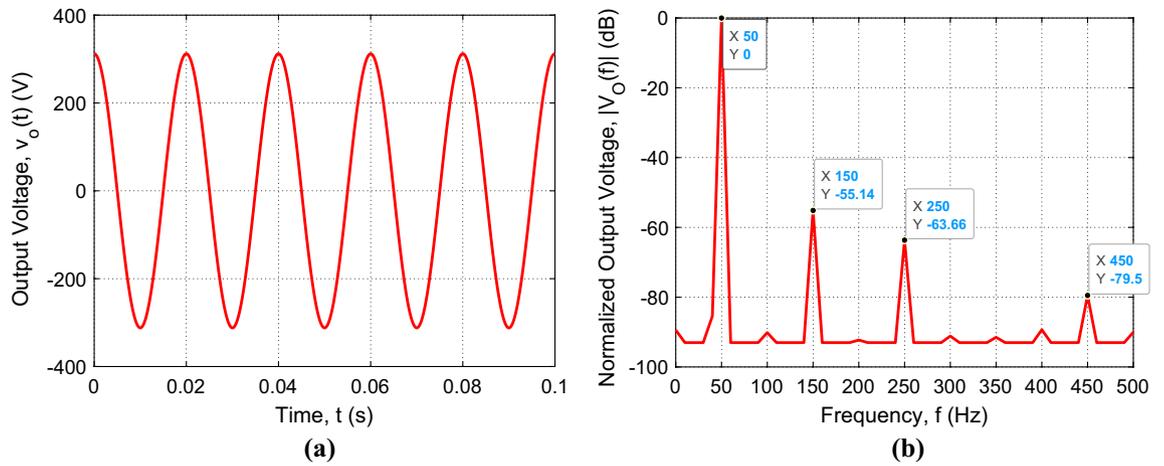
#### Power loss in the voltage-source inverter

There are four main causes of power loss in the proposed inverter design; these can be summarized as follows.

- Power dissipation due to switching losses in the H-bridge,  $P_S$ .
- Heat power dissipation in the IGBTs of the H-bridge,  $P_H$ .
- Power dissipation in the control system,  $P_C$ .
- Power dissipation in the internal resistance,  $r_F$ , of the coil of SSF,  $P_F$ .

Thus, the total power loss can be expressed as follows.

$$P_L = P_S + P_H + P_C + P_F \tag{33}$$



**Figure 18.** The sinusoidal voltage measured by Tektronix oscilloscope model TDS 2012B at the output of the SSF of the proposed inverter for load impedances varying from  $Z_L = 11\Omega$  ( $I_L = 20\text{ A}$ ) to  $Z_L = 440\Omega$  ( $I_L = 0.5\text{ A}$ ) with periodic time  $T = 0.02\text{ s}$ ; the SSF parameters are  $C_F = 750\ \mu\text{F}$ ,  $L_F = 13.5\text{ mH}$ , and  $r_F = 3.1\text{ m}\Omega$ . **(a)** Time-waveform of the inverter output voltage,  $v_O(t)$ . **(b)** The corresponding normalized spectrum magnitude,  $|V_O(f)|$ , obtained by the FFT option of the oscilloscope.

*IGBT switching loss*

In one time period (cycle) of the inverter output voltage, each of the four IGBT is switched “ON” and “OFF” once. Let the total switching energy for a single IGBT be  $e$ . Thus, the total switching loss of the inverter can be expressed as follows.

$$P_S = 8ef_r \tag{34}$$

where,  $f_r$  is the frequency of the inverter output voltage (consider  $f_r = 50\text{ Hz}$  for the present case).

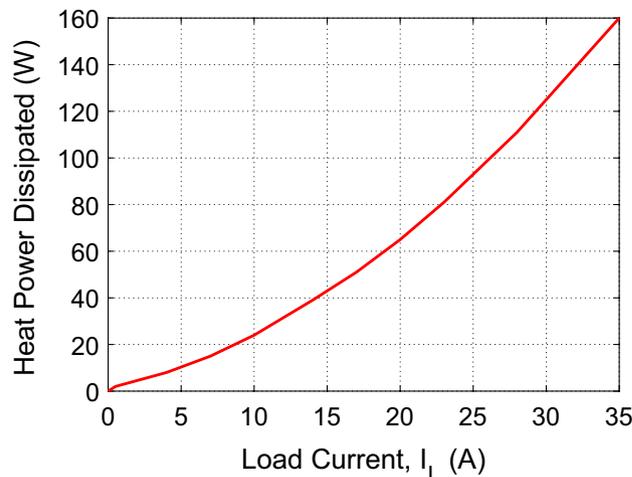
The ON/OFF switching losses (for one IGBT in one cycle of the output voltage) are given in the datasheet<sup>12</sup> for IC of 15 A and VCC of 400 V. Thus, one can set  $e = 0.7\text{ mJ}$  in (34) as a typical value of the switching loss.

$$P_S = 8 \times 0.7 \times 10^{-3} \times 50 = 0.28\text{ W}, I_L = 15\text{ A} \tag{35}$$

Thus, the switching power loss is very small and can be negligible. However, for load current  $I_L = 10\text{ A}$ , the switching loss,  $P_S$ , doesn't exceed the value given by (35).

*Heat power dissipation*

The heat power dissipated in one IGBT (model Infineon SGP15N60) of the H-bridge is presented in Fig. 19 as a function of the load current as given in the manufacturer datasheet<sup>12</sup>. It is shown that the dissipated power in the form of heat energy exhibits a second-order dependence on the IGBT collector current. For the IGBT H-Bridge presented in Fig. 4, the load current is approximately equal to the IGBT collector current. Since, the



**Figure 19.** Heat power dissipated in one IGBT of the H-bridge as a function of the load current<sup>12</sup>.

proposed voltage-source inverter is designed for loads that are, typically, limited to 10 A current, from the curve presented in Fig. 19, one can write,

$$P_H = 2 \times 25 = 50 \text{ W}, I_L = 10 \text{ A} \quad (36)$$

#### Power dissipation in the control circuit

The power dissipated in the circuits of the control system shown in Fig. 15 is the sum of the power dissipated in the Arduino Uno microcontroller, the power dissipated in the Espressif ESP32-Wroom-32 microcontroller, and the power dissipated in the feedback circuit. Due to the high input impedance of the OP-Amp-based differential amplifier, the power dissipated in the control circuit can be approximated as follows.

$$P_C = P_\mu + P_{DSP} + \frac{|V_0|^2}{r+R} \approx P_\mu + P_{DSP} + \frac{|V_0|^2}{R} \quad (37)$$

where,  $P_\mu$  is power dissipated in the microcontroller (typically 1.07 W),  $P_{DSP}$  is the power dissipated in the DSP unit and the three ADCs (typically 0.7 W). Thus, for a resistive load of  $Z_L = 22\Omega$  (i.e.  $I_L = 10 \text{ A}$ ), and considering that  $r = 5.33 \text{ k}\Omega$  and  $R = 1 \text{ M}\Omega$ , the power dissipated in the control unit can be calculated as follows.

$$P_C \approx 1.07 + 0.7 + 10^2 \times \frac{22^2}{10^6} = 1.8 \text{ W}, I_L = 10 \text{ A} \quad (38)$$

Thus, the power dissipated in the control system is much smaller than the power delivered to the load.

#### Power dissipation in the SSF

According to<sup>13</sup>, the magnetic loss of the core made of MnZn ferrite N87 (the material used for the coil used in the proposed inverter design) is negligible for frequencies below 1 kHz. Therefore, the magnetic loss of the ferrite core is neglected in the present study. Thus, the power dissipated in the SSF can be approximated as follows.

$$P_F \approx I_L^2 r_F \quad (39)$$

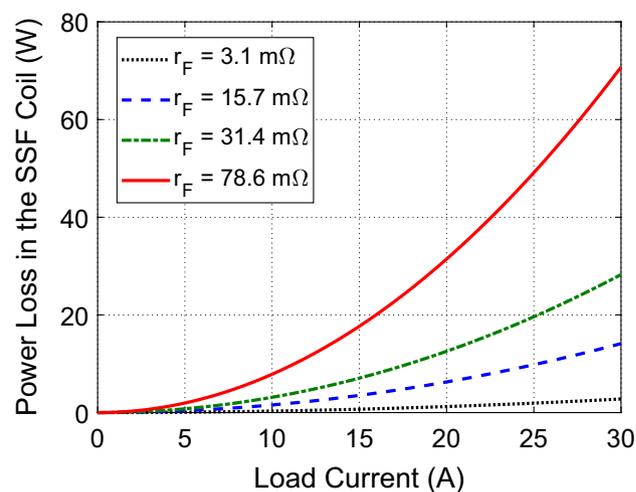
A coil of high-quality wire has a small  $r_F$  and, hence, the dissipated power is very low in comparison to the power delivered to the load. In Appendix B<sup>14,15</sup> it is shown that a coil of MnZn ferrite core with  $D_C = 3 \text{ cm}$ ,  $D_W = 2 \text{ mm}$ , and  $N = 6$  has inductance  $L = 13.5 \text{ mH}$  and internal resistance  $r_F = 1.6 \text{ m}\Omega$ . In this case, for a load current  $I_L = 10 \text{ A}$ ,

$$P_F \approx 10^2 \times 0.0031 = 0.31 \text{ W}, I_L = 10 \text{ A} \quad (40)$$

For the same value of the coil inductance ( $L_F = 13.5 \text{ mH}$ ) used for optimum design of the proposed voltage-source inverter, the coil resistance,  $r_F$ , depends on the relative permeability,  $\mu_r$ , of the ferrite core as shown in Table B.2 of Appendix B. The dependence of the power dissipated in the coil of the SSF on the load current,  $I_L$ , for different values of the coil resistance,  $r_F$ , is presented in Fig. 20. It is shown that using a ferrite core of higher permeability results in a lower value of  $r_F$  and, consequently, reduces the power loss in the coil of the SSF.

#### Total power dissipation

By summation of the four types of power loss encountered in the proposed voltage-source inverter as explained above, the total power loss can be evaluated. Table 2 gives a summary of the typical values of the power dissipated



**Figure 20.** Power dissipated in the SSF as a function of the load current,  $I_L$  for different values of the coil resistance,  $r_F$ .

| Type of power loss         | Value of power loss (W) |
|----------------------------|-------------------------|
| $P_S$                      | 0.28                    |
| $P_H$                      | 50.00                   |
| $P_C$                      | 1.80                    |
| $P_F$                      | 0.31                    |
| Total power loss ( $P_L$ ) | 52.39                   |

**Table 2.** Typical values of the power dissipated in the proposed voltage-source inverter for load current  $I_L = 10$  A (i.e.  $Z_L = 22\Omega$ ).

in the proposed voltage-source inverter for output voltage  $V_0 = 220$  V and load current  $I_L = 10$  A, where the SSF design parameters are set to  $C_F = 750 \mu\text{F}$ ,  $L_F = 13.5$  mH, and  $r_F = 3.1$  m $\Omega$ .

The SSF design parameters are  $C_F = 750 \mu\text{F}$ ,  $L_F = 13.5$  mH, and  $r_F = 3.1$  m $\Omega$ .

### Efficiency of the voltage-source inverter

The power,  $P_o$ , delivered to the load is calculate as follows.

$$P_o = I_L^2 R_L \quad (40)$$

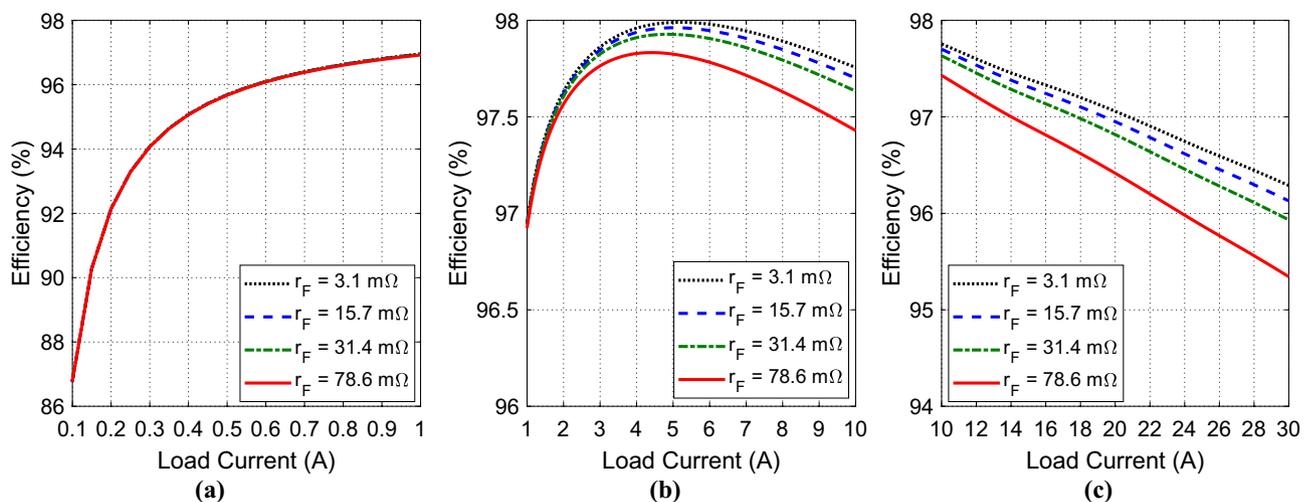
Thus, the typical efficiency of the proposed voltage-source inverter for  $V_0 = 220$  V,  $I_L = 10$  A, and for the total power loss as evaluated in the previous sub section can be obtained as follows.

$$\eta = \frac{P_o}{P_o + P_L} = \frac{2200}{2200 + 52.39} \times 100\% = 97.7\% \quad (41)$$

However, the efficiency of the proposed inverter is plotted versus the load current,  $I_L$ , for different values of the coil resistance,  $r_F$ , as shown in Fig. 21. For low values of the load current,  $0.1 \leq I_L \leq 1.0$  A, the efficiency monotonically increases from 87% to 97% as shown in Fig. 21a. It is clear that, for such low values of the load current, the inverter efficiency is almost independent of the coil resistance,  $r_F$ . When the load current lies within the range,  $1.0 \leq I_L \leq 10$  A, the efficiency ranges between 97% and 98% with a peak value of 98% as shown in Fig. 21b. For large values of the load current,  $10 \leq I_L \leq 30$  A, the efficiency monotonically decreases from about 97.5% to about 95.5% shown linear dependence as shown in Fig. 21c. It is clear that for  $I_L > 1$  A, the inverter efficiency decreases with increasing  $r_F$ .

### Comparison with other inverter designs

A summary of comparisons with other designs of voltage-source inverters available in literature is presented in Table 3. Note that the performance measures THD, AE, AFR, FE, FFR, and  $\eta$  are defined above in the third section titled “Stability requirements of the voltage source”. The list of comparison includes six performance parameters: the AE and AFR as measures of amplitude stability, the FE and FFR as measures of frequency stability, the THD (dB) as a measure of sinusoidal shape purity of the output voltage, and the inverter efficiency. It is shown that the voltage-source inverter proposed in the present work gives the lowest THD and the highest efficiency among the other inverter designs listed in Table 2. Also, the performance measures, AE, AFR, FE, and



**Figure 21.** Efficiency of the proposed voltage-source inverter as a function of the load current in the range (a)  $I_L = 0.1$  to 1.0 A, (b)  $I_L = 1.0$  to 10 A, and (c)  $I_L = 10$  to 30 A, for different values of the coil resistance,  $r_F$ .

| Work    | THD (dB) | AE (%) | AFR (%) | FE (%) | FFR (%) | $\eta$ (%) |
|---------|----------|--------|---------|--------|---------|------------|
| 7       | -27.1    | NA     | NA      | NA     | NA      | 95.2       |
| 16      | -26.0    | NA     | NA      | NA     | NA      | 93.8       |
| 17      | -25.0    | NA     | NA      | NA     | NA      | 94.1       |
| 18      | -24.8    | NA     | NA      | NA     | NA      | 96.7       |
| 19      | -22.0    | NA     | NA      | NA     | NA      | 93.7       |
| 20      | -25.0    | NA     | NA      | NA     | NA      | 94.1       |
| 21      | -28.0    | NA     | NA      | NA     | NA      | 90.0       |
| Present | -57.0    | 0.5    | 0.2     | 0.3    | 0.15    | 97.7       |

**Table 3.** Performance comparison with other voltage-source inverter designs available in literature.

FFR are not mentioned explicitly in the listed publications. It is shown in Table 3 that the design requirements listed in Table 1 are achieved by the proposed design of the voltage-source inverter.

## Discussion

A novel design of a stabilized single-phase voltage-source inverter has been designed to be used in photovoltaic systems employed in nuclear installations for feeding sensitive loads. Such types of loads require a voltage source with quite stabilized magnitude and frequency. The inverter is based on an H-bridge of four type IGBTs with gate drivers and optocoupler isolators. The frequency and magnitude stabilization has been achieved through a robust control system where the Arduino Uno microcontroller is used for direct switching of the H-bridge and the Espressif ESP32-wroom-32 microcontroller with the Espressif DSP library (ESP-DSP) is used to implement the DSP unit for harmonic analysis of the time waveform of the output voltage. The central unit of the control system is the ESP32 DSP whose commands are issued to the Arduino Uno microcontroller through serial communication. A feedback system has been designed to measure the frequency and amplitude of the output voltage applied to the load. The frequency measurement is achieved through a frequency counter whereas the amplitude measurement is carried out through a fast ADC. It is shown that proposed control system is able to stabilize both the amplitude and frequency of the voltage applied to the load and, also, reduces the switching losses of the IGBTs of the inverter. The Proteus simulator is used to investigate the performance of the proposed voltage-source inverter. Also, a prototype has been fabricated for the proposed inverter for experimental evaluation of its performance. Both the simulation results and the experimental measurements have shown that the proposed inverter has stabilized magnitude and frequency with almost zero THD. Also, the inverter efficiency has been shown to be greater than 97%.

## Data availability

All data generated during this study are included in this article.

Received: 7 February 2024; Accepted: 19 June 2024

Published online: 04 July 2024

## References

- Xinling, W. & Cheng, Z. Design and simulation of voltage fluctuation rate monitor system based on virtual instrument technology. *Energy Procedia* **17**, 450–455 (2012).
- Tennakoon, S., Perera, L., Robinson, D. A. & Perera, S. Flicker transfer in radial power systems. in *Australasian Universities Power Engineering Conference (AUPEC 2004)*. Accessed 26–29 Sept 2004.
- Wayback Machine. *Comparison of Photovoltaic Array Maximum Power Point Tracking Techniques* (2010). Accessed 09 Jul 2010.
- Diouri, O., Errahimi, F. & Es-Sbai, N. Regulation of the output voltage of an inverter in case of load variation. *IOP Conf. Ser. Mater. Sci. Eng.* <https://doi.org/10.1088/1757-899X/353/1/012021> (2018).
- Wang, L., Yan, R. & Saha, T. K. Voltage regulation challenges with unbalanced PV integration in low voltage distribution systems and the corresponding solution. *Appl. Energy* **256**, 1–8. <https://doi.org/10.1016/j.apenergy> (2019).
- Kabalc, E. Review on novel single-phase grid-connected solar inverters: Circuits and control methods. *Sol. Energy* **198**(2020), 247–274. <https://doi.org/10.1016/j.solener.2020.01.063> (2020).
- Dhanamjayulu, C. *et al.* Design and implementation of a single-phase 15-level inverter with reduced components for solar PV applications 2021. *IEEE Access* <https://doi.org/10.1109/ACCESS.2020.3046477> (2021).
- Lulbadda, K. L. & Hemapala, U. Use of solar PV inverters during night-time for voltage regulation and stability of the utility grid. *Clean Energy* **6**, 646–658. <https://doi.org/10.1093/ce/zkac042> (2022).
- Choeung, C. *et al.* *LMI-Based Robust Voltage Regulation of a Single-Phase Inverter* 1–11 (Springer, 2023).
- <https://espressif-docs.readthedocs-hosted.com/projects/esp-dsp/en/latest/esp-dsp-apis.html#fft>.
- Plauska, I., Liutkevičius, A. & Janavičiūtė, A. Performance evaluation of C/C++, MicroPython, Rust and TinyGo programming languages on ESP32 microcontroller. *Electronics* **12**(1), 143 (2022).
- <https://www.infineon.com/cms/en/product/power/igbt/>.
- Dobák, S., Beatrice, C., Tsakaloudi, V. & Fiorillo, F. Magnetic losses in soft ferrites. *Magnetochemistry* **8**(6), 60. <https://doi.org/10.3390/magnetochemistry8060060> (2022).
- Coulbaly, S., Malec, D., Bley, V., Mary, D. & Schlegel, B. New use of Mn–Zn ferrite material in power electronics integrated LC filters. *Engineering* **9**(12), 993 (2017).
- Kogias, G., Holz, D. & Zaspalis, V. New MnZn ferrites with high saturation flux density. *Jpn. Soc. Powder Powder Metall.* **61**(S1), S201–S203 (2014).

16. Dhanamjayulu, C. *et al.* Design and implementation of multilevel inverters for fuel cell energy conversion system. *IEEE Access* **8**, 183690–183707 (2020).
17. Majumdar, S., Mahato, B. & Jana, K. C. Implementation of an optimum reduced components multicell multilevel inverter (MC-MLI) for lower standing voltage. *IEEE Trans. Ind. Electron.* **67**(4), 2765–2775 (2019).
18. Liu, J., Wu, J. & Zeng, J. Symmetric/asymmetric hybrid multilevel inverters integrating switched-capacitor techniques. *IEEE J. Emerg. Sel. Top. Power Electron.* **6**(3), 1616–1626 (2018).
19. Mahato, B., Majumdar, S., Vatsyayan, S. & Jana, K. C. A new and generalized structure of MLI topology with half-bridge cell with minimum number of power electronic devices. *IETE Tech. Rev.* **38**(2), 267–278 (2021).
20. Dhanamjayulu, C. & Meikandasivam, S. Implementation and comparison of symmetric and asymmetric multilevel inverters for dynamic loads. *IEEE Access* **6**, 738–746 (2017).
21. Bana, P. R. *et al.* Closed-loop control and performance evaluation of reduced part count multilevel inverter interfacing grid-connected PV system. *IEEE Access* **8**, 75691–75701 (2020).

## Acknowledgements

The publication of this article was funded by the Science, Technology & Innovation Funding Authority (STDF) in cooperation with The Egyptian Knowledge Bank (EKB).

## Author contributions

All authors contributed equally to this all work. All authors reviewed the manuscript.

## Funding

Open access funding provided by The Science, Technology & Innovation Funding Authority (STDF) in cooperation with The Egyptian Knowledge Bank (EKB).

## Competing interests

The authors declare no competing interests.

## Additional information

**Supplementary Information** The online version contains supplementary material available at <https://doi.org/10.1038/s41598-024-65331-7>.

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