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Electrically induced insulator-to-metal transition in InP-based ion-gated transistor

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With the growing awareness of energy savings and consumption for a sustainable ecosystem, the concept of iontronics, that is, controlling electronic devices with ions, has become critically important. Composite devices made of ions and solid materials have been investigated for diverse applications, ranging from energy storage to power generation, memory, biomimetics, and neuromorphic devices. In these studies, three terminal transistor configurations with liquid electrolytes have often been utilized because of their simple device structures and relatively easy fabrication processes. To date, oxide semiconductors and layered materials have mainly been used as active materials. However, inorganic compound semiconductors, which have a long history of basic and applied research, hardly function as channel materials in ion-gated transistors, partly because of the Schottky barrier at the electrode interface. Herein, we show that a typical group III–V compound semiconductor, InP, is available as a high-performance channel for ion-gated transistors with an on/off current ratio of $\approx 10^5$ and a subthreshold swing as small as 93 mV/dec at room temperature. We fabricated AuGe/Ni contact electrodes via annealing to obtain the Ohmic contacts over a wide temperature range. The electrical resistance of InP was drastically decreased by the ionic liquid gating, which led to an electrically induced insulator-to-metal transition. Bulk compound semiconductors are well characterized and have relatively high carrier mobilities; thus, devices combined with electrolytes should prompt the development of iontronics research for novel device functionalities.

Recent progress in iontronics, in which ions play an important role in the device architecture, has attracted significant attention from various research areas^{1–4}. For example, along with conventional Li-ion batteries, all-solid-state batteries are expected to become key devices for achieving sustainable systems for human activities. In addition, in recent studies on unused energy, energy harvesting from waste heat via the ionic thermoelectric effect^{5–9} and from mechanical vibration with polarized ions^{10–13} have been studied as possible small power sources in self-powered systems. Nano scale interfaces between ions and electronic materials are ideal for the exploration of novel device functionalities.

In the study of iontronic devices, ion-gated field-effect transistors (FETs) are recognized as important research platforms^{4,14,15}. This is because the physical and chemical properties of channel materials can be modified by the alignment of ions on the surface, which is controlled by an external voltage. For example, various electronic phase transitions have been realized in functional materials with FET structures^{4,15} by accumulating high-density charge carriers at the solid–liquid interface. Moreover, beyond the typical scheme of electrostatic FETs, ion intercalations^{16–18}, redox reactions¹⁵, and neuromorphic synaptic devices^{19,20} have been demonstrated. On the other hand, however, the available channel materials for ion-gated FET configurations have been limited mostly to oxides, organic semiconductors, and two-dimensional layered materials; thus, expanding the range of these materials is crucial to accelerating the development of basic iontronics research.

One of the target materials for the transistor channels is group III–V compound semiconductors, which have played the central roles in modern high-speed circuits by utilizing modulation-doped FET structures²¹. These compound semiconductors have moderate band gaps ranging from 0.3 eV to 1.5 eV and relatively high electron mobilities, forming sharp hetero interfaces to construct defect-free two-dimensional electron gases²¹.

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As a result, a high-speed switching operation, low energy consumption, and a large on/off ratio of the drain-source current I_D are realized. Thus, the application of bulk compound semiconductors to the channel materials of ion-gated FETs is utmost importance for the pursuit of high-performance iontronic devices.

The fabrication of ion-gated FETs based on III-V semiconductors has been difficult, partly because of the high contact resistance at the interface between the electrodes and channels. This problem is typically encountered when fabricating devices based on insulating materials with low Fermi levels. For example, in the case of oxide insulators such as SrTiO_3 and KTaO_3 , Ar ion bombardment was performed to etch the underlayer of the electrodes^{22,23} and selectively remove oxygen ions. This oxygen deficiency induced thin conductive layers, which resulted in the Ohmic contact at the electrode interfaces^{24–26}. As for the compound semiconductors, it was reported that the contact resistance at room temperature was reduced by employing AuGe/Ni electrodes with high-temperature annealing treatments^{27–31}. This suggests that achieving low contact resistance in ion-gated devices based on III-V semiconductors over a wide temperature range can be done by finding an appropriate annealing condition through a systematic investigation of the annealing process.

In this study, we present the fabrication of ion-gated FETs based on semi-insulating InP and gate control of the electrical transport properties (see the “Methods” for details of the device fabrication process and measurements). A small amount of ionic liquid was applied to the surface of an InP single crystal to form an electric double layer transistor structure, as shown schematically in Fig. 1a. AuGe/Ni electrodes with a thickness of approximately 140/35 nm were deposited by resistance heating and electron beam evaporations and subjected to a high-temperature annealing to obtain a good Ohmic contact. We systematically investigated the annealing time t_A dependences of the transfer curves (the change in I_D as a function of the gate voltage V_G) and of the electrical transport at temperatures as low as 10 K. Finally, it is revealed that metallic transport was induced in the initially insulating InP by an ionic-liquid gating, which provides a further research arena for the development of iontronics using high-carrier-mobility materials.

Results and discussion

Details of the device structure and the concept behind its fabrication are summarized in Fig. 1. Figure 1a schematically shows the device structure of the ion-gated InP, where the ionic liquid between the gate electrode and channel acts as a gate dielectric. When V_G is applied to the gate electrode, electric double layers are formed on the surface of InP and the gate electrode, inducing a strong electric field at the interfaces. The drain and source electrodes were fabricated by depositing AuGe and Ni, respectively, as shown in Fig. 1b. According to previous reports^{27–31}, the contact resistance of n-type InP can be reduced using AuGe/Ni electrodes via additional annealing procedures. Ni in the topmost layer diffuses toward the InP surface through AuGe during annealing. Consequently, an intermediate semiconductor layer, possibly an alloy of Ni and P, is formed to suppress the

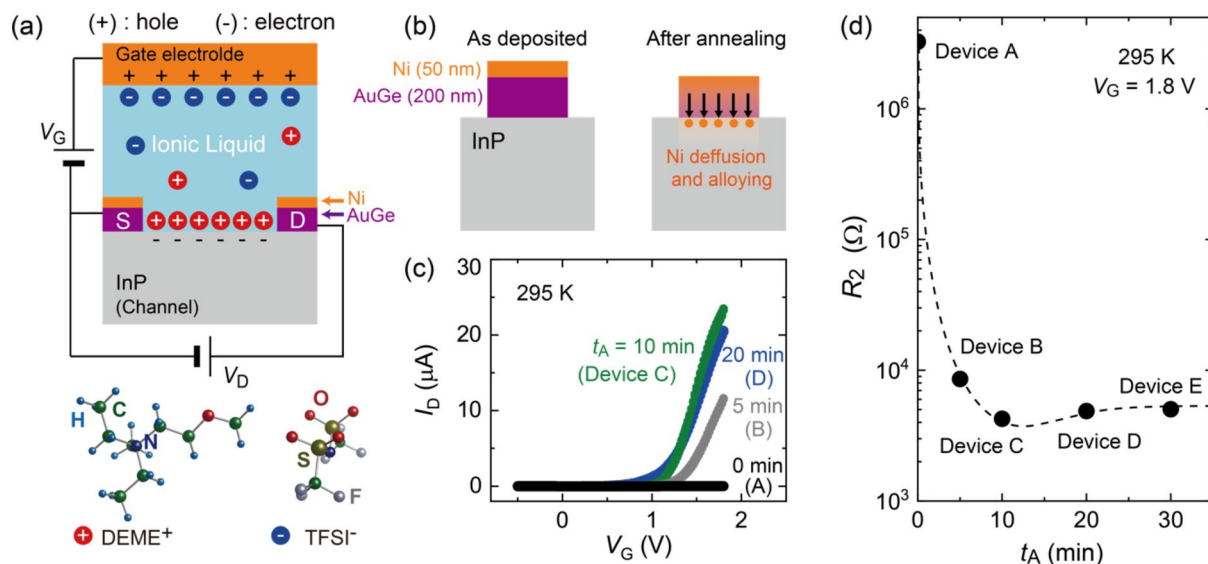


Fig. 1. Structure of ion-gated InP device and annealing effect on contact electrodes. (a) Schematic device structure of ion-gated InP with electric double layers. When a positive gate voltage V_G is applied to the gate electrode, the cations (DEME⁺) and anions (FTFSI⁻) are aligned on the channel and the gate electrode, respectively, to form the electric double layers. Here, S and D represents the source and drain electrodes, respectively. See the “Methods” for details of the device fabrication. (b) Annealing effect on contact electrodes. After annealing, Ni in the topmost layer diffuses toward the InP surface. (c) Typical transfer characteristics (drain-source current I_D versus gate voltage V_G) at 295 K for different annealing times t_A . The annealing temperature was 420 °C for all the measurements. The values of I_D increases with increasing V_G , showing that the electron carriers are doped under positive V_G for annealed devices. The drain voltage V_D was 0.1 V. (d) Two terminal resistance R_2 as a function of t_A . The values of R_2 at 295 K were evaluated as the resistance between the drain and source electrodes.

contact resistance³⁰. Figure 1c shows the transfer characteristics at 295 K for the ion-gated InP devices A ($t_A = 0$ min), B ($t_A = 5$ min), C ($t_A = 10$ min), and D ($t_A = 20$ min). The annealing temperature was set at 420 °C throughout the present study based on the discussions on making an Ohmic contact in previous studies^{27–31}. When t_A was 0 min, I_D did not increase under positive V_G . In contrast, I_D showed an upturn at approximately $V_G = 1.0$ V and increased further with increasing V_G in the annealed devices. Here, both the forward and reverse scans were plotted and mostly overlapped. This shows that the charge carriers were induced in a reversible manner against sweeping V_G . Moreover, the negligible hysteresis suggests that the electrochemical reaction was unlikely. Figure 1d shows the room-temperature values of the two-terminal resistances R_2 of devices A, B, C, D, and E ($t_A = 30$ min) for $V_G = 1.8$ V. The values of R_2 consist of the contact resistance and channel resistance; therefore, a comparison of R_2 can be a good measure for qualitatively evaluating the modulation of the contact resistance. With increasing t_A , R_2 significantly decreased from 3 MW to 4 kW for several minutes of annealing. This strongly suggests that the contact resistance was suppressed owing to the formation of an Ohmic contact at the interface between electrode and InP. Notably, the typical t_A value needed to obtain Ohmic electrodes in InP only ranged from several seconds to minutes in previous reports^{27–30}. These recipes seem reasonable because R_2 at 295 K hardly varied for longer t_A , as shown in Fig. 1d.

At low temperatures, however, R_2 exhibited a drastic contrast. To evaluate the t_A dependence of the contact resistance, we systematically measured R_2 of the ion-gated InP with varying V_G and temperatures. Figure 2 shows the temperature dependence of R_2 at $V_G = 1.8$ V for devices B, C, D, and E. When $t_A = 5$ min, R_2 exhibited insulating behavior, even though the room-temperature value of R_2 was suppressed to the order of 10 kW by gating. When we annealed the device for 10 min, R_2 was measurable down to the lowest temperature of the present experiments, 10 K. For further expansion of t_A , the low-temperature values of R_2 were much more suppressed but did not show a drastic change when t_A was extended from 20 to 30 min. This suggests that the formation of the intermediate semiconductor layer at the electrode interface is almost saturated at around 20 min. See Supplementary Figure S1 for the temperature dependence of R_2 on other V_G values.

The effect of annealing on the electrodes was also confirmed through the analysis with atomic force microscopy (AFM). For the AFM measurements, we prepared four devices: F ($t_A = 0$ min), G ($t_A = 10$ min), H ($t_A = 20$ min), and I ($t_A = 30$ min). Figure 3 shows the development of the surface morphology of the electrodes with increasing t_A . At $t_A = 0$ min, the AFM topography image in Fig. 3a demonstrated a sharp boundary between the electrode and InP. With increasing t_A up to 30 min, we found that the surface and edges of the electrodes became uneven, as shown in Fig. 3b–d. We also investigated the height profile along the red lines in Fig. 3a–d and plotted them in Fig. 3e and Supplementary Fig. S2, where the origin of the x-axis was set at the edge of the electrodes. Figure 3e shows the data only for devices F and H for clarity. The height of the AuGe/Ni electrode was

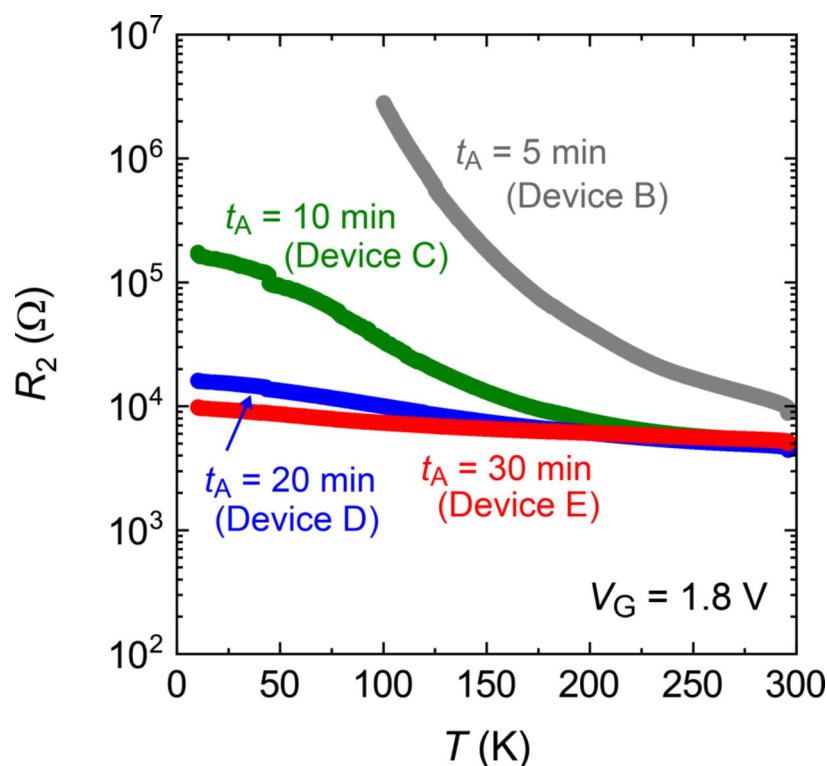


Fig. 2. Comparison of temperature T dependence of two-terminal resistance R_2 for different annealing times t_A . The gate voltage V_G was maintained at 1.8 V for all the devices. With increasing t_A from 5 min for device B to 10 min for device C and 20 min for device D, R_2 at low temperatures decreased. When t_A was further extended to 30 min for device E, the T dependence of R_2 moderately changed, suggesting that the annealing effect was saturated at approximately $t_A = 20$ min.

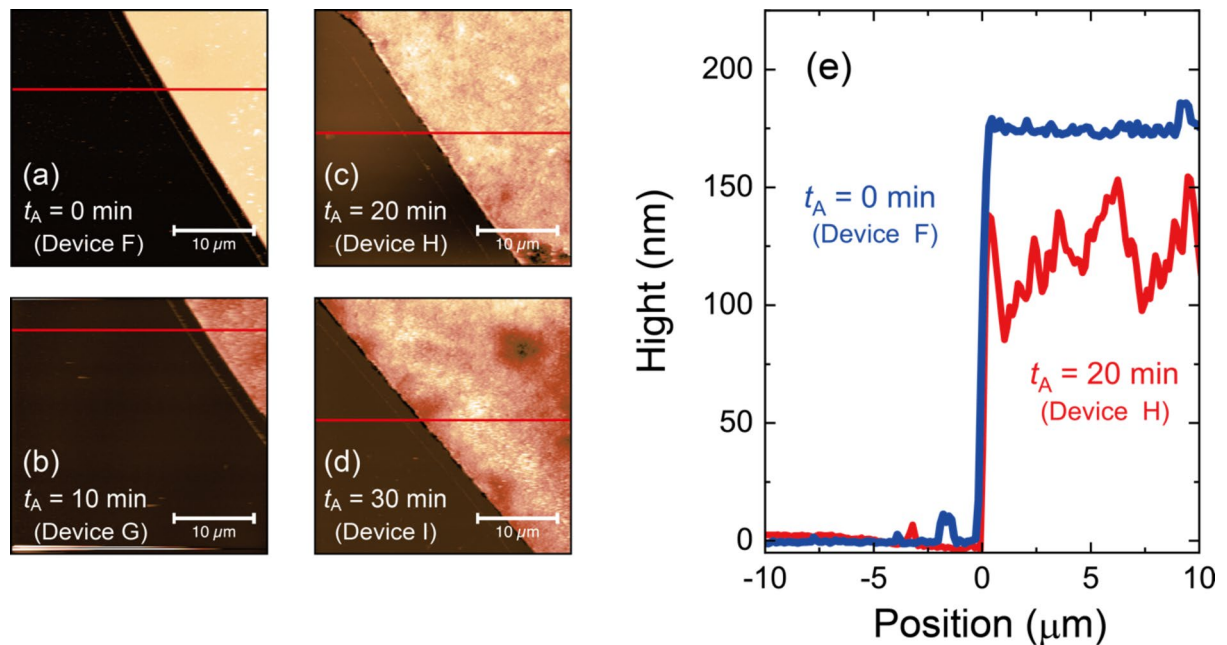


Fig. 3. Atomic force microscopy (AFM) analyses of AuGe/Ni electrodes. (a)–(d) AFM topography image of boundary of InP and AuGe/Ni electrode. The four devices, F, G, H, and I, were prepared with the annealing times of $t_A = 0, 10, 20$, and 30 min, respectively. (e) Height profile along red lines in (a) and (c). The height of the AuGe/Ni electrode remained almost constant in device F with $t_A = 0$ min. The unevenness in the height of AuGe/Ni layers was confirmed in devices H, which was due to the atom migration through the high-temperature annealing process. See Supplementary Figure S2 for the height profiles of other devices.

almost constant in device F with $t_A = 0$ min; in contrast, the heights of the AuGe/Ni layers exhibited unevenness in device H, which was more pronounced for devices with longer t_A (see Supplementary Fig. S2). This indicates that atom migration and the formation of the intermediate semiconductor layer continuously developed with t_A in this time scale. From the results in Figs. 2 and 3, we conclude that at least 20 min of annealing are required to obtain the low contact resistance that is valid for wide temperature regions. This value of t_A is much longer than those in previous studies, where the typical t_A ranged from several seconds to minutes^{27–31}. Although the low temperature electrical transport measurement was enabled, the mechanism for reducing the contact resistance with long annealing time is unclear. Further investigations such as composition and structural analyses of the intermediate semiconductor layer is necessary, which will be conducted using a high energy X-ray beam in a synchrotron radiation facility and reported in a future work.

After determining $t_A = 20$ min at 420°C as an appropriate annealing condition, we fabricated another InP device with $t_A = 20$ min (device J) and systematically investigated the transistor characteristics. Figure 4a shows the transfer curves of device J at 295 K when the drain-source voltage V_D was 0.5 V. A negligibly small hysteresis was observed, where the forward and reverse scans overlapped. The threshold voltage V_{TH} was estimated to be approximately 1.25 V from the slope of the transfer curve, as indicated by the dashed line. As seen in the transfer curve plotted with a log scale, the subthreshold swing was found to be 93 mV/dec at $V_G = 0.7$ V, suggesting a potential for high-performance transistor operation. The ratio of the on- and off-currents was as large as 10^5 , indicating the large tunability of the carrier densities in the InP channel by the gate electric field. The FET properties were also confirmed by observing the output curves, as shown in Fig. 4b. Figure 4c shows the temperature dependence of the sheet channel resistance R_S , which was estimated by normalizing the four-terminal resistance to the length and width of the channel (see Supplementary Fig. S3). The temperature dependence of R_S demonstrated insulating behavior when V_G was less than 1.2 V. With increasing V_G , R_S was suppressed and finally showed a metallic behavior when $V_G = 2.0$ V was applied, achieving an electrically induced insulator-to-metal transition.

The insulator-to-metal transition shown in Fig. 4c is consistent with the transfer curve shown in Fig. 4a. As shown in Fig. 4c, the increase in R_S at low temperatures was suppressed by applying V_G . The values of R_S showed divergence-like temperature dependencies below $V_G = 1.2$ V and shifted to nearly temperature independent behavior above $V_G = 1.2$ V. Meanwhile, in Fig. 4a, V_{TH} was about 1.25 V, above which I_D steeply increased in proportion to V_G . Therefore, the insulator-to-metal transition in ion-gated InP would have occurred at $V_G \approx V_{TH}$. The reason that R_S versus temperature curves showed the insulating behaviors in the subthreshold regime, where V_G is lower than V_{TH} , would be that the carrier density is not sufficient to maintain the electrical conduction at low temperatures^{32–34}. In other words, percolative carrier doping is realized below V_{TH} . It is suggested that the electrically induced carriers can be inhomogeneously doped because of the imperfect ordering of cations and anions^{32,35} and also the Coulomb potential induced by ions near the interface³⁶, which makes mobile carriers localize at low temperatures. When V_G becomes larger than V_{TH} , the chemical potential rises into the conduction

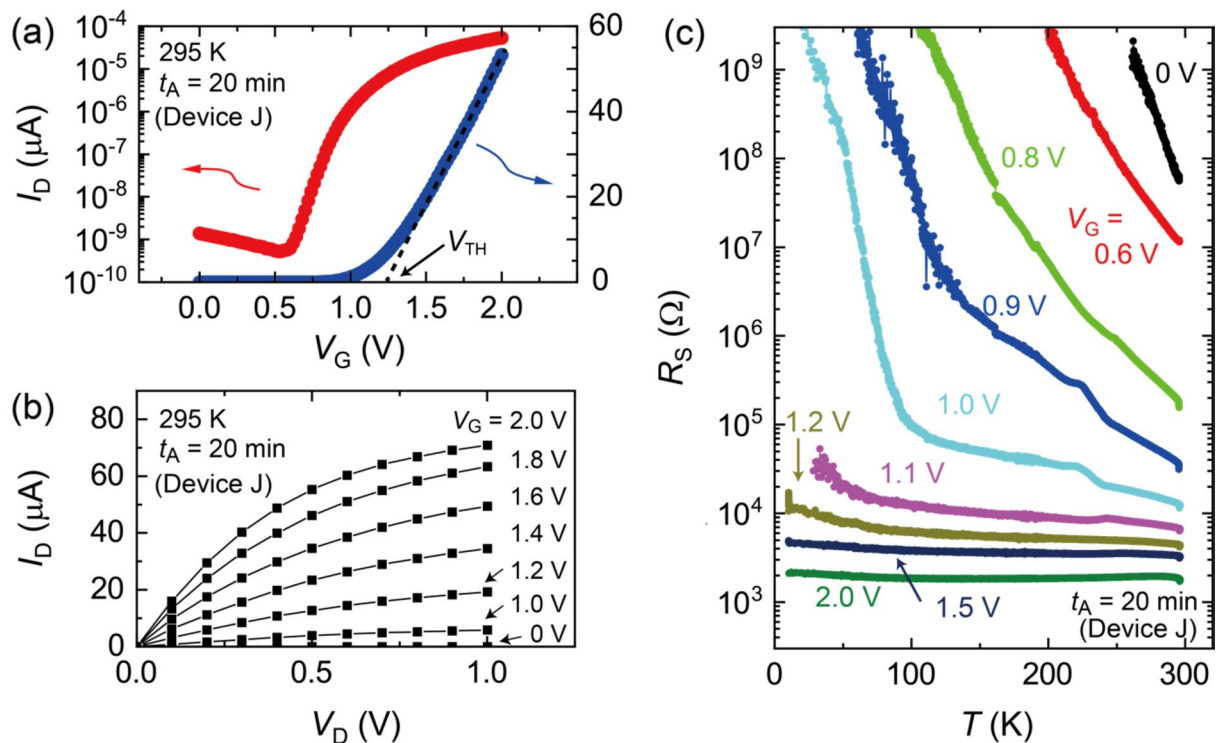


Fig. 4. Insulator-to-metal transition in ion-gated InP. (a) Transfer curve (gate voltage V_G dependence of drain-source current I_D) of device J at 295 K. The annealing time t_A of device J was 20 min. The drain-source voltage V_D was 0.5 V. The threshold voltage V_{TH} was estimated to be approximately 1.25 V from the slope of the curve. (b) Output characteristics (V_D dependence of I_D) at 295 K of device J. A typical n-type field effect transistor operation was observed. (c) Temperature T dependence of sheet resistance R_s of device J. The values of R_s at low temperatures were suppressed with increasing V_G , and an almost flat T dependence was observed when V_G was larger than 1.2 V.

band, and the electrons are accumulated according to the relationship between the sheet carrier density N and V_G , $eN = C_{EDL}(V_G - V_{TH})$. Here, e and C_{EDL} are the elementary charge and the capacitance of the electric double layer, respectively. Therefore, when a typical value of C_{EDL} , $10 \mu\text{F}/\text{cm}^2$ ^{37–41}, is tentatively assumed, N at $V_G = 2 \text{ V}$ is $5 \times 10^{13} \text{ cm}^{-2}$. High-density electrons are induced in the FET channel in this V_G region; thus, the randomness of the carrier distribution is less dominant in the electrical conduction. Consequently, the gated surface electrons exhibited metallic conduction from room temperature to the lowest temperature as shown in Fig. 4c.

Conclusions

We revealed the systematic evolution of the electrical transport properties of ion-gated InP against electrostatic carrier doping. With recent advancements in iontronics, it is highly required to expand the material variety of channels for ion-gated FETs. In particular, the application of III-V compound semiconductors to iontronic devices is promising because of their relatively high carrier mobilities and well characterized material properties. We fabricated the electric double layer transistors based on the semi-insulating InP single crystals. The n-type transistor operations were successfully observed by reducing the contact resistance at the electrode interface with AuGe/Ni Ohmic contacts through the annealing procedure. Ion gating is a versatile technique for carrier doping and continuous modulation of the carrier density at the surface of the InP single crystal, resulting in achieving the electrically-induced insulator-to-metal transition, which has been difficult to realize in ion-gated FETs based on bulk compound semiconductors. The present approach is applicable to other compound semiconductors, which would lead to the emergence of novel electronic properties and the development of the iontronic devices.

Methods

Device fabrication

To control the electron carrier density in InP, an electric double layer transistor structure was fabricated on the (111) surface of Fe-doped semi-insulating InP. An optical image of the device is presented in Supplementary Fig. S3. The single crystals of InP that we used in this study were doped with Fe to increase resistivity. We purchased the single crystals with electrical resistivity larger than $10^7 \Omega\text{cm}$ at room temperature from MO Sangyo Co., Ltd. The electrodes and channels were formed using standard photolithography and a metal evaporation process. We first evaporated the AuGe layer by resistance heating evaporation and then the Ni layer by electron beam evaporation, whose thicknesses were approximately 140 and 35 nm, respectively. To reduce the contact resistance, the devices were annealed after the lift-off process, as discussed in detail in the main

text (see Supplementary Figure S4 for the comment on the contact resistance in Device J). A small amount of an ionic liquid, *N,N*-dimethyl-*N*-(2-methoxyethyl)-*N*-methylammonium bis-(trifluoromethylsulfonyl)-imide (DEME-TFSI), was deposited to cover both the channel and gate electrodes and perform gating experiments with a side gate configuration. When V_G is applied, an electric double layer is formed on the surface of the InP channel. The thickness of the electric double layer is order of 1 nm and works as a nano-gap capacitor in the transistor configuration. It has been reported that the capacitance of the electric double layer is as large as $10 \mu\text{F}/\text{cm}^2$ ^{37–41} or larger. Here, it is noted that the strong electric field induced in the electric double layer can cause an unexpected chemical reaction on the channel surface. That is often accompanied by an irreversible modulation of electrical conductivity in channels. In Figs. 1c and 4a, the transfer curves were shown for both the forward and reverse scans. The reversibility of I_D and the negligible hysteresis suggest that the chemical reaction was unlikely to have occurred.

Electrical measurements

To evaluate the transfer characteristics (the gate voltage V_G dependence of the drain-source current I_D) of the ion-gated InP, I_D was measured under the application of V_G and the drain-source voltage V_D with a semiconductor parameter analyzer (E5270, Agilent). The temperature dependence of the sheet resistance R_s was measured from 295 K to 10 K using a conventional Gifford-McMahon type refrigerator (PASCAL CO., LTD.) and a temperature controller (model 335, Lake Shore Cryotronics). In the ion-gated device structures, I_D can flow through the InP channel and the ionic liquid. See Supplementary Figure S5 for the evaluation of the resistance of the ionic liquid.

Data availability

The authors confirm that the data supporting the findings of this study are available within the article and the supplementary information.

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Author contributions

S.S., H.S., A.O., and K.M. fabricated the devices. S.S. and S.O. developed the measurement system. S.S., H.S., T.H., and S.O. planned the study and performed electrical measurements. The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Declarations

Competing interests

The authors declare no competing interests.

Additional information

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