scientific reports

Check for updates

OPEN

Interleaved quartic high gain DC–DC converter

T. Sakthiram[1], L. Yogesh[1], Rahul Srikanth[1], M. Prabhakar[2]✉ & Kazem Varesi[3]

This research paper presents a high-gain DC–DC converter with ultra-step-up voltage gain capability. The proposed converter is synthesized from a two-phase interleaved boost converter (IBC), and its voltage gain is doubled by adopting a voltage lift capacitor. To enhance its voltage gain capability, a floating capacitor-based gain extension cell is adopted subsequently. This cell yields a voltage gain that is cubed times the output voltage obtained from a classical boost converter (CBC). By cascading the two stages, the voltage gain of the proposed converter is enhanced to quartic times (4th power) that of the CBC. The proposed gain extension concept is validated by conducting practical experiments on a 16 V to 400 V, 150 W prototype version. Practically, the prototype converter delivers 150 W to the load and operates at a full-load efficiency of 92.7% when its switches are operated at safe duty ratio values. Under dynamic conditions, the proposed converter regulates the output voltage to 400 V quickly over a wide range of input voltage and load current variations; the overshoots and undershoots are also negligible. The maximum voltage gain of the proposed converter momentarily increases to 37 when the input voltage is drastically reduced to 10.8 V while the switches are still operated at safe duty ratio values. The voltage stress on the semiconductor devices is only a fraction of the output voltage due to the hybrid voltage gain extension technique. The input current is also ripple-free as the switches in the IBC structure are always operated at a duty ratio of 50%, and only the third switch is controlled to meet the required voltage gain. The salient features of the proposed converter are clearly highlighted by comparing it with several converters that possess quadratic, cubic, and quartic voltage gain functions. The common-ground connection between the source and the load in the proposed converter is an added preferable feature for PV applications.

Keywords DC–DC converters, Power conversion, Power electronics, Microgrids

The escalating energy demands, driven by the proliferation of industrial loads, electric vehicles, data centres, etc., underscore the urgency of transitioning to renewable energy sources (RES) for curbing carbon emissions. Solar energy emerges as a prime candidate, given its widespread availability and perpetual abundance[1]. However, photovoltaic (PV) generation typically operates at low voltage levels (12–60 V), posing challenges when integrating with the standard 380 V DC grid. This integration often necessitates high-gain power electronic converters[2].

High-gain converters (HGCs) are crucial for achieving elevated voltage levels. Classical boost converters (CBCs) face limitations in high-gain applications, prompting the adoption of gain extension techniques like voltage multiplier cells (VMCs). While VMCs offer higher voltage gain and reduced voltage stress on the switch, their effectiveness is constrained by additive voltage amplification, necessitating additional components[3–7]. Furthermore, impulsive charging susceptibility in power switches and diodes compromises the efficiency of VMC-based solutions. These challenges highlight the imperative need to adopt innovative approaches for efficiently integrating the low-voltage PV panels into the high-voltage grids.

Coupled inductors (CIs) are employed within the CBC structure to achieve a high voltage gain ratio, which can be easily extended by adjusting the turns ratio[8–10]. In[8–10], the voltage lift technique is adopted along with complementary switching to achieve twice the voltage gain of CBC with ripple-free input current. Employing a diode capacitor multiplier (DCM) network integrated with CIs and VMCs achieves significant voltage amplification in[11]. However, its scalability is still limited due to the linear gain obtained.

To achieve high voltage amplification while minimizing voltage stress, power circuit topologies combine switched capacitors (SCs) and switched inductors (SIs) with CBC[12,13]. The transition between series and parallel operation in SIs inherently causes pulsating input currents. To further enhance the efficiency of switched

[1]School of Electrical Engineering, Vellore Institute of Technology, Chennai Campus, Vellore, India. [2]Centre for Smart Grid Technologies, Vellore Institute of Technology, Chennai Campus, Vellore, India. [3]Power Electronics Research Laboratory (PERL), Faculty of Electrical Engineering, Sahand University of Technology, Tabriz, Iran. ✉email: prabhakar.m@vit.ac.in

inductor networks, an inductor-capacitor-inductor (LCL) network is employed, extending voltage gain at the expense of LC oscillations[14–16]. Although the converter in[14] achieves an impressive voltage gain amplification of 12.7, it operates at a high duty ratio of 0.67 due to the linear voltage gain profile. Another notable drawback is that most of the power topologies employing SIs often utilize one power switch that experiences high current stress more than the input current. Hence, there is a need for topologies with higher-order voltage amplification.

The converter in[17] utilizes a unique combination of SCs and SIs with dual switches to achieve a higher-than-quadratic voltage gain level at reduced switch stress magnitudes. However, limitations in voltage regulation, relying solely on the number of SC cells, are its main drawbacks.

Quadratic boost converters (QBCs) are combined with existing gain extension techniques such as SCs and SIs to further extend the voltage gain of the SI-based converters[18–20]. By adopting active SI-based topologies, component count is reduced. However, a notable drawback lies in the increased complexity of driving power MOSFETs with a floating ground. In[21], a hybrid quadratic converter is presented. Despite offering a high voltage gain value, the voltage stress on the diodes used in the gain extension cells is higher.

In[22], a converter with a quadratic voltage gain function is described. The converter shares a common ground between the input and the output. The converter described in[23] adopts a hybrid QBC with an embedded SC and VMC to achieve enhanced quadratic voltage amplification. In[24], a modified QBC featuring floating power switches and an energy recycling scheme using SCs is introduced. The innovative scheme enables remarkable voltage amplification while simultaneously reducing the current stress on inductors. Similar approaches that embed QBCs with existing gain extension mechanisms like VMCs or SCs achieve substantial voltage amplification while minimizing the voltage stress are detailed in[25,26].

Generally, CI-based converters, when paired with suitable gain extension techniques, meet the high-voltage gain needs effectively. When CIs are implemented in QBC-based structures, impressive voltage amplification profiles are obtained[27–34]. In such structures, hybrid combinations of gain extension techniques are adopted, viz., CI-SC[28], CI with DCMs[29], QBC with SC[30], and CI-VMC[31], to mainly reduce the voltage stress on the switches. In[32], a QBC equipped with a three-winding CI is introduced. An impressive voltage amplification of 20 at a secured duty ratio of 0.56 is obtained while requiring smaller-sized inductors only. However, addressing factors like size, weight, and leakage inductance is crucial for optimal performance. Additionally, implementing clamping circuitry to mitigate voltage spikes caused by leakage inductance adds to their design complexity. Thus, single-switch higher-order converters, like cubic or quartic boost converters, present alternative solutions.

In[33], a modular single-switch cubic boost converter (SS-C^{3}BC) with modified diode-inductor-capacitor (DLC) voltage-boosting cells is proposed. The converter in[34] adopts the SS-C^{3}BC structure and is cascaded with a VMC to achieve ultra-high voltage gain. The voltage stress on the switch is also reduced due to the adopted structure. The converters in[35,36] employ an energy recycling scheme to reduce the voltage rating of the capacitors besides achieving cubic voltage gain capability.

Intriguingly, the converter presented in[37] introduces a novel single-switch bi-quadratic boost design and employs a switched inductor-capacitor network (SLCN) to attain an excellent voltage gain characteristic; the voltage gain is quartic times (fourth power of) the CBC's voltage gain. Nevertheless, the switch is subjected to an increased voltage stress due to its proximity to the output. Additionally, the input current ripple is also on the higher side. In all the single-switch QBCs presented in[33–37], the power handling capability is constrained as the switch bears a higher current load than the input current. To enhance the power handling capability, higher-order converters often employ multiple-parallel-operated power switches.

Evidently, IBCs operate two CBCs in parallel to reduce the input current stress and ripple. Interleaving multiple QBC structures effectively minimizes the input current ripple. In[38], two QBC structures are interleaved to create an interleaved QBC (IQBC); coupling its two phases with a voltage-lift capacitor yields a remarkable voltage gain of 16.66. Nevertheless, the voltage gain falls short of single-switch converters that employ the same number of components. In[39], cubic voltage gain functionality is achieved by using multiple power switches. Cubic boost converters (C^{3}BC) are created by integrating IBC with QBC structures, enabling cubic voltage gain functionality. Despite using many components, the converter operates at high efficiency values even at elevated voltage conversion ratios, besides drawing smooth current from the input.

In this manuscript, a high gain converter with a quartic voltage conversion ratio profile is presented. The main contributions of this paper are (i) introducing a novel gain extension cell, (ii) synthesizing a floating-capacitor-based converter stage with cubic voltage gain capability, and (iii) synthesizing a converter that possesses quartic voltage gain functionality. This paper is articulated as follows: In "Introduction" section, existing converters are thoroughly reviewed and the proposed converter is introduced. "Power circuit and its operating principle" section describes the power circuit configuration and its operating principle. The design expressions are derived from basic principles and presented in "Voltage conversion and design equations" section. In "Experimental results and discussion" section, the experimental results obtained from a laboratory prototype converter are described along with the inferences. "Benchmarking the proposed converter" section presents a detailed comparison between the proposed converter and other similar converters that are available in the literature. Finally, the concluding remarks are presented, and the manuscript is wrapped up.

Power circuit and its operating principle

Description of the power circuit

Figure 1 portrays the power circuit of the proposed quartic high-gain converter (Q^{4}HGC). The proposed converter is synthesized by cascading two different stages. Stage 1 comprises a two-phase IBC coupled with a voltage lift capacitor C_{Lift}. The output from stage 1 is coupled to stage 2 through the capacitor C_1. Stage 2 is synthesized using discrete inductors L_3, L_4, and L_5, which act as the classical energy storage inductors in boost-derived topologies. They aid in enhancing the voltage gain obtained from their respective previous stages. The negative plates of capacitors C_2 and C_3 are connected to the positive plates of C_1 and C_2 respectively. The series

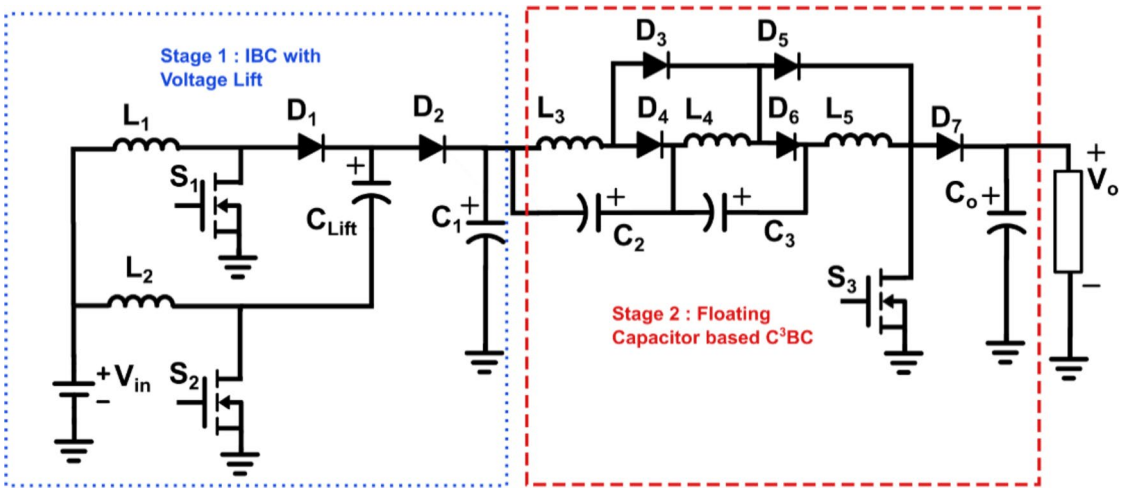

Fig. 1. Power circuit diagram of the proposed quartic high gain converter (Q^4HGC).

combination of capacitors aids in charging the inductors and obtaining higher voltage levels. Thus, the voltage gain developed in stage 2 is split across the intermittent capacitors C_2 and C_3. The discrete inductors, capacitors, and the diodes D_3-D_6, along with the single switch S_3 are carefully synthesized to operate as a floating capacitor cubic cell (F-C^3BC). Diode D_7 acts as a boost rectifier diode in a CBC, and C_0 is the output filter capacitor.

Operating principle

In the proposed Q^4HGC, S_1 and S_2, located in stage 1, are operated with a fixed duty ratio of $\delta_1 = \delta_2 = 0.5$ and with a phase-shift of 180° to obtain a ripple-free input current. The operation of stage 2 is controlled by S_3, and its operation is independent of S_1 and S_2. Nevertheless, the operation of S_3 is synchronized with S_1 for easier control of the proposed Q^4HGC. The following valid assumptions are made to easily understand the operating principle.

(i) All the switching elements are ideal.
(ii) The duty ratio of S_3 is less than that of S_1 (and S_2), i.e., $\delta_3 < \delta_2$.
(iii) The converter draws continuous current from the input, and all the inductors operate in continuous conduction mode (CCM).
(iv) All the inductors are precharged.

Mode 1 ($0 < t < t1$)

This mode commences when S_1 and S_3 are turned ON at $t = t_0$. The discrete inductor L_1 charges linearly through the S_1. Since the switch S_2 is OFF, inductor L_2 discharges and transfers its stored energy to capacitor C_1 through C_{Lift} and D_2. Diode D_1 is reverse-biased as S_1 is conducting. In stage 2, the currents through the inductors L_3, L_4, and L_5 linearly rise through the diodes D_3, D_5, and S_3 respectively. The energy stored in C_1 is transferred to L_3, D_3,D_5, and S_3. The energy stored in L_4 begins to rise linearly towards the potential across the series combination of C_1 and C_2.

Similarly, L_5 is also charged by the effective series combination of C_1, C_2, and C_3. Diodes D_4 and D_6 are reverse-biased as the discrete inductors remain in charging condition. Since D_7 acts like the boost-rectifier diode, it also remains in the reverse-biased state as S_3 is conducting and the output capacitor C_0 supplies the load requirement. Mode 1 ends at $t = t_1$ when the current through L_3, L_4 and L_5, reaches their respective maximum values $I_{L_3,\max}$, $I_{L_4,\max}$, and $I_{L_5,\max}$. The equations governing this mode of operation are given by (1)–(7), while the equivalent circuit during Mode 1 is depicted in Fig. 2(a).

$$i_{L_1} = I_{L_1,\min} + \frac{V_{L_1}}{L_1}t = I_{L_1,\min} + \frac{V_{in}}{L_1}t \tag{1}$$

$$i_{L_2} = I_{L_2,\max} + \frac{V_{L_2}}{L_2}t = I_{L_2,\max} - \frac{(V_{in} + v_{C_{Lift}} - v_{C_1})}{L_2}t \tag{2}$$

$$i_{L_3} = I_{L_3,\min} + \frac{V_{L_3}}{L_3}t = I_{L_3,\min} + \frac{v_{C_1}}{L_3}t \tag{3}$$

$$i_{L_4} = I_{L_4,\min} + \frac{V_{L_4}}{L_4}t = I_{L_4,\min} + \frac{v_{C_1} + v_{C_2}}{L_4}t \tag{4}$$

$$i_{L_5} = I_{L_5,\min} + \frac{V_{L_5}}{L_5}t = I_{L_5,\min} + \frac{v_{C_1} + v_{C_2} + v_{C_3}}{L_5}t \tag{5}$$

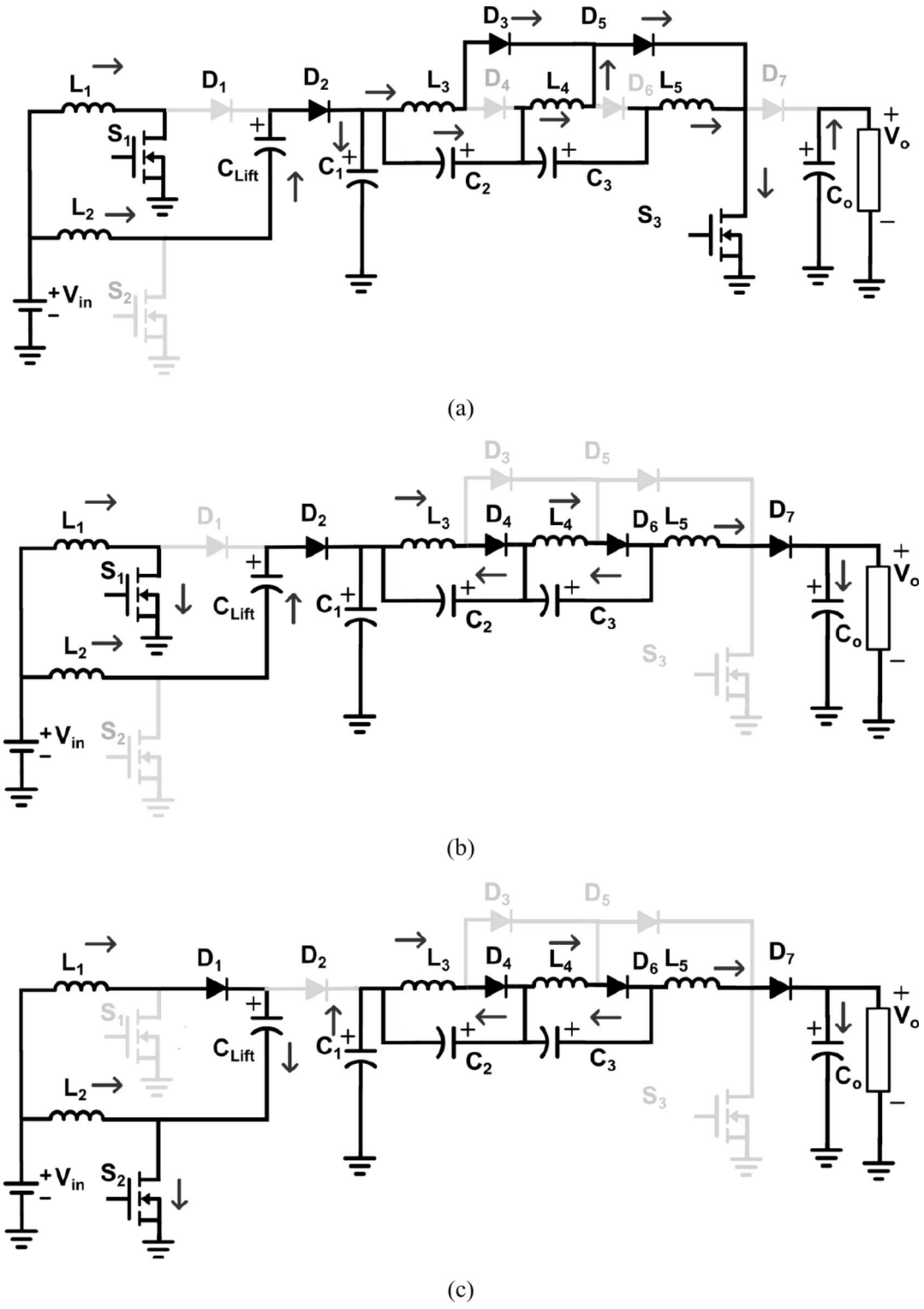

Fig. 2. Equivalent circuit of proposed Q^{4}HGC in (**a**) Mode 1, (**b**) Mode 2, and (**c**) Mode 3.

$$v_{C_x} = V_{C_x,\min} - \frac{i_{C_x}}{C_x} t \ where\, x = 1,2,3,4 \tag{6}$$

$$v_{C_{Lift}} = V_{C_{Lift},\min} + \frac{i_{C_{Lift}}}{C_{Lift}} t \tag{7}$$

Mode 2 (t1 < t < t2)
Mode 2 commences at t = t_1 when S_3 is turned OFF while S_1 continues to remain in the ON state. Inductor L_1 continues to charge through S_1 while L_2 continues to charge C_1. Since S_3 is turned OFF, due to the electrical inertia of L_5, D_7 is forward-biased. Likewise, D_4 and D_6 are also forward-biased due to the electrical inertia of the inductors L_3 and L_4, respectively.

Simultaneously, D_3 and D_5 are reverse-biased. The discrete L_3 and L_4 transfer their stored energy into capacitors C_2 and C_3 through the D_4 and D_6, forming independent loops. The inductor L_5 transfers its stored energy and charges capacitor C_0 through D_7 besides meeting the load requirement. Mode 2 comes to an end at t = t_2 when the currents through L_1 and L_2 attain their respective maximum and minimum values given by $I_{L_1,\max,}$ and $I_{L_2,\min}$. The equations governing stage 1 remain unchanged, while the equations governing stage 2 are given by (8)–(11). The equivalent circuit during Mode 2 is portrayed in Fig. 2(b).

$$i_{L_3} = I_{L_3,\max} - \frac{V_{L_3}}{L_3} t = I_{L_3,\max} - \frac{v_{C_2}}{L_3} t \tag{8}$$

$$i_{L_4} = I_{L_4,\max} - \frac{V_{L_4}}{L_4} t = I_{L_4,\max} - \frac{v_{C_3}}{L_4} t \tag{9}$$

$$i_{L_5} = I_{L_5,\max} - \frac{V_{L_5}}{L_5} t = I_{L_5,\max} - \frac{(V_0 - v_{C_1} - v_{C_2} - v_{C_3})}{L_4} t \tag{10}$$

$$v_{C_x} = V_{C_x,\min} + \frac{i_{C_x}}{C_x} t \ where\, x = 2,3,4 \tag{11}$$

Mode 3 (t_2 < t < T)
Mode 3 operation begins when S_1 is turned ON while S_2 and S_3 continue to be turned OFF. Due to electrical inertia, L_1 forward-biases D_1 and transfers its energy to C_{Lift} while L_2 linearly charges through S_2. In stage 2, diodes D_4, D_6, and D_7 remain forward-biased due to the energy stored in the inductors L_3, L_4, and L_5. Eventually, the inductors L_3, L_4, and L_5 reach their minimum energy levels ($I_{L_3,\min,}$ $I_{L_4,\min,}$ and $I_{L_5,\min}$) while the capacitors C_2, C_3, and C_0 reach their maximum energy level. Simultaneously, current through L_2 reaches its maximum value $I_{L_2,\max}$. Thus, at time t = T, one switching cycle is completed when S_1 and S_3 are turned ON again while S_2 is turned OFF. In Mode 3, the equations governing stage 2 are the same as in (8)–(11). The equations for stage 1 during Mode 3 are given by (12), (13). The equivalent circuit during Mode 3 is shown in Fig. 2(c). The characteristic waveforms of the proposed Q⁴HGC are depicted in Fig. 3.

$$i_{L_1} = I_{L_1,\max} - \frac{V_{L_1}}{L_1} t = I_{L_1,\min} - \frac{(v_{C_{Lift}} - V_{in})}{L_1} t \tag{12}$$

$$i_{L_2} = I_{L_2,\min} + \frac{V_{L_2}}{L_2} t = I_{L_2,\min} + \frac{V_{in}}{L_2} t \tag{13}$$

Voltage conversion and design equations

In this section, the voltage conversion ratio of the proposed Q⁴HGC, the voltage and current stress for the switching elements, and the passive elements are derived.

Voltage conversion ratio

The voltage gain expression of the proposed quartic boost converter is derived by applying voltage-second balance across the inductors. The voltage gain expression is also intuitively understood by considering gain across different stages in the proposed converter.

The first stage consists of IBC with voltage-lift technique that provides twice the voltage gain of a CBC across the capacitor C_1 and is given by (14).

$$M_{Stage1} = \frac{V_{C_1}}{V_{in}} = \frac{2}{(1-\delta_1)} \tag{14}$$

The second stage consists of a floating capacitor-based cubic cell boost converter. The capacitor C_1 acts like a stiff source for this stage. Thus, the cumulative voltage gain is obtained as a product of the voltage amplification obtained across stage 1 and stage 2. However, since the capacitor's negative end is connected to the positive plate of previous stage capacitors, the voltage developed across these intermittent capacitors is found to be reduced by a factor of δ_3. Alternatively, the voltage gain of F-C³BC is also derived by applying volt-second balance across inductors L_3 to L_5 as presented through (15)–(18).

$$V_{L_{3,ON}} + (1-\delta_3)\left(V_{L_{3,OFF}}\right) = \delta_3\left(v_{C_1}\right) + (1-\delta_3)(-v_{C_2}) = 0 \tag{15}$$

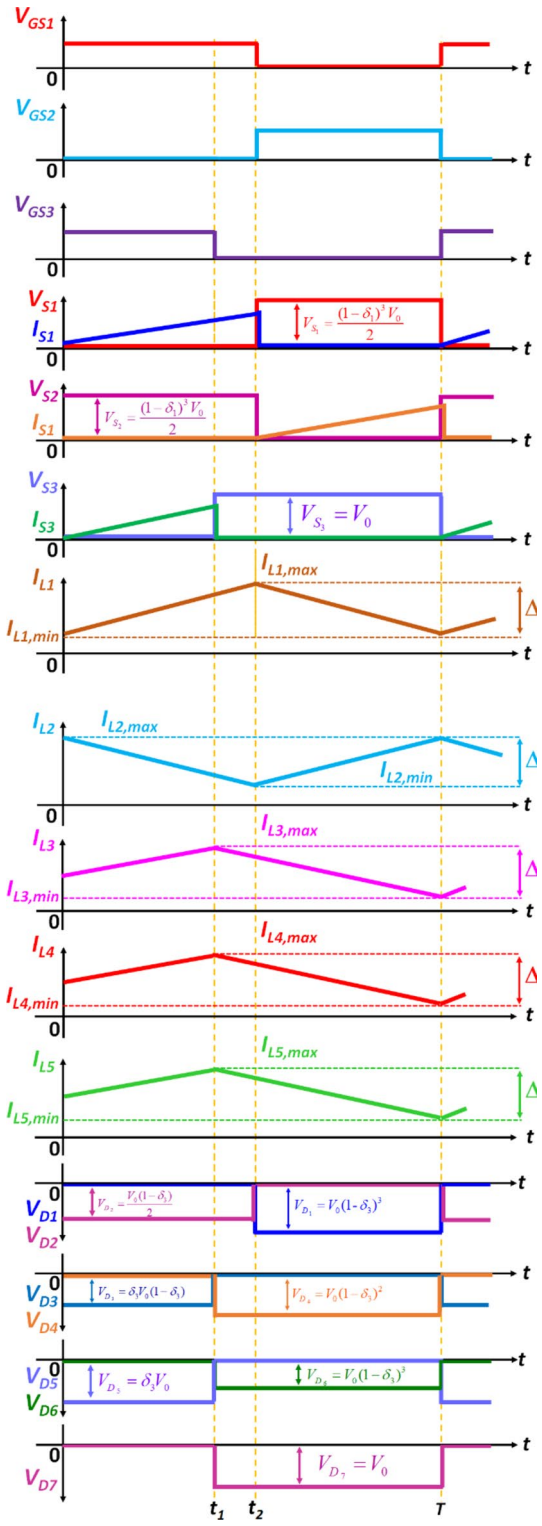

Fig. 3. Characteristic waveforms of the proposed Q^{4}HGC.

$$V_{L_{4,ON}} + (1-\delta_3)\left(V_{L_{4,OFF}}\right) = \delta_3\left(v_{C_1}+v_{C_2}\right) + (1-\delta_3)(-v_{C_3}) = 0 \tag{16}$$

$$V_{L_{5,ON}} + (1-\delta_3)\left(V_{L_{5,OFF}}\right) = \delta_3\left(v_{C_1}+v_{C_2}+v_{C_3}\right) + (1-\delta_3)(v_{C_1}+v_{C_2}+v_{C_3}-V_0) = 0 \tag{17}$$

$$M_{Stage2} = \frac{V_o}{v_{C_1}} = \frac{1}{(1-\delta_2)^3} \tag{18}$$

From the voltage gain contributed by the two stages, the overall voltage gain of the Q^{4}HGC is obtained and presented in (19).

$$M = M_{Stage1} * M_{Stage2} = \frac{V_o}{V_{in}} = \frac{2}{(1-\delta_1)(1-\delta_3)^3} \tag{19}$$

When the duty ratio (δ) of both the stages is equal, i.e., $\delta_1 = \delta_2 = \delta_3 = \delta$, the effective voltage gain is the 4th power of (quartic times) the voltage gain obtained from a CBC structure. Since the operation of S_3 is independent of S_1 and S_2, the proposed converter possesses two degrees of freedom, viz., its ability to provide the desired voltage amplification while drawing ripple-free current from the source. For instance, S_1 and S_2 are operated at a fixed duty ratio of 0.5 with a phase shift of 180° to eliminate the input current ripple while δ_3 is adjusted to obtain the required voltage gain. Thus, the proposed converter is well-suited for PV applications as its duty ratio values are safe and the input current is also free from ripples. Figure 4 exhibits the voltage gain capability of the proposed Q^{4}HGC along with its practical operating point.

Switch ratings

In the proposed converter, since S_1 and S_2 are part of the IBC structure, they experience the same voltage stress as that of the CBC and is given by (20).

$$V_{S_1} = V_{S_2} = \frac{V_{in}}{(1-\delta_1)} = \frac{(1-\delta_1)^3 V_0}{2} \tag{20}$$

The current stress of S_1 is determined when it is conducting (during mode 1 or mode 2). As L_1 charges through S_1 and the input current is shared by the two interleaved phases, the current stress of S_1 is given by (21).

$$I_{S_1} = I_{L_1} = \frac{I_{in}}{2} \tag{21}$$

When S_2 is turned ON, L_1 transfers its energy to C_{Lift} through S_2 while L_2 also charges through S_2. Hence, its current stress is relatively higher than that of S_1, and itd is given by (22).

$$I_{S_2} = I_{L_1} + I_{L_2} = I_{in} \tag{22}$$

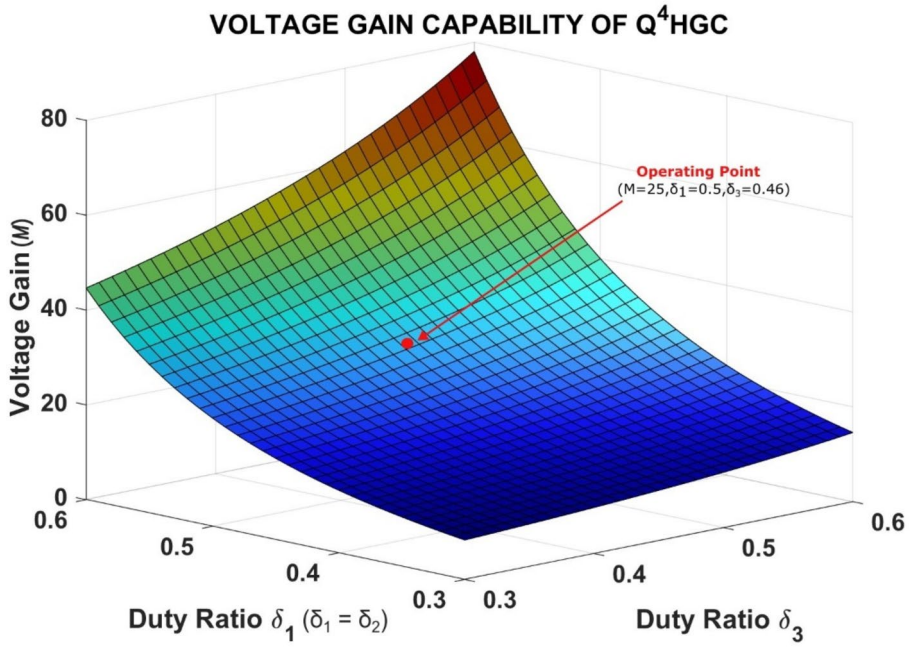

Fig. 4. 3D plot showing the voltage gain capability of Q^{4}HGC and its operating point.

Since S_3 is located near the output port, its voltage stress is the same as V_0. When S_3 is ON, inductors L_3, L_4, and L_5 charge through S_3. Hence, its current stress is given by the sum of current through inductors L_3, L_4, and L_5 as expressed in (23).

$$I_{S_3} = I_{L_3} + I_{L_4} + I_{L_5} = I_{in}\frac{(1-\delta_1)((2-\delta_2)+(1-\delta_2)^2)}{2} \tag{23}$$

Ratings of diodes

The diodes experience voltage stress when operating in reverse-biased conditions. Their voltage stress magnitudes are quantified as the potential difference across their anode and cathode terminals. D_1 is reverse-biased during mode 1; its anode is clamped to the ground by S_1, and its cathode is connected to C_1. Hence, its voltage stress is given by (24). Similarly, D_2 is reverse-biased when S_2 is turned ON during mode 3. Its anode and cathode terminals are connected to C_{Lift} and C_1 respectively. Therefore, it experiences a voltage stress that is given by (25).

$$V_{D_1} = v_{C_1} = \frac{2V_{in}}{(1-\delta_1)} = V_0(1-\delta_3)^3 \tag{24}$$

$$V_{D_2} = v_{C_1} - v_{C_{Lift}} = \frac{V_0(1-\delta_3)}{2} \tag{25}$$

Diodes D_1 and D_2 carry the currents that flow through L_1 and L_2, respectively. Hence, their current stress level is given by (26).

$$I_{D_1} = I_{L_1}, I_{D_2} = I_{L_2} = \frac{I_{in}}{2} \tag{26}$$

Diodes D_3 and D_5 are reverse-biased during modes 2 and 3. The anode and cathode terminals of D_3 are connected to C_2 and C_3, respectively. Hence its voltage stress is given by (27). In the case of D_5, its cathode terminal is clamped at V_0, and its anode is at a relatively lower potential level of C_3; its voltage rating is given by (28).

$$V_{D_3} = v_{c_3} = \frac{2\delta_3 V_{in}}{(1-\delta_1)(1-\delta_3)^2} = \delta_3 V_0(1-\delta_3) \tag{27}$$

$$V_{D_5} = V_0 - v_{c_1} - v_{c_2} - v_{c_3} = \frac{2\delta_3 V_{in}}{(1-\delta_1)(1-\delta_3)^3} = \delta_3 V_0 \tag{28}$$

During mode 1, the diodes D_3 and D_5 are forward-biased and carry the currents that flow through L_3 and L_4, respectively. Therefore, their current stress is given by (29) and (30).

$$I_{D_3} = I_{L_3} = \frac{(1-\delta_1)I_{in}}{2} \tag{29}$$

$$I_{D_5} = I_{L_4} = \frac{(1-\delta_1)(1-\delta_3)I_{in}}{2} \tag{30}$$

During mode 1, diodes D_4 and D_6 are under reverse-biased conditions. Consequently, the anode of D_4 is grounded as switch S_3 conducts. Hence, its voltage stress is given by determining the voltage developed across C_3 with respect to ground and expressed using (31). Similarly, D_6 experiences a voltage stress value that is equal to the sum of potentials developed across the capacitors C_1, C_2, and C_3 as expressed in (32).

$$V_{D_4} = v_{c_2} + v_{c_1} = \frac{2V_{in}}{(1-\delta_1)(1-\delta_3)} = V_0(1-\delta_3)^2 \tag{31}$$

$$V_{D_6} = v_{c_1} + v_{c_2} + v_{c_3} = \frac{2V_{in}}{(1-\delta_1)(1-\delta_3)^2} = V_0(1-\delta_3)^3 \tag{32}$$

The diodes D_4 and D_6 operate in mode 2 or 3 when S_3 is turned OFF and carry the current through L_3 and L_4, respectively. Therefore, their current stress is expressed by (33) and (34). Since D_7 is located close to the output port, its voltage stress is equal to V_0, and it carries current through inductor L_4.

$$I_{D_4} = I_{L_3} = \frac{(1-\delta_1)I_{in}}{2} \tag{33}$$

$$I_{D_6} = I_{L_4} = \frac{(1-\delta_1)(1-\delta_3)I_{in}}{2} \tag{34}$$

Design of magnetics

The optimal characteristics of the magnetic elements play a crucial role in ensuring the effective operation of the power converter. The inductor values in boost-derived converters are derived based on the duty ratio (δ), voltage

across the individual inductors, operating frequency, and the individual current ripple values. The generalized equation to arrive at the inductor value is given by (35).

$$L_x = \frac{\delta_i \, V_{L_x,ON}}{f_s \Delta i_{L_x}}, \; i{=}1 \text{ to } 3, \; x = 1 \text{ to } 5 \tag{35}$$

where δ is the duty ratio of the switch, $V_{L_x,ON}$ is the voltage across the individual inductor, Δi_{L_x} is the individual inductor current ripple, and f_s is the switching frequency.

For CCM operation, the actual value of the inductors must be more than the critical inductance ($L_{critical}$) value that is expressed using (35a).

$$L_{x-critical} = \frac{\delta R_0}{2 f_s M^2}, \; x = 1 \text{ to } 5 \tag{35a}$$

where R_0 is the load resistance value.

In the proposed converter, L_1 and L_2 operate under identical conditions. Hence, their value is determined using (36) and (37).

$$L_1 = \frac{\delta_1 \, V_{in}}{f_s \Delta i_{L_1}} \tag{36}$$

$$L_2 = \frac{\delta_2 \, V_{in}}{f_s \Delta i_{L_2}} \tag{37}$$

Inductor L_3 is charged by the capacitor C_1 when S_3 is ON. Therefore, the value of L_3 is determined using (38).

$$L_3 = \frac{\delta_3 \, v_{c_1}}{f_s \Delta i_{L_3}} = \frac{2\delta_3 V_{in}}{f_s \Delta i_{L_3}(1-\delta_1)} \tag{38}$$

The voltage impressed across L_4 and L_5 is considerably higher since they are charged by the series combination of the previous stage capacitors. Hence, their values are obtained using the design expressions presented in (39) and (40).

$$L_4 = \frac{\delta_3 \, (v_{c_1} + v_{c_2})}{f_s \Delta i_{L_4}} = \frac{2\delta_3 V_{in}}{f_s \Delta i_{L_4}(1-\delta_1)(1-\delta_3)} \tag{39}$$

$$L_5 = \frac{\delta_3 \, (v_{c_1} + v_{c_2} + v_{c_3})}{f_s \Delta i_{L_5}} = \frac{2\delta_3 V_{in}}{f_s \Delta i_{L_5}(1-\delta_1)(1-\delta_3)^2} \tag{40}$$

Determination of capacitance values

The capacitance values are determined based on the ripple voltage impressed across the individual capacitors and the current that passes through them. The capacitance value of C_1 and C_2, which is in stage 1, is given by (41).

$$C_{1,2} = \frac{\delta_{1,2} I_{in}}{f_s \Delta v_{C_{1,2}}} \tag{41}$$

In the proposed Q^{4}HGC, capacitors in stage 1 have higher capacitance values as they carry higher currents. The capacitors in stage 2 carry lower currents due to the voltage gain.

Their capacitance values are obtained from the expression given by (42).

$$C_k = \frac{\delta_3 I_{C_k}}{f_s \Delta v_{C_k}}, \; k = 3, 4, 5 \tag{42}$$

Experimental results and discussion

To validate the proposed voltage gain hypothesis, a laboratory prototype model of the Q^{4}HGC is fabricated with the specifications mentioned in Table 1. The components listed in Table 2 are used to construct the prototype converter. An Arm Cortex®-M4-based processor STM32F411RE Nucleo-64 microcontroller is used to generate the gating signal and implement the closed-loop control algorithm. The gate pulses generated from the microcontroller are applied to IR25600 dual low-side MOSFET drivers. The amplified pulses are applied to the gate terminal of the power switches. The key waveforms obtained from the prototype converter are captured using a mixed-domain oscilloscope (MDO4014C) along with differential high-voltage and current probes. Figure 5(a) depicts the photograph of the prototype Q^{4}HGC. The experimental setup that is used to obtain the test results is portrayed in Fig. 5(b).

Figure 6 depicts the voltage gain capability of the proposed Q^{4}HGC. The gating pulses are applied to S_1 and S_2 (CH2 and CH3) at a duty ratio of 0.5 with a 180° phase-shift. CH1 depicts the input voltage (16 V), and the voltage developed across the output is shown in CH4. Obviously, 400 V is obtained across the output terminals when the input is 16 V. Thus, the proposed voltage gain concept is validated; the practical voltage gain value is 25.

Parameter	Value
Input voltage (V_{in})	16 V
Switching frequency (f_s)	100 kHz
Duty ratio of S_1, S_2 (δ_1)	0.5
Output voltage (V_0)	400 V
Duty ratio of S_3 (δ_3)	0.46
Output power (P_0)	150 W

Table 1. Specifications of the proposed converter.

Circuit element	Device type	Part number (specifications)
Switch (S_1, S_2)	MOSFET	IRFB4410Z (100 V, 88 A, 8 mΩ)
Switch (S_3)	MOSFET	NTHL041N60S5H (600 V, 57 A, 33 mΩ)
Diodes (D_2,D_1)	Fast recovery diode	DSS 16–01 A (100 V, 16 A, 0.64 V)
Diodes (D_2,D_4, D_5,D_6)	Fast recovery diode	MUR1540 (400 V,15 A, 1.05 V)
Diode (D_3)	Fast recovery diode	MUR1520 (200 V, 15 A, 0.85 V)
Diode (D_7)	Fast recovery diode	BYV29X-600 (600 V, 9 A, 1.26 V)
Inductors (L_1, L_2, L_3)	Ferrite core	PCV2-104–10 L (100 µH, 10 A)
Inductor (L_4)	Ferrite core	PCV2-564–6 L (564 µH, 6 A)
Inductor (L_5)	Ferrite core	PCV2-105–02 L (1 mH, 2 A)
Capacitors (C_{lift}, C_2, C_3,C_4)	Polypropylene	Film Capacitor (3.3 µF, 250 V)
Capacitor (C_0)	Electrolytic	B43644J65 66M067 (56 µF, 500 V)
Capacitor (C_1)	Electrolytic	EKMG101ELL101MJ20S (100 µF, 100 V)

Table 2. Components used to fabricate and test the prototype Q^{4}HGC.

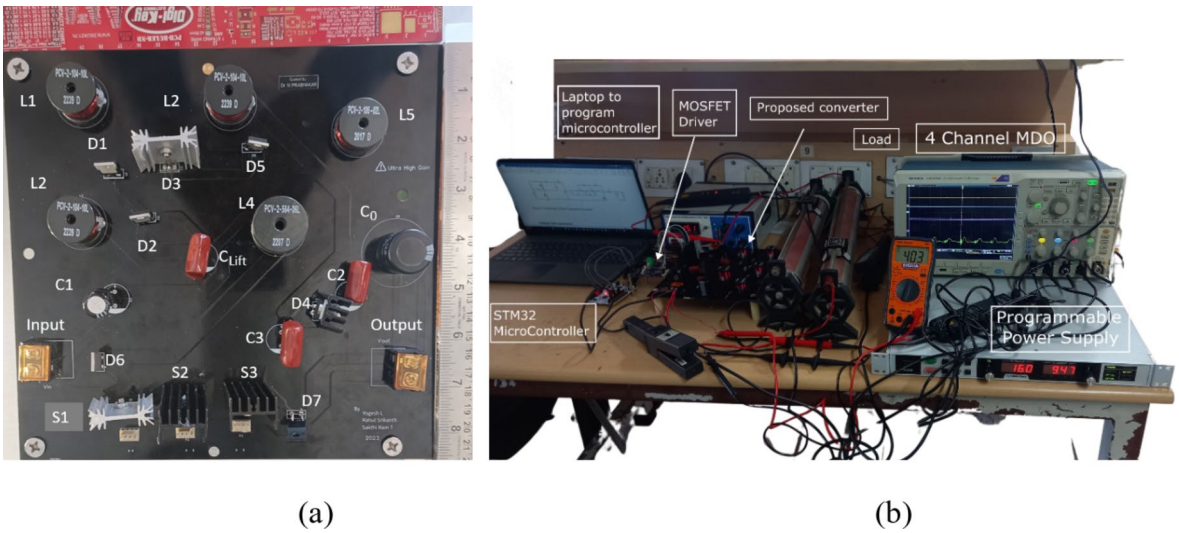

Fig. 5. Photograph showing (**a**) the top-view of the prototype Q^{4}HGC, and (**b**) the experimental setup used to capture the results.

Figure 7 validates the proper operation of the switches and their voltage stress levels with respect to the output voltage. CH1 and CH2 show the voltage across switch S_1 and S_2, respectively. Their complementary operation is verified from these oscillograms. S_1 and S_2 share similar voltage stress due to their complementary operation. Additionally, since they are employed in stage 1, their voltage stress is practically 32 V, which is only 8% of V_0.

The practical value matches with the analytical value. Since the voltage stress on the two switches is very low, MOSFETs with very low R_{DS-ON} are employed to lower the conduction losses. The operation of S_3 is synchronized with S_1. The switch S_3 is operated at a slightly lower duty ratio of 0.46 and is adjusted to achieve the required voltage gain at nominal load conditions. Since S_3 is located closer to the output port, its voltage stress is V_0 as depicted in CH3. However, since the current stress on S_3 is reduced, its loss is reduced.

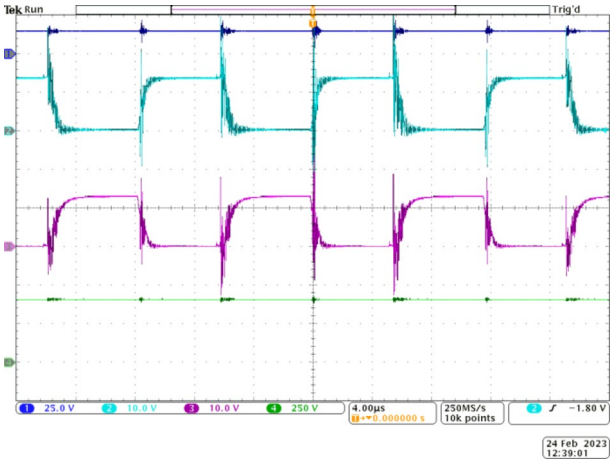

Fig. 6. Experimental results to demonstrate the voltage gain capability of the proposed Q^{4}HGC. CH1—input voltage, CH2—gate pulse to S_1, CH3—gate pulse to S_2, and CH4—output voltage.

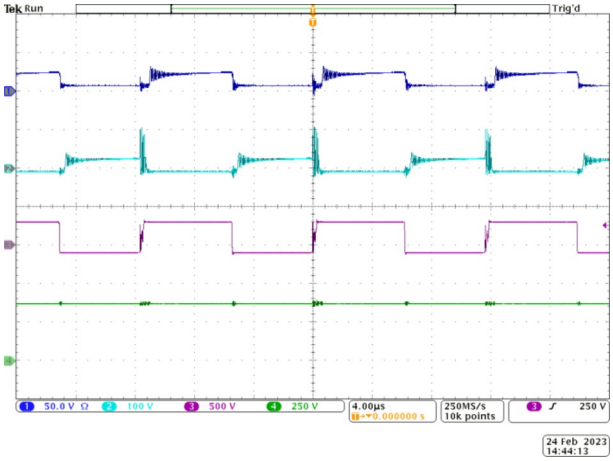

Fig. 7. Experimental waveforms to validate the voltage stress across the switches of the proposed Q^{4}HGC. CH1, CH2, CH3 –voltage across S_1, S_2, and S_3 respectively, CH4—output voltage.

Figure 8 demonstrates the complementary operation of S_1 and D_1 through the waveforms portrayed in CH1 and CH2. Similarly, CH3 and CH4 validate the complementary working S_2 and D_2 as per the operating principle. Further, diode D_1 experiences a voltage stress of around 64 V (16% of V_0) as observed from CH2. The value matches with the theoretically calculated counterpart. From the CH4 waveform, D_2 experiences a voltage stress of about 32 V, which is the same as that of S_1 and S_2. Therefore, all switching elements in stage 1, except D_1, experience a very low voltage stress of 32 V, which is just 8% of V_0, while the voltage stress on D_1 is 16% of V_0. Once again, the lower voltage stress on the diodes employed in stage 1 permits the choice of diodes with lower voltage drops to enhance the efficiency.

Figure 9 demonstrates the operation of stage 2. The voltage stress across the diodes D_1, D_4, D_5, and D_6 is depicted through the waveforms in CH1 to CH4, respectively. Diode D_5 is expected to operate when S_3 is ON. Hence, D_5 and S_3 operate symmetrically and is verified from CH3 and CH4. Diode D_5 experiences a higher voltage stress of 185 V as its cathode terminal is clamped to V_0 when S_3 is OFF. Diodes D_4 and D_6 operate complementary to D_3 and D_5 respectively. Diode D_4 experiences a voltage stress of 121 V, which accounts for only 30% of V_0 while D_6 is subjected to a higher voltage stress of 221 V, which is in accordance with the theoretical calculations. Except for D_6 and D_7, the voltage stress on the remaining diodes used in the floating capacitor cell is well below 50% of V_0. Thus, the choice of an appropriate gain extension mechanism is validated.

The correlated operation of S_3 and D_7 is verified through the experimental waveforms presented in Fig. 10. Switch S_3 is operated at a very low duty ratio of 0.46 as observed from CH1. The voltage stress across S_3 is portrayed through CH2, and the value is as expected. Since S_3 is located closer to the output terminals, its voltage stress is the same as V_0. The complementary operation of D_7 with respect to S_3 is also demonstrated by correlating the waveforms presented in CH2 and CH3. Diode D_7 is also subjected to a voltage stress that is equal to V_0 based on its location. However, the switching and conduction losses across S_3 and D_7 are significantly reduced due to their lower current stress levels.

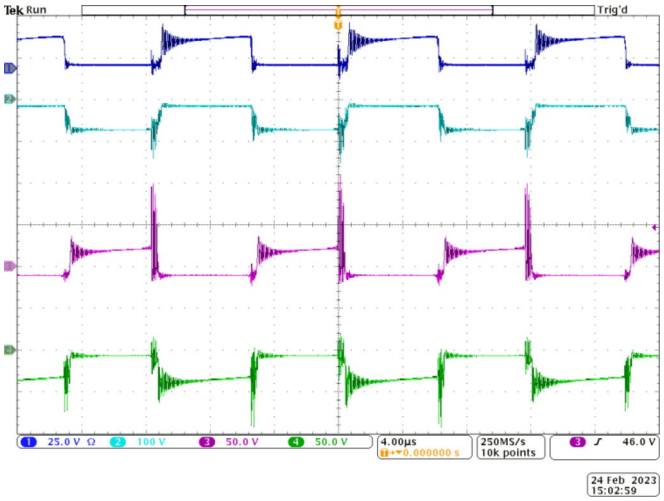

Fig. 8. Experimental waveforms to demonstrate the operation of IBC stage, CH1—voltage across S_1, CH2—voltage across D_1, CH3—voltage across S_2, and CH4—voltage across D_2.

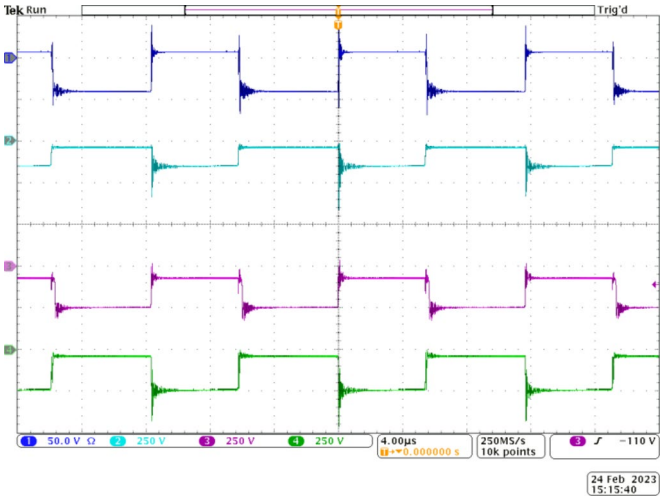

Fig. 9. Experimental waveforms to demonstrate the working of stage 2. CH1—voltage across D_1, CH2—voltage across D_4, CH3—voltage across D_5, and CH4—voltage across D_6.

Figure 11 depicts the efficiency of the proposed converter under full-load conditions. From the waveforms, the converter delivers 150 W to the load at an output voltage of 400 V. The input current is smooth and almost ripple-free due to the interleaving mechanism employed in stage 1.

The magnitude of the input current is computed to be 10.11 A when 16 V is applied. Thus, the prototype converter operates at an impressive efficiency of 92.7% under full-load conditions. The efficiency plot of the proposed Q^{4}HGC at different load conditions is portrayed in Fig. 12. The practical values match closely with the simulated values; the minor variation in simulation is due to the stray losses associated with the passive elements.

The non-ideal elements of the power circuit are (i) the stray resistance of the inductors, (ii) ON-state resistance of the switches, (iii) the ON-state resistance of the diodes, and (iv) the ON-state voltage drop of the diodes. Figure 13(a) shows the equivalent circuit of the proposed power converter with all the non-ideal elements. The power loss dissipated across the various components of the proposed converter is categorized as (i) loss across the switch, (ii) loss across the diodes, and (iii) loss across the inductors[9,10,39]. Based on the equations presented in (43)-(47), the power loss distribution of the proposed converter at full-load condition is obtained and plotted in Fig. 13(b). Most of the losses occur across the diodes.

$$P_{\mathrm{sw,loss}} = I^2{}_{\mathrm{sw,RMS}} \times R_{\mathrm{sw,ON}} + P_{\mathrm{sw,ON}} + P_{\mathrm{sw,OFF}} \tag{43}$$

$$I_{\mathrm{sw,RMS}} = \sqrt{\frac{D}{3}} I_{\mathrm{sw}} \tag{44}$$

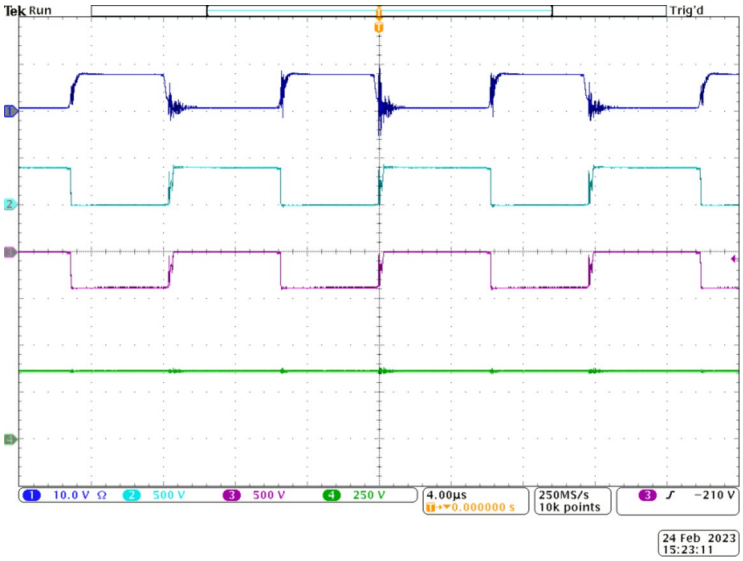

Fig. 10. Experimental waveforms to demonstrate the operation of S_3 and D_7. CH1—gate pulses to S_3, CH2—voltage stress on S_3, CH3—voltage stress on D_7, and CH4—V_0.

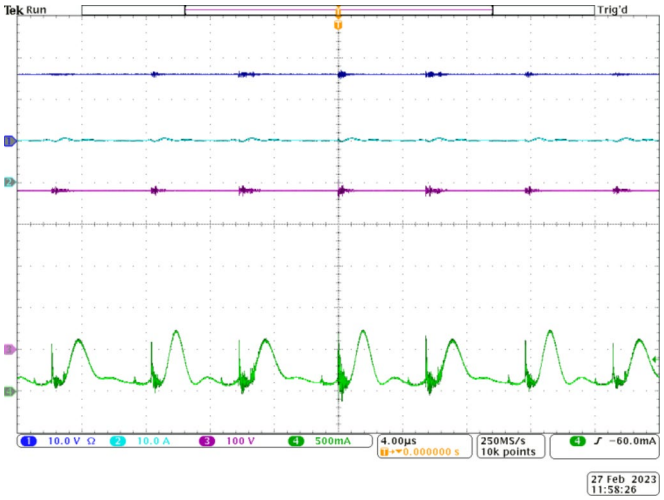

Fig. 11. Experimental waveforms to demonstrate the efficiency of the proposed Q^{4}HGC at full-load condition. CH1—V_{in}, CH2—input current, CH3—V_0, and CH4—load current.

$$P_{diode\_loss} = \left(V_{diode\_ON} \times I_{diode}\right) + \left(I_{diode}^2 \times R_{diode\_ON}\right) \tag{45}$$

$$I_{\text{diode,RMS}} = \sqrt{\frac{D}{3}} I_{diode} \tag{46}$$

$$P_{inductor\_loss} = I^2{}_{inductor} R_{inductor} + P_{iron} \tag{47}$$

The dynamic performance of the proposed converter is examined by implementing a simple closed-loop control technique. A potential divider-based network is adopted to reduce the actual output voltage to a safer level (i.e., < 3.3 V) and fed as input to the analog-to-digital converter (ADC) peripheral of the microcontroller. The output of the ADC is infested with noises and is filtered by implementing an appropriate software-based filter. The filtered-ADC output is used to obtain the error signal by comparing it with the reference voltage. The error signal is then fed to a discrete-time proportional controller with lower and upper saturation values on duty ratio to protect the switches. The controller is suitably tuned to provide a very quick response with minimal overshoot. Figure 14 depicts the schematic block diagram of the closed-loop control technique that is employed.

Figure 15 demonstrates the line regulation characteristics of the prototype converter. Under nominal conditions, the Q^{4}HGC delivers 150 W to the load at 400 V. The duty ratio of S_3 is adjusted by using closed-loop

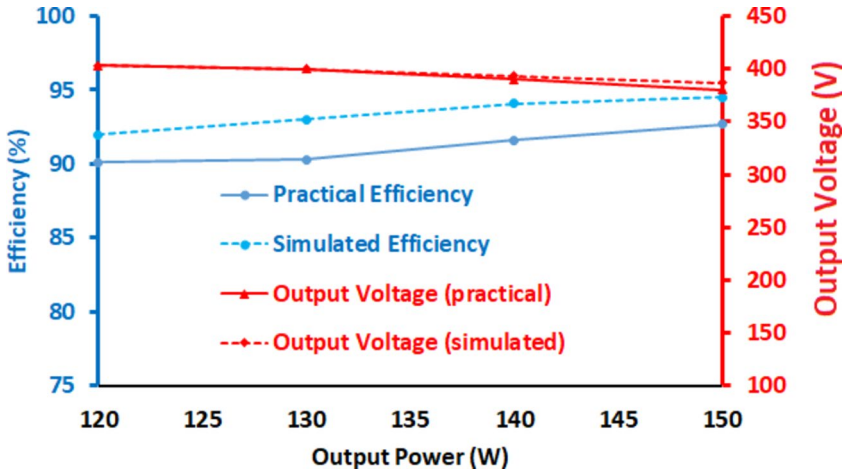

Fig. 12. Efficiency curve at various load conditions during simulation and experimentation.

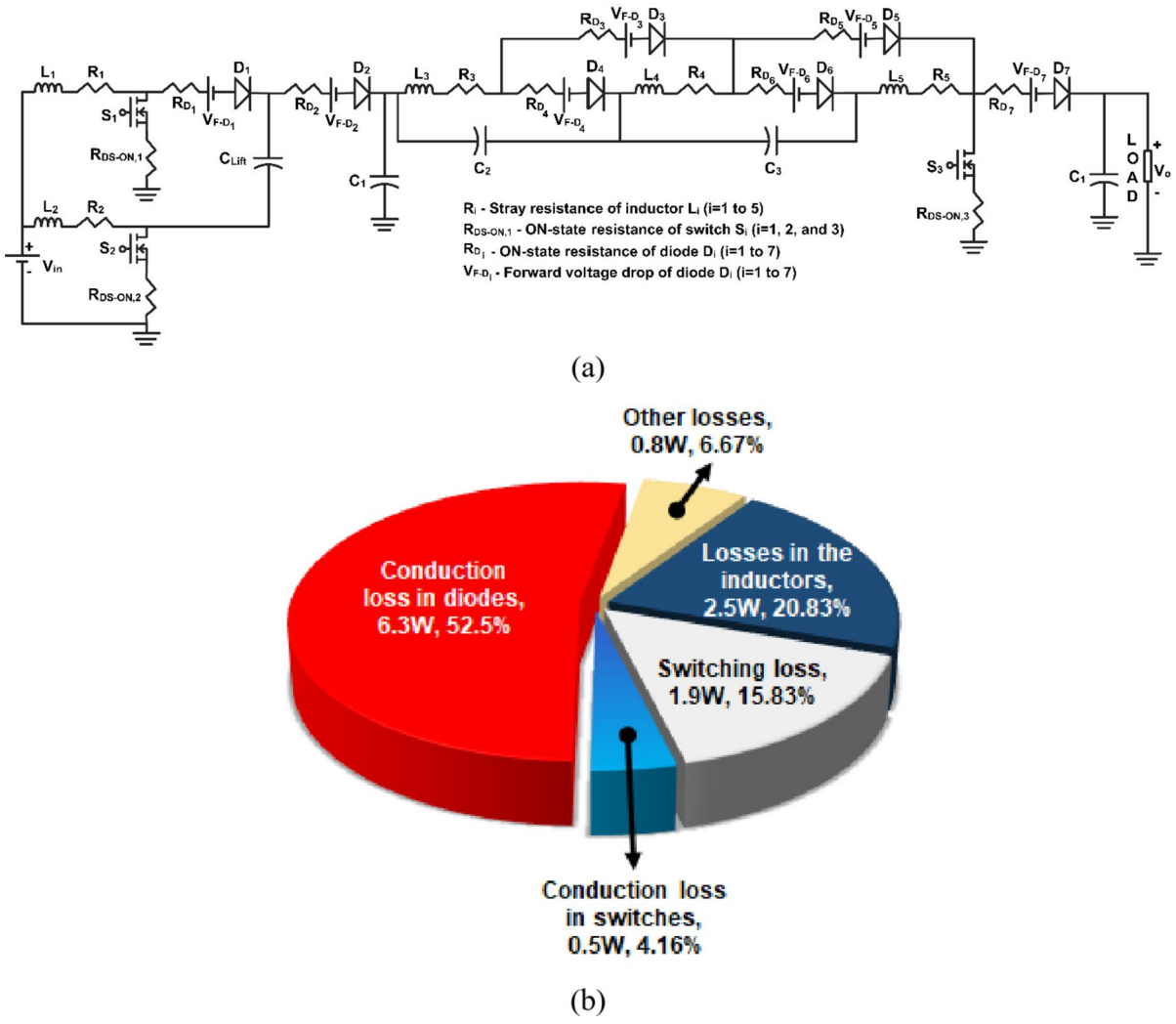

Fig. 13. Diagrams depicting the (**a**) equivalent circuit with non-ideal elements and (**b**) loss distribution profile of the Q^4HGC under full-load condition.

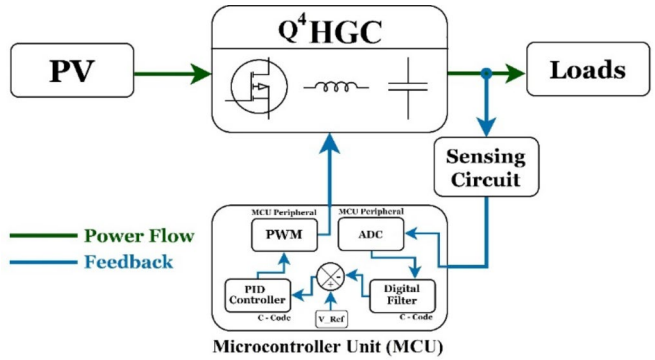

Fig. 14. Block diagram of the closed-loop control implementation.

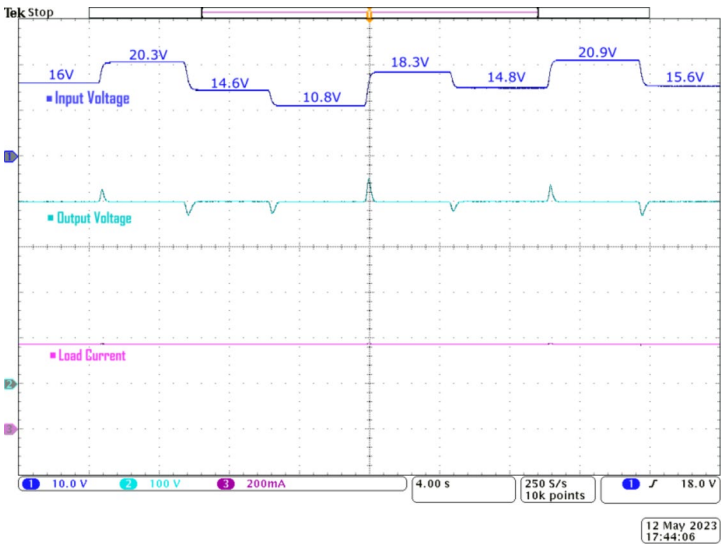

Fig. 15. Experimental waveforms to showcase the line voltage regulation capability of the proposed Q⁴HGC, CH1—input voltage, CH2—output voltage, and CH3—load current.

control. When the input voltage is randomly varied from 10.8 to 20.9 V in a stepped manner, the closed-loop control mechanism acts on the converter, and the output voltage value is quickly restored to the nominal value of 400 V with minimal undershoot and overshoot. The proposed converter momentarily achieves a maximum voltage amplification of 37 while stepping up from 10.8 to 400 V.

Figure 16 illustrates the load regulation capability of the proposed Q⁴HGC. The proposed converter effectively maintains a stable output voltage across a broad spectrum of load current changes, and is evident from the practical waveforms. The proposed Q⁴HGC meets the load requirements at 400 V even when the load current varies from 330 to 464 mA. In terms of power levels, the proposed converter maintains the output voltage at 400 V when the load fluctuates between 132 and 185 W. This practical evidence confirms the converter's adaptability and reliability in managing the diverse load scenarios despite line voltage fluctuations while delivering a constant voltage of 400 V to the output.

Benchmarking the proposed converter

In this section, the proposed converter is compared with recent and similar state-of-the-art high-gain DC–DC converters to appreciate its superior features. The converters that are chosen for comparison are presented in various references as outlined in Table 3. To understand and validate the superior features of the proposed Q⁴HGC, the converters that are chosen for comparison yield a voltage gain > 13 and belong to either quadratic, cubic, or quartic variants. The main comparison attributes are elaborated in the following sub-sections. All the converters compared provide voltage amplification greater than 10.

Voltage gain (*M*) and duty ratio

All the converters that are compared in Table III yield excellent voltage conversion ratios. The converter presented in[36] yields the maximum voltage gain of 32.5 at a slightly higher duty ratio of 63%. Converters presented in[31,34] attain the second lowest voltage amplification of 14.8 and 14.16, respectively. The converter in[31] is a QBC variant

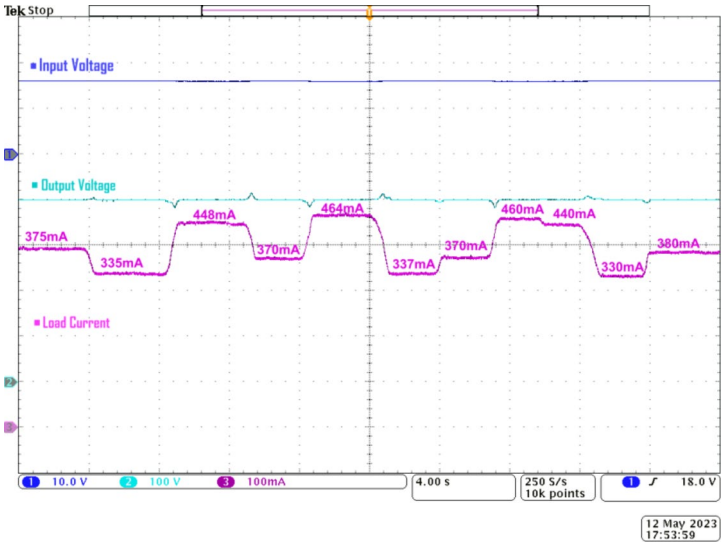

Fig. 16. Experimental waveforms to verify the load regulation capability of the proposed converter, CH1—input voltage, CH2—output voltage, and CH3—load current.

Attributes	Converter presented in						Proposed Q⁴HGC
	31	34	35	36	37	39	
V_{in}	27 V	12 V	45 V	20	48	18 V	16 V
V_0	400 V	170 V	800 V	650 V	650	380 V	400 V
M	14.81	14.16	17.78	32.5	13.5	21.1	25
D	0.5	0.48	0.632	0.63	0.48	$\delta_0 = 0.50$ $\delta_3 = 0.57$	$\delta_1 = 0.50$ $\delta_3 = 0.46$
N_{mag}	2 (1 simple inductor and 2 CI)	3	3	3	3	4	5
N_{Sw}	2	1	1	1	1	3	3
N_{Di}	4	7	5	7	7	5	7
TCU	12	16	12	16	16	16	20
M/TCU	1.2	0.885	1.481	2.03	0.846	1.31	1.25
M/TCU at $\delta = 0.5$	1.25	1	0.667	0.9375	1	1	1.6
Current stress of the switch (% of I_{in})	Min = 60% Max = 100%	Min = 194% Max = 194%	Min = 150% Max = 150%	Min = 100% Max = 100%	Min = 194% Max = 194%	Min = 39% Max = 100%	Min = 46% Max = 100%
Source current nature	Pulsating	Continuous with ripple	Pulsating	Pulsating	Pulsating	Ripple-free	Ripple-free
Gain extension technique	QBC with coupled inductor and DCM	Single Switch Cubic Boost Converter with SCs	Active inductor-capacitor-two diodes (LC2D) network	active switched inductor-capacitor network (SLCN)-based	active switched inductor-capacitor network (SLCN)-based	IBC with lift capacitor cascaded to QBC	Floating Capacitor based cubic Cell + IBC
Voltage gain function	Quadratic	Quadratic	Cubic	Cubic	Quartic	Cubic	Quartic
η (%)	94.9	–	91.6	90.04	95.48	95.6	92.7

Table 3. Comparison of the proposed Q⁴HGC and some similar converters. N_{mag} no. of magnetic elements, N_{Sw} no. of switches, N_{Di} no. of diodes, TCU total components used.

that is operated at a duty ratio of 50%, while the converter in[34] yields twice the cubic amplification using a VMC-based single switch C³BC. Moreover, the converter in[34] is operated at the second lowest duty ratio of 48%, resulting in the second lowest voltage gain value. The converter introduced in[39] and the proposed Q⁴HGC utilize an interleaved arrangement at the input side to mitigate input current ripple.

The proposed Q⁴HGC achieves the second-highest voltage amplification of 25, albeit operating S_3 at a notably low duty ratio of 46%, the lowest among all compared converters. On the other hand, the converter outlined in[39] achieves an impressive voltage amplification of 21.11, operating S_3 at a much higher duty ratio of 57%. The converter presented in[37] yields the lowest voltage conversion ratio of 13.5 at the second lowest duty ratio of 48%. The converter described in[36] attains the highest voltage amplification, albeit at the second highest duty ratio value of 63%. Figure 17 illustrates the voltage gain plot of all the converters compared in Table 3. The proposed Q⁴HGC yields the highest voltage conversion ratio mainly due to the gain extension techniques adopted.

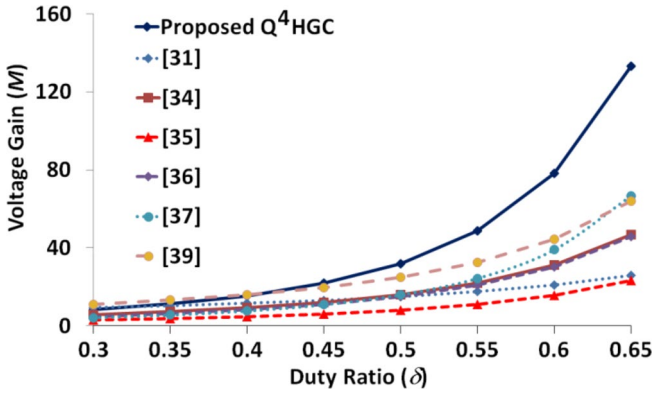

Fig. 17. Voltage gain plot of all the converters compared in Table 3.

Total components used (*TCU*) and *M/TCU* ratio

To gain a deeper understanding of the components used in the converter, the ratio of voltage gain (M) to total components used (TCU) serves as a comparative metric. The excellent voltage gain values provided by all converters are understood from the M/TCU value, which exceeds 1 for all the converters except the converters presented in[34,37]. Despite possessing excellent voltage gain profiles, their performance is hindered primarily due to the lower duty ratio of 48%. The converter outlined in[36] demonstrates an exceptional M/TCU ratio of 2.03, which is the highest. The second highest M/TCU value is 1.48, which is obtained by the converter in[35]. The converters in[35,36] utilize only 12 and 16 components, respectively. However, as both these converters were operated at significantly higher duty ratio values, they yielded higher voltage gain values.

The converter presented in[39] achieves a remarkable M/TCU of 1.31 at a much lower duty ratio of 0.57. The proposed Q^{4}HGC achieves a commendable M/TCU ratio of 1.25 while utilizing only 20 components. To standardize and eliminate the influence of duty ratio, the M/TCU ratio is calculated for all the converters at a fixed duty ratio of 50%. Surprisingly, except for the converters presented in[35,36], the M/TCU ratio of all the other converters is either greater than or equal to 1. Both the converters in[35,36] operate at the highest duty ratio value, which is responsible for their excellent M/TCU values. Expectedly, the proposed Q^{4}HGC demonstrates the highest M/TCU value of 1.6 at the normalized duty ratio of 50%, followed by the converter outlined in[31]. Thus, the excellent voltage gain capability of the proposed Q^{4}HGC and the judicious use of components in it are validated.

Voltage stress on the switches and diodes

The proposed converter and the one detailed in[39] share a common feature of employing three power switches, in contrast with the majority of compared converters, which utilize only one power switch. The converter described in[31] utilizes two switches, notably with low voltage stress values. The voltage stress across the switch with a higher value is still only 38.75% of V_0. Likewise, the converters presented in[34,36] exhibit maximum switch voltage stress values that are well-below V_0. Consequently, the converters employ MOSFETs with lower R_{DS-ON} values and achieve good efficiency values. The converters discussed in[35,37] utilize only one power switch experiencing the same voltage stress of V_0. In the proposed converter and the one described in[39], two switches are subjected to the least voltage stress, representing only 8% and 9.4% of V_0 respectively. In both these converters, one among the three switches experiences a voltage stress, which is the same as V_0. Figure 18 portrays the comparative attributes as a radial chart.

The normalized voltage stress value is obtained to showcase the advantageous features of the proposed converter. Several parameters are defined as follows. The switch voltage stress (SVS) is computed as V_{sw}/V_{in} and presented as a comparative attribute. Figure 19 demonstrates the SVS variation of all the converters compared in Table IV. Two of the three switches employed in the proposed converter experience the least variations. The normalized diode voltage stress ($NDVS$) and normalised switch voltage stress ($NSVS$) refer to the ratio of maximum voltage across the diode to V_0 and the switch to V_0, respectively, total voltage stress (TVS) is defined as the sum of voltage stress across all the semiconductor devices. It is computed and expressed as a percentage of V_0 as given by (48). To get an idea about the average voltage stress in the converter, the normalized TVS ($NTVS$) value is obtained and presented in (49).

$$TVS = \sum \left(\frac{V_{D_i}}{V_0} + \frac{V_{S_i}}{V_0} \right) \times 100 \tag{48}$$

$$NTVS = \frac{1}{N_{devices}} \sum \left(\frac{V_{D_i}}{V_0} + \frac{V_{S_i}}{V_0} \right) \times 100 \tag{49}$$

where V_{D_i} and V_{S_i} refers to the peak voltage stress of ith diode and switch respectively and $N_{devices}$ refers to the number of switching elements.

Most of the converters have at least one diode and power switch that experiences a voltage stress that is equal to V_0. Consequently, 4 out of 7 converters, including the proposed converter, exhibit a maximum $NDVS$ and

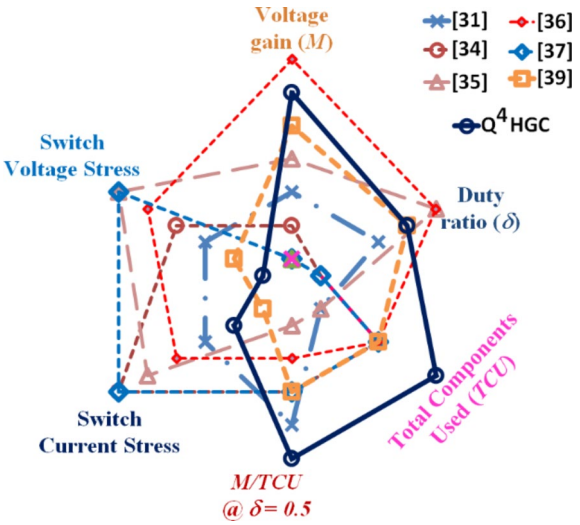

Fig. 18. Radial chart depicting the attributes based on which the converters compared.

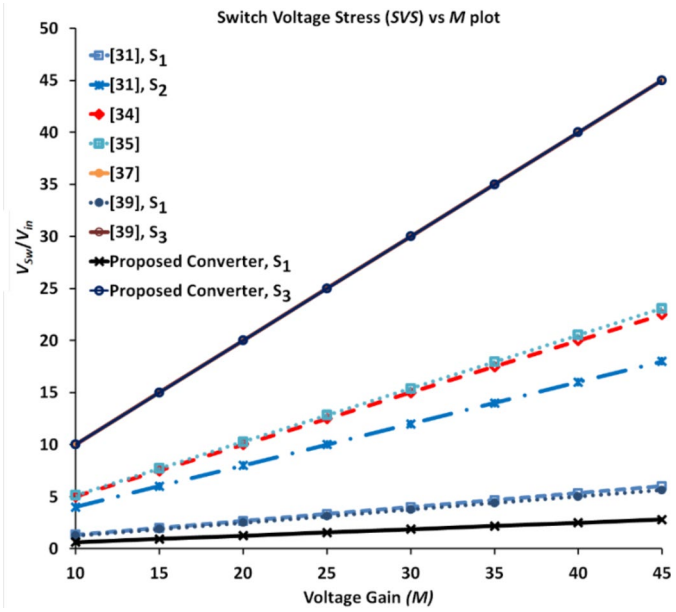

Fig. 19. Variation of *SVS* versus *M* for all the converters compared in Table 4.

NSVS value of 100%. Converters presented in[34,37] exhibit the least and second lowest *NDVS* values of 50% and 61%, respectively, whereas the converter presented in[31] experiences the lowest *NSVS* of 38.75%. The converter presented in[31] has the least *TVS* value since it exhibits the lowest *NSVS* and *NDVS* values.

To gain a clearer perspective on the average stress across components, the normalized total voltage stress (*NTVS*) is calculated and compared. The proposed converter stands out with the second lowest *NTVS* value of 40.4%, outperforming all other compared converters except the one in[31], which has the lowest *NTVS* of 37.41%. However, it is important to note that although the switch of the converter presented in[31] has reduced stress, it experiences significantly higher current stress. This could potentially lead to lower efficiency at higher power levels. To further evaluate the performance of these converters, a new term effectiveness index (*EI*) is introduced. The *EI* is defined as the ratio of *M* and *NTVS*. The proposed converter outperforms all the converters except the one presented in[36], which has an *EI* of 0.72, compared to the proposed converter's *EI* of 0.62. However, the converter in[37] is operated at a duty ratio of 0.63. When the proposed converter's duty ratio is matched, its *EI* value shoots up to 1.95 and outperforms the other converters by a huge margin. Thus, the judicious utility of all the components is justified. Figure 20 portrays the comparative metrics related to voltage stress on the semiconductor devices as a radial chart.

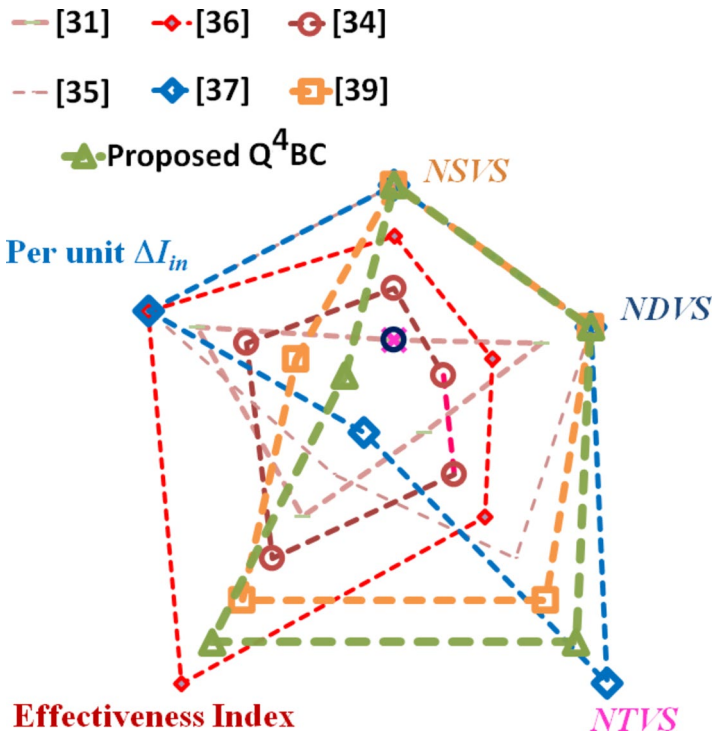

Fig. 20. Radial chart depicting the voltage stress on the semiconductor devices used in the converters compared in Table 4.

Attributes	Converter presented in						Proposed Q⁴HGC
	31	34	35	36	37	39	
SVS = V_{sw}/V_{in}	$\frac{V_{S_1}}{V_{in}} = \frac{1}{(1-\delta)}$ $\frac{V_{S_2}}{V_{in}} = \frac{2-D}{(1-\delta)^2}$	$\frac{1}{(1-\delta)^3}$	$\frac{1}{(1-\delta)^3}$	$\frac{1}{(1-\delta)^3}$	$\frac{1}{(1-\delta)^4}$	$\frac{V_{S_1}}{V_{in}} = \frac{V_{S_2}}{V_{in}} = \frac{1}{(1-\delta)}$ $\frac{V_{S_3}}{V_{in}} = \frac{2}{(1-\delta)^3}$	$\frac{V_{S_1}}{V_{in}} = \frac{V_{S_2}}{V_{in}} = \frac{1}{(1-\delta)}$ $\frac{V_{S_3}}{V_{in}} = \frac{2}{(1-\delta)^4}$
NSVS (%)	38.75	50	100	61	100	100	100
NDVS (%)	92	50	100	61	100	100	100
TVS (%)	247.7	298	337	303	429	345	404
NTVS (%)	41.28	37.41	56.27	45.46	53.63	43.4	40.4
Effective ness index (*M/NTVS*)	0.36	0.38	0.32	0.72	0.25	0.49	0.62
Input current ripple (% of I_{in})	133	18	200	200	200	3.43	3.25

Table 4. Comparative metrices related to voltage stress of the devices used in the proposed Q⁴HGC and some similar converters. *SVS* switch voltage stress, *NSVS* normalized switch voltage stress, *NDVS* normalized diode voltage stress, *TVS* total voltage stress, *NTVS* normalized total voltage stress.

Source current behaviour

Generally, the effective implementation of the MPPT algorithm often hinges on the current drawing profile of the intermediate high-gain converters.

In PV applications, a converter that draws smooth and ripple-free current from the input port is preferred. Among the converters compared in Table 4, only the proposed Q⁴HGC and the one described in[39] draw smooth and ripple-free current from the input. Additionally, the converter detailed in[34] demonstrates continuous input current with controllable ripple, dictated by the inductance. All the other converters draw pulsating current from their respective input ports. Figure 20 pictorially depicts the key attributes of all the converters compared in Table 4. The input current ripple profiles of all the converters are portrayed in Fig. 21. Table 5 presents the comparative attributes of some interleaved high-gain DC-DC converters and the proposed Q4HGC. The beneficial features, viz., high voltage gain capability and the component utility factor of the proposed are observed.

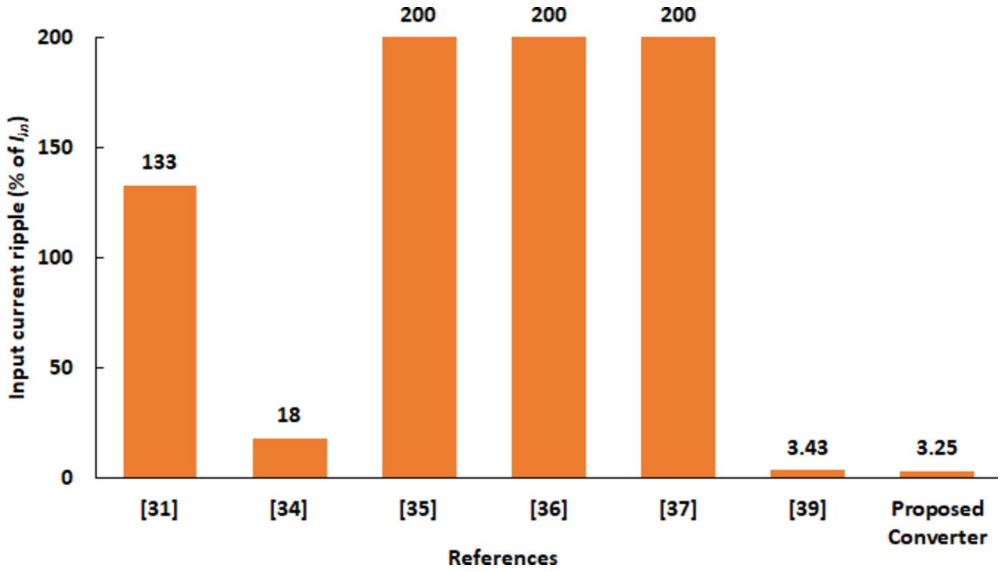

Fig. 21. Input current ripple values (in percentage) of the converters compared in Table 4 and portrayed as a bar graph.

Attributes	Converter presented in						Proposed Q^{4}HGC
	8	9	10	29	38	39	
V_{in}	18 V	18 V	18 V	18 V	24 V	18 V	16 V
V_0	380 V	380 V	380 V	380 V	380 V	380 V	400 V
M	21.11	21.11	21.11	21.11	15.833	21.1	25
D	0.5	0.5	0.5	0.5	0.65	$\delta_0 = 0.50$ $\delta_3 = 0.57$	$\delta_1 = 0.50$ $\delta_3' = 0.46$
N_{mag}	2 CIs	2 CIs	2 CIs	2 CIs	2 CIs	4	5
N_{Sw}	2	2	2	2	2	3	3
TCU	16	18	14	18	14	16	20
M/TCU	1.32	1.17	1.57	1.17	1.13	1.31	1.25

Table 5. Comparison of the proposed Q^{4}HGC with some interleaved converters.

Conclusion

In this paper, a non-isolated high-gain DC-DC converter with quartic voltage gain capability was introduced and discussed. The proposed converter was synthesized from a two-phase IBC structure with a voltage lift capacitor, and its voltage gain was significantly enhanced by adopting a floating capacitor-based cubic voltage gain cell. The experimental results obtained from a laboratory prototype version of the proposed converter confirmed its excellent voltage gain capability. Under practical conditions, the converter yielded a voltage gain of 25 (16 V input to 400 V output) and delivered 150 W to the load at an impressive efficiency of 92.7%. The proposed Q^{4}HGC employed three switches, and the voltage stress on two switches was just 8% of the output voltage due to the adopted gain extension concept. The voltage stress on five out of the seven diodes was less than 50% of the output voltage; only the output diode was subjected to a higher voltage stress level. Since an interleaving mechanism was adopted, the converter drew smooth and ripple-free current from the input port; the current stress on the switches was also significantly reduced. By implementing a closed-loop control, the output voltage of the Q^{4}HGC was regulated. When the input voltage and load current underwent step changes over a wide range, the proposed converter responded swiftly, and its output voltage was restored to 400 V quickly with minimal undershoots and overshoots. In fact, the maximum voltage gain of the proposed converter momentarily increased to 37 while the switches were still operated at safe duty ratio values. To appreciate the beneficial features of the proposed converter, it was compared with some state-of-the-art converters possessing quadratic, cubic, and quartic voltage gain capabilities. The proposed converter excels in terms of higher voltage gain capability, better utilization of components, reduced voltage stress on the devices, and ripple-free input current operation. The converter possesses a common-ground connection between the input and output ports; it is an additional advantage for PV applications. Due to its salient advantageous features, the proposed Q^{4}HGC is likely to be a good candidate topology for interfacing the low-voltage PV input with the high-voltage DC bus. Further, by incorporating open-circuit, short-circuit, and other protection mechanisms, the converter could be employed in a DC microgrid.

Data availability

All data generated or analysed during this study are included in this published article.

Appendix

State-space analysis and small signal model of the proposed converter

In this section, the focus lies in representing the low-frequency characteristics and response to small-signal variations using a state-space model. The well-known input and output relations in state-space form are given by (50), (51).

$$\dot{x} = Ax + Bu \tag{50}$$

$$y = Cx + Du \tag{51}$$

The voltage across the capacitors and current through inductors are chosen as state variables. The ON-state resistance of the diodes and magnetic elements is ignored while the loop resistances (r_1 and r_2) are included. The state variables are represented by the equation (52).

$$x = \begin{bmatrix} I_{L_1} & I_{L_2} & I_{L_3} & I_{L_4} & I_{L_5} & V_{C_{Lift}} & V_{C_1} & V_{C_2} & V_{C_3} & V_{C_0} \end{bmatrix}^T,\ \mathrm{y} = v_0,\ \text{and}\ u = v_{in} \tag{52}$$

Using the equations obtained during the operating modes and expressing them in state-space form, the state model of the system is derived and presented in (53)–(56). The two transfer functions viz., output voltage to duty ratio (G_{vd}) and output voltage to input voltage (G_{vg}) are determined and expressed using (55) and (56). Since all the poles of the transfer function lie of the left half of the s-plane, the proposed converter is stable. The control to output transfer functions of the system are derived by fixing one duty ratio a constant and varying the other.

$$\mathbf{A} = \begin{pmatrix} -\frac{r1}{L_1} & 0 & 0 & 0 & 0 & -\frac{1-\delta_1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & -\frac{r1}{L_2} & 0 & 0 & 0 & \frac{1-\delta_1}{L_2} & -\frac{1-\delta_1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & -\frac{r2}{L_3} & 0 & 0 & 0 & \frac{\delta_3}{L_3} & -\frac{1-\delta_3}{L_3} & 0 & 0 \\ 0 & 0 & 0 & -\frac{r2}{L_4} & 0 & 0 & \frac{\delta_3}{L_4} & \frac{\delta_3}{L_4} & -\frac{1-\delta_3}{L_4} & 0 \\ 0 & 0 & 0 & 0 & -\frac{r2}{L_5} & 0 & \frac{1}{L_5} & \frac{1}{L_5} & \frac{1}{L_5} & -\frac{1-\delta_3}{L_5} \\ \frac{1-\delta_1}{C_{\mathrm{lift}}} & -\frac{\delta_1}{C_{\mathrm{lift}}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{\delta_1}{C_1} & -\frac{\delta_1}{C_1} & -\frac{\delta_1}{C_1} & -\frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1-\delta_3}{C_2} & -\frac{\delta_3}{C_2} & -\frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1-\delta_3}{C_3} & -\frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1-\delta_3}{C_0} & 0 & 0 & 0 & 0 & -\frac{1}{R_0 \cdot C_0} \end{pmatrix} \tag{53}$$

$$B_\delta = \begin{bmatrix} \frac{V_{C_{Lift}}}{L_1} & -\frac{V_{C_{Lift}}+V_{C_1}}{L_2} & \frac{V_{C_1}+V_{C_2}}{L_3} & \frac{V_{C_1}+V_{C_2}+V_{C_3}}{L_4} & \frac{V_{C_0}}{L_5} & -\frac{I_{L_1}+I_{L_2}}{C_{Lift}} & \frac{I_{L_2}-I_{L_3}-I_{L_4}}{C_1} & -\frac{I_{L_3}-I_{L_4}}{C_2} & -\frac{I_{L_4}}{C_3} & -\frac{I_{L_5}}{C_o} \end{bmatrix}^T \tag{54}$$

$$B = \begin{bmatrix} \frac{1}{L_1} & \frac{1}{L_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{55}$$

$$C = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}^T \text{and } D\text{is a null-matrix} \tag{56}$$

$$\frac{v_0}{\hat{v}_{in}} = \frac{4.69 \times 10^{14} s^6 + 3.06 \times 10^{17} s^5 + 1.59 \times 10^{24} s^4 + 5.94 \times 10^{26} s^3 + 1.54 \times 10^{33} s^2 + 1.83 \times 10^{35} s + 3.19 \times 10^{41}}{s^{10} + 999.90 s^9 + 3.59 \times 10^9 s^8 + 2.83 \times 10^{12} s^7 + 4.32 \times 10^{18} s^6 + 2.58 \times 10^{21} s^5 + 1.94 \times 10^{27} s^4 + 8.42 \times 10^{29} s^3 + 2.36 \times 10^{35} s^2 + 7.30 \times 10^{37} s + 1.27 \times 10^{40}} \tag{57}$$

The closed-loop control to output transfer function of the proposed Q^4-HGC is achieved by fixing δ_1 constant while varying δ_3 and vice versa. The two transfer functions are given by (56) and (57).

$$\frac{v_0}{\hat{\delta}_3} = \frac{-1.316 \times 10^4 s^9 + 3.737 \times 10^9 s^8 - 5.831 \times 10^{13} s^7 + 1.172 \times 10^{19} s^6 - 7.929 \times 10^{22} s^5 + 1.07 \times 10^{28} s^4 - 3.357 \times 10^{31} s^3 + 2.328 \times 10^{36} s^2 - 2.94 \times 10^{39} s + 2.632 \times 10^{43}}{s^{10} + 999.9 s^9 + 3.587 \times 10^9 s^8 + 2.825 \times 10^{12} s^7 + 4.317 \times 10^{18} s^6 + 2.579 \times 10^{21} s^5 + 1.944 \times 10^{27} s^4 + 8.417 \times 10^{29} s^3 + 2.363 \times 10^{35} s^2 + 7.297 \times 10^{37} s + 1.268 \times 10^{40}} \tag{58}$$

$$\frac{v_0}{\hat{\delta}_1} = \frac{1.116 \times 10^{11} s^7 + 1.511 \times 10^{16} s^6 + 3.878 \times 10^{20} s^5 + 5.108 \times 10^{25} s^4 + 3.857 \times 10^{29} s^3 + 4.945 \times 10^{34} s^2 + 8.173 \times 10^{37} s + 1.022 \times 10^{43}}{s^{10} + 999.9 s^9 + 3.587 \times 10^9 s^8 + 2.825 \times 10^{12} s^7 + 4.317 \times 10^{18} s^6 + 2.579 \times 10^{21} s^5 + 1.944 \times 10^{27} s^4 + 8.417 \times 10^{29} s^3 + 2.363 \times 10^{35} s^2 + 7.297 \times 10^{37} s + 1.268 \times 10^{40}} \tag{59}$$

From the transfer functions, the step responses of the proposed converter are obtained and plotted in Fig. 22. The converter exhibits a quick response and settles within 30 ms.

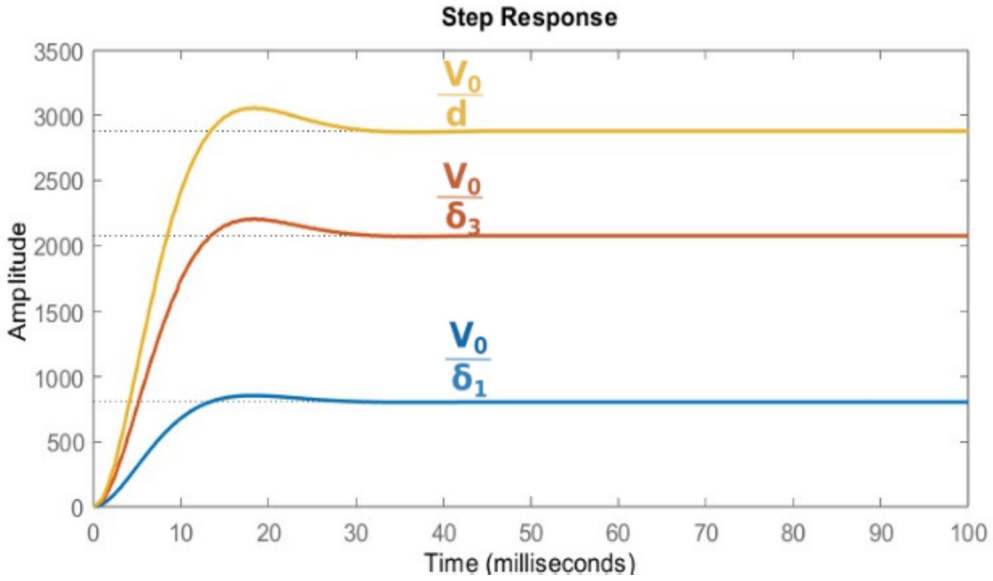

Fig. 22. Step responses of the converter obtained from output voltage versus individual duty ratio of the switches and the overall duty ratio.

The control of the proposed converter is achieved by varying δ3 and the corresponding transfer function is given by (57). The open-loop response of the system was inherently unstable, with a gain margin of 0.56 dB and a phase margin of − 6.97°, indicating poor stability and a tendency toward instability. To improve the performance an PI controller is designed is MATLAB PID tuner. The designed PID controller has proportional and integral gains given by Kp = 0.000593 and Ki = 0.0697. After implementing the PID controller, significant improvements were observed in the closed-loop system. The gain margin increased to 25.17 dB, and the phase margin improved to 119.98°, indicating a much more stable and robust system response. The integral action in the PID controller effectively mitigates steady-state errors, while the proportional action enhances the dynamic response, ensuring improved performance and stability under varying system conditions. The open-loop and closed-loop Bode diagrams are presented in Fig. 23.

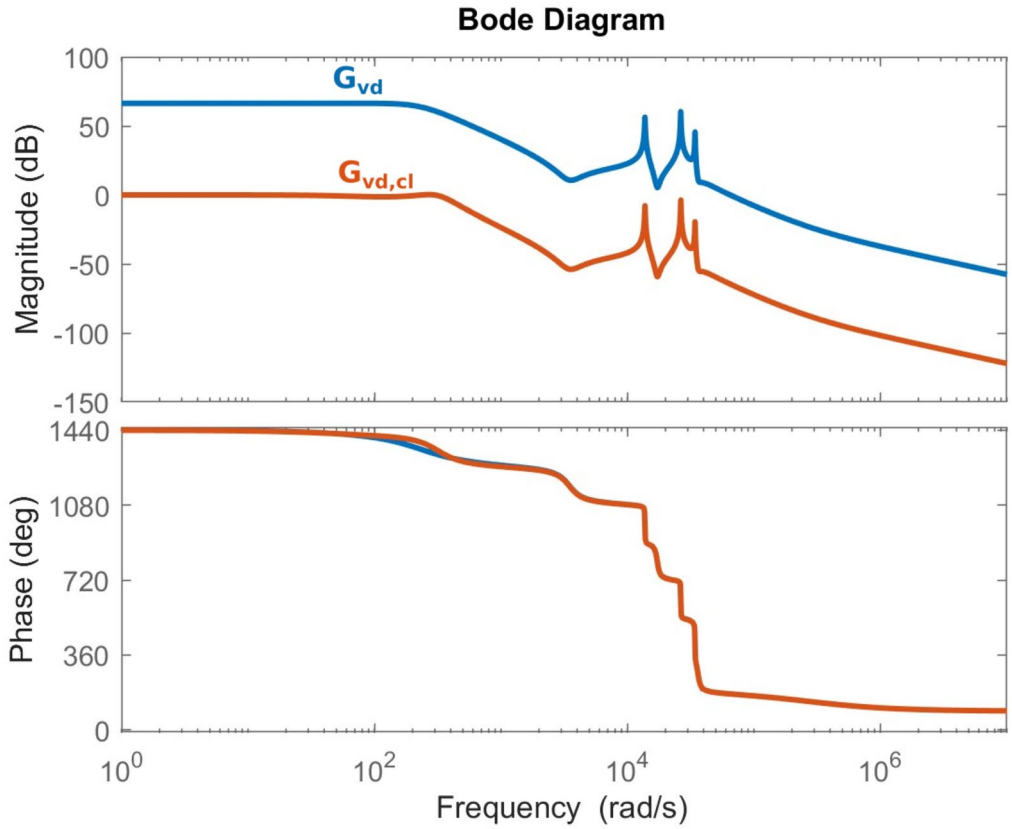

Fig. 23. Step responses of the converter obtained from output voltage versus individual duty ratio of the switches and the overall duty ratio.

Received: 29 July 2024; Accepted: 19 December 2024
Published online: 02 January 2025

References

1. Mumtaz, F. et al. Review on non-isolated DC-DC converters and their control techniques for renewable energy applications. *Ain Shams Eng. J.* **12**, 3747–3763 (2021).
2. Rajulapatti, A. & Prabhakar, M. High gain multi-input converter with inherent current sharing mechanism for photovoltaic application. *Sol. Energy* **233**, 118–133 (2022).
3. Venugopal, R. et al. Review on unidirectional non-isolated high gain DC–DC converters for EV sustainable DC fast charging applications. *IEEE Access* **11**, 78299–78338 (2023).
4. Tarzamni, H., Gohari, H. S., Sabahi, M. & Kyyrä, J. Nonisolated high step-up DC–DC converters: comparative review and metrics applicability. *IEEE Trans. Power Electron.* **39**, 582–625 (2024).
5. Valarmathy, A. S. & Prabhakar, M. High gain interleaved boost-derived DC-DC converters—A review on structural variations, gain extension mechanisms and applications. *Adv. Electr. Eng. Electron. Energy* **8**, 100618 (2024).
6. Mansour, A. S. & Zaky, M. S. A new extended single-switch high gain DC–DC boost converter for renewable energy applications. *Sci. Rep.* **13**, 264 (2023).
7. Hosseinpour, M. et al. Design and analysis of an interleaved step-up DC–DC converter with enhanced characteristics. *Sci. Rep.* **14**, 14413 (2024).
8. Valarmathy, A. S. & Prabhakar, M. Non-isolated high gain DC–DC converter with ripple-free source current. *Sci. Rep.* **14**, 973 (2024).
9. Valarmathy, A. S. & Prabhakar, M. High gain interleaved DC-DC converter with ripple free input current and low device stress. *Int. J. Electron.* https://doi.org/10.1080/00207217.2024.2312569 (2024).
10. Valarmathy, A. S., Prabhakar, M. & Varesi, K. Non-isolated high gain DC–DC converter for PV-fed DC microgrid. *Int. J. Sustain. Eng.* **17**, 32–50 (2024).
11. Alencar Freitas, A. A. et al. Non-isolated high step-up DC–DC converter based on coupled inductors, diode-capacitor networks, and voltage multiplier cells. *Int. J. Circuit Theory Appl.* **50**, 944–963 (2022).
12. Andrade, M. S. S., Faistel, T. M. K., Guisso, R. A. & Toebe, A. Hybrid high voltage gain transformerless DC–DC converter. *IEEE Trans. Ind. Electron.* **69**, 2470–2479 (2022).
13. Mansour, A. S. et al. High gain DC/DC converter with continuous input current for renewable energy applications. *Sci. Rep.* **12**, 12138 (2022).
14. Tewari, N. & Thazhathu, S. V. Family of modular, extendable and high gain DC-DC converter with switched inductor and switched capacitor cells. *IET Power Electron.* **13**, 1321–1331 (2020).
15. Bao, D. et al. Switched inductor double switch high gain DC-DC converter for renewable applications. *IEEE Access* **9**, 14259–14270 (2021).
16. Zhang, G., Jin, N., Yu, S. S. & Zhang, Y. An x-shaped-switching-network high-step-up converter for grid integration of renewable energy sources. *AEU Int. J. Electron. Commun.* **136**, 153776 (2021).

17. Reddy, B., Mahato, S. N. & Tewari, N. Dual switch ultra-high gain DC–DC converter with low voltage stress. *AEU Int. J. Electron. Commun.* **173**, 154995 (2024).
18. Gopinathan, S., Rao, V. S. & Sundaramurthy, K. Switched inductor-capacitor-based quasi-Z source converter for renewable energy source integration. *Int. J. Circuit Theory Appl.* **51**, 4646–4667 (2023).
19. Subhani, N. et al. An improved non-isolated quadratic DC-DC boost converter with ultra-high gain ability. *IEEE Access* **11**, 11350–11363 (2023).
20. Alsolami, M. & Allehyani, A. A non-isolated high voltage gain DC–DC converter-based hybrid switched LC network for renewable energy applications. *Int. J. Circuit Theory Appl.* **50**, 2055–2074 (2022).
21. Thirukkuralkani, K. N., Srinivasan, K. & Karthikeyan, V. A single switch hybrid quadratic converter for grid-integrated renewable energy system. *Int. J. Circuit Theory Appl.* **51**, 4276–4293 (2023).
22. Varesi, K., Hassanpour, N. & Saeidabadi, S. Novel high step-up DC–DC converter with increased voltage gain per devices and continuous input current suitable for DC microgrid applications. *Int. J. Circuit Theory Appl.* **48**, 1820–1837 (2020).
23. ALgamluoli, A. F. & Wu, X. Ultra-high voltage gain DC–DC converter based on new interleaved switched capacitor inductor for renewable energy systems. *Int. J. Circuit Theory Appl.* **52**, 2435–2465 (2024).
24. Naresh, S. V. K., Peddapati, S. & Alghaythi, M. L. A non-isolated high quadratic step-up converter for fuel cell electric vehicle applications. *Int. J. Circuit Theory Appl.* **51**, 3841–3864 (2023).
25. Kalahasthi, R. B., Ramteke, M. R., Suryawanshi, H. M. & Kothapalli, K. A single-switch high-gain DC–DC converter for photovoltaic applications. *Int. J. Circuit Theory Appl.* **50**, 1194–1215 (2022).
26. Schmitz, L., Martins, D. C. & Coelho, R. F. Comprehensive conception of high step-up DC-DC converters with coupled inductor and voltage multipliers techniques. *IEEE Trans. Circuits Syst. I Regul. Pap.* **67**, 2140–2151 (2020).
27. Habibi, S., Rahimi, R., Ferdowsi, M. & Shamsi, P. Coupled inductor-based single-switch quadratic high step-up DC–DC converters with reduced voltage stress on switch. *IEEE J. Emerg. Sel. Top. Ind. Electron.* **4**, 434–446 (2023).
28. Rezaie, M., Abbasi, V. & Kerekes, T. High step-up DC–DC converter composed of quadratic boost converter and switched capacitor. *IET Power Electron.* **13**, 4008–4018 (2020).
29. Samuel, V. J., Keerthi, G. & Mahalingam, P. Coupled inductor-based DC–DC converter with high voltage conversion ratio and smooth input current. *IET Power Electron.* **13**, 733–743 (2020).
30. Karimi Hajiabadi, M., Lahooti Eshkevari, A., Abdoli, I., Mosallanejad, A. & Salemnia, A. A quadratic step-up DC-DC converter with high gain, reduced voltage stress, and component counts. *Int. J. Circuit Theory Appl.* **51**, 2186–2206 (2023).
31. Hajiabadi, M. K., Mosallanejad, A. & Salemnia, A. A high step-up DC-DC converter based on coupled inductor and diode-capacitor with improved voltage gain and efficiency, and reduced voltage stress for photovoltaic systems. *Int. J. Circuit Theory Appl.* **51**, 787–806 (2023).
32. Abbasi, V., Mohammadi Tanha, K. & Rezaie, M. Ultrahigh step-up DC-DC converter consisting quadratic boost converter, multiplier cell, and three windings coupled inductor. *Int. J. Circuit Theory Appl.* **51**, 147–176 (2023).
33. Varesi, K. & Ghorbani, M. A generalized common-ground single-switch continuous input-current boost converter favourable for DC microgrids. *Int. J. Circuit Theory Appl.* **48**, 1658–1675 (2020).
34. Hao, Y., Guo, K., Liu, L., Cai, W. & Liu, F. Improved cubic boost converter based on voltage closed-loop control. *Energy Rep.* **8**, 87–95 (2022).
35. Kumar, G. G., Sai Krishna, M. V., Kumaravel, S. & Babaei, E. Multi-stage DC-DC converter using active LC2D network with minimum component. *IEEE Trans. Circuits Syst. II Express Briefs* **68**, 943–947 (2021).
36. Kumaravel, S. & Babu, P. E. Reduced switch voltage stress ultra-gain DC-DC converter for high voltage low power applications. *IEEE Trans. Circuits Syst. II Express Briefs* **69**, 1277–1281 (2022).
37. Babu, P. E., Vemparala, S., Pavithra, T. & Kumaravel, S. Switched LC network-based multistage ultra-gain DC-DC converter. *IEEE Access.* **10**, 64701–64714 (2022).
38. Samuel, V. J., Keerthi, G. & Mahalingam, P. Interleaved quadratic boost DC–DC converter with high voltage gain capability. *Electr. Eng.* **102**, 651–662 (2020).
39. Samuel, V. J., Keerthi, G. & Mahalingam, P. Non-isolated DC–DC converter with cubic voltage gain and ripple-free input current. *IET Power Electron.* **13**, 3675–3685 (2020).

Author contributions

T. S, L. Y, RS – Conception, design of the work, analysis, interpretation of data, drafting the work. M. P – Conception, design of the work, analysis, interpretation of data, drafting the work, reviewing and supervision. KV – Interpretation of data, reviewing and supervision. All authors reviewed the manuscript.

Funding

Open access funding provided by Vellore Institute of Technology.

Declarations

Competing interests

The authors declare no competing interests.

Ethical approval and consent to participate

NHANES is a public database. The NHANES protocol was approved by the NCHS Research Ethics Review Board (https://www.cdc.gov/nchs/nhanes/irba98.htm). All methods performed according to relevant guidelines and regulations.

Additional information

Correspondence and requests for materials should be addressed to M.P.