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Energy-efficient design of CNTFET-based quaternary arithmetic circuits

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The vast interconnection between digital logic blocks is the main challenge faced in chip designing, which leads to increased area overheads and average power consumption. One possible solution to overcome this challenge is to make use of multi-valued logic. However, for implementing multi-valued logic, new design techniques that deliver low-power and high-speed performance need to be explored. In this paper, carbon nanotube field effect transistor (CNTFET) based standard quaternary logic gates have been designed using pass transistor logic and voltage divider circuit techniques. The simulation results for the standard quaternary logic gates have been obtained using HSPICE with standard 32 nm CNTFET Stanford model. The results for the standard quaternary inverter circuit at a supply voltage of 0.9 V show average power consumption, delay, power delay product (PDP), energy delay product (EDP), and area of 31.446 nW, 7.948 ps, 0.249 aJ, 1.986×10^{-30} Js, and 13,287 λ^2, respectively. Similarly, the performance metrics, i.e., PDP and EDP are 0.597 aJ and 6.535×10^{-30} Js for standard quaternary NAND circuit and 0.099 aJ and 1.046×10^{-30} Js for standard quaternary NOR circuit, respectively. The proposed designs are superior in power consumption, PDP, and EDP in contrast to existing designs. The area occupancy and robustness of proposed standard quaternary inverter is also investigated by implementing layouts and performing Monte Carlo simulations. Further, the functionality of proposed quaternary logic gates is verified by using quaternary multiplier (QMUL) and quaternary half adder (QHA) as application examples. The proposed QMUL and QHA show PDP of 97.60 aJ and 95.937 aJ, respectively, which are quite encouraging when compared with literature. The new methodology for designing quaternary circuits reported in this work is expected to improve the performance of computing devices.

Keywords MVL, Quaternary logic, CNTFET, Low power, Noise margin, Quaternary multiplier

Over the years, the demand for energy-efficient and high-speed computing devices has significantly increased[1–3]. These computing devices require high-density integration for processing large amount of information at enhanced data rates. The conventional binary logic-based digital systems (with two distinct levels) are unfit for such modern computing devices, owing to interconnect issues associated with these systems[4]. The interconnections in integrated circuit designing using binary logic systems lead to energy consumption and propagation delay as the size of transistors is decreased[5–7]. As information density and processing speed increase, continuing with binary logic designs becomes increasingly challenging[8].

The limitations of binary logic are well compensated by non-binary logic. Non-binary logic is often called multi-valued logic (MVL), for example, ternary logic and quaternary logic[9]. With the help of the MVL, more information can be transferred over a set of wires. Also, every register can hold a greater number of bits because interconnect complexity and chip area decrease[10]. It has been proved that among all radices, the ternary logic (radix 3) is the most efficient radix in terms of its hardware implementation[11]. However, using quaternary logic (radix 4) offers all the benefits of MVL systems, such as area reduction due to its fewer interconnects, and the important advantage of being easily interfaced with traditional binary logic circuits[12].

Si-MOSFET technology has been used for designing MVL circuits for the last few years. However, in the era of nanoelectronics, as the technology goes beyond 32 nm, the Si-MOSFET technology failed to provide satisfactory results to design MVL-based circuits due to short channel effects (SCEs) and high leakage currents[13–15]. CNTFETs are highly suited for MVL systems due to their outstanding properties, such as high carrier mobility, scalability, and the ability to modify their threshold voltage by altering nanotube dimensions[16].

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These features make CNTFETs efficient at supporting the accurate voltage levels required for multi-valued logic operations. Furthermore, CNTFETs exhibit better switching speed performance than traditional Si-MOSFET technology, making them a promising contender for next-generation logic designs[17]. Integrating MVL logic with CNTFETs could facilitate compact circuit layouts, reduce transistor counts, and improve computational throughput, addressing critical issues in advanced semiconductor technology[18]. Additionally, CNTFET-based MVL circuits hold capability for relevance in data storage and communication systems, where efficient encoding and processing of large-scale data are essential. Designing these circuits supports pursuing advanced computing concepts that fulfil the increasing demands of high-speed and low-power integrated systems. Examples of CNTFET-based ternary logic circuits include ternary logic gates[19], ternary multipliers[20,21], ternary half adders[22], ternary flip-flops[23], ternary full adders[24], and ternary SRAM[25]. Examples of CNTFET-based quaternary logic circuits include quaternary logic gates[9,26–31], quaternary decoders[26,27,32], quaternary multiplexers[33,34], quaternary half adders[18,26,27,30], quaternary full adders[17,33–35], quaternary multipliers[26,30,36], quaternary successor and predecessor[18,33].

The fundamental building blocks of MVL circuits are ternary and quaternary logic gates. The ternary and quaternary logic gates are used to design various ternary and quaternary arithmetic circuits, respectively[37,38]. For instance, if the power and delay of standard quaternary gates, namely standard quaternary inverter (SQI), standard quaternary NAND (SQNAND), and standard quaternary NOR (SQNOR), are reduced, it will result in an overall power-delay-product (PDP) and energy-delay-product (EDP) improvement of the circuit in which they are deployed. Shams ul Haq et al.[38] and A. Paul et al.[31] have proposed standard quaternary gates in the recent past. These standard quaternary gates have been used in the implementation of half adder, multiplier[38], and asynchronous up/down counter[39] circuits. The logic gates proposed by A. Paul et al.[31] are more efficient than other designs in terms of power, energy, and fabrication cost. However, on the other hand, the logic gates proposed by Shams ul Haq[38] are designed with the integration of resistive random-access memory (RRAM) and CNTFET technologies to have the advantages of low-power dissipation, improved delay, and low PDP, while achieving non-volatility. The application of hybrid CNTFET-RRAM technology exhibits potential for implementing desired logic, although the integration of these two technologies encounters specific device limitations. Reliability concerns become especially evident when scaling RRAM below 25 nm. A considerable issue emerges from the endurance limitations in CNTFET-RRAM technology.

Studies of literature pertaining to standard quaternary gates[9,26,40] and their use in quaternary logic circuits reveal that there is dire demand for novel techniques based on quaternary gates and circuits that can deliver low-power and high-speed performance of systems in which they are deployed[30,41].

QMUL is a fundamental arithmetic block in digital circuits, which is widely utilized in arithmetic logic units (ALUs), address calculation modules, floating-point units, and cache memories[42]. In[26], the authors have presented a QMUL using quaternary transmission gates (QTGs). The main disadvantage of the designs is the excessive use of QTGs, which increases the number of transistors and power consumption. The utilization of QTGs is unnecessary when a fixed voltage is meant to be transferred. Their excessive usage has led to a high transistor count. In addition to this, three power supplies have been used in this design, which increases the number of connections thereby increasing cost of design and production[43]. In[32], the authors have presented a single-V_{DD} QMUL circuit using multiplexers. This design consists of two parts. The first part makes intermediate products through quaternary decoders and quaternary multiplexers. In the second part, the results obtained from the first stage are converted to quaternary values through an encoder. The voltage division occurs by constantly switched on transistors, which provide less resistance and cause far more static power dissipation than diode-connected transistors used in[44]. In[41], QMUL has been designed using three supply voltages and standard quaternary NAND and NOR designs. The use of three power supplies leads to the elimination of voltage divisions but increases the complexity of connections undesirably and also causes increased static current, which contributes to power overheads[40]. To tackle the above-said challenges faced by the researchers, we have introduced energy-efficient quaternary logic circuits. The key features of proposed quaternary circuits are as follows:

i. The proposed circuits deploy PTL and voltage divider approaches for enhancing power efficiency.
ii. Besides this, the proposed circuits rely on a single supply, which can reduce the cost of design and production owing to fewer connections.
iii. Effective chiral vector optimization has been performed in this work for various quaternary logic circuits so as to improve upon various performance parameters.
iv. The proposed circuits showcase improvement not only in power consumption but also in the performance metrics, i.e., PDP and EDP, using 32 nm CNTFET technology. Further, comparative analysis has been established in terms of layout for SQI circuits and in terms of figure of merit (FOM) for quaternary multiplier and half adder circuits for highlighting the outstanding performance of proposed circuits.

This paper is organized into seven sections. Introduction introduces the motivation for designing the CNTFET-based quaternary logic circuits, research issues in designing quaternary circuits, and the advantages of CNTFET technology over Si-MOSFET technology. Multi-valued logic system explains quaternary logic systems. Carbon nanotube field effect transistor (CNTFET) explains the description of CNTFETs. Design evolution: from existing to proposed circuits briefly elaborates on existing CNTFET-based quaternary logic circuits and describes the proposed quaternary circuits. Result and discussion discussed the results of the proposed quaternary gates. The proposed quaternary multiplier and quaternary half adder are discussed and compared with existing designs in Application circuits using proposed designs. The paper is summarized in Conclusion.

Multi-valued logic system

Modern very large-scale integration (VLSI) technology requires faster data transmission using fewer interconnections. CNTFET-based quaternary logic circuits can be used to fulfil this requirement. A quaternary logic system uses four states to represent the functionality of a circuit[45]. The logic levels of a quaternary logic system with the corresponding voltage level have been represented in Table 1.

The quaternary inverter, quaternary NAND (QNAND), and quaternary NOR (QNOR) are commonly used quaternary logic gates. The quaternary logic gates design various quaternary logic circuits, such as quaternary decoders, quaternary comparators, quaternary multiplexers, quaternary adders, and quaternary multipliers. The quaternary inverter circuits can be further classified into four categories: positive quaternary inverter (PQI), intermediate quaternary inverter (IQI), negative quaternary inverter (NQI), and standard quaternary inverter (SQI). The functionality of the quaternary inverters can be expressed mathematically using the Eqs. (1)-(4)[27].

$$\mathrm{PQI}\,(\mathrm{x}) = \begin{cases} 0, & x = 3 \\ 3, & x \neq 3 \end{cases} \tag{1}$$

$$\mathrm{IQI}\,(\mathrm{x}) = \begin{cases} 3, & x = 0\ or\ 1 \\ 0, & x \neq 2\ or\ 3 \end{cases} \tag{2}$$

$$\mathrm{NQI}\,(\mathrm{x}) = \begin{cases} 3, & x = 0 \\ 0, & x \neq 0 \end{cases} \tag{3}$$

$$\mathrm{SQI}\,(\mathrm{x}) = 3 - \mathrm{x} \tag{4}$$

The QNAND logic gate can be further categorized into four categories: positive quaternary NAND (PQNAND), intermediate quaternary NAND (IQNAND), negative quaternary NAND (NQNAND), and standard quaternary NAND (SQNAND). The functions of various QNAND gates are expressed using the following Eqs. (5)-(8):

$$\mathrm{PQNAND}(\mathrm{A},\mathrm{B}) = \begin{cases} 0, & if\ \overline{\min(\mathrm{A},\mathrm{B})} = 0 \\ 3, & otherwise \end{cases} \tag{5}$$

$$\mathrm{IQNAND}(\mathrm{A},\mathrm{B}) = \begin{cases} 3, & if\ \overline{\min(\mathrm{A},\mathrm{B})} = 2\ or\ 3 \\ 0, & otherwise \end{cases} \tag{6}$$

$$\mathrm{NQNAND}(\mathrm{A},\mathrm{B}) = \begin{cases} 3, & if\ \overline{\min(\mathrm{A},\mathrm{B})} = 3 \\ 0, & otherwise \end{cases} \tag{7}$$

$$\mathrm{SQNAND}\,(\mathrm{A},\mathrm{B}) = \overline{\min(A,\ B)} \tag{8}$$

Similarly, the QNOR logic gate can be classified into four categories: positive quaternary NOR (PQNOR), intermediate quaternary NOR (IQNOR), negative quaternary NOR (NQNOR), and standard quaternary NOR (SQNOR). The functionality of various QNOR logic gates can be represented using Eqs. (9)-(12):

$$\mathrm{PQNOR}(\mathrm{A},\mathrm{B}) = \begin{cases} 0, & if\ \overline{\max(\mathrm{A},\mathrm{B})} = 0 \\ 3, & otherwise \end{cases} \tag{9}$$

$$\mathrm{IQNOR}(\mathrm{A},\mathrm{B}) = \begin{cases} 3, & if\ \overline{\max(\mathrm{A},\mathrm{B})} = 2\ or\ 3 \\ 0, & otherwise \end{cases} \tag{10}$$

$$\mathrm{NQNOR}(\mathrm{A},\mathrm{B}) = \begin{cases} 3, & if\ \overline{\max(\mathrm{A},\mathrm{B})} = 3 \\ 0, & otherwise \end{cases} \tag{11}$$

$$\mathrm{SQNOR}\,(\mathrm{A},\mathrm{B}) = \overline{\max(A,\ B)} \tag{12}$$

The quaternary logic gates are essential building blocks in digital circuits. Designing a quaternary logic-based circuit requires nano transistors with multi-threshold voltage (multi-V_{th}) properties. Therefore, CNTFETs are the most suitable for designing quaternary logic circuits. The overview of CNTFET has been elaborated in the next section.

Logic level	Voltage level
0	0
1	$V_{DD}/3$
2	$2^*V_{DD}/3$
3	V_{DD}

Table 1. Quaternary logic levels and their corresponding voltage levels.

Carbon nanotube field effect transistor (CNTFET)

This section is subdivided into two subsections. "Structure of CNTFET" and "Characteristics of CNTFET" describe the structure and characteristics of the CNTFET device, respectively.

Structure of CNTFET

A CNTFET comprises carbon nanotubes (CNTs) that are prepared by rolling a graphene sheet into a cylindrical structure[46]. In a CNT, the direction of rolling a graphene sheet is called a chirality vector, represented using a pair (m, n) known as a chiral number[47,48]. The electrical and physical properties of CNT can be determined by chiral number. A CNTFET exhibits semiconductor property if the difference between m and n is neither a multiple of 3 (m-$n \neq 3$) nor zero (m-$n \neq 0$)[49]. In other cases, CNT would behave as metallic[50]. The diameter of CNT (D_{CNT}) is determined by the chiral vector as defined in Eq. (13)[51]. The structure of the CNTFET with the conducting channel replaced by CNT is shown in Fig. 1. The key process parameters of the CNTFET include gate length (L_g), gate height (H_g), oxide thickness (T_{ox}), CNT width (W_g), D_{CNT} and CNT pitch (P). The relationship governing the dependence of W_g on P, D_{CNT}, and the number of CNT (N) is presented in Eq. (13).

$$D_{CNT} = \sqrt{3}a_0/\ \pi\ \sqrt{m^2 + mn + n^2} \cong\ 0.0783\sqrt{m^2 + mn + n^2} \tag{13}$$

$$W_g = \mathrm{Max}\left[W_{min}\ (N-1)\ P + D_{CNT}\right] \tag{14}$$

Where, a_0 is the interatomic distance between each carbon atom and its neighbor, and W_{min} is the minimum W_g established during the lithographic process.

In CNTFET technology, the threshold voltage (V_{th}) adjustment is easy and precise in comparison with Si-MOSFET technology. Hence, the quaternary logic circuits can be designed efficiently using CNTFET. The V_{th} of a CNTFET can be represented mathematically according to Eq. (15)[52]:

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \cong \frac{0.436}{D_{CNT}} \tag{15}$$

Where, a is the carbon-to-carbon atom distance. Equation (15) illustrates that an increase in D_{CNT} (chiral vector) leads to decreases in V_{th}. This approach motivates the design of MVL circuits using MOSFET-like CNTFETs.

Characteristics of CNTFET

Figure 2(a) shows I_D versus V_{DS} curves for various V_{GS} values. The plot shows that higher V_{GS} values result in higher I_D. Figure 2(b) shows the I_D versus V_{GS} plots of the CNTFET device. The plot infers that increasing chirality vector leads to higher I_D. In Fig. 2(c), the V_{th} is analyzed against chiral values. It is evident that V_{th} decreases as chiral value increases. This analysis reveals the behaviour of the CNTFET device in different operating conditions, in particular demonstrating V_{GS} and V_{DS} influence on I_D and V_{th}.

Design evolution: from existing to proposed circuits

This section is subdivided into two sections. Section 4.1 provides the comprehensive review of existing approaches used in designing SQI circuits. While Sect. 4.2 outlines the methodological details of the proposed SQI, SQNAND, and SQNOR circuits.

Existing circuits

In SQI-1[27], the voltage division concept has been used to generate all quaternary voltage levels, as shown in Fig. 3(a). Voltage division refers to the distribution of high voltage levels into relatively lower voltage values. SQI-1 uses dedicated paths to generate four different logic levels at the output. Also, this design has diode-connected CNTFETs (T_2, T_3, T_6, and T_7) having a chiral value (19,0) in series between pull-up and pull-down CNTFETs in the middle part of the circuit. The diode-connected CNTFET behaves as a diode and allows the flow of current in one direction due to the inherent characteristics of the CNTFET structure.

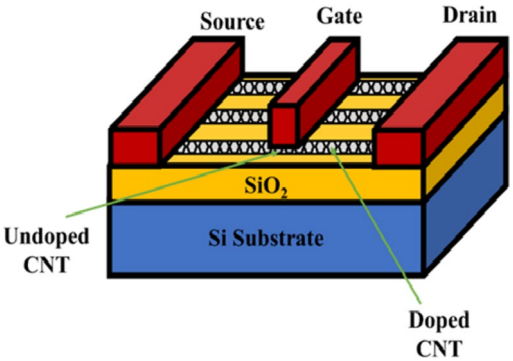

Fig. 1. Structure of CNTFET.

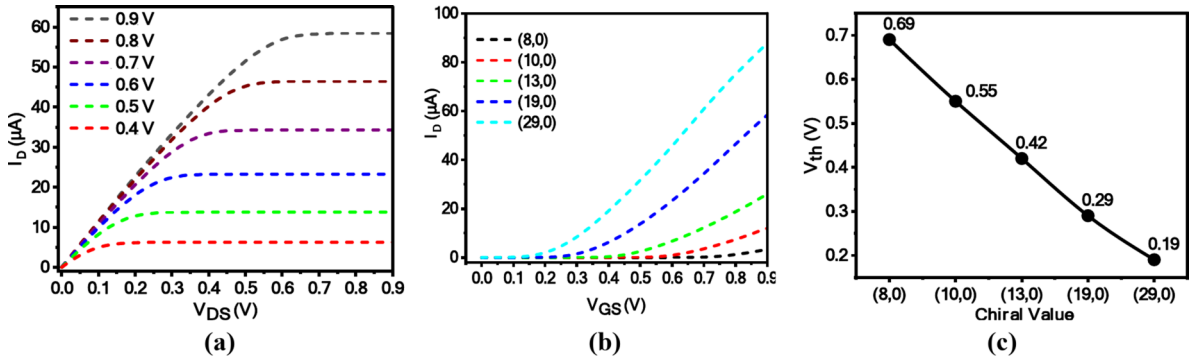

Fig. 2. Input and output characteristics of n-channel CNTFET **(a)** I_D versus V_{DS} for various values of V_{GS} **(b)** I_D versus V_{GS} at various values of chiral vector **(c)** V_{th} versus chiral values.

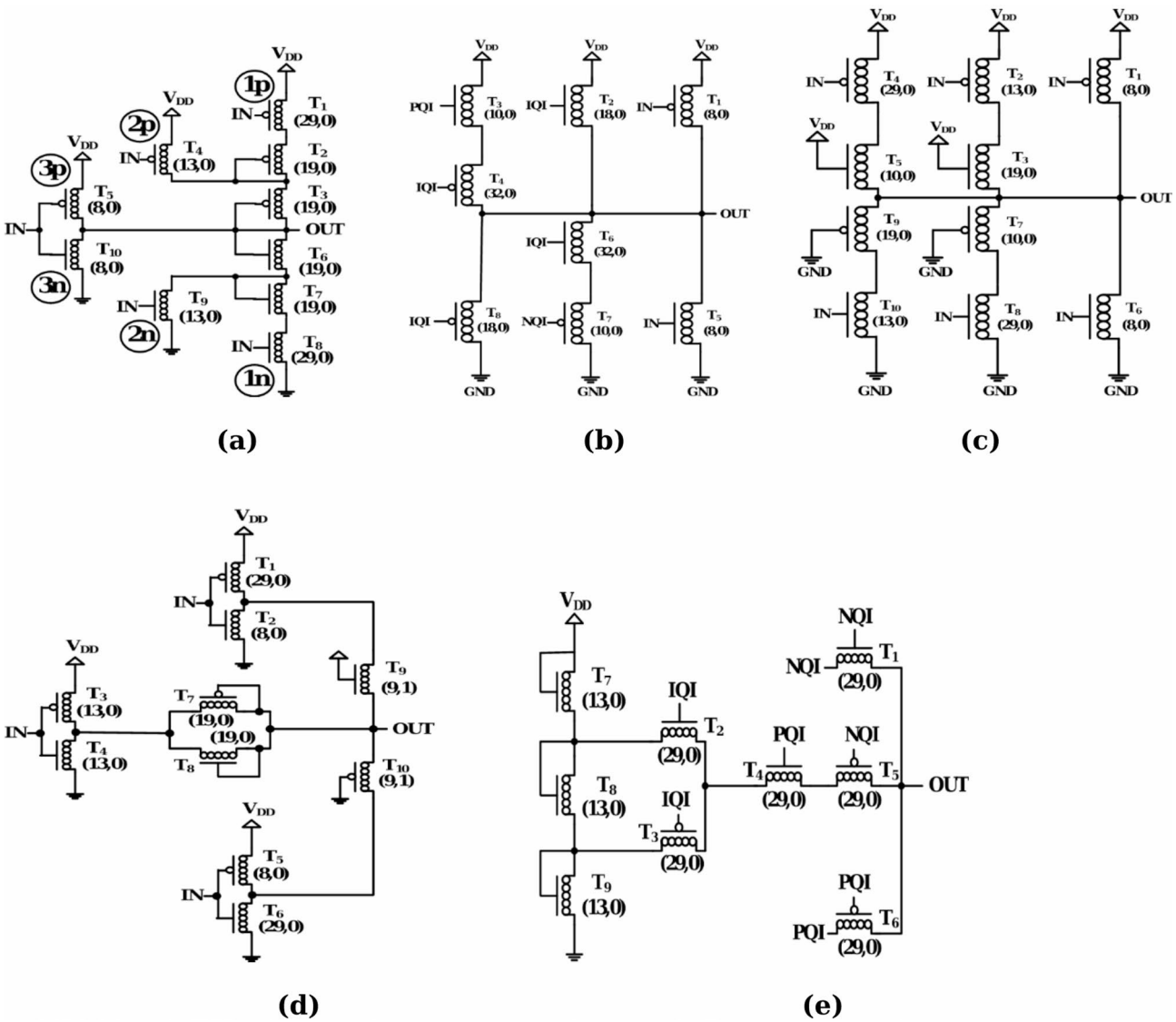

Fig. 3. Various SQI circuits **(a)** SQI-1[27], **(b)** SQI-2[40], **(c)** SQI-3[53], **(d)** SQI-4[30], and **(e)** SQI-5[31].

The design of SQI-2[40] is depicted in Fig. 3(b) using 14 CNTFETs, including NQI, PQI, and IQI. Various paths have been used in this circuit to generate all four logic levels at the output. Logic '0' and '3' appear at the output through transistors T_5 and T_1, respectively. In this design, two independent paths are used to generate logic '1' and logic '2' levels. Therefore, there are more degrees of freedom to adjust the diameters of the nanotube at the cost of area.

The SQI-3[53] has been implemented using 10 CNTFETs, as displayed in Fig. 3(c). The design shows higher power consumption, as four out of ten CNTFETs in SQI are always turned ON. The design of SQI-4[30] used diode-connected CNTFETs to produce the quaternary voltage levels at the output as depicted in Fig. 3(d). This design utilized various paths to generate four logic levels at the output. The SQI-4 benefits from the advantages of diode-connected CNTFETs, which reduces the power consumption in static mode. SQI-5[31] is designed using a voltage divider and PTL concept as displayed in Fig. 3(e). The SQI-5 used only three different chirality, i.e., (8,0), (13,0), and (29,0). Other designs utilize at least four to six types of chirality in CNTFETs.

Proposed methodology

Having understood about the various SQI design approaches reported by the researchers in the recent past, this section describes the details of the proposed SQI (refer "Proposed SQI circuit"), SQNAND, and SQNOR circuits (refer "Proposed SQNAND and SQNOR circuits").

Proposed SQI circuit

Figure 4 illustrates the proposed SQI circuit designed using 15 CNTFETs. The proposed SQI circuit has been implemented using a voltage divider and PTL configuration, wherein the intermediate branch of SQI-5 has been altered to generate voltage logic levels '1' and '2' with an improved critical path. It is important to note here that PTL configurations suffer from voltage degradation and reduced logic swing. However, these limitations of PTL are substantially mitigated through the utilization of CNTFET with a chiral vector of (29,0), exhibiting a low threshold voltage of approximately 0.19 V. CNTFETs inherently exhibit very low threshold voltages, which facilitates efficient carrier transport and significantly reduces voltage drop during signal transmission. Further, this characteristic ensures full swing output and preserves signal integrity, making the proposed quaternary logic gates suitable for complex multi-valued logic systems.

The voltage divider generates two voltage levels: V_1 (0.3 V) and V_2 (0.6 V) for logic '1' and logic '2', respectively, eliminating the need for additional power supplies. A voltage divider circuit[31] has been constructed using three N-type CNTFETs with chiral value (13,0). The circuit is designed using four distinct paths for each logic level. Additionally, other inverter circuits, including PQI, NQI, and IQI[27], have been utilized in the proposed SQI. The turning points of the proposed SQI circuit are displayed in Table 2.

When input is connected to logic '0', the output of NQI is logic '3', and T6 is turned ON, therefore, logic '3' (0.9 V) is transferred to the output. When the input is connected at logic '1', the output for PQI and IQI is logic '3', whereas the output of NQI is logic '0'. Therefore, T_7 and T_8 are turned ON, producing logic '2' as output. When input is connected to logic '2', the output of PQI is logic '3', and the output of NQI and IQI is logic '0'. So T_{13} and

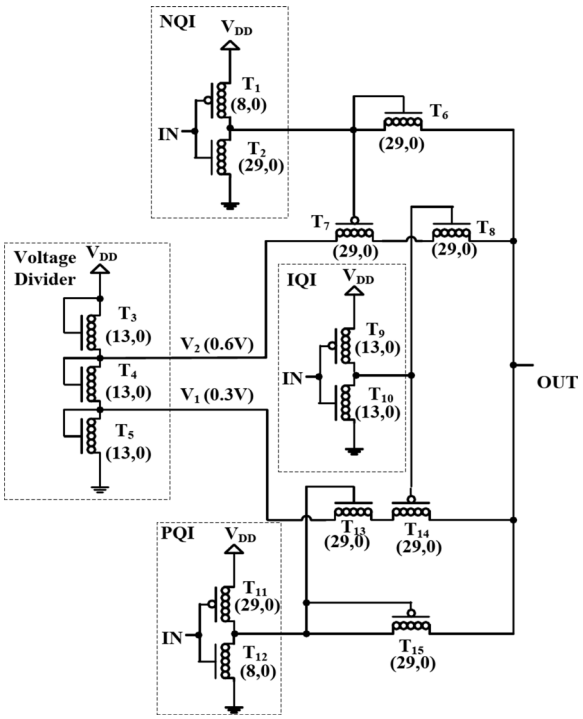

Fig. 4. The proposed SQI circuit.

Input	Transistors															Output
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}	
0	ON	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	3
1	OFF	ON	ON	ON	ON	OFF	ON	ON	ON	OFF	ON	OFF	ON	OFF	OFF	2
2	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	1
3	OFF	ON	ON	ON	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	ON	0

Table 2. Status of CNTFETs for proposed SQI.

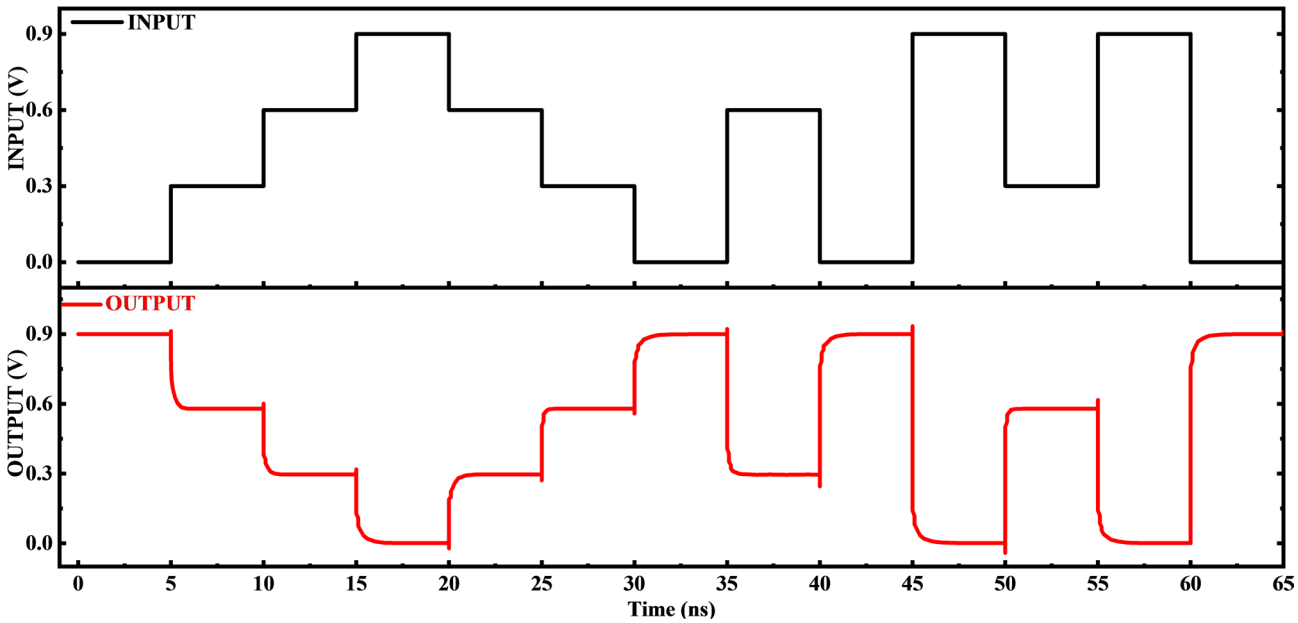

Fig. 5. Transient response of the proposed SQI circuit.

T_{14} are turned ON, and logic '1' is sent to the output. When input = '3', the output of PQI is logic '0', and T_{15} is ON, so logic '0' (0 V) is passed to the output. The transient response of the proposed SQI design is depicted in Fig. 5, which validates the functionality from Table 2.

Proposed SQNAND and SQNOR circuits

The proposed designs of SQNAND and SQNOR circuits are depicted in Figs. 6(a) and 6(b), using the same design methodology as the proposed SQI. The proposed SQNAND circuit has been designed using conventional PQNAND, IQNAND, and NQNAND circuits[40]. Similarly, the proposed SQNOR circuit utilized components of the conventional PQNOR, IQNOR, and NQNOR designs[40]. The proposed designs use a voltage divider circuit with chiral values (13,0) to produce intermediate logic levels. The proposed SQNAND and SQNOR designs use the following chiral values: (8,0), (13,0), and (29,0).

Furthermore, six transistors (3 P-type and 3 N-type CNTFETs) have been configured as pass transistors to transfer values from the input to the output paths. Tables 3 and 4 demonstrate the turning points of the proposed SQNAND and SQNOR circuits, respectively.

If either input A or B is at logic level '0', the PQNAND, IQNAND, and NQNAND circuits each produce an output of logic '3'. Consequently, the output of the proposed SQNAND will also be logic '3'. When one input is at logic '1' and the other is at logic '1' or a higher level, both PQNAND and IQNAND generate an output of logic '3', while the NQNAND produces logic '0'. As a result, the output of the SQNAND is logic '2'. If one input is at logic '2' and the other is at logic '2' or higher, the PQNAND gate outputs logic '3', whereas both the IQNAND and NQNAND gates output logic '0'. Therefore, the output of the SQNAND gate is logic '1'. Finally, when both inputs are at logic level '3', all three circuits, PQNAND, IQNAND, and NQNAND output logic '0'. Thus, the output of the SQNAND gate is logic '0'. The turning points of the proposed SQNAND and SQNOR circuits are tabulated in Tables 3 and 4, respectively. The proposed SQNOR gate operates similarly to the SQNAND gate, generating multi-level logic utilizing outputs from PQNOR, IQNOR, and NQNOR. Depending on the input combinations, the SQNOR gate produces outputs ranging from logic '0' to '3'.

SQNAND and SQNOR are essential components for quaternary logic design. Transient response has been demonstrated to evaluate their functionality, as shown in Fig. 7. The input patterns include two inputs that transition simultaneously, and the output curves demonstrate proper functionality, as observed in Tables 3 and 4.

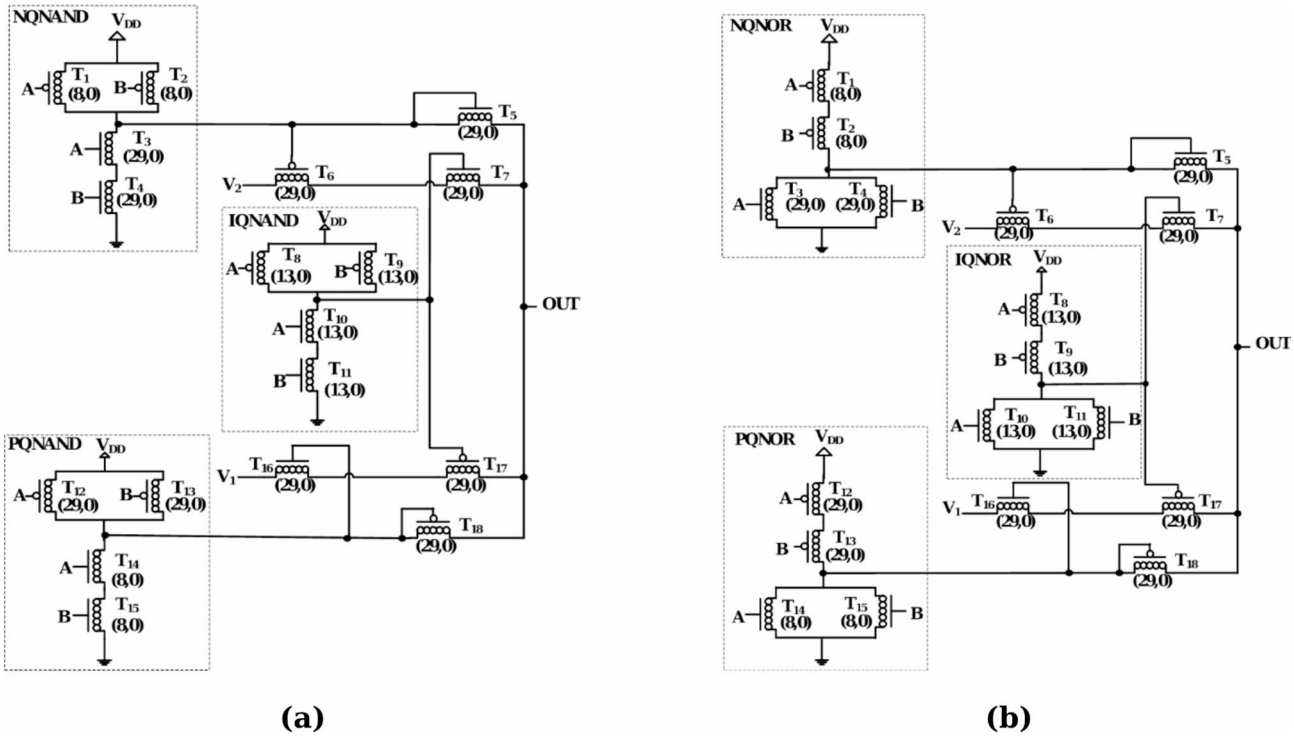

Fig. 6. Proposed circuits **(a)** SQNAND, and **(b)** SQNOR.

Input		Transistors																		Output
A	B	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}	T_{16}	T_{17}	T_{18}	
0	0	ON	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	3
0	1	ON	OFF	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	3
0	2	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	3
0	3	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	3
1	0	OFF	ON	ON	OFF	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	3
1	1	OFF	OFF	ON	ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	2
1	2	OFF	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	2
1	3	OFF	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	2
2	0	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	3
2	1	OFF	OFF	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	2
2	2	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	1
2	3	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	1
3	0	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	3
3	1	OFF	OFF	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	2
3	2	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	1
3	3	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	0

Table 3. Status of CNTFETs for proposed SQNAND.

Result and discussion

For fair comparison, the proposed designs and earlier reported designs have been simulated in HSPICE at room temperature using the 32 nm Stanford University CNTFET model[54]. This section is organized into five subsections. The performance of proposed and earlier reported gates is compared in "Variation in supply voltage and process parameter" for variations in supply voltage (V_{DD}). "Noise margin calculation" compares the noise margin (NM) performance of proposed and existing SQI, SQNAND, and SQNOR gates. The effect of process variations such as temperature, pitch, and number of CNTs is investigated in "Effect of process variations". Monte Carlo (MC) simulation of the proposed SQI circuit is conducted for P_{avg}, T_{pd}, and NM in "Monte Carlo analysis". The performance evaluation of various quaternary logic gates for different performance matrices is described

Input		Transistors																	Output
A	B	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}	T_{15}	T_{16}	T_{17}	T_{18}	
0	0	ON	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	3
0	1	ON	OFF	OFF	ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	2
0	2	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	1
0	3	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON	0
1	0	OFF	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	2
1	1	OFF	OFF	ON	ON	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	2
1	2	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	1
1	3	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON	0
2	0	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	1
2	1	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	1
2	2	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	1
2	3	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	ON	ON	0
3	0	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	0
3	1	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	0
3	2	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	0
3	3	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	0

Table 4. Status of CNTFETs for proposed SQNOR.

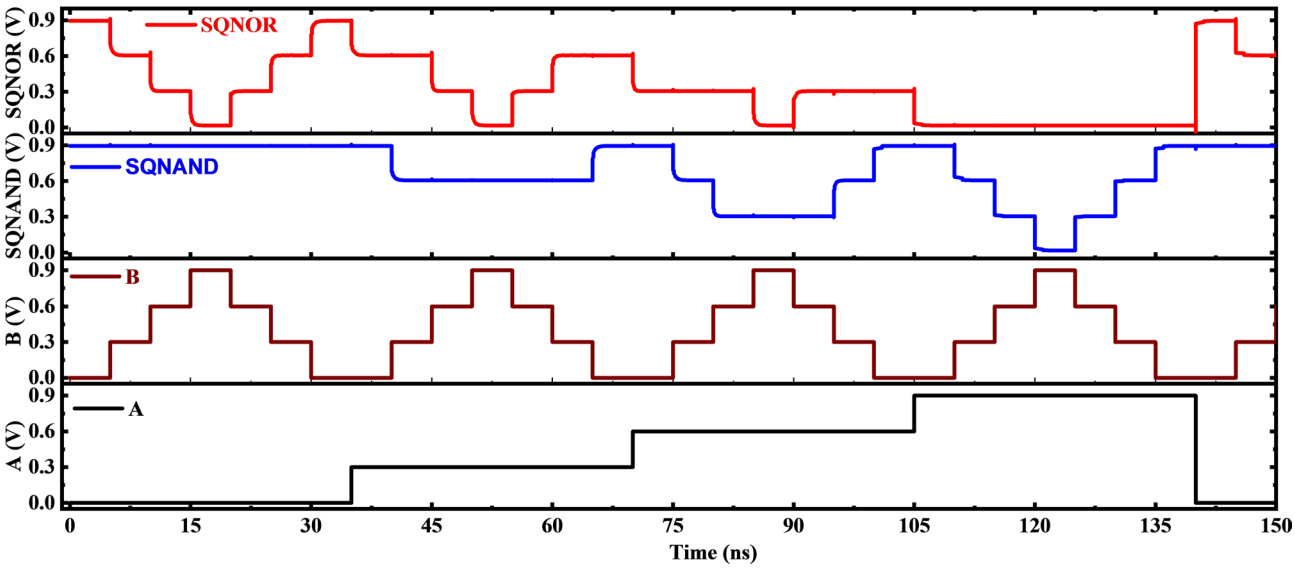

Fig. 7. Transient response of the proposed SQNAND and SQNOR.

in "Performance evaluation". The CNTFET model parameter values considered for simulations are depicted in Table 5.

To evaluate the driving ability of designs, a load capacitor of 0.1 fF with a typical V_{DD} of 0.9 V is considered for simulations. In the realistic environment the logic circuits (the quaternary logic gates, arithmetic circuits, etc.) will be used before digital signal processing stage for performing both arithmetic and logic functions[55]. The input capacitance of digital signal processing stage will be acting as a load to the quaternary logic gates as well as QMUL and QHA, which hover in the range from 0.1 fF to 5 fF. This is the reason for using 0.1 fF for simulation of gates as well as QMUL/QHA. Moreover, we have taken 0.1 fF as load capacitor in light of previously published articles. For instance, the existing QHA/QMUL circuits reported by various researchers have also adopted a range of capacitance values from 0.1 fF to 5 fF as a load[26,32,41,56,57].

The layouts of various SQI circuits have been presented in Fig. 8. The layouts are designed using MOCMOS-CN library of Electric software. The SQI-1 can be considered as highly area efficient, as it consumes lowest area (6438 λ^2) among considered SQI designs. On the other hand, SQI-5 consumes largest chip area (14250 λ^2). The area of the proposed SQI is 13287 λ^2, which is comparable with other SQI designs. The areas occupied by the voltage divider and PTL sections in the layout of the proposed SQI are 1957 λ^2 and 11330 λ^2, respectively.

Parameter	Description	Value
L_{ch}	Physical Channel Length	32 nm
L_{ss}	Length of doped CNT source-side extension region	32 nm
L_{dd}	Length of doped CNT drain-side extension region	32 nm
L_{geff}	Scattering mean free path in the intrinsic CNT	100 nm
Pitch	The distance between the centers of two neighboring CNTs within the same device	20 nm
L_{eff}	The mean free path in p+/n + doped CNT	15 nm
K_{ox}	Dielectric constant of high-k top gate dielectric material	16
T_{ox}	Thickness of high-k top gate dielectric material	4 nm
K_{sub}	Dielectric constant of substrate (*SiO2*)	4
C_{sub}	Coupling capacitance between the channel region and the substrate	40 aF/μm

Table 5. CNTFET model parameters and their values.

Variation in supply voltage and process parameter

The impact of V_{DD} variations on the proposed circuits is analyzed through simulations at 0.8 V, 0.9 V (typical), and 1 V, with results construed in "Variation in V_{DD} for SQI circuits", "Variation in V_{DD} for SQNAND circuits", and "Variation in V_{DD} for SQNOR circuits" for SQI, SQNAND, and SQNOR circuits, respectively.

Variation in V_{DD} for SQI circuits

Performance comparisons between the proposed SQI design and existing implementations are displayed in Fig. 9, highlighting four key parameters. The design of SQI-1[27] consumes maximum power among all SQI designs, as depicted in Fig. 9(a). The average power (P_{avg}) consumption for the proposed SQI design and SQI-5[31] is minimum among other SQI designs.

The impact of variations in V_{DD} on the propagation delay (T_{pd}) of all the considered SQI designs is displayed in Fig. 9(b). The SQI-1 design[27] shows lowest T_{pd} among all SQI designs but at the cost of higher power consumption. Further, two important FOM, i.e., PDP and EDP, are considered in this work for a fair comparison of different SQI circuits. The PDP and EDP versus V_{DD} plots for various SQI designs are shown in Figs. 9(c, d), respectively. It is clear from Figs. 9(c, d) that the proposed SQI design outperforms other SQI designs in terms of PDP and EDP.

Variation in V_{DD} for SQNAND circuits

Figure 10 depicts the impact of V_{DD} variations on performance parameters, namely, P_{avg}, T_{pd}, PDP, and EDP, respectively. The P_{avg}, PDP, and EDP values increase while the T_{pd} values decrease with an increase in V_{DD}. The proposed SQNAND shows the lowest values of P_{avg} as depicted in Fig. 10(a), while the SQNAND-1[27] infers lowest values of T_{pd} (refer to Fig. 10(b)). The proposed SQNAND and SQNAND-4[31] show the lowest PDP values (refer Fig. 10(c)). As far as EDP is concerned, the proposed SQNAND shows lowest values at 0.9 V and 1 V. At V_{DD}=0.8 V, the EDP performance is lowest for SQNAND-4[31]. The EDP values for the proposed SQNAND are high at V_{DD}=0.8 V (refer to Fig. 10(d)) owing to a minute increase in T_{pd} at this voltage level (refer to Fig. 10(b)).

Variation in V_{DD} for SQNOR circuits

The P_{avg} and T_{pd} versus V_{DD} plots for various SQNOR designs considered in this work are depicted in Figs. 11(a, b), respectively. The P_{avg} for the proposed SQNOR design is remarkably low in contrast to other SQNOR designs depicted in Fig. 11(a). The T_{pd} for SQNOR-1[27] design is minimum, as depicted in Fig. 11(b). Similarly, PDP and EDP for all SQNOR designs at different V_{DD} values are depicted in Figs. 11(c, d), respectively. From Figs. 11(c, d), it is evident that the proposed SQNOR design shows lowest values of PDP and EDP in contrast to other designs and is best suited to design energy-efficient circuits.

Noise margin calculation

This section describes the simulation methodology adopted for calculating noise margin (NM) and the corresponding results obtained for circuits considered in present research work. The voltage transfer characteristics (VTC) of the quaternary inverter and a visual representation of the quaternary NM are displayed in Fig. 12. According to the definition of quaternary NM, the output voltage levels are V_{O3}, V_{O2}, V_{O1}, and V_{O0}, while the input voltage levels are V_{I0}, V_{IL1}, V_{IH1}, V_{IL2}, V_{IH2}, and V_{I3}. The critical voltages are characterised by the slope (dV_{out}/dV_{in}) at -1, which determines the noise margin. For various SQI, SQNAND, and SQNOR logic gates, the NM at various logic levels is calculated using Eqs. (16–21), and the obtained results are depicted in Tables 6 and 7, and 8, respectively. The proposed design has the improved NM value.

$$NM_3 = V_{O3} - V_{I3} \tag{16}$$

$$NM_{H2} = V_{IH2} - V_{O2} \tag{17}$$

$$NM_{L2} = V_{O2} - V_{IL2} \tag{18}$$

$$NM_{H1} = V_{IH1} - V_{O1} \tag{19}$$

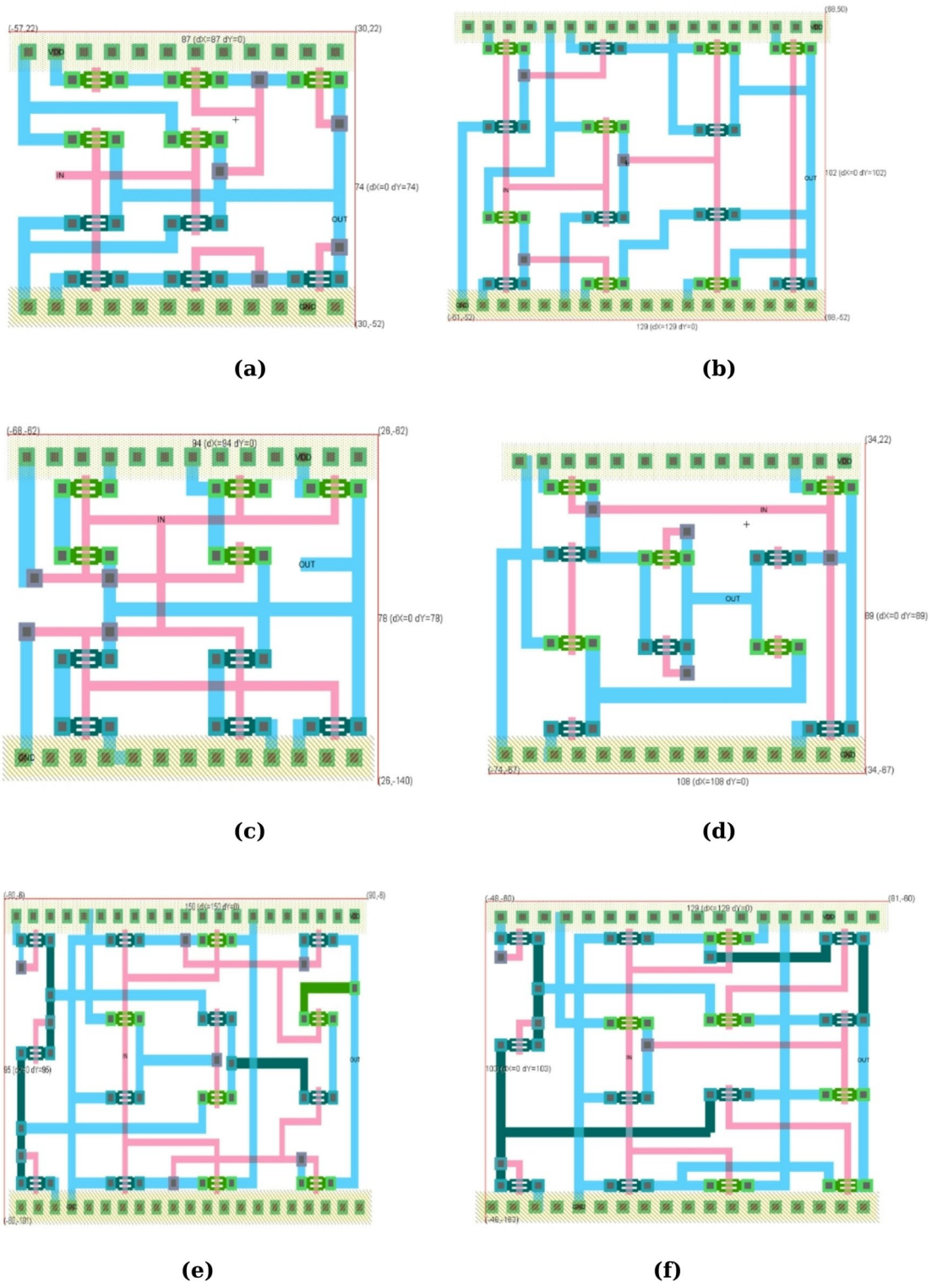

Fig. 8. Layouts of various SQIs **(a)** SQI-1[27], **(b)** SQI-2[39], **(c)** SQI-3[53], **(d)** SQI-4[30], **(e)** SQI-5[31], and **(f)** proposed SQI.

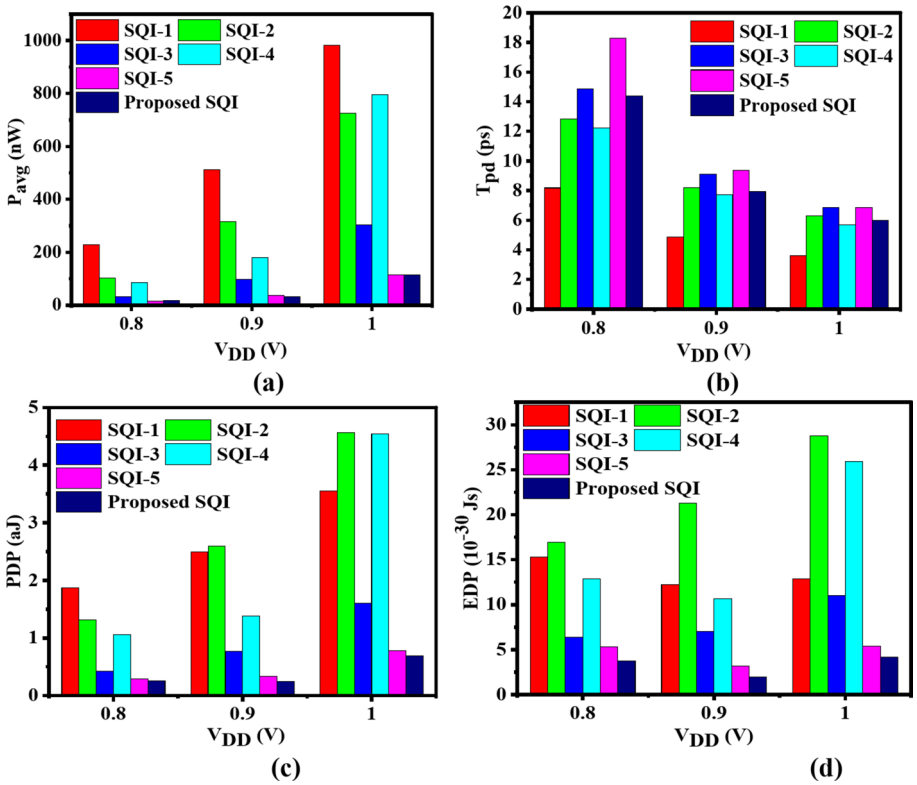

Fig. 9. Simulation results for SQIs at different V_{DD} **(a)** P_{avg}, **(b)** T_{pd}, **(c)** PDP, and **(d)** EDP.

$$NM_{L1} = V_{O1} - V_{IL1} \tag{20}$$

$$NM_0 = V_{I0} - V_{O0} \tag{21}$$

$$SNM = \text{Min.}\ (NM_3,\ NM_{H2}, NM_{L2}, NM_{H1}, NM_{L1}, NM_0) \tag{22}$$

The VTC curves for proposed designs of SQI, SQNAND, and SQNOR are depicted in Fig. 13. The SNM for proposed designs of SQI, SQNAND, and SQNOR are 124.20 mV, 91.69 mV, and 95.53 mV, respectively.

Effect of process variations

It is important to investigate the impact of process variations on digital circuits to validate their functionality. Therefore, the effect of variation in temperature, pitch, and number of CNT for proposed quaternary logic gates has been investigated in this section. The proposed quaternary logic gates have been analyzed at various temperature values ranging from 20 °C to 100 °C as displayed in Figs. 14(a, b). As the temperature increases, the P_{avg} and PDP also increase due to higher intrinsic carrier concentration and enhanced thermal energy.

The effect of pitch variation has been analyzed for proposed quaternary logic gates for values varying from 18 nm to 22 nm with a step size of 1 nm (refer Figs. 15(a, b)). With the increase in pitch variations, the P_{avg} and PDP values for all proposed quaternary logic gates slightly increases.

Number of CNT have also been varied for analysing their impact on the performance of proposed standard quaternary gates. As the number of CNTs increases, the drive current also increases, owing to which P_{avg} and PDP values also rises. Figure 16 illustrates the increase in power dissipation and PDP as the number of CNTs increases.

Monte Carlo analysis

Monte Carlo (MC) simulation has been performed to validate the reliability of the proposed SQI circuit. The reliability of the proposed SQI design is examined by random variation in the process parameters of CNTFET technology such as number of CNTs, oxide thickness, pitch, and channel length. MC simulation has been conducted for 100 iterations. The above-mentioned process parameters have an individual normal Gaussian distribution with $\pm 3\sigma = \pm 15\%$. Figure 17 shows the MC simulation results for the proposed SQI design at V_{DD} of 0.9 V. The mean values for P_{avg} and T_{pd} for the proposed SQI are 29.049 nW and 7.20 ps, respectively which are very close to nominal values observed at typical process corner. The coefficient of variance calculated for P_{avg} and T_{pd} of SQI is 0.268 and 0.026 respectively. The low values of coefficient of variance for P_{avg} and T_{pd} confirms the robustness of the proposed SQI design.

The process variation for NM has been investigated to check the reliability of the proposed quaternary logic gates. Figure 18 depicts the NM analysis for various proposed quaternary logic gates with the variation in V_{DD}.

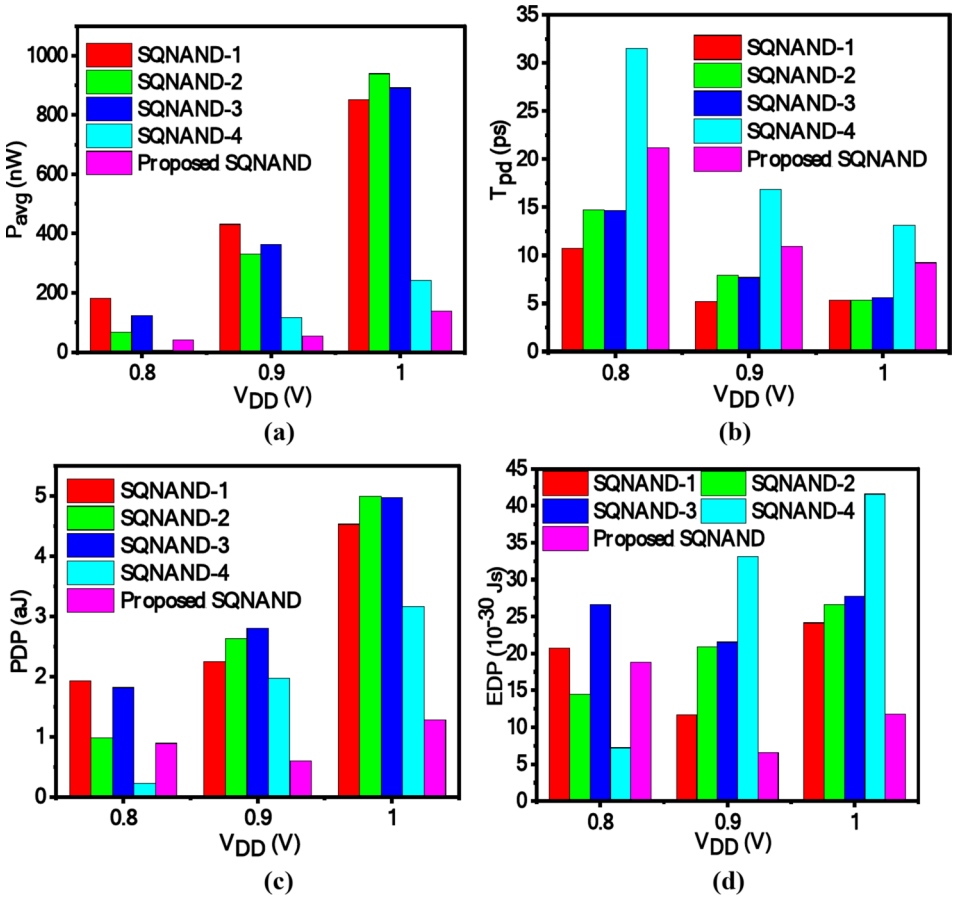

Fig. 10. Simulation results for SQNAND gates at different V_{DD} **(a)** P_{avg}, **(b)** T_{pd}, **(c)** PDP, and **(d)** EDP.

Performance evaluation

The performance evaluation of various quaternary gates is presented in Tables 9 and 10 for different metrics such as P_{avg}, T_{pd}, PDP, EDP, and NM at a supply voltage of 0.9 V. The P_{avg} of the proposed SQI is 16.25, 10.03, 3.11, 5.72, and 1.14 times lower than SQI-1, SQI-2, SQI-3, SQI-4, and SQI-5, respectively. The proposed SQI demonstrates 10.03, 10.41, 3.11, 5.57, and 1.35 times lower PDP compared to SQI-1, SQI-2, SQI-3, SQI-4, and SQI-5, respectively. Further, the proposed SQI has an EDP 6.15, 10.73, 3.55, 5.38, and 1.59 times lower than SQI-1, SQI-2, SQI-3, SQI-4, and SQI-5, respectively. Similarly, the proposed SQNAND displays 3.76, 4.41, 4.68, and 3.29 times lower PDP than SQNAND-1, SQNAND-2, SQNAND-3, and SQNAND-4, respectively. Compared to SQNAND-1, SQNAND-2, SQNAND-3, and SQNAND-4, the EDP of the proposed SQNAND is 1.79, 3.20, 3.29, and 5.07 times lower, respectively. The proposed SQNOR exhibits 5.22, 9.37, 5.75, and 1.17 times lower PDP than SQNOR-1, SQNOR-2, SQNOR-3, and SQNOR-4, respectively. The EDP for the proposed SQNOR is 15.19, 60.68, 24.15, and 9.84 times lower than SQNOR-1, SQNOR-2, SQNOR-3, and SQNOR-4, respectively. The NM of the proposed SQI and[27] is better than all other considered SQI designs. Besides this, the NM of the proposed SQNAND and SQNOR is better than designs reported in[27] and [30].

Application circuits using proposed designs

Arithmetic circuits are essential digital systems that enable various mathematical operations such as addition, subtraction, multiplication, and division. These circuits must enhance the speed and efficiency of systems such as calculators, microprocessors, and digital signal processors.

Proposed multiplier circuit

The QMUL circuit, as depicted in Fig. 19, has been designed and analyzed using the proposed SQNAND circuit. There are four building blocks for the QMUL circuit, namely, voltage divider, quaternary to binary decoder, product circuit, and carry circuit. Two voltage levels, V_1 (0.3 V) and V_2 (0.6 V), are generated through the voltage divider circuit as displayed in Fig. 4. The structure of QMUL utilizes these voltage levels to replace multiple power supplies with a single supply.

A quaternary to binary decoder[35] has been used to decode a quaternary input into a binary output as displayed in Fig. 19(a). When the input value of A is 0, 1, 2, and 3, then the respective binary signals A_0, A_1, A_2, and A_3 are high. Similarly, when the value of input B is 0, 1, 2, and 3, then the binary signals B_0, B_1, B_2, and B_3 are high, respectively.

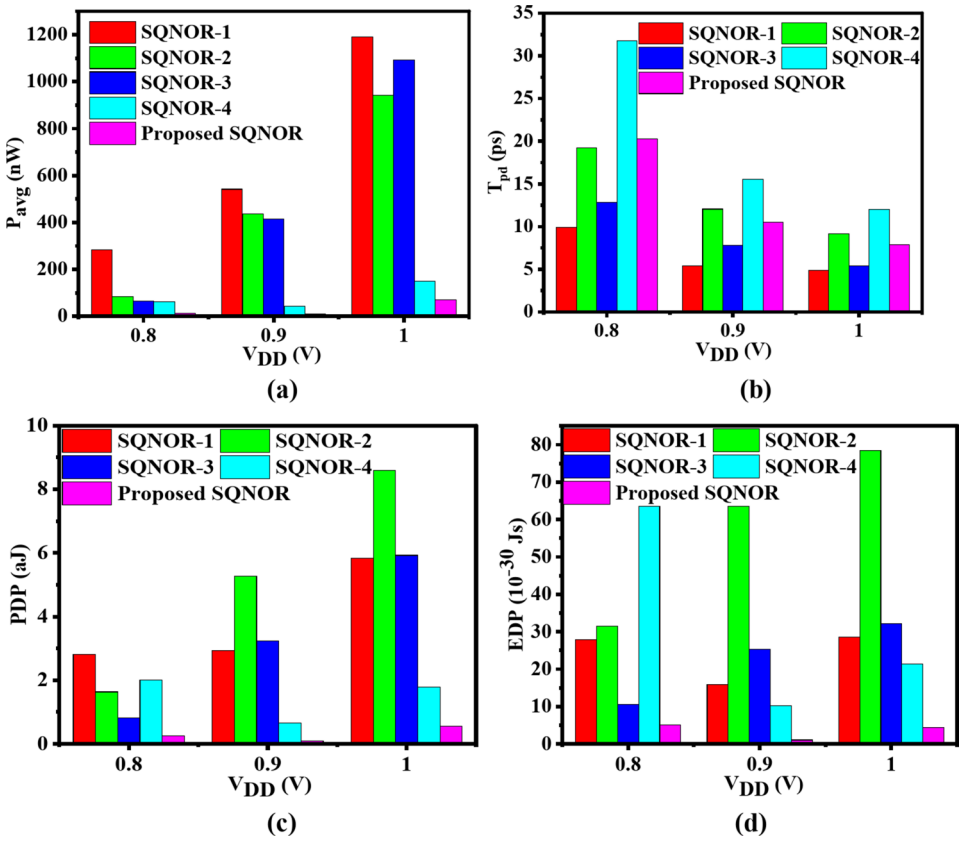

Fig. 11. Simulation results for SQNOR gates at different V_{DD} **(a)** P_{avg}, **(b)** T_{pd}, **(c)** PDP, and **(d)** EDP.

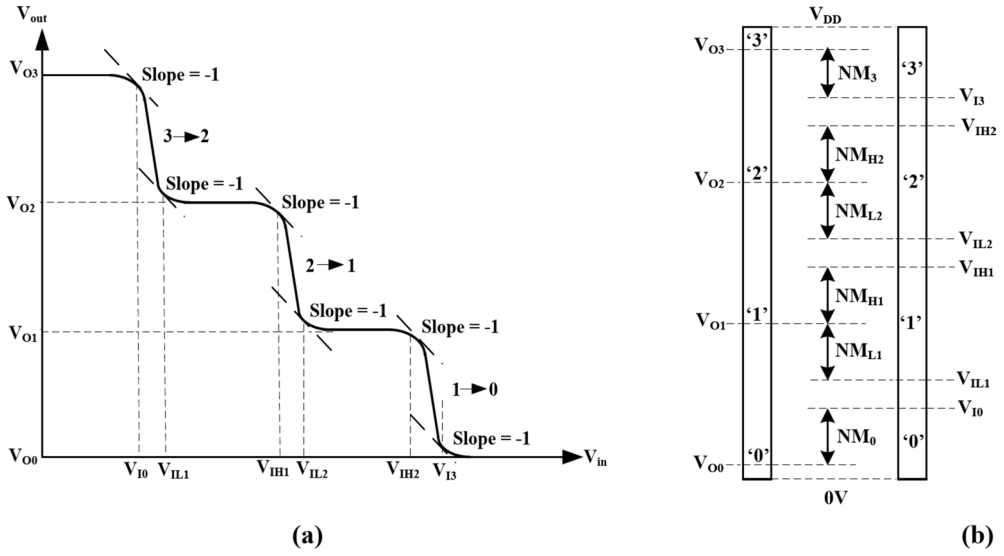

Fig. 12. Noise margin calculation **(a)** Typical VTC curve of a quaternary inverter, **(b)** Visual demonstration for quaternary NM.

The design structure used in[41] has been used to design product and carry circuits for the proposed QMUL as displayed in Figs. 19(b, c). "B" and "Q" symbols indicate binary and quaternary gates, respectively. The outputs generated from the quaternary to binary decoder have been forwarded as inputs to product and carry circuit. The product of two quaternary numbers is generated using the product circuit (QMUL) from Fig. 19(b), and carry is produced at the output (QCarry) through carry circuit from Fig. 19(c). The K-map for product and carry circuits of the proposed quaternary multiplier is depicted in Fig. 20.

Ref.	NM_3 (mv)	NM_{H2} (mv)	NM_{L2} (mv)	NM_{H1} (mv)	NM_{L1} (mv)	NM_0 (mv)	SNM (mv)
SQI-1[27]	120.76	121.51	119.87	120.87	120.51	121.76	119.87
SQI-2[40]	144.01	136.03	133.06	134.06	135.03	145.01	133.06
SQI-3[53]	120.78	130.59	128.49	129.49	129.59	121.77	120.78
SQI-4[30]	120.76	144.67	144.87	145.86	136.95	121.76	120.76
SQI-5[31]	122.19	154.01	148.01	149.01	153.01	127.32	122.19
Proposed SQI	124.20	154.01	148.01	149.01	153.01	127.66	124.20

Table 6. Noise margin calculation for various SQI circuits.

Ref.	NM_3 (mv)	NM_{H2} (mv)	NM_{L2} (mv)	NM_{H1} (mv)	NM_{L1} (mv)	NM_0 (mv)	SNM (mv)
SQNAND-1[27]	87.952	146.92	86.052	154.79	92.875	154.63	86.052
SQNAND-2[40]	150.00	167.80	95.723	170.55	103.32	175.02	95.723
SQNAND-3[30]	87.966	160.46	93.172	164.37	96.606	154.64	87.966
SQNAND-4[31]	124.50	154.01	148.01	149.01	153.10	122.27	122.27
Proposed SQNAND	91.690	183.01	113.00	185.01	122.22	159.55	91.690

Table 7. Noise margin calculation for various SQNAND gates.

Ref.	NM_3 (mv)	NM_{H2} (mv)	NM_{L2} (mv)	NM_{H1} (mv)	NM_{L1} (mv)	NM_0 (mv)	SNM (mv)
SQNOR-1[27]	153.63	93.872	153.79	87.050	145.92	88.949	87.050
SQNOR-2[40]	174.02	104.32	169.55	96.722	166.80	160.00	96.722
SQNOR-3[30]	153.64	97.605	163.37	94.170	159.46	88.964	88.964
SQNOR-4[31]	121.19	154.01	148.01	149.01	153.01	130.47	121.19
Proposed SQNOR	156.40	124.01	184.00	114.00	182.01	95.534	95.534

Table 8. Noise margin calculation for various SQNOR gates. The final noise margin is the minimum noise margin amongst all noise margins (NM_3, NM_{H2}, NM_{L2}, NM_{H1}, NM_{L1}, and NM_0), as mentioned in Eq. (22):

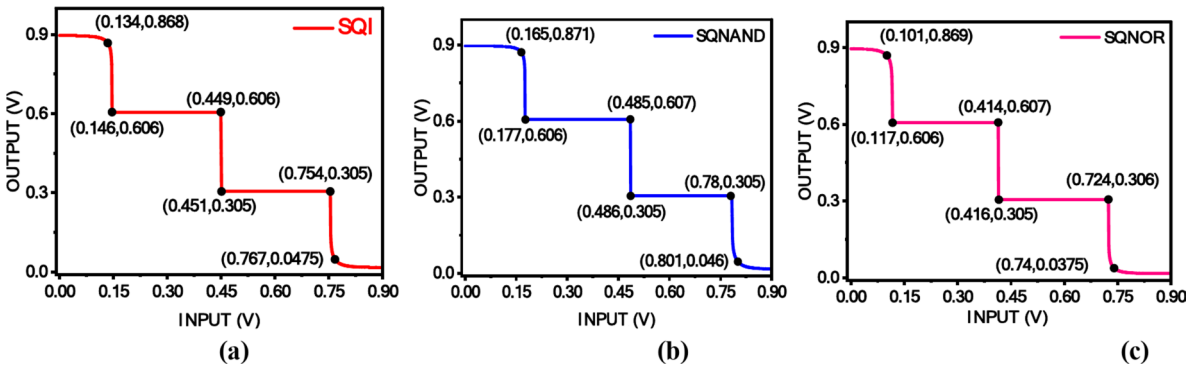

Fig. 13. VTC curve for proposed **(a)** SQI, **(b)** SQNAND, and **(c)** SQNOR.

The logic expressions for product and carry circuits of the quaternary multiplier obtained from Fig. 20 are expressed using Eqs. (23)-(24).

$$\mathrm{QMUL} = 1^{*}\left(A_1B_1 + A_3B_3\right) + 2^{*}\left(A_1B_2 + A_2B_1 + A_2B_3 + A_3B_2\right) + A_1B_3 + A_3B_1 \tag{23}$$

$$\mathrm{QCARRY} = 1^{*}\left(A_2B_2 + A_2B_3 + A_3B_2\right) + 2^{*}\left(A_3B_3\right) \tag{24}$$

The transient response of the proposed quaternary multiplier has been depicted in Fig. 21 with all possible combinations. The output of the proposed quaternary multiplier is consistent with its performance for inputs A and B.

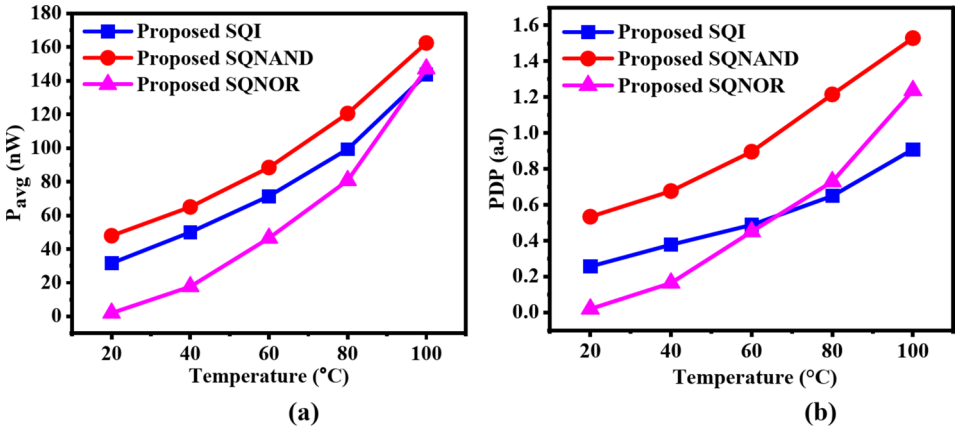

Fig. 14. Effect of variation in temperature for proposed quaternary logic gates in terms of **(a)** P_{avg}, **(b)** PDP.

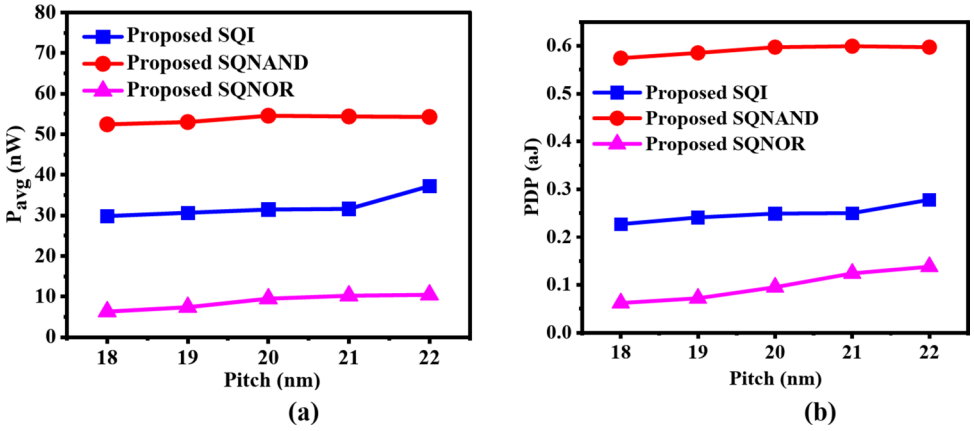

Fig. 15. Effect of variation in pitch for proposed quaternary logic gates in terms of **(a)** P_{avg}, **(b)** PDP.

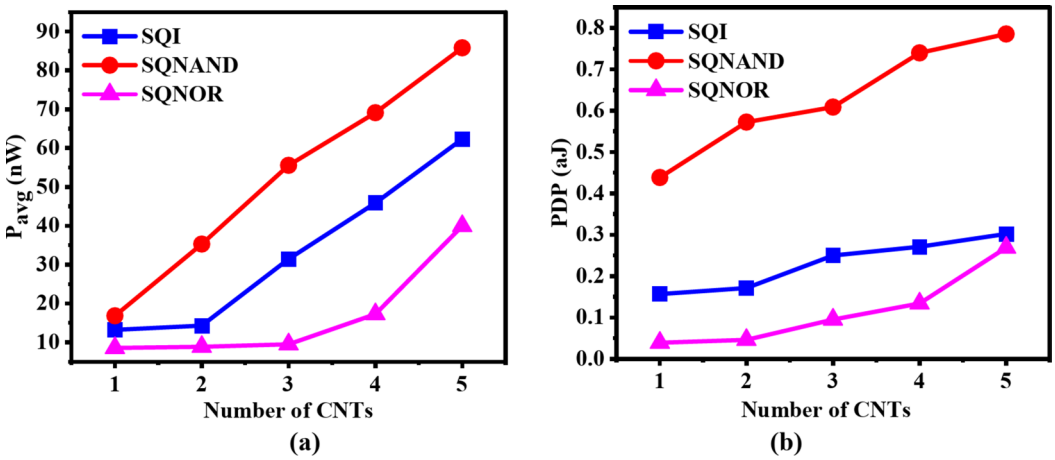

Fig. 16. Effect of variation in number of CNTs for proposed quaternary logic gates in terms of **(a)** P_{avg}, **(b)** PDP.

The performance parameters for the various quaternary multiplier circuits are shown in Table 11. A comparison has been made with literature. The FOM (PDP*No. of CNTFETs) has been adopted for a fair comparison of the proposed quaternary multiplier with earlier reported quaternary multipliers. The proposed multiplier circuit outperforms other multipliers in terms of P_{avg} and PDP. Besides this, FOM of the proposed

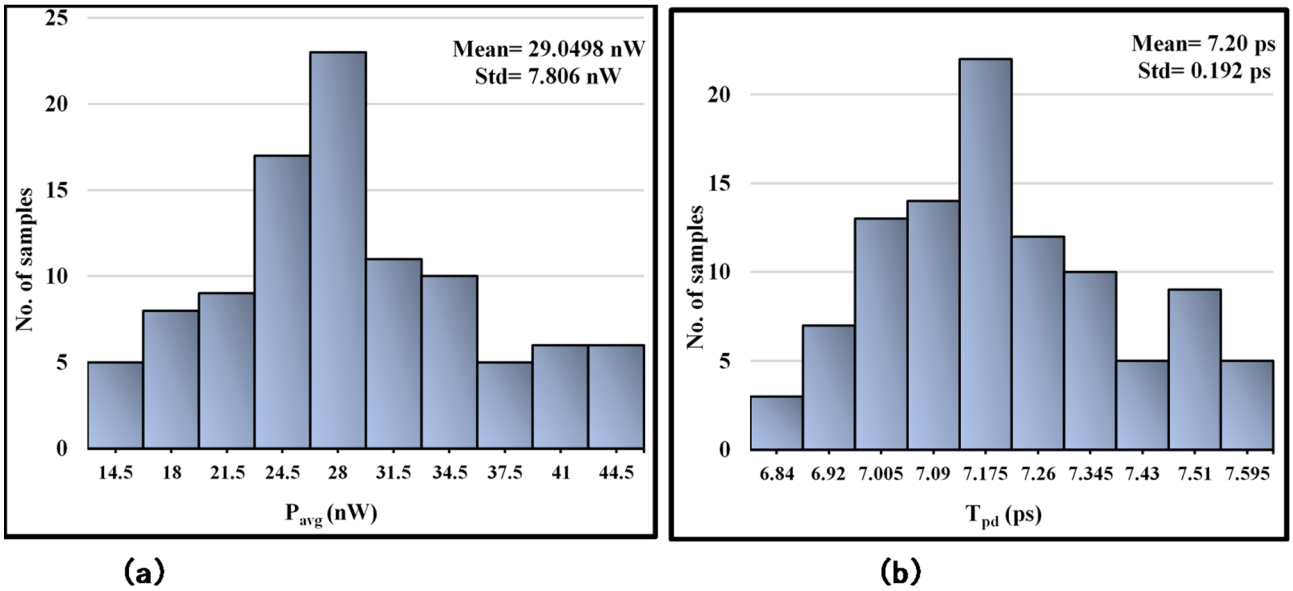

Fig. 17. MC simulation results for the proposed SQI design at V_{DD} = 0.9 V **(a)** P_{avg}, **(b)** T_{pd}.

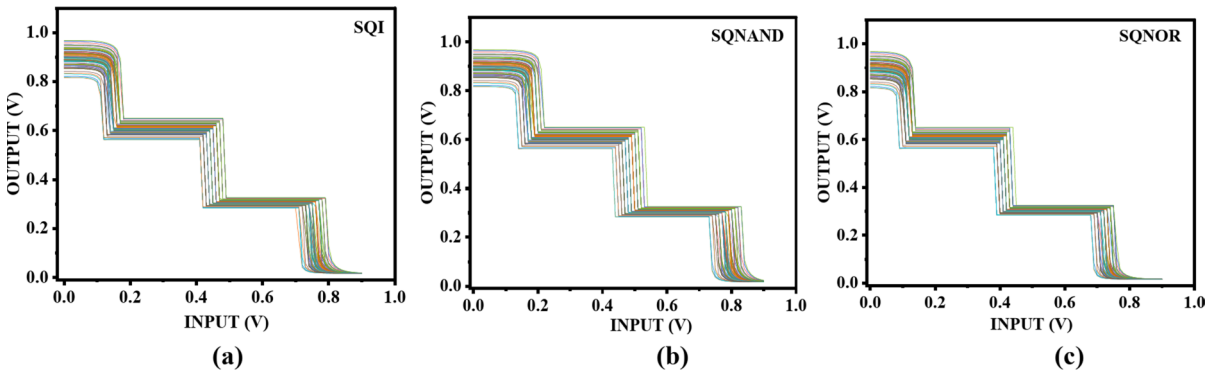

Fig. 18. Noise margin analysis of 100 iterations for **(a)** proposed SQI, **(b)** proposed SQNAND, **(c)** proposed SQNOR.

Ref.	P_{avg} (nW)	T_{pd} (ps)	NM (mV)	PDP (aJ)	EDP (10^{-30} Js)	Area (λ^2)	PDAP (aJ.λ^2)
SQI-1[27]	511.10	4.886	119.87	2.499	12.215	6438	16088.56
SQI-2[40]	315.63	8.217	133.06	2.593	21.312	13,158	34118.69
SQI-3[53]	97.983	9.088	120.78	0.776	7.052	7332	5689.63
SQI-4[30]	179.96	7.710	120.76	1.387	10.699	9612	13331.84
SQI-5[31]	36.034	9.373	122.19	0.337	3.165	14,250	4802.25
Proposed SQI	31.446	7.948	124.20	0.249	1.986	13,287	2988.24

Table 9. Performance evaluation of SQIs.

multiplier and[26] are better than other existing designs. This is evident that the proposed quaternary multiplier is a power efficient circuit. Table 12 demonstrates the number of devices and transistor count used to design the proposed quaternary multiplier.

Proposed half adder circuit

Another arithmetic circuit, the quaternary half adder (QHA) circuit, has been designed using the proposed SQNAND and SQNOR circuits as depicted in Figs. 22(a)-22(b). The building blocks for the proposed QHA

Ref.	P_{avg} (nW)	T_{pd} (ps)	NM (mV)	PDP (10^{-18} J)	EDP (10^{-30} Js)
SQNAND circuits					
SQNAND-1[27]	431.13	5.211	86.052	2.247	11.711
SQNAND-2[40]	331.50	7.943	95.723	2.633	20.915
SQNAND-3[30]	363.69	7.695	87.966	2.798	21.535
SQNAND-4[31]	116.97	16.831	122.27	1.968	33.136
Proposed SQNAND	54.557	10.945	91.690	0.597	6.535
SQNOR circuits					
SQNOR-1[27]	541.88	5.415	87.050	2.934	15.892
SQNOR-2[40]	437.55	12.044	96.722	5.270	63.475
SQNOR-3[30]	413.56	7.817	88.964	3.232	25.271
SQNOR-4[31]	42.510	15.566	121.19	0.661	10.30
Proposed SQNOR	9.476	10.507	95.534	0.562	1.046

Table 10. Performance evaluation of SQNAND and SQNOR gates.

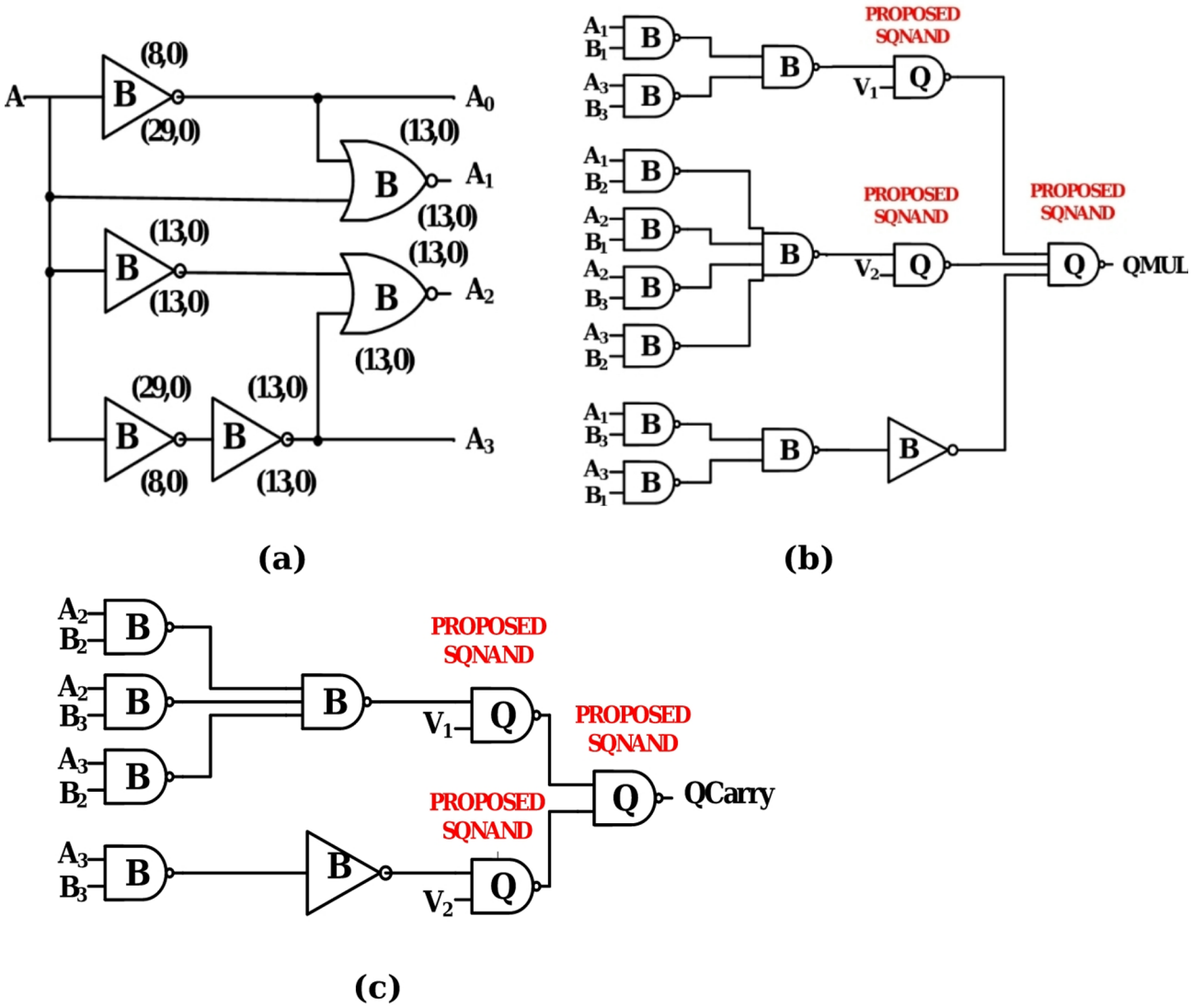

Fig. 19. Various blocks of quaternary multiplier: **(a)** quaternary-to-binary decoder[35], **(b)** product circuit[41], and **(c)** carry circuit[41].

A \ B	0	1	2	3
0	0	0	0	0
1	0	1	2	3
2	0	2	0	2
3	0	3	2	1

(a)

A \ B	0	1	2	3
0	0	0	0	0
1	0	0	0	0
2	0	0	1	1
3	0	0	1	2

(b)

Fig. 20. K-map for quaternary multiplier **(a)** product circuit, **(b)** carry circuit.

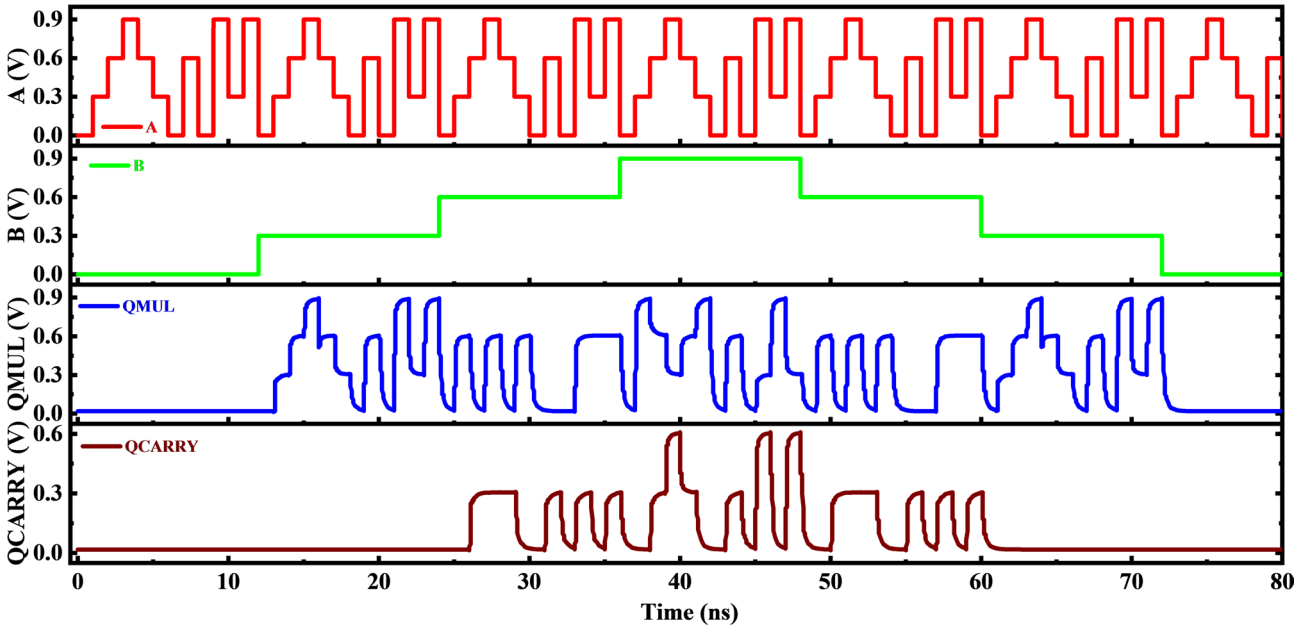

Fig. 21. Transient response for quaternary multiplier.

Ref.	P_{avg} (µW)	T_{pd} (ps)	PDP (aJ)	No. of CNTFETs	Supply count	Chiral vector	FOM (aJ)
[26]	5.379	21.928	117.95	94	3	(10,0), (19,0), (29,0)	11,088
[32]	20.36	31.137	633.94	122	1	(8,0), (10,0), (11,0), (19,0), (26,0), (29,0)	77,341
[41]	4.768	77.51	369.56	138	3	(10,0), (19,0), (29,0)	51,000
Proposed QMUL	**0.915**	106.67	**97.60**	**241**	**1**	**(8,0) (13,0) (29,0)**	**23,521**

Table 11. Performance evaluation of quaternary multipliers.

circuit are namely a voltage divider, quaternary to binary decoder, a sum circuit (refer to Fig. 22(a)), and a carry generator circuit (refer to Fig. 22(b)).

The structure utilized in[41] was employed to design sum and carry generating circuits for the proposed QHA. The outputs of the quaternary to binary decoder were used as inputs in the sum and carry generator circuit. The sum of two quaternary numbers is computed using the sum circuit, and the carry is produced at the output via the carry circuit. Figure 23 depicts the K-map for the sum and carry generating circuits of the proposed QHA.

The logic expression for sum and carry circuits of quaternary half adder obtained from Fig. 23 are expressed using Eqs. (25)-(26).

$$\mathrm{QSUM} = 1^{*}(A_0B_1 + A_1B_0 + A_2B_3 + A_3B_2) + 2^{*}(A_0B_2 + A_1B_1 + A_2B_0 + A_3B_3) + A_0B_3 + A_1B_2 + A_2B_1 + A_3B_0 \quad (25)$$

$$\mathrm{QCARRY} = 1^{*}(A_1B_3 + A_2B_2 + A_2B_3 + A_3B_2 + A_3B_3) \quad (26)$$

Devices	Number of devices	Transistor count	Subtotal of transistors
Voltage divider	1	3	3
Proposed SQNAND (2 inputs)	5	21	105
Proposed SQNAND (3 inputs)	1	27	27
Q2B decoder	2	16	32
Binary Inverter	2	2	4
Binary 2-NAND	14	4	56
Binary 3-NAND	1	6	6
Binary 4-NAND	1	8	8
Total	27	87	241

Table 12. Total transistor counts of the proposed quaternary multiplier.

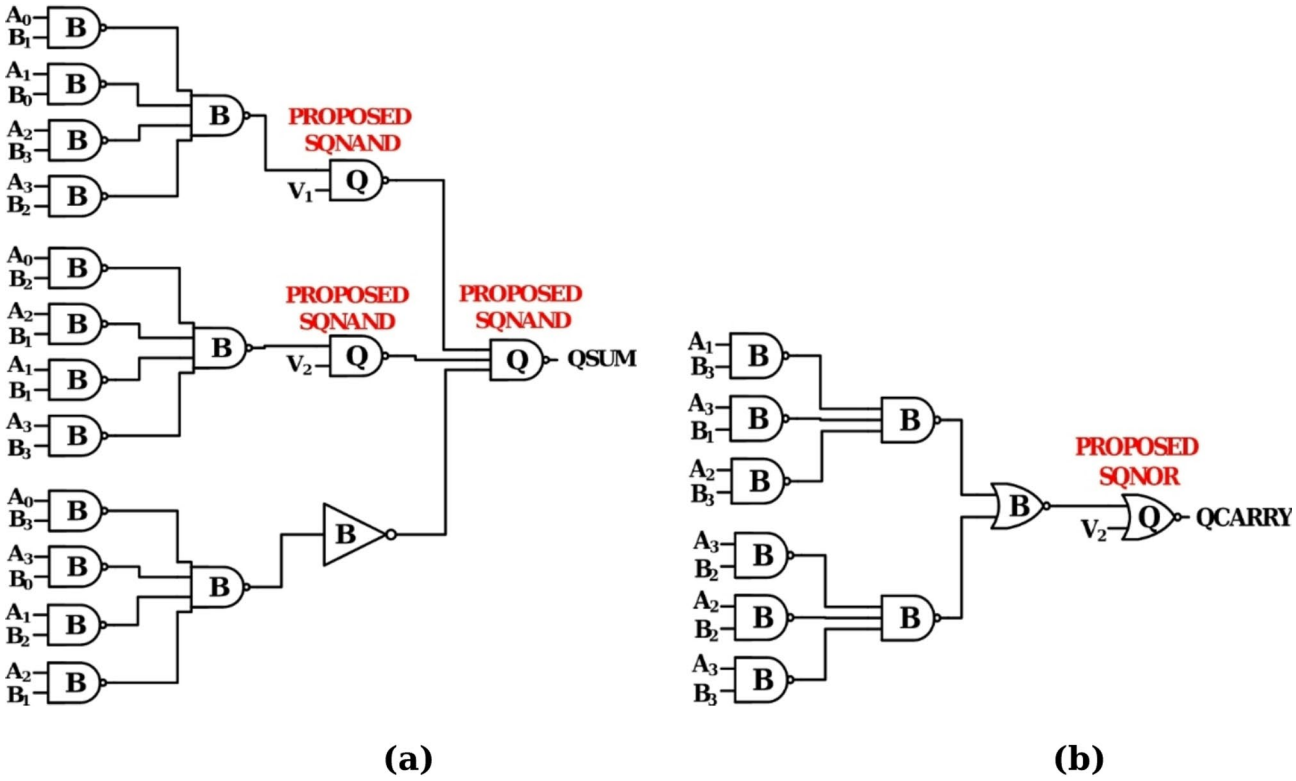

Fig. 22. Various blocks of quaternary half adder: **(a)** sum circuit[41], and **(b)** carry circuit[41].

The transient response for the proposed QHA has been depicted in Fig. 24, which validates the working operation for inputs A and B. The performance parameters for the various QHA circuits are shown in Table 13, which shows the improvement of the proposed QHA. Existing circuits require several power supplies, whereas the proposed circuits are designed using one power supply. Though the single supply voltage approach uses more number of voltage levels to achieve output logic levels, it offers numerous advantages over multiple supply voltage approach. First, it offers fewer number of interconnections, thereby reducing complexity and cost of production of the design. Second, it has only one source of short circuit dynamic power (occurring at logic level equal to half of V_{DD}) in contrast to multiple sources in case of multiple supply voltage approach[58]. The FOM (PDP* No. of CNTFETs) has been used to compare the proposed QHA to previously reported circuits. The proposed QHA circuit performs better in terms of P_{avg} and PDP. Aside from that, the FOM of the suggested half adder and[56] outperforms previous designs. It is clear that the proposed QHA is a power-efficient circuit. Table 14 shows the number of devices and transistors utilized to design the proposed QHA. The transistor counts for QMUL and QHA are 241 and 218 respectively. The proposed QMUL/QHA circuits can be used to design quaternary full adder (QFA) and quantum multiplier–accumulator (QMAC) as well as higher order adder and multiplier circuits as the manufacturing methodology using CNTFET devices has grown in recent years. One of the finest examples for the same is the work reported in[59], wherein a 16-bit microprocessor comprising more than 14,000 CNTFETs has been fabricated using industry-standard design flows and processes.

A \ B	0	1	2	3
0	0	1	2	3
1	1	2	3	0
2	2	3	0	1
3	3	0	1	2

(a)

A \ B	0	1	2	3
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1

(b)

Fig. 23. K map for quaternary half adder **(a)** sum circuit, **(b)** carry circuit.

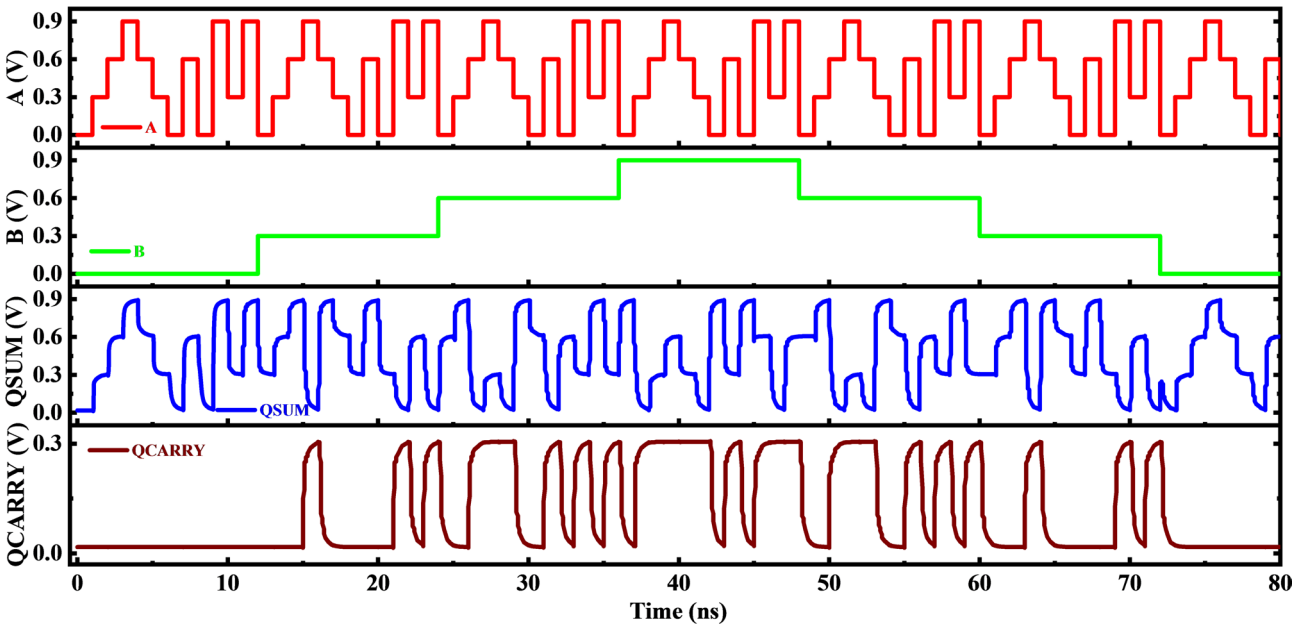

Fig. 24. Transient response for proposed quaternary half adder.

Conclusion

In this paper, novel designs of quaternary logic gates, viz., SQI, SQNAND, and SQNOR using CNTFET technology have been proposed. The proposed designs outperformed existing circuits in terms of average power consumption, PDP, and EDP. The proposed SQI exhibits 10.03, 10.41, 3.11, 5.57, and 1.35 times lower PDP than SQI-1, SQI-2, SQI-3, SQI-4, and SQI-5, respectively. Also, the EDP for the proposed SQI is 6.15, 10.73, 3.55, 5.38, and 1.59 times lower than SQI-1, SQI-2, SQI-3, SQI-4, and SQI-5, respectively. Similarly, the proposed designs of SQNAND and SQNOR gates performed better than existing designs in terms of PDP and EDP. Besides this, two combinational circuits, namely quaternary multiplier and quaternary half adder, have been designed using

Ref.	P_{avg} (µW)	T_{pd} (ps)	PDP (aJ)	No. of CNTFETs	Supply Count	Chiral vector	FOM (aJ)
[26]	5.882	20.573	121.01	214	3	(10,0), (19,0), (29,0)	25,897
[41]	5.518	80.61	444.80	188	3	(10,0), (19,0), (29,0)	83,622
[32]	11.20	38.075	426.44	161	2	(10,0), (19,0), (26,0), (29,0)	68,565
[56]	1.2163	81.217	98.782	73	3	(8,0), (13,0), (19,0), (29,0)	7211
Proposed QHA	**0.946**	**101.40**	**95.937**	**218**	**1**	**(8,0) (13,0) (29,0)**	**20,915**

Table 13. Performance evaluation of quaternary half adders.

Devices	Number of devices	Transistor count	Subtotal of transistors
Voltage divider	1	3	3
Proposed SQNAND (2 inputs)	2	21	42
Proposed SQNAND (3 inputs)	1	27	27
Q2B decoder	2	16	32
Binary Inverter	1	2	2
Binary 2-NOR	1	4	4
Binary 2-NAND	18	4	72
Binary 3-NAND	2	6	12
Binary 4-NAND	3	8	24
Total	31	91	218

Table 14. Total transistor counts of the proposed quaternary half adder.

proposed designs of SQNAND and SQNOR. The proposed quaternary multiplier and quaternary half adder provide superior performance in terms of average power consumption and PDP. The quaternary logic circuits proposed in this work are anticipated to improve the performance of computing devices.

Data availability

All data generated or analyzed during this study are included within this article.

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Declarations

Competing interests
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