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Dual-source 17/25-Level ANPC inverter with low stress on devices and reduced part count suitable for hybrid energy systems

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This paper proposes a unity-gain active-neutral-point-clamped (ANPC) multilevel inverter topology utilizing two DC sources, ten switches, and four DC-link capacitors. The proposed inverter generates 17 and 25 output voltage levels by leveraging input voltage ratios of $V_2 = 3V_1$ (triple) and $V_2 = 5V_1$ (quintuple), respectively. Unlike conventional designs, the topology eliminates the need for an H-bridge to produce bipolar voltage waveforms, thereby reducing the number of switches exposed to the maximum output voltage from four (in H-bridge-based structures) to two. Additionally, the inverter supports diverse load types across a wide range of power factors. Comparative analysis demonstrates that the proposed topology achieves the lowest number of conducting switches (only three) to generate any output voltage level, minimizing voltage drop, device losses, and conduction losses while enhancing overall efficiency and output voltage quality. Furthermore, it requires fewer DC sources and switches compared to existing 25-level inverters. Experimental results from a laboratory-scale prototype validate the effective operation of the proposed ANPC inverter in both 17- and 25-level configurations.

The growing demand for high-efficiency, high-quality power conversion in renewable energy systems, electric vehicles, and industrial drives has propelled the advancement of multilevel inverter (MLI) technologies[1,2]. Multilevel inverters are distinguished by their ability to synthesize staircase voltage waveforms, significantly reducing total harmonic distortion (THD) and electromagnetic interference compared to conventional two-level inverters. Traditional MLI topologies—such as neutral-point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) designs—have laid the foundation for high-power applications. However, these architectures often suffer from high component counts, complex voltage balancing requirements, and elevated voltage stress on switching devices, which escalate costs, control complexity, and reliability concerns[3].

Recent researches have focused on improved MLI configurations to mitigate these challenges by optimizing the trade-off between part count, voltage stress, and output quality. Innovations such as switched-capacitor networks, asymmetric DC source arrangements, and advanced modulation strategies have demonstrated promising results in reducing component numbers and improving efficiency[4–6]. Nevertheless, many existing solutions still face limitations in scalability, device stress, or dependency on numerous isolated DC sources, which constrain their practicality in cost-sensitive applications[7]. The switched-capacitor based MLIs suffer from impulsive charging/discharging current of capacitors, which may damage the on-path semiconductors and reduce the lifespan of capacitors. The soft-charging cells are usually adopted to overcome this issue[8,9]. Using DC-link capacitors in MLIs can simultaneously reduce the number of DC sources and increase the number of levels, but in expense of losing voltage boosting ability. An asymmetric MLI with four DC sources, four DC-link capacitors, ten switches, and 14 MOSFETs is presented in[10] that provides 35 voltage levels, where two switches are exposed to a voltage stress higher than peak output voltage ($V_{o,max}$). Furthermore, another two switches have to withstand a voltage stress equal to $V_{o,max}$, which leads to a high total voltage stress. The total summation of input sources is less than the maximum output voltage, which means that the converter operates as a step-down converter. A unity-gain 17-level inverter is presented in[11] that is consisted of three DC sources, two DC-link capacitors, nine switches and ten MOSFETs, where the voltage stress of all switches is less than the $V_{o,max}$. An

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asymmetric unity-gain dual source 11-level inverter is presented in[12] that is composed of two DC sources, two DC-link capacitors, seven switches, and eight MOSFETs, where only two switches have to block a voltage stress of equal $V_{o, max}$. In[13], a generalized DC-link capacitors based multilevel inverter topology is proposed, which in its basic form utilizes four switches to create the desired voltage levels. In this structure, two half-bridges have been used for bipolar voltage waveform generation, where none of the switches has to withstand the voltage stress of $V_{o, max}$. In[14], a 13-level inverter topology is presented, in which three DC-link capacitors and a switched-capacitor have been utilized. The voltage balancing between the three DC-link capacitors is the main challenge of this topology that requires complicated control techniques. In[15,16] two similar unity-gain 9-level inverter topologies are presented that differ only at realization of bidirectional switches. Both topologies combine two DC-link capacitors with two switched-capacitors, where only two switches are exposed to a voltage stress of equal to $V_{o, max}$. Two 7-level inverter topologies are presented in[17,18] that use two DC-link capacitors with two switched-capacitors to provide a voltage boosting factor of 1.5, while none of the semiconductors has to block the voltage stress of $V_{o, max}$. Another 7-level inverter topology composed of nine switches, two DC-link capacitors and a switched-capacitor is presented in[19] that provides a voltage gain of 1.5. The voltage stress of all switches is less than the $V_{o, max}$. The detailed comparative analysis on similar existed 17- and 25-level ANPC topologies (presented in[20-35] has been provided in Sect. 4. Another ANPC structure is presented in[36] that employs two DC sources, ten switches, four diodes and two switched-capacitors to provide nine output voltage levels with unity gain. In[37] a five-level ANPC is presented that utilizes single DC source, nine switches, two diodes, two DC-link capacitors, a single switched-capacitor and an impulsive charging current limiter inductor. While suppressing capacitor's impulsive charging current, it provides 1.5 boosting factor. A seven-level ANPC is presented in[38], which utilizes single DC source, seven switches, six diodes, two DC-link capacitor and two switched-capcitors to provide boosting factor of 1.5. Despite the extensive progress on dual-source and capacitor-based multilevel inverters, most existing topologies still suffer from one or more limitations, including the requirement of a high number of isolated DC sources, reliance on an H-bridge that increases device stress, a large number of conducting switches per level, and the inability to naturally balance capacitor voltages. These challenges increase the overall cost, complexity, and reduce the efficiency of the system, particularly in renewable and hybrid energy applications where compactness and reliability are critical.

To address these issues, this paper proposes a dual-source multi-level inverter architecture that can provide 17- or 25-level output voltages, depending on the magnitude of input DC sources. It requires only three conducting switches per voltage level, and ensures natural capacitor voltage balancing. The significance of generating up to 25 levels lies in achieving superior waveform quality, lower THD, reduced EMI, and higher efficiency, which are critical for demanding high-performance power conversion applications. The operation of the proposed inverter relies on asymmetric input voltage ratios: $V_2 = 3V_1$ for 17-level and $V_2 = 5V_1$ for 25-level operation. These ratios are essential because they ensure that all voltage steps are unique and equally spaced. If the input voltages deviate from the designed ratios, the inverter will still function, but some output levels may merge or become unevenly spaced, leading to fewer distinct voltage levels and slightly degraded harmonic performance.The proposed inverter has H-bridge free structure, where only two (instead of four) switches have to tolerate a voltage stress of $V_{o, max}$. This reduction in voltage stress not only enhances efficiency and thermal performance but also permits the use of lower-rated, cost-effective semiconductor devices. Furthermore, another key advantage is that only three switches is required to be on to generate any desired voltage level, which leads to lower voltage drop on devices and higher achievable output voltage on the load. The combination of H-bridge elimination, reduced conduction path, dual-level scalability without additional devices, and verified high efficiency distinguishes the proposed topology from previously reported dual-source inverters. The proposed design can flexibly generate both 17 and 25 output levels with unity gain using the same hardware, achieving high efficiency with fewer components compared to conventional approaches. 17 level version may be chosen when a small filter is acceptable and overall bill-of-materials/efficiency are prioritized. Also, when filter minimization and power-quality/EMI margins dominate, 25 level version is chosen. Since the proposed desin supports both 17 and 25 levels without adding parts, the level selection can be made at deployment to minimize total cost (inverter + filter) for the same THD and rated power.

The remainder of this paper is organized as follows: Sect. 2 details the configuration and operational principles of the proposed dual-source inverter. Section 3 presents the Nearest Level modulation strategy. Section 4 provides the results of comparative analysis. Section 5 validates the topology through experimental results, including efficiency analysis and THD performance. Finally, Sect. 6 concludes the study.

2. Proposed multilevel inverter
2.1 Configuration
Figure 1 shows the proposed double-input active neutral-point clamped multilevel inverter, which utilizes two DC supplies, ten power switches (6 unidirectional and 4 bidirectional) and four DC-link capacitors, as (1).

$$N_{DC} = 2, \ N_S = N_{GD} = 10, \ N_M = 14, \ N_C = 4, \ N_D = 0 \tag{1}$$

Based on the magnitude of DC sources, the proposed inverter can generate 17 or 25 voltage levels. For ternary-ordered magnitude of DC sources ($V_2 = 3V_1$), the proposed inverter can provide 17 voltage levels, while for quinary-ordered inputs ($V_2 = 5V_1$) it can produce 25 voltage levels. The proposed inverter does not require any diode, which enables it to supply variety of load types from zero to unity power factors. Regardless of the number of generated levels, there exists only three conducting semiconductors on current flow path.
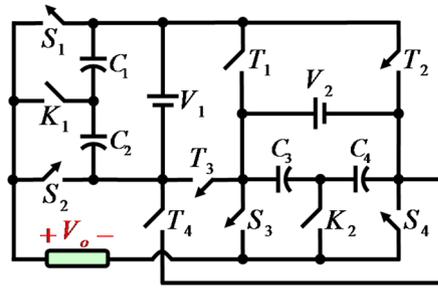
Fig. 1. Proposed ANPC multilevel inverter.

State	$S_1S_2S_3S_4K_1K_2T_1T_2T_3T_4$	V_o
1	1,010,001,000	0
	0101000001	
2	0001100001	V_{dc}
3	1,001,000,001	$2V_{dc}$
4	1,000,011,000	$3V_{dc}$
5	0101001000	$4V_{dc}$
6	1,000,010,010	$5V_{dc}$
7	1,001,001,000	$6V_{dc}$
8	0001100010	$7V_{dc}$
9	1,001,000,010	$8V_{dc}$
10	0010101000	$-1V_{dc}$
11	0110001000	$-2V_{dc}$
12	0100010001	$-3V_{dc}$
13	1,010,000,001	$-4V_{dc}$
14	0100010100	$-5V_{dc}$
15	0110000001	$-6V_{dc}$
16	0010100100	$-7V_{dc}$
17	0110000100	$-8V_{dc}$

Table 1. Switching scheme of proposed 17-level inverter.

2.2 Operational modes and switching schemes
2.2.1 17-Level version
In order to generate 17 voltage levels at the output, the magnitude of DC sources should be selected as (2).

$$V_2 = 3\,V_1 = 6\,V_{dc} \tag{2}$$

Since two DC-link capacitors are paralleled with each input, the voltage of each capacitor is naturally balanced to half of the input voltage, as shown in (3).

$$V_{C_1} = V_{C_2} = \frac{V_1}{2} = V_{dc}, \ V_{C_3} = V_{C_4} = \frac{V_2}{2} = 3\,V_{dc} \tag{3}$$

Table 1 shows the switching scheme of proposed 17-level inverter, where "1" and "0" denotes the "on" and "off" states, respectively.

For clear understanding, the equivalent circuits of proposed 17-level inverter at different operational states has been shown in Fig. 2. As seen from Table 1; Fig. 2, the proposed inverter successfully generates 8 positive, 8 negative and a zero voltage-level (0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, $\pm 5V_{dc}$, $\pm 6V_{dc}$, $\pm 7V_{dc}$, $\pm 8V_{dc}$), with maximum output voltage of $8V_{dc}$, while $V_2 = 3V_1 = 6V_{dc}$. Also, it is observed that at each state, there exists a path for both the positive and negative load current, which enables the proposed converter to feed the variety of loads from zero to unity power factor.

Table 2 shows the voltage stress (in per-unit) of switches in proposed 17-level inverter. As seen, only two switches (T_2, T_3) have to tolerate the voltage stress of equal to maximum output voltage ($V_{o,\,max}$), while the voltage stress of other switches is much lower than the $V_{o,\,max}$. The total voltage stress of proposed 17-level inverter is $48V_{dc}$ (6 per-unit).
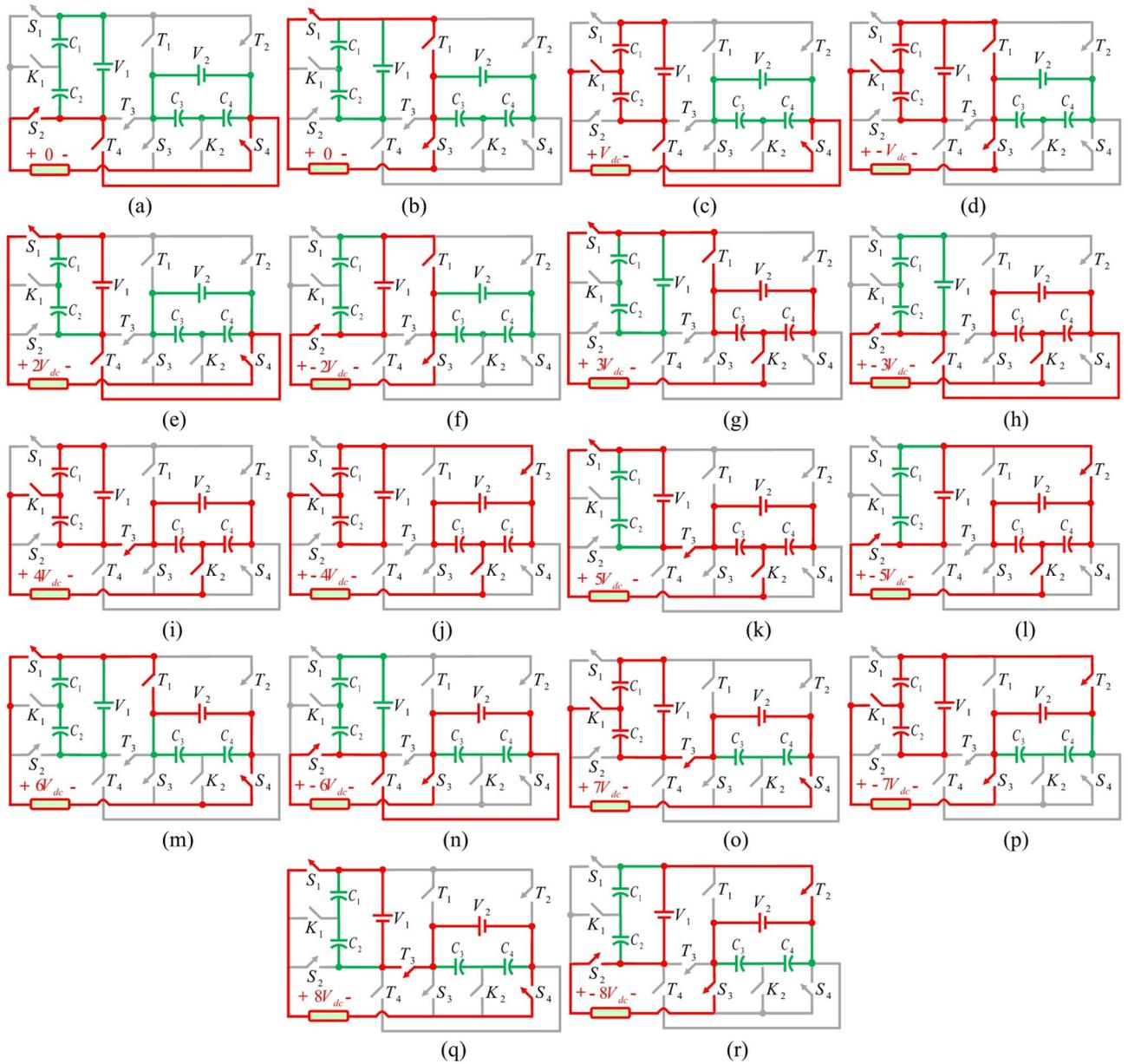
Fig. 2. Equivalent circuits of proposed inverter (17-level version, $V_2 = 3V_1 = 6V_{dc}$) during different voltage levels.

Switch	Voltage stress Value	Per-unit	Switch	Voltage stress Value	Per-unit
S_1	$2V_{dc} = 0.25V_{o,max}$	0.25	K_2	$3V_{dc} = 0.375V_{o,max}$	0.375
S_2	$2V_{dc} = 0.25V_{o,max}$	0.25	T_1	$6V_{dc} = 0.75V_{o,max}$	0.75
S_3	$6V_{dc} = 0.75V_{o,max}$	0.75	T_2	$8V_{dc} = V_{o,max}$	1
S_4	$6V_{dc} = 0.75V_{o,max}$	0.75	T_3	$8V_{dc} = V_{o,max}$	1
K_1	$V_{dc} = 0.125V_{o,max}$	0.125	T_4	$6V_{dc} = 0.75V_{o,max}$	0.75
Total voltage stress (TVS)			Value		$48V_{dc}$
			Per unit		6

Table 2. Voltage stress of switches in proposed 17-level inverter.

2.2.1 25-Level version

The number of voltage levels in proposed inverter can be enhanced to 25 voltage-levels, without any additional part, only by choosing the magnitude of input DC sources as (4).

$$V_2 = 5\,V_1 = 10\,V_{dc} \tag{4}$$

Accordingly, the voltage of C_1-C_4 capacitors is naturally regulated as (5).

$$V_{C_1} = V_{C_2} = \frac{V_1}{2} = V_{dc}, \ V_{C_3} = V_{C_4} = \frac{V_2}{2} = 5\,V_{dc} \tag{5}$$

Table 3 shows the switching pattern of proposed inverter at its 25-level version. The equivalent circuits have also been presented in Fig. 3. As seen, the proposed inverter can produce 25 voltage levels, including 12 positive, 12 negative and one zero level, with peak value of $V_{o,\ max}=12V_{dc}$, where $V_2=5V_1=10V_{dc}$. Table 4 shows the voltage stress of switches at proposed 25-level inverter.

At 25-level version, similar to 17-level version, only two switches (T_2, T_3) have to withstand the voltage stress of equal to peak output voltage. The total voltage stress on switches is equal to $74V_{dc}$ (6.167 per-unit).

3. Nearest-level modulation method

In this study, the Nearest-Level Method (NLM) has been used for generating switching pulses of switches. The NLM has been chosen because it offers the best balance of simplicity, low switching loss, and excellent THD performance for a high-level inverter. In contrast, other techniques like Selective Harmonic Elimination (SHE) and SPWM are more suited for low-level converters where harmonic elimination or carrier-based shaping is critical. For theproposed 17/25-level inverter, NLM achieves near-optimal output quality with minimal control complexity and maximum efficiency. The NLM technique operates by selecting the nearest available voltage level to the reference waveform at each sampling instant. In this technique, a sinusoidal reference waveform (v_{Ref}) is generated with the desired amplitude (V_{Ref}) and frequency (f_{Ref}=50 Hz), as shown in (6).

$$v_{Ref} = V_{Ref}\,\mathrm{Sin}(2\pi f_{Ref}) \tag{6}$$

The valid range for V_{Ref} is $[0-(M_a{\times}V_{o,\ max})]$, where the modulation index (M_a) is defined as (7).

$$M_a = V_{Ref}/V_o\mathrm{,max} \tag{7}$$

State	$S_1S_2S_3S_4K_1K_2T_1T_2T_3T_4$	V_o
1	1,010,001,000 0101000001	0
2	0001100001	$1V_{dc}$
3	1,001,000,001	$2V_{dc}$
4	0100011000	$3V_{dc}$
5	0000111000	$4V_{dc}$
6	1,000,011,000	$5V_{dc}$
7	0000110010	$6V_{dc}$
8	1,000,010,010	$7V_{dc}$
9	0101001000	$8V_{dc}$
10	0001101000	$9V_{dc}$
11	1,001,001,000	$10V_{dc}$
12	0001100010	$11V_{dc}$
13	1,001,000,010	$12V_{dc}$
14	0000101000	$-1V_{dc}$
15	0101000100	$-2V_{dc}$
16	1,000,010,001	$-3V_{dc}$
17	0000110001	$-4V_{dc}$
18	0100010001	$-5V_{dc}$
19	0000110100	$-6V_{dc}$
20	0100010100	$-7V_{dc}$
21	1,010,000,001	$-8V_{dc}$
22	0010100001	$-9V_{dc}$
23	0110000001	$-10V_{dc}$
24	0010100100	$-11V_{dc}$
25	0110000100	$-12V_{dc}$

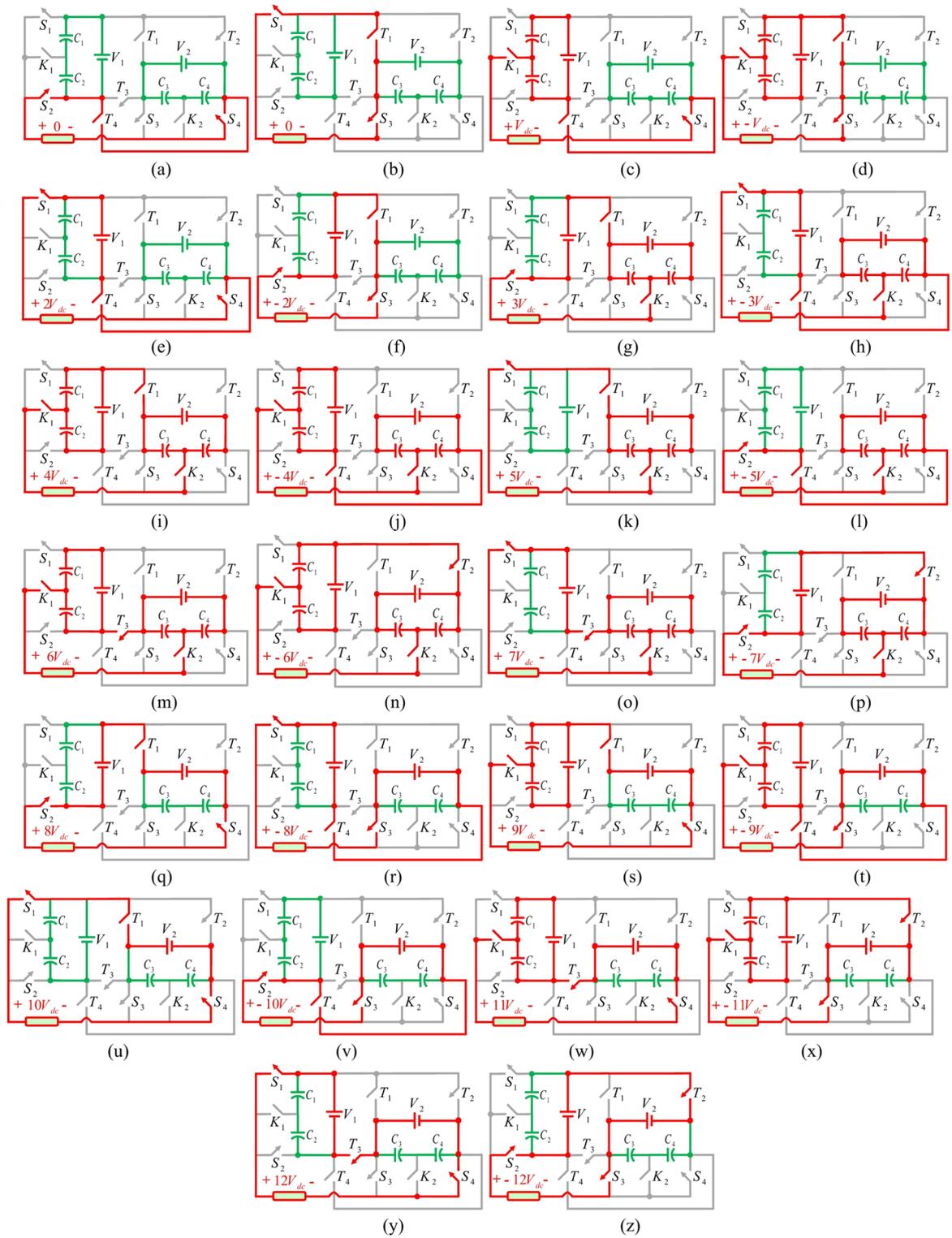**Table 3**. Switching scheme of proposed 25-level inverter.

Fig. 3. Equivalent circuits of proposed inverter (25-level version, $V_2 = 5V_1 = 10V_{dc}$) during different voltage levels.

At each sampling instant, the reference value is compared with the available voltage levels, and the nearest level is selected, which is translated into appropriate switching signals for the inverter's switching devices. The simplicity of NLM lies in its straightforward level selection process, which eliminates the need for complex calculations or carrier-based modulation schemes. Furthermore, the NLM technique demonstrates lower switching losses compared to PWM based modulation techniques. Figure 4 depicts the implemented of NLM on the proposed

| Switch | Voltage stress | | Switch | Voltage stress | |
	Value	Per-unit		Value	Per-unit
S_1	$2V_{dc}=0.17V_{o,\,max}$	0.17	K_2	$5V_{dc}=0.417V_{o,\,max}$	0.417
S_2	$2V_{dc}=0.17V_{o,\,max}$	0.17	T_1	$10V_{dc}=0.83V_{o,\,max}$	0.83
S_3	$10V_{dc}=0.83V_{o,\,max}$	0.83	T_2	$12V_{dc}=V_{o,\,max}$	1
S_4	$10V_{dc}=0.83V_{o,\,max}$	0.83	T_3	$12V_{dc}=V_{o,\,max}$	1
K_1	$V_{dc}=0.083V_{o,\,max}$	0.083	T_4	$10V_{dc}=0.83V_{o,\,max}$	0.83
Total voltage stress (TVS)			Value		$74V_{dc}$
			Per unit		6.167

Table 4. Voltage stress of switches in proposed 25-level inverter.
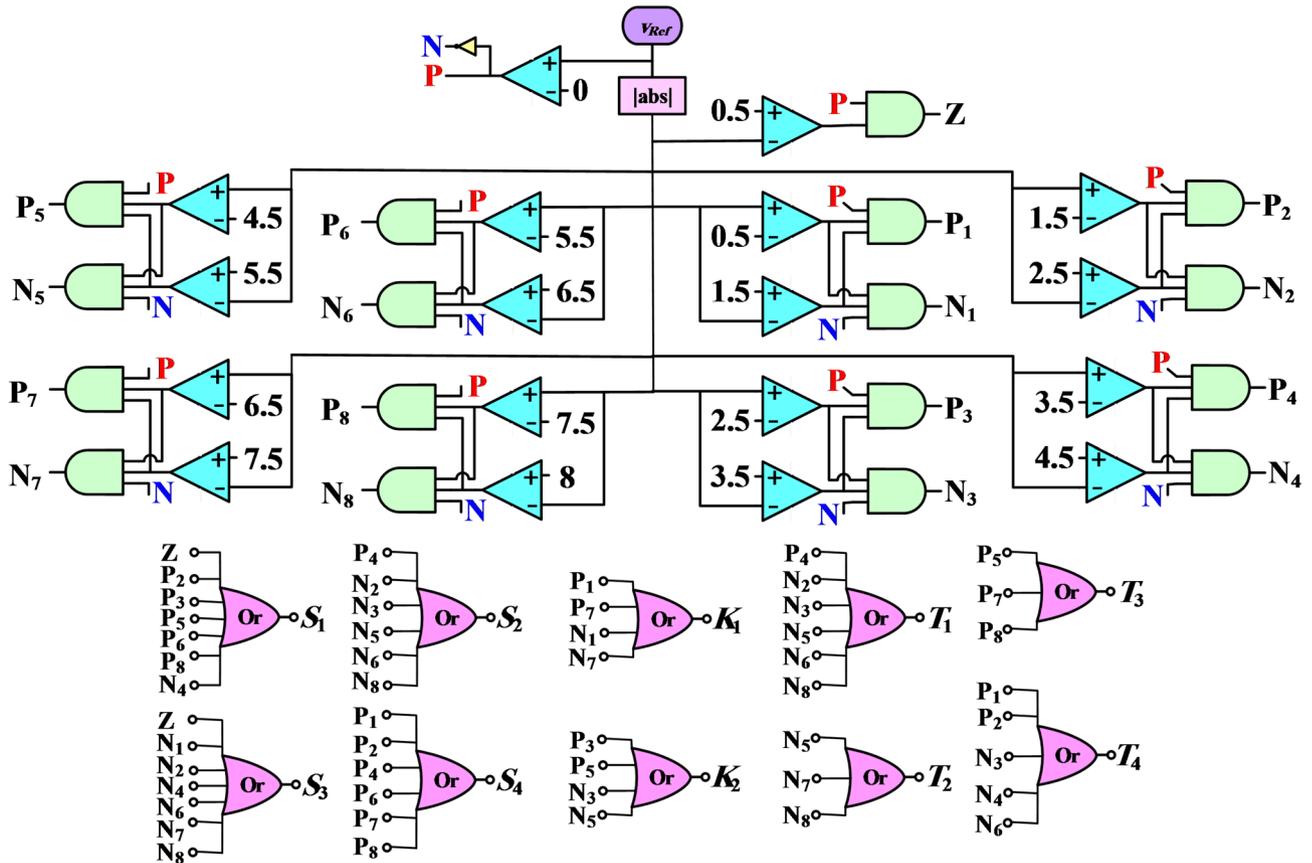
Fig. 4. Implementation of NLM on the proposed 17-level ANPC inverter.

17-level ANPC inverter through logic circuits. The logic circuit shown in Fig. 4 can be further extended to accommodate the 25-level configuration.

4. Comparative analysis

In this section, comparative analysis is performed between the proposed 17/25-level inverter and its similar counterparts presented in[20–35], from viewpoints of number of levels (N_L), DC sources (N_{DC}), switches (N_S), MOSFETs (N_M), capacitors (N_C), diodes (N_D), gain, maximum number of conducting semiconductors (NCS), total voltage stress (TVS), maximum voltage stress (MVS), number of semiconductors tolerating maximum output voltage (NSMOV), cost factor (CF), and the capability of feeding the inductive loads (ILFC).

Table 5 summarizes the comparison results. The mathematical definition of TVS_{pu}, MVS_{pu} and gain have been shown in (8).

$$TVS_{Pu}=\frac{TVS}{V_{o,\max}},\; MVS_{pu}=\frac{MVS}{V_{o,\max}},\; Gain=\frac{V_{o,\max}}{\sum_{i=1}^{n}V_i} \tag{8}$$

Topology	N_L	N_{DC}	N_S	N_M	N_C	N_D	Gain	MCS	TVS $\times V_{dc}$	TVS Pu	MVS$_{pu}$	NSMOV	CF $\alpha=0.5$	CF $\alpha=1.5$	ILFC
[20]	17	4	10	10	0	0	1	5	36	4.5	1	2	2.8824	3.9412	Y
[21]	17	4	9	12	0	0	1	3	40	5	1	2	2.7059	3.8824	Y
[22]	17	4	8	10	0	0	1	3	36	4.5	1	2	2.4118	3.4706	Y
[23]	17	4	10	12	0	0	1	4	44	5.5	1	2	3	4.2941	Y
[24]	17	4	10	10	0	0	1	5	32	4	0.75	–	2.8235	3.7647	Y
[25]	17	4	8	10	0	0	1	3	36	4.5	1	2	2.4118	3.4706	Y
[22]	17	4	14	16	4	0	1	6	34	4.25	0.5	0	4.7353	5.7353	Y
[27]	17	4	9	10	0	0	1	4	33	4.125	0.75	0	2.6029	3.5735	Y
[28]	17	2	9	12	4	0	1	3	27	3.375	0.625	0	1.7279	2.1250	Y
Proposed	17	2	10	14	4	0	1	3	48	6	1	2	2	2.7059	Y
[29]	25	2	10	10	4	8	1	4	54	4.5	0.833	0	1.94	2.3	Y
[30]	25	2	10	10	4	16	1	3	70	5.83	1	2	2.6332	3.0996	Y
[31]	25	4	10	12	0	0	1	4	54	4.5	0.833	0	1.96	2.68	Y
[32]	25	4	10	12	0	0	1	4	54	4.5	0.833	0	1.96	2.68	Y
[33]	25	4	16	20	8	–	1	6	56	4.667	0.5	0	4.2134	4.9601	Y
[34]	25	4	12	12	0	0	1	6	60	5	0.833	0	2.32	3.12	Y
[35]	25	7	12	18	0	0	0.923	3	92	7.66	1	2	4.4324	6.5772	Y
Proposed	25	2	10	14	4	0	1	3	74	6.167	1	2	1.3667	1.86	Y

Table 5. Comparison Results.
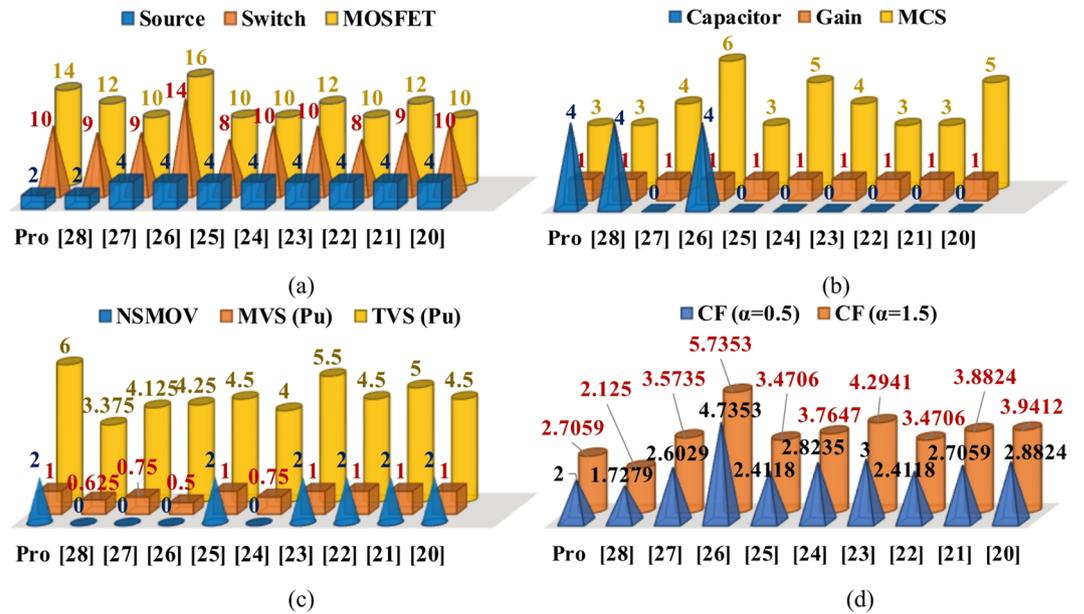
Fig. 5. Comparison results for 17-level topologies, (**a**) N_{DC}, N_S, N_M, (**b**) N_C, Gain, MCS, (**c**) TVS (*Pu*), MVS (*Pu*), NSMOV, (**d**) CF ($\alpha=0.5$), CF ($\alpha=1.5$).

Also, in literature, different definitions have been proposed for the Cost Function (CF). In this study, the commonly used definition, shown in (9) has been employed, which is the most comprehensive definition, containing as much as possible effective parameters.

$$CF = \frac{(N_S + N_C + N_D + (\alpha \times TVS_{Pu})) \times N_{DC}}{N_L} \tag{9}$$

Figures 5 and 6 serve as graphical evidence of the comparative analysis. While Table 5 provides numerical values, Figs. 5 and 6 make the contribution of the work more transparent and accessible.
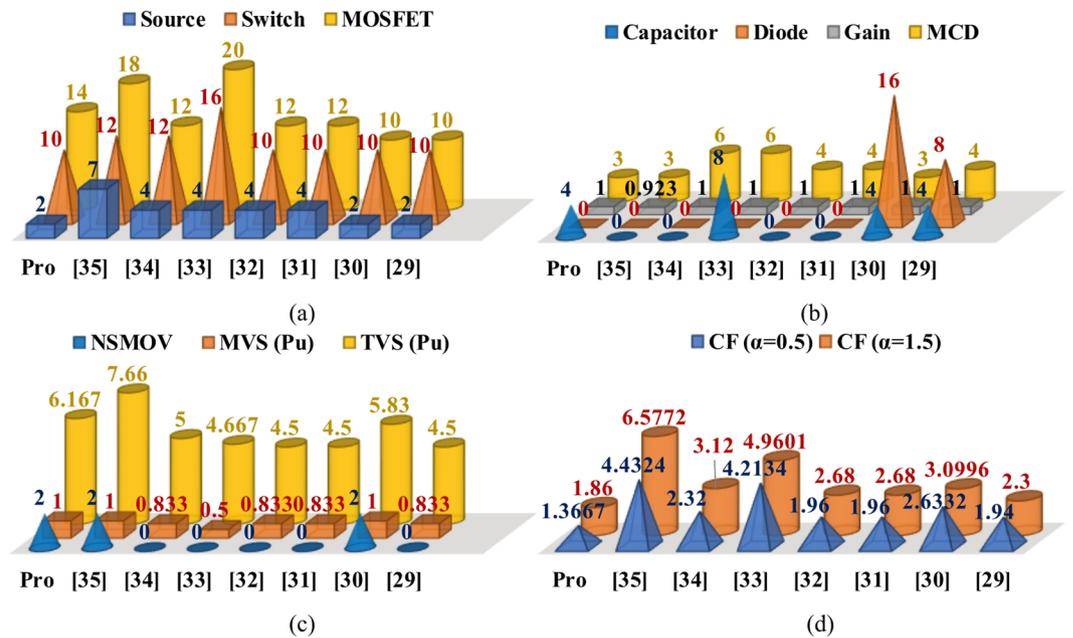
Fig. 6. Comparison results for 25-level topologies, (**a**) N_{DC}, N_S, N_M, (**b**) N_C, N_D, Gain, MCS, (**c**) TVS (*Pu*), MVS (*Pu*), NSMOV, (**d**) CF ($\alpha = 0.5$), CF ($\alpha = 1.5$).

4.1 17-Level topologies

According to Table 5; Fig. 5(a), the proposed 17-level topology and[28] require only 2 DC sources, while all other converters utilize 4 DC sources. The reduced count of sources dramatically reduces the total size, mass and cost of converter. The number of switches employed in the proposed topology is 10, which is equal to or fewer than that of[20,23,24,26]. None of the converters use the diodes. The proposed topology and[26,28] use 4 capacitor, while the other structures are capacitor-free structures. The proposed converter and all the considered 17-level converters provide unity voltage gain, where the maximum output voltage is equal to the summation of input voltage sources. As seen from Fig. 5(b), the proposed converter and[21,22,25,28] employ minimum number of switches (only 3 switches) to generate each voltage level, which may lead to lower voltage drop and losses. According to Fig. 5(c), the TVS in proposed converter is higher than the others. Also, the two switches in proposed topology and[20–23,25] have to withstand a voltage stress of $V_{o,max}$. The maximum voltage stress on semiconductors of[24,26–28] is less than the $V_{o,max}$. In this study, the cost analysis has been repeated for two different weighting factors of TVS, $\alpha = 0.5$ and $\alpha = 1.5$. According to Fig. 5(d), for both $\alpha = 0.5$ and $\alpha = 1.5$, the proposed topology provides the second least CF value. All the considered converters are able to successfully feed the inductive loads with variety of power factors. The proposed topology is superior to[20] in terms of reduced DC source requirement, fewer conduction switches, H-bridge elimination, and scalability to 25 levels, making it more efficient, cost-effective, and versatile for practical high-performance power conversion.

4.1 25-Level topologies

According to Fig. 6(a), the proposed topology and[29,30] utilize only 2 DC sources to provide 25 voltage levels at the output, which is fewer than the other structures. Furthermore, the proposed topology requires only 10 switches, which is equal to or fewer than that of other topologies. The number of MOSFETs in proposed topology is 14, which is fewer than that of[33,35]. Based on Fig. 6(b), the proposed topology and[29,30] require 4 capacitors to generate 25 voltage levels, while this amount for[33] is 8. The other converters are capacitor-free structures. The topologies presented in[29] and[30] respectively use 8 and 16 diodes, while the proposed topology and the other ones are diode-free structures. Among considered structures, the converter presented in[35] operates as a step-down converter (the maximum output voltage is less than the summation of all input sources), while the proposed topology and the other structures provide unity-gain. During generation of any voltage level in proposed topology, only 3 semiconductors are in conducting state, which is equal to or fewer than that of other structures.

According to Fig. 6(c), the two switches in proposed topology have to tolerate a voltage stress of $V_{o,max}$. The topology presented in[35] has the highest total voltage stress (in per-unit). The second highest TVS belongs to the proposed topology, which is considered as its main drawback. According to Fig. 6(d), the proposed topology provides the least CF for both weighting factors of $\alpha = 0.5$ and $\alpha = 1.5$. Here again, all the considered topologies are capable of feeding inductive loads with variety of power factors. The[28] is limited to 17 levels only, while the proposed design can flexibly operate at both 17- and 25-level configurations using the same hardware, simply by changing the input DC voltage ratio. This scalability is not possible in[28]. Furthermore, the proposed 25-level inverter achieves a significantly higher ratio of number of levels to the number of DC sources, switches, MOSFETs and capacitors, meaning it generates more levels per device. This indicates a more efficient utilization of components and highlights the practicality of the proposed design for high-quality power conversion with
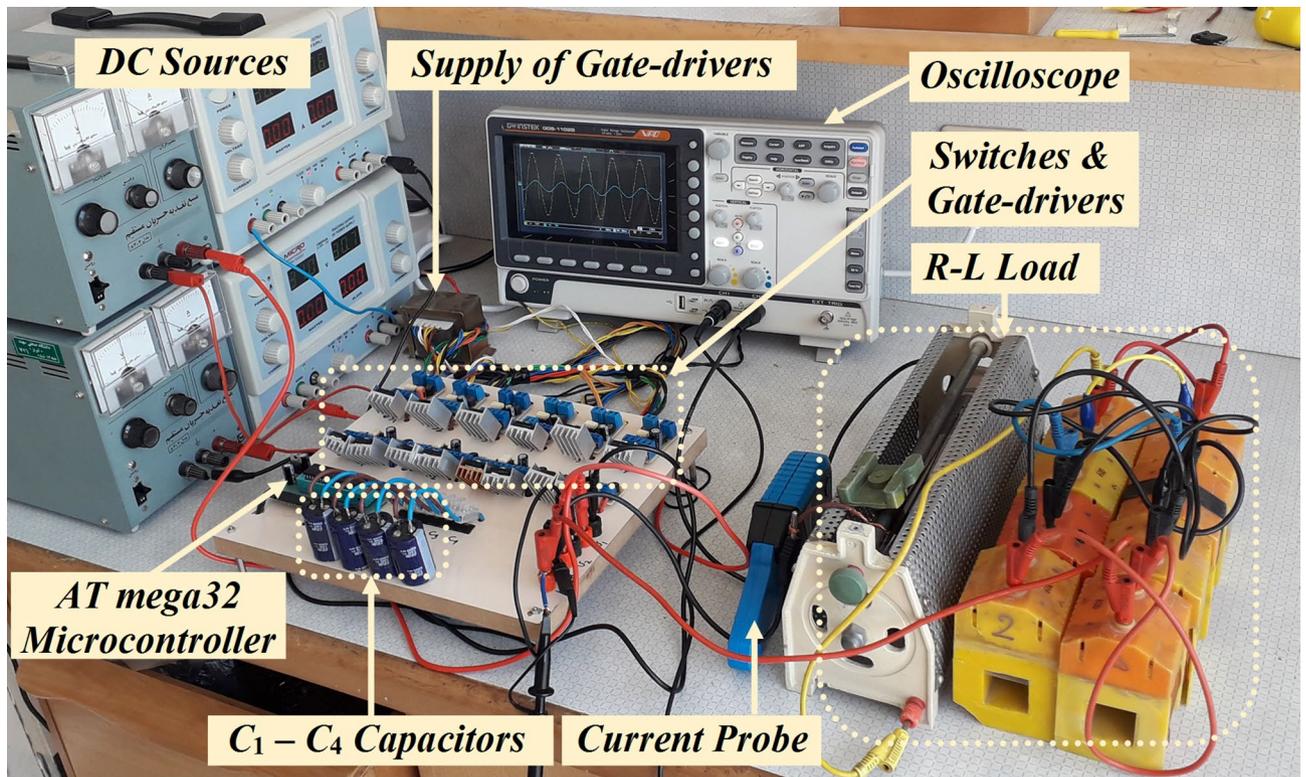
Fig. 7. Laboratory-scaled prototype of proposed inverter.

Parameter	Value in proposed topology	
	17-Level	**25-Level**
Input voltages (V_1, V_2)	$V_1 = 45V$, $V_2 = 135V$	$V_1 = 30V$, $V_2 = 150V$
Output voltage (V_o)	$V_o = 180V$	
Load R-L)	48.8Ω, $77mH$	49.3Ω, $77mH$
Output Power (P_o)	$P_o \approx 270W$	
Capacitances (C_1, C_2, C_3, C_4)	$2200\mu F$, $100V$	
MOSFETs	IRFP450 (500V, 14A)	
Microcontroller	AVR ATMEGA32A	
MOSFET driver	TLP250	
Modulation index	$M_a \approx 1$	
Modulation method	Nearest Level	
Output voltage waveform frequency	50 Hz	

Table 6. Parameter values employed in experimental analysis.

reduced part count. Although[30] has a slightly lower *TVS*, the proposed topology eliminates 16 diodes, reduces total device count by almost 50%, requires fewer conduction devices per level, and achieves the lowest CF values. Moreover, the proposed design has been experimentally validated, confirming its practical feasibility and efficiency advantages.

5. Experimental and simulation validations

The laboratory-scaled prototype of proposed topology has been implemented with output power of $270W$ (shown in Fig. 7).

Table 6 summarizes the parameter values employed during experimental validations.

Figure 8(a)–(b) present the output voltage and load current waveforms of proposed topology, respectively at 17- and 25-level versions. At 17-level version (shown in Fig. 8(a)), where $V_1 = 45V$ and $V_2 = 135V$, the proposed topology has successfully produced 17 voltage levels including $0, \pm 22.5V, \pm 45V, \pm 67.5V, \cdots, \pm 157.5V, \pm 180V$. The peak output voltage is about $180V$ (with small voltage drop on devices), which provides a unity voltage gain. Considering $Z_L = 48.8 + j0.077\omega$ (where $\omega = 2\pi f$) as the load, a sinusoidal current with the magnitude
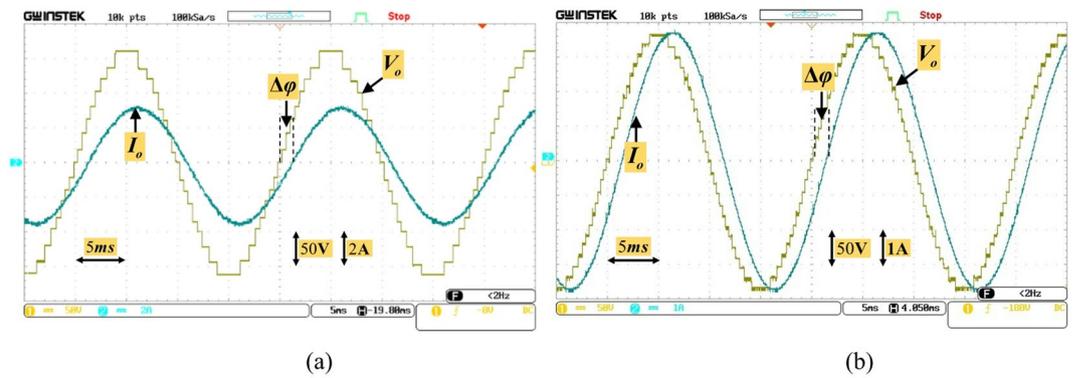
(a)   (b)

Fig. 8. Experimentally obtained output voltage and load current waveforms of proposed topology at; (**a**) 17-Level, (**b**) 25-level, versions.

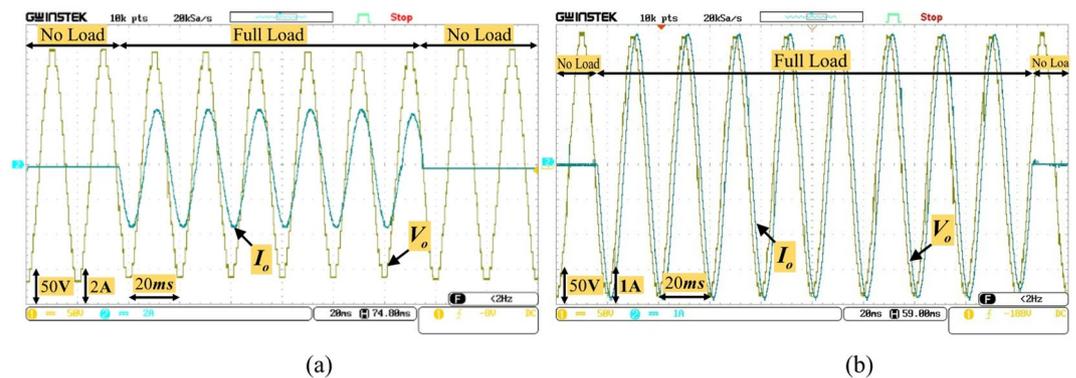(a)   (b)

Fig. 9. Experimentally obtained output voltage/load current waveforms of proposed topology during sudden load change at; (**a**) 17-Level, (**b**) 25-level, versions.

of about 3.3A passes through the load. Due to the resistive-inductive nature of the load, there exists a phase difference of about $\Delta\varphi = 26°$ between the load current and voltage waveforms. Also, at 25-level version (shown in Fig. 8(b)), where $V_1 = 30V$ and $V_2 = 150V$, the proposed topology can effectively generate 25 voltage steps including $0, \pm 15V, \pm 30V, \pm 45V, \cdots, \pm 165V, \pm 180V$. The maximum output voltage is about $180V$. Since a load of $Z_L = 49.3 + j0.077\ \omega$ is supplied by the proposed inverter, a sinusoidal current with the peak value of 3.2A flows through the load. Here again, a phase difference of about $\Delta\varphi = 26°$ is seen between the load voltage and current waveforms.

Figure 9 (a)–(b) show the dynamic performance of proposed inverter during sudden load step change conditions at both 17- and 25-level versions.

As seen, at both 17- and 25-level scenarios, the proposed inverter can effectively produce desired output voltage waveform during full-load and no-load conditions. During full-load condition, the output voltage magnitude experiences a very small reduction compared to the no-load condition, which is due to the voltage drop on the conducting devices. Figures 10 and 11 show the voltage and current waveforms of C_1-C_4 capacitors respectively at 17- and 25-level versions.

As seen from Fig. 10, at 17-level version, the voltage on C_1-C_4 is regulated respectively on 22.5V, 22.5V, 67.5V, and 67.5V. According to Fig. 11, at 25-level version, the voltage on C_1-C_4 capacitors is regulated respectively on 15V, 15V, 75V, and 75V. As seen, the proper sizing of capacitors has restricted their voltage ripple. Unlike switched-capacitor inverters, the proposed topology uses DC-link capacitors that are continuously connected to their input sources and naturally balanced to half of the source voltage. Therefore, aside from the short startup transient, no significant inrush current occurs during operation. This structural difference explains why the capacitor current waveforms in Figs. 10 and 11 are nearly equal to the load current rather than several times higher.

The voltage waveforms of switches at 17-level version have been shown in Fig. 12. According to experimental results, the peak voltage stress among semiconductors is about $180V$ ($V_{o,\ max}$), which belongs to T_2 and T_3 switches (verified by Table II). The voltage stress of other switches is much less than the peak output voltage.

Figure 13 shows the efficiency of proposed topology. As seen, the efficiency of 17-level and 25-levelversions of the proposed inverter are respectively about 97.7% and 97.6%, which have been obtained at the output powers of 270 W and 268 W, respectively. As shown in Fig. 13, the efficiency of the 25-level version is slightly lower ($\sim 97.6\%$) compared to the 17-level version ($\sim 97.7\%$). This small difference can be explained as follows:
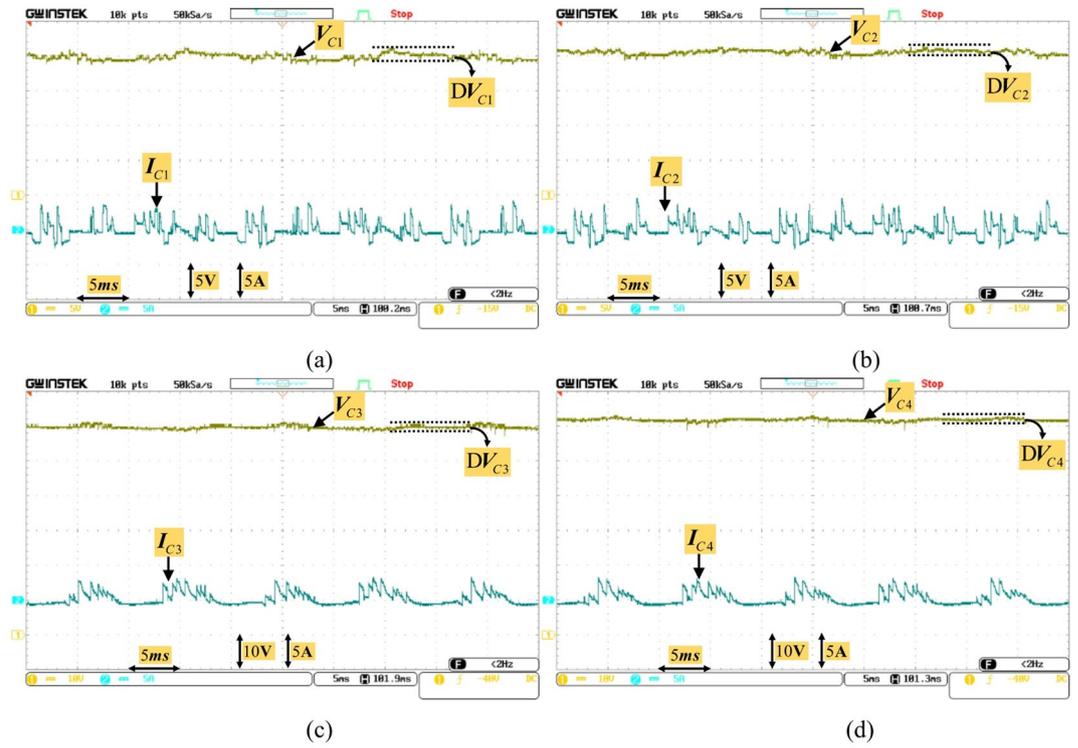
Fig. 10. Voltage and current waveforms of (**a**) C_1, (**b**) C_2, (**c**) C_3, (**d**) C_4, at 17-level proposed inverter.
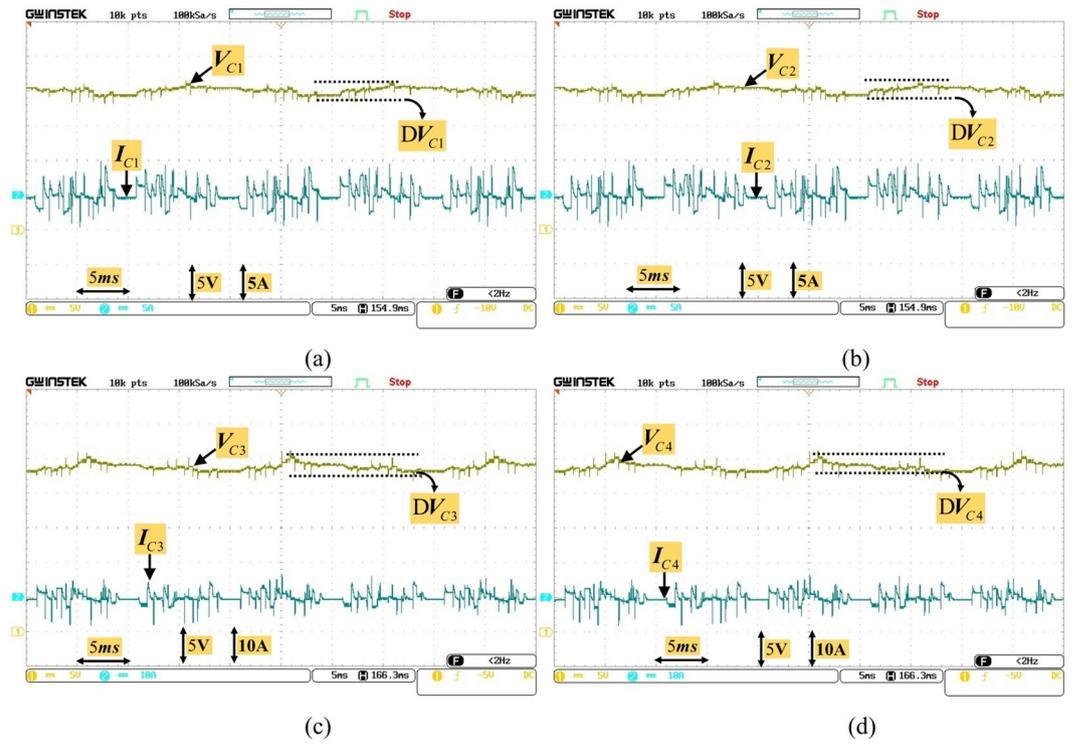
Fig. 11. Voltage and current waveforms of (**a**) C_1, (**b**) C_2, (**c**) C_3, (**d**) C_4, at 25-level proposed inverter.
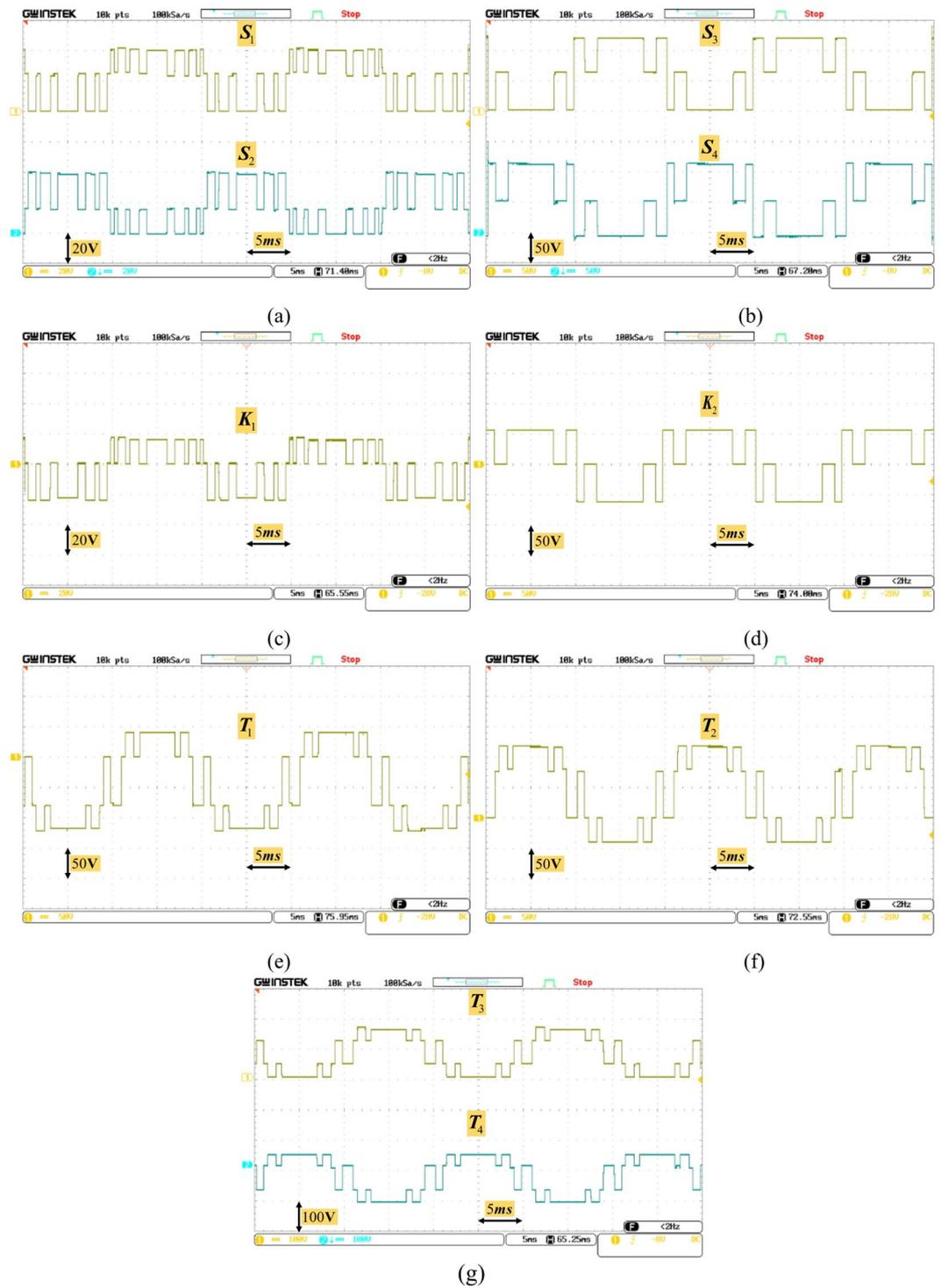
Fig. 12. Voltage waveforms of semiconductors (**a**) S_1-S_2, (**b**) S_3-S_4, (**c**) K_1, (**d**) K_2, (**e**) T_1, e) T_2, and e) T_3-T_4, at 17-level proposed inverter.

- Increased Switching Events: In the 25-level mode, more output voltage steps are generated within one fundamental cycle. Although the nearest-level modulation (NLM) minimizes switching frequency, the total number of commutations per cycle is higher in the 25-level case compared to the 17-level case. This leads to slightly higher switching and conduction losses.
- Higher Total Voltage Stress (TVS): The 25-level configuration has a higher total standing voltage (6.167 p.u. vs. 6.0 p.u. for the 17-level). This results in slightly higher device stress and marginally increased losses across semiconductors.
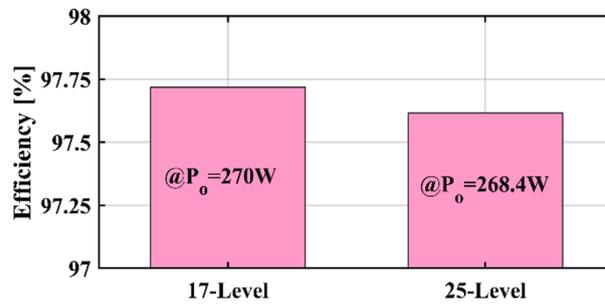
Fig. 13. Efficiency of proposed inverter.
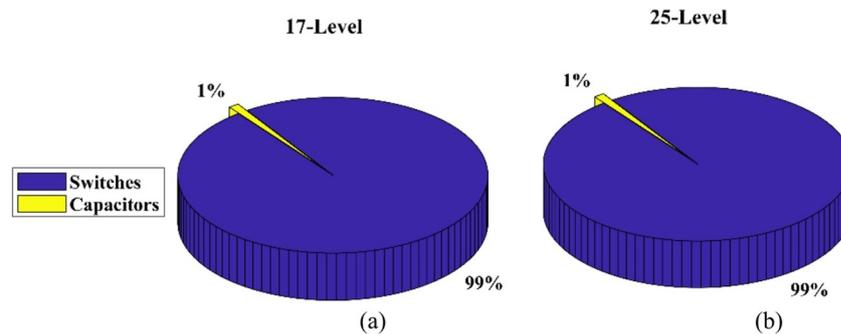
Fig. 14. Loss distribution between the switches and capacitors of proposed inverter, (**a**) 17-Level, (**b**) 25-Level.

Fig. 15. Power loss occurred on semiconductors in proposed inverter.

- Capacitor Current Ripple: In the 25-level mode, the DC-link capacitors handle smaller voltage steps but more frequent charging/discharging cycles, which contributes to additional (though small) ESR-related power loss.

The reduction in efficiency in 25-level version is very minor (only $\approx 0.1\%$), and both versions achieve quite high efficiency ($> 97.5\%$), which confirms that the proposed topology maintains proper performance in both 17-level and 25-level versions, with the small difference being inherent to the higher-level operation.

The total power loss on semiconductors of 17 and 25-level versions are respectively about 6.24 W and 6.48 W. Also, the total power loss on ESR of capacitors of 17 and 25-level versions are respectively about 0.068 W and 0.073 W. Thus, according to Fig. 14, the 99% of total power losses of the proposed inverter belongs to the semiconductors at both 17 and 25-level versions.

Figure 15 displays the power loss of semiconductors in proposed inverter. Furthermore, Fig. 16 shows the power loss distribution between the semiconductors at both 17 and 25-level versions of the proposed inverter.

As seen from Figs. 15 and 16, the highest power loss occurs on switch K_1, which is 17% and 19% of total switch losses, respectively at 17 and 25-level versions. Owing to usage of nearest level as the modulation technique, the semiconductors operate at quite low frequencies, which accordingly leads to quite small switching and rather high conduction losses. The total power losses on semiconductors (switching + conduction) in 17- and 25-level versions are about $6.24 W$ and $6.48 W$ respectively.

Figure 17 illustrates the share of each capacitor on total capacitor losses. At both 17 and 25-level versions, the share of capacitors on first DC-link (C_1 and C_2) is higher than that of those on second DC-link (C_3 and C_4).
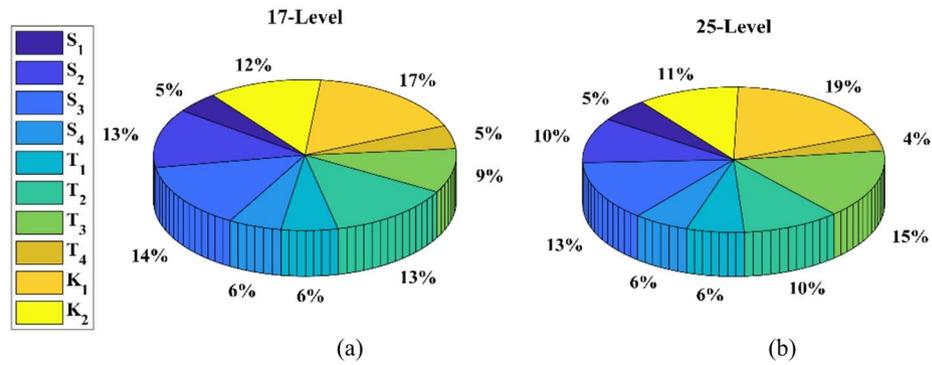
Fig. 16. Loss distribution between the switches of proposed inverter, (**a**) 17-Level, (**b**) 25-Level.
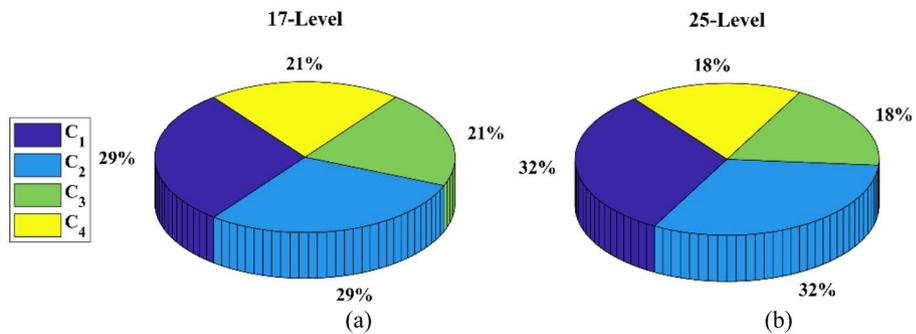

Fig. 17. Loss distribution between the capacitors of proposed inverter, (**a**) 17-Level, (**b**) 25-Level.

As seen, the percentage share of losses in capacitors C_1 and C_2 is higher in the 25-level case due to their more frequent charge/discharge cycles. However, it should be emphasized that the absolute value of total capacitor losses remains very small in both cases compared to semiconductor losses.

Additional simulations of the proposed 17- and 25-level inverter using PSCAD/EMTDC has been performed and the results have been shown Fig. 18 shows. The study considered step changes in the resistive part of the load while monitoring the output voltage, load current, and capacitor voltages to validate the natural voltage balancing mechanism. At both 17- and 25-level versions, from $t = 0$ s to $t = 0.2$ s, the inverter operates with the base load Z_1 ($R_1 = 48.8\Omega$, $L_1 = 77$mH), producing the expected 17-level or 25-level output voltage waveform along with balanced capacitor voltages. At $t = 0.2$ s, the resistive load is suddenly reduced from 48.8Ω to 12.2Ω (75% reduction, equal to $0.25R_1$), resulting in a sharp increase in load current. At $t = 0.3$ s, the resistance is increased from 12.2Ω to 73.2Ω (600% increase, equal to $1.5R_1$). At $t = 0.4$ s, the resistance is decreased to 36.6Ω (50% reduction, equal to $0.75R_1$). Finally, at $t = 0.5$ s, the resistance is increased to 61Ω (166% increase, equal to $1.25R_1$). At both versions, throughout all aforementioned transitions, the proposed inverter consistently maintains the output voltage waveform with nearly constant peak amplitude, aside from negligible variations caused by parasitic elements. Importantly, the DC-link capacitors automatically balance at their intended voltages: capacitors C_1 and C_2 stabilize at half of the first input source, and capacitors C_3 and C_4 stabilize at half of the second input source. These results confirm that the proposed topology in its both 17-level and 25-level versions is capable of withstanding significant load fluctuations while preserving both the desired multilevel output waveform and the natural voltage balance of the DC-link capacitors.

6. Conclusions

In this paper, a double-input active neutral point clamped inverter topology has been proposed that is capable of producing unity voltage gain with 17 and/or 25 voltage levels at the output port, based on the magnitude of input DC voltage sources. The proposed inverter requires 4 DC-link capacitors and 10 switches, 4 of which are bidirectional ones. Since the proposed inverter doesn't require an H-bridge to generate the bipolar voltage waveform, only two switches (instead of four) is exposed to a voltage stress of equal to maximum output voltage. The proposed inverter is capable of feeding any load type with variety of power factors. Compared to similar 17/25-level inverters, the proposed topology requires fewer number of DC sources, which leads to fewer size and cost. Also, it provides lower CF values than its similar counterparts. The results of experimental analysis confirm the correct operation of the proposed inverter.
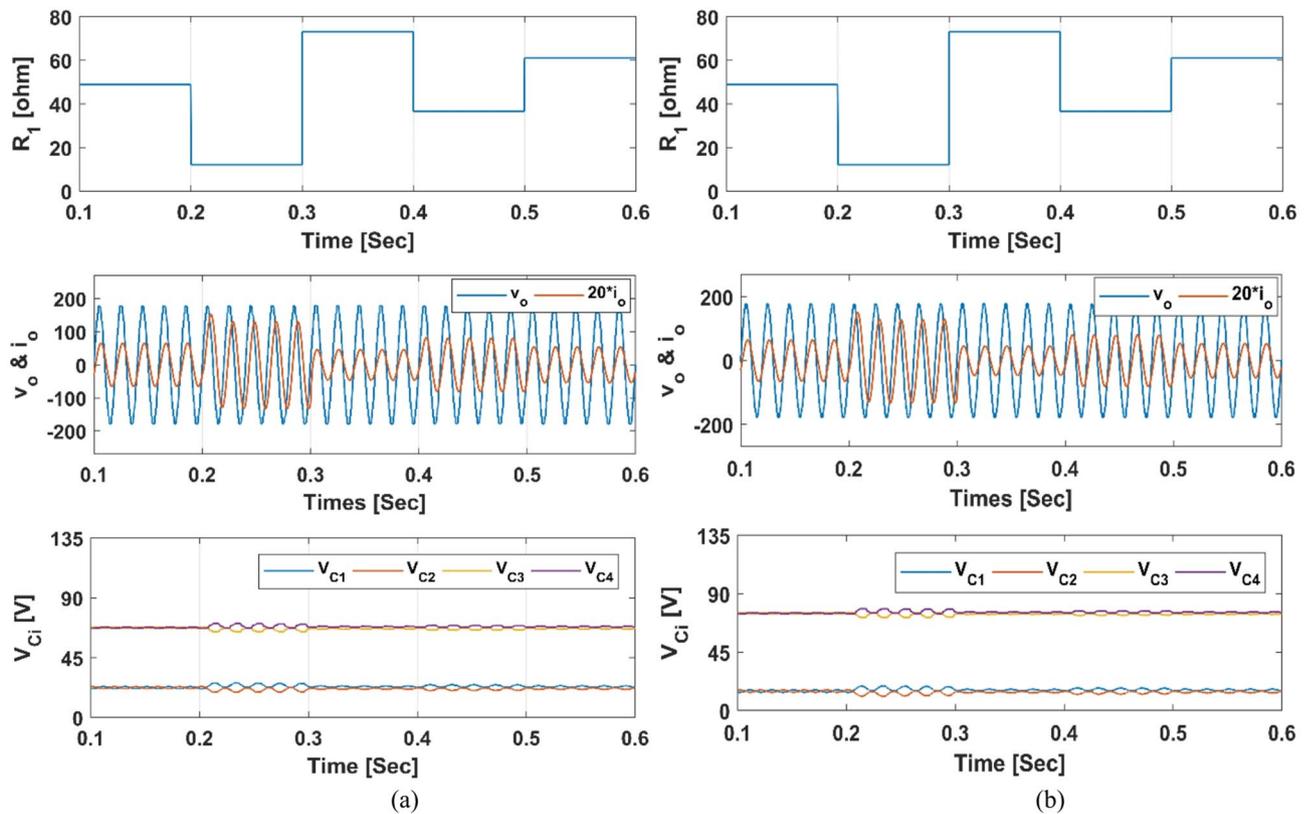
Fig. 18. Simulation results (output voltage, load current, and capacitor voltages) of proposed inverter at, (**a**) 17-Level, (**b**) 25-Level, versions, during step changes in resistive part of the load.

Data availability
The datasets used and/or analyzed during the current study available from the corresponding author on reasonable request.

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Conceptualization, M. A. and K. V.; methodology, M. A. and K. V.; software, M. A. and K. V.; validation, M. A., K. V. and M. K.; investigation, M. A., K. V., M. K. and M. A. J. S.; resources, M. A., K. V., and M. K.; data curation, M. A., K. V., and M. K.; writing—original draft preparation, M. A., K. V., and M. K.; supervision, K. V. and M. A. J. S.; Funding acquisition: K. V.; Visualization: K. V.; writing—review and editing: M. A., K. V., and M. A. J. S.; project administration, K. V.; Formal analysis: M. A., and K. V., All authors have read and agreed to the published version of the manuscript.

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Declarations

Competing interests

The authors declare no competing interests.

Additional information

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