scientific reports

Check for updates

OPEN

High gain non-isolated step-up DC-DC converter proper for renewable energy applications

Rana Rostami[1]✉, Seyed Hossein Hosseini[1,2] & Mohammad Bagher Bannae Sharifian[1]

This paper introduces a quadratic-based DC-DC converter with high voltage gain, specifically optimized for DC microgrid applications. The proposed topology offers several key merits, including enhanced voltage gain, reduced voltage stress on switching components, continuous input current, a common ground between the input and output, high efficiency, and synchronized switch operation. A detailed analysis is provided on its operational principles, steady-state characteristics, design considerations, and efficiency evaluation, along with dynamic modeling and control assessment. To emphasize its benefits, the proposed converter is compared with existing topologies. The effectiveness of the design is validated through experimental testing on a 200W prototype, operating with an input voltage of 20V and delivering an output voltage of 200V.

Keywords Step-up converter, High gain voltage, Minimum power loss, Reduced blocking voltage

With the increasing integration of distributed generation sources, DC microgrid technology continues to advance. Since DC power generators typically produce low output voltages, high efficiency and high-gain DC-DC converters are essential to meet the voltage requirements of DC loads [1]. In addition to their crucial role in renewable energy systems, these high-gain converters are widely employed in various applications, including battery backup solutions for uninterruptible power supplies, high-intensity discharge lamp ballasts for automotive headlamps, electric traction systems, and certain medical devices [2].

Traditionally, conventional DC-DC boost converters have been utilized for voltage step-up applications. However, one major drawback is that the voltage stress on the switching device is equivalent to the output voltage. As a result, high-voltage-rated switches must be chosen, leading to increased conduction losses. Furthermore, achieving a high voltage gain requires operating at large duty cycles, which not only amplifies conduction losses and voltage spikes but also intensifies the diode reverse recovery issue, potentially affecting overall system performance [3].

Various advanced DC-DC circuit topologies have been developed to achieve high voltage gain by converting low-voltage sources into elevated DC output voltages. These designs incorporate multiple voltage-boosting techniques, such as switched inductor and switched capacitor (SC) methods, cascading structures, interleaved configurations, voltage multiplier cells, and hybrid approaches that integrate these methods [4–11]. While these strategies effectively enhance voltage gain, many suffer from inherent drawbacks, including the use of multiple components and hard-switching operations, which compromise their efficiency and suitability for high-gain applications.

To overcome these challenges, multi-stage or multi-level strategies have been introduced, generally categorized into three main sections: cascading, interleaving, and multilevel configurations. Despite their potential to improve voltage gain, these converters often encounter issues such as complex control requirements, an increased number of components, and higher system costs. Interleaved structures, as proposed in [12] and [13], have gained attention for photovoltaic applications due to their capability to reduce input current ripple, making them particularly beneficial in such scenarios. However, their practical implementation is prevented, by the intricacy of the control mechanism and elevated costs.

Among various voltage-boosting techniques, the SC approach, which operates on the charge pump principle, is a commonly employed method for achieving high voltage gain, as demonstrated in [14–16]. Nevertheless, SC-based topologies present a significant limitation: they generate high peak currents through capacitors, which can result in substantial power losses and increased electromagnetic interference. Despite this drawback, the

[1]Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz 51666-16471, Iran. [2]Faculty of Engineering, Near East University, Mersin 10, PO BOX:99138, Nicosia, North Cyprus, Turkey. ✉email: rana.rostami@tabrizu.ac.ir

voltage multiplier technique has emerged as a more cost-effective and efficient solution. Comprising diodes and capacitors, voltage multiplier circuits enable significant voltage gain while maintaining a relatively simple structure [17–19]. However, although studies in [20] and [21] highlight the capability of voltage multipliers to achieve high voltage levels, their dependence on a large number of components escalates both cost and system size. Furthermore, a major limitation of voltage multiplier circuits is the excessive voltage stress imposed on the circuit components.

Another widely implemented method for increasing input voltage and achieving high voltage gain in DC-DC converters is the voltage lift technique [22–24]. This approach relies on charging a capacitor to a predefined voltage level before utilizing the stored charge to elevate the output voltage. By continuously applying this principle and incorporating additional capacitors, higher voltage levels can be attained through extended configurations such as re-lift, triple-lift, and quadruple-lift techniques.

The switched inductor technique operates using two distinct configurations: the passive switched-inductor unit (PSL) and the active switched-inductor unit (ASL). In ASL-based designs, the circuit comprises active switches and inductors, whereas PSL units utilize diodes in combination with inductors [25, 26]. The ASL approach significantly enhances the voltage boost capability by first charging the inductors in parallel through two power switches. When the switches are turned off, the stored energy is then released in series, effectively increasing the output voltage, as outlined in [27, 28].

Motivated by the advantages and limitations of existing high step-up converters, this paper introduces an innovative DC-DC topology tailored for DC microgrid applications. The proposed design offers several key benefits, enhancing performance and efficiency in high step-up voltage conversion. Main contributions and features of this paper are classified as follows:

- The proposed topology, enables high voltage gain without being limited by the duty cycle, allowing it to operate across the full range from 0 to 1
- Imposing low voltage stress on the switches, allowing the use of low-voltage-rated switches with minimal on-resistance. This reduction in resistance decreases conduction losses and improves overall efficiency.
- Providing a continuous input current with minimal ripple
- Utilizing two power switches operating in synchronization.
- The input and output sides share a common ground.

The rest sections of this work are titled as follows:

Section "Proposed Step up DC-DC Converter" includes theoretical study to reach converter's boosting gain, dynamic study and compassion study. In Sect. 3 experimental results are studied in detail. Section 4 includes work conclusion.

Proposed step up DC-DC converter

Figure 1 illustrates the basic structure of the proposed boost converter. The proposed converter includes: two switches (S_1, S_2), three inductors (L_1, L_2, L_3), three diodes (D_1, D_2, D_3) and capacitors (C_1, C_2, C_3, Co). This converter operates in two modes, continues and discontinues conduction mode (CCM, DCM). Some assumption is considered to have a comprehensive study, as follows:

- Equivalent series resistance (ESR) of all semiconductors are ignored.
- Voltage of all capacitors is considered in the constant value (due to its large magnitude)
- The transient intervals are not considered in the operational modes, because of its shorter time than switching period of time.

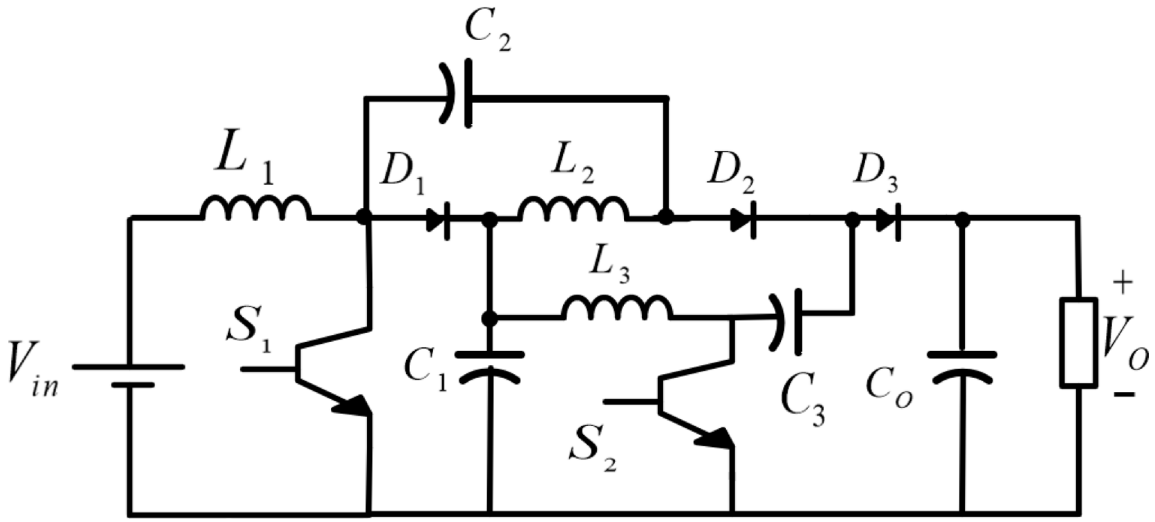


Fig. 1. Proposed converter.

Both of CCM and DCM operation modes are described in the following sections.

Analysis of CCM mode

CCM operation mode of the proposed converter consists of two-time intervals. S_1 and S_2 are turned on in the same time, or S_1 and S_2 are turned off in the same time. The idealized waveform of the proposed non-isolated boost converter is depicted in the Fig. 2.

First operation mode

In this time interval, S_1 and S_2 are turned on. This time interval endures (1-D) T. D_1 and D_3 are off and D_2 is on. The blocking voltage of $D_1$and D_3 are, VC_1 andV_{C3}-$V_{o,}$ respectively. Inductors L_1, L_2 and L_3 are in the charging position. Figure 3 shows the converter's condition in this time interval. Inductors voltages are obtained via Eqs. (1–4):

$$-V_{in} + V_{L1} = 0 \tag{1}$$

$$-V_{C2} - V_{L2} + V_{C1} = 0 \tag{2}$$

$$-V_{C1} + V_{L3} = 0 \tag{3}$$

$$V_{C3} = V_{C2} \tag{4}$$

Second operation mode

Figure 4 illustrates the proposed boost converter's elements condition in the second time interval. In this mode, S_1 is in on state and S_2 is in off state. D_1 and D_2 are blocked via voltage V_{C1} and V_{C2}-V_O, respectively. Diode D_3 is in forward bias. Inductors L_1, L_2 and L_3 are in charge, charge and discharge position, respectively. Equations (4–6) gives voltage of the inductors:

$$-V_{C1} + V_{L3} - V_{C3} + V_O = 0 \tag{5}$$

$$-V_{in} + V_{L1} + V_{C1} = 0 \tag{6}$$

$$V_{L2} + V_{C2} = 0 \tag{7}$$

$$V_{C1} = \frac{V_{in}}{1 - D} \tag{8}$$

$$V_{C2} = V_{C3} = \frac{DV_{in}}{1 - D} \tag{9}$$

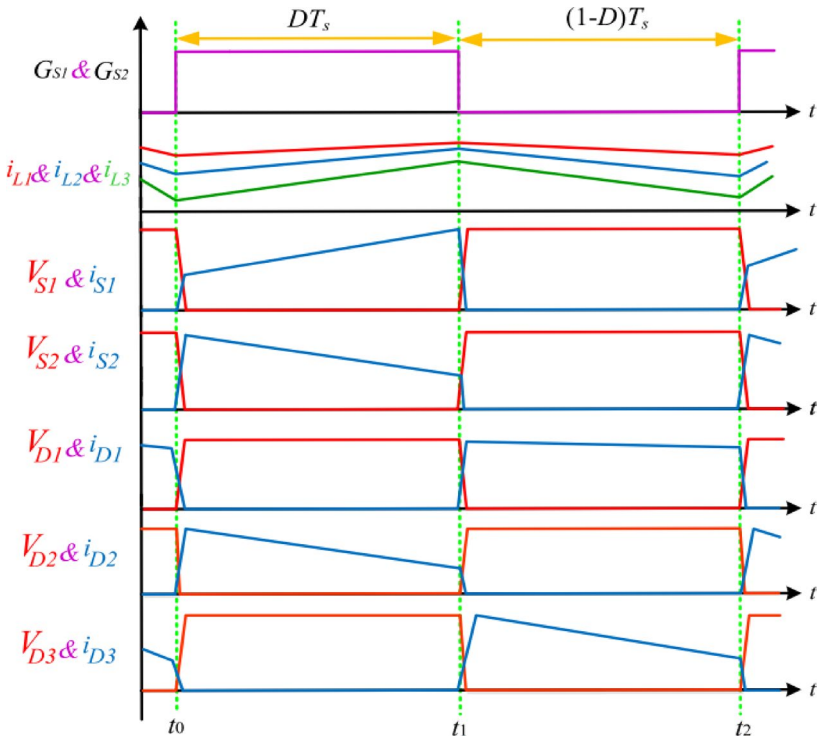


Fig. 2. Voltage and current waveform of $L_1 \sim L_3$ and $D_1 \sim D_3$.

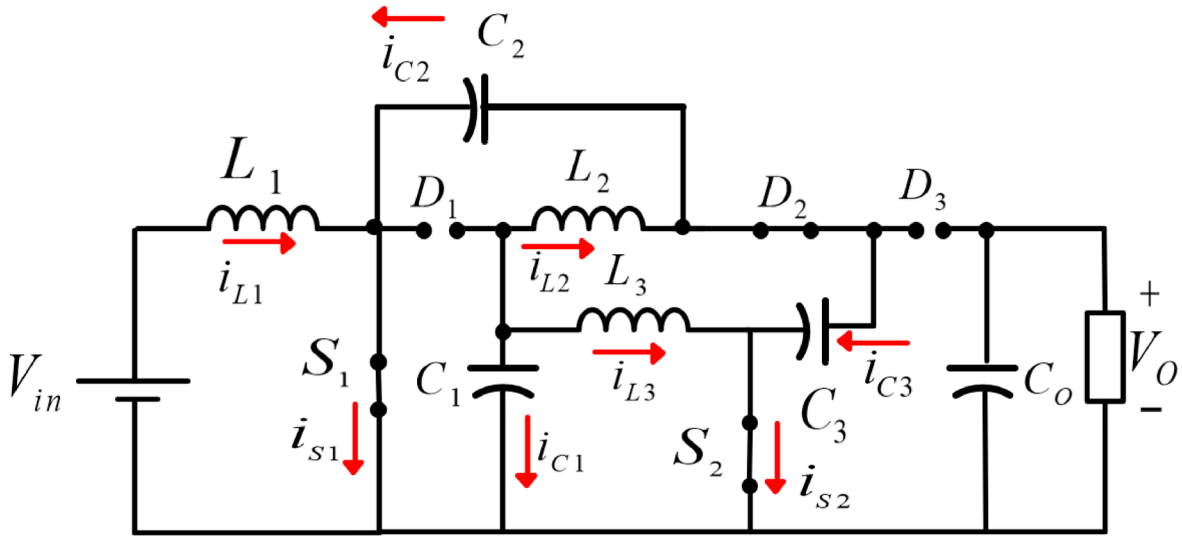


Fig. 3. Proposed converter in the first switching interval.

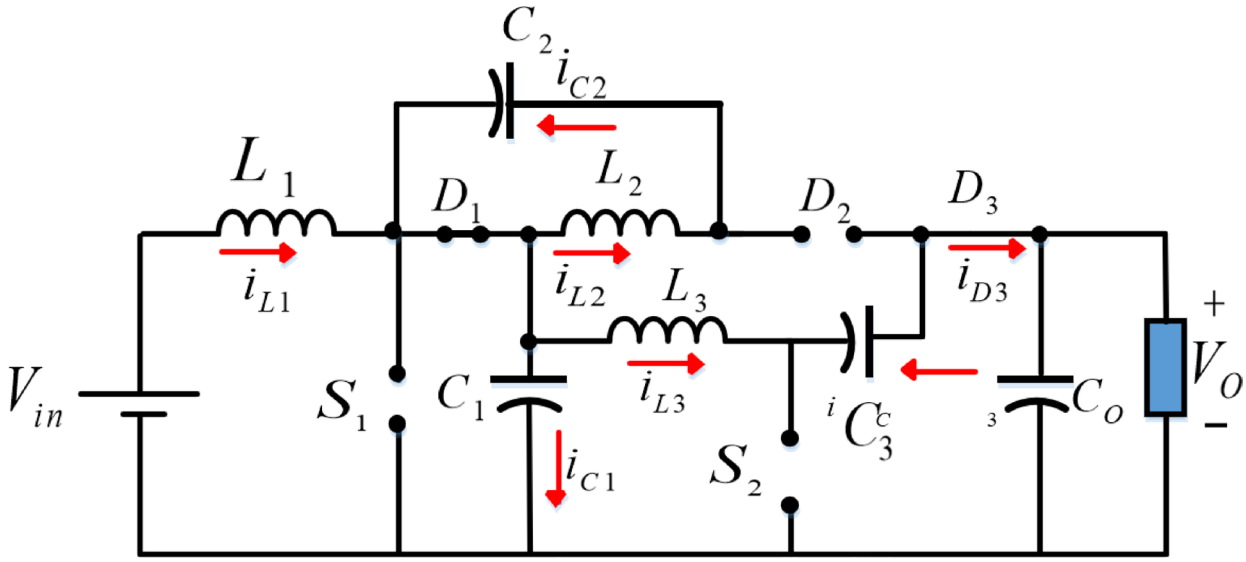


Fig. 4. Proposed converter in the second switching interval.

Volt–second law

Average voltage of inductors in the period of time is equal to zero [29]. By employing volt-second law, capacitors voltage is obtained as follows:

$$\int_0^T V_{L1}(t)dt = \int_0^{DT} V_{in}dt + \int_{DT}^T (V_{in} - V_{C1})dt = 0 \tag{10}$$

$$V_{C1} = \frac{V_{in}}{1-D} \tag{11}$$

$$\int_0^T V_{L2}(t)dt = \int_0^{DT} (V_{C1} - V_{C2})dt + \int_{DT}^T -V_{C2}dt = 0 \tag{12}$$

$$V_{C2} = \frac{D}{(1-D)}V_{in} \tag{13}$$

$$\int_0^T V_{L3}(t)dt = \int_0^{DT} (V_{C1} + V_{C3} - V_O)dt + \int_{DT}^T V_{C1}dt = 0 \tag{14}$$

$$V_{C3} = \frac{D}{(1-D)} V_{in} \tag{15}$$

By using capacitor voltages, the voltage gain has been calculated as follows:

$$M_{CCM} = \left(\frac{V_O}{V_{in}}\right) = \left(\frac{2-D^2}{(1-D)^2}\right) \tag{16}$$

The blocking voltage of diodes and switches could be calculated as follows:

$$V_{S1} = \frac{V_{in}}{1-D} \tag{17}$$

$$V_{S2} = \frac{V_{in}}{(1-D)^2} \tag{18}$$

$$V_{D1} = \frac{V_{in}}{1-D} \tag{19}$$

$$V_{D2} = \frac{DV_{in}}{(1-D)^2} \tag{20}$$

$$V_{D3} = \frac{V_{in}}{(1-D)^2} \tag{21}$$

Analyze of DCM mode

DCM Condition.

The first two DCM operating modes exhibit similar behavior; therefore, this section focuses exclusively on Mode II of DCM. In this mode, all switches and diodes are turned off, and the corresponding relationship derived using Kirchhoff's Voltage Law (KVL) is as follows:

$$-V_{in} + V_{L1} - V_{C2} - V_{L2} + V_{C1} = 0 \tag{22}$$

Utilizing the volt-second balance principle on the input inductors, accompanied by several derivations, enables the determination of the voltages across capacitors *C*1, *C*2, *C*3, as well as the output voltage.

$$V_{C1} = \frac{V_{in}(D+D')}{D'} \tag{23}$$

$$V_{C2} = \frac{DV_{in}}{D'} \tag{24}$$

$$V_{C3} = \frac{DV_{in}}{D'} \tag{25}$$

$$V_O = \frac{V_{in}(D - D^2 + 1 + D')}{D'} \tag{26}$$

$$G_{DCM} = \frac{V_O}{V_{in}} = \frac{(D - D^2 + 1 + D')}{D'} \tag{27}$$

Additionally, through the application of the charge balance principle to the capacitors, followed by a sequence of derivations, it becomes possible to calculate the current flowing through the inductors.

$$I_{L1} = \frac{I_O(1 + D - D^2)}{D'} \tag{28}$$

Assuming IL1 = IL1(peak) /2, then IL1(peak) can be obtained, as follows:

$$I_{L1(peak)} = \frac{2V_O(1 + D - D^2)}{D'R_O} \tag{29}$$

Furthermore, the following equation can be formulated for the inductor, as below:

$$\Delta i_{L1} = \frac{V_{L1}\Delta t}{L_1} = \frac{V_{in}D}{L_1 f_s} \tag{30}$$

Time duration of the mode III can be calculated as:

$$D' = \frac{4\tau G_{DCM}}{D} \tag{31}$$

where, τ is a dimensionless variable, and it is defined, as follows:

$$\tau = \frac{f_s L_{eq}}{R_O} \tag{32}$$

Boundary conduction mode (BCM)

A. Boundary condition

To ensure CCM operation in the proposed circuit, the minimum current through the L_1 must remain above zero. The minimum current of the L_1 and ΔI_{L1} can be determined as:

$$\begin{cases} V_{L1} = V_{in}, \dfrac{L_1 dI_{L1}}{dt} = V_{in} \Rightarrow dI_{L1} = \dfrac{V_{in} dt}{L_1} \\ dt = DT_S, T_S = \dfrac{1}{f_S}, \Delta I_{L1} = dI_{L1}, \Delta I_{L1} = \dfrac{V_{in} D}{L_1 f_S} \end{cases} \tag{33}$$

$$\begin{cases} I_{L1,\min} = I_{L1} - \dfrac{\Delta I_{L1}}{2} \\ I_{L1,\max} = I_{L1} + \dfrac{\Delta I_{L1}}{2} \end{cases} \tag{34}$$

The minimum required values of the L_1 to maintain CCM, as illustrated in Fig. 5, are as given.

$$\begin{cases} I_{L1,\min} = 0 \Rightarrow I_{L1} \geq \dfrac{\Delta I_{L1}}{2} \\ \Rightarrow \dfrac{I_O(1 + D - D^2)}{(1 - D)^2} \geq \dfrac{V_{in} D}{2 L_1 f_S} \\ L_1 \geq \dfrac{D(1 - D)^4 R}{2 f_S (1 + D - D^2)^2} \end{cases} \tag{35}$$

Current calculation

Mode I: During this time interval, Kirchhoff's Current Law (KCL) govern the relationships in the circuit.

$$I_{L1} + I_{C2} - I_{S1} = 0 \tag{36}$$

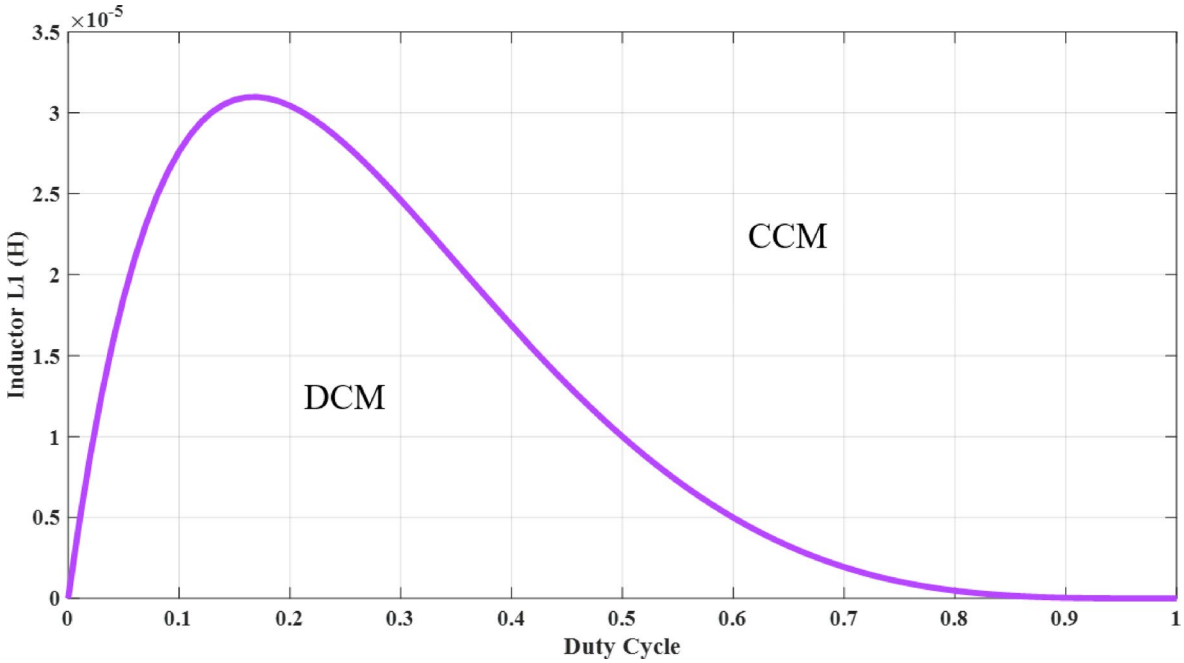


Fig. 5. The minimum needed values of the L1 for CCM function.

$$I_{L2} + I_{C1} + I_{L3} = 0 \tag{37}$$

$$I_{L2} - I_{C2} - I_{D2} = 0 \tag{38}$$

$$I_{D2} - I_{C3} = 0 \tag{39}$$

$$I_{L3} + I_{C3} - I_{S2} = 0 \tag{40}$$

$$I_{CO} + I_O = 0 \tag{41}$$

$$I_{S2} + I_{C1} + I_{S1} - I_{in} = 0 \tag{42}$$

Mode II: Using KCL, the corresponding equations for this mode can be derived as:

$$I_{L1} - I_{D1} + I_{C2} = 0 \tag{43}$$

$$I_{D1} - I_{C1} - I_{L2} - I_{L3} = 0 \tag{44}$$

$$I_{L2} - I_{C2} = 0 \tag{45}$$

$$I_{D3} + I_{C3} = 0 \tag{46}$$

$$I_{L3} + I_{C3} = 0 \tag{47}$$

$$I_{D3} - I_{CO} - I_O = 0 \tag{48}$$

$$I_{CO} + I_O + I_{D1} - I_{L2} - I_{L3} - I_{in} = 0 \tag{49}$$

Current stress of the components
The currents through the semiconductor components during the first and second switching subintervals can be expressed as follows:

$$I_{S1-Mode1} = \frac{I_O(2D^2 - 4D + 1)}{(1-D)^2 D} \tag{50}$$

$$I_{S2-Mode1} = \frac{I_O}{(1-D)D} \tag{51}$$

$$I_{D1-Mode2} = \frac{I_O(2-D)}{(1-D)^2} \tag{52}$$

$$I_{D2-Mode1} = \frac{I_O}{D} \tag{53}$$

$$I_{D3-Mode2} = \frac{I_O}{1-D} \tag{54}$$

Additionally, the currents flowing through the capacitors during the first and second switching subintervals can be expressed as:

$$I_{C1-Mode1} = -\frac{I_O(2-D)}{(1-D)} \tag{55}$$

$$I_{C1-Mode2} = \frac{DI_O(2-D)}{(1-D)^2} \tag{56}$$

$$I_{C2-Mode1} = -\frac{I_O(1-D)}{D} \tag{57}$$

$$I_{C2-Mode2} = I_O \tag{58}$$

$$I_{C3-Mode1} = \frac{I_O}{D} \tag{59}$$

$$I_{C3-Mode2} = -\frac{I_O}{1-D} \tag{60}$$

$$I_{CO-Mode1} = -I_O \tag{61}$$

$$I_{CO-Mode2} = \frac{DI_O}{1-D} \tag{62}$$

Assuming ripple-free currents for inductors during CCM operation, the average currents can be calculated as shown below:

$$I_{L1} = I_{in} = \frac{I_O(1 + D - D^2)}{(1 - D)^2} \tag{63}$$

$$I_{L2} = I_O \tag{64}$$

$$I_{L3} = \frac{I_O}{1 - D} \tag{65}$$

Additionally, the average currents for the converter's switches and diodes can be approximated as follows:

$$I_{S1,avg} = \frac{I_O(2D^2 - 4D + 1)}{(1 - D)^2} \tag{66}$$

$$I_{S2,avg} = \frac{I_O}{(1 - D)} \tag{67}$$

$$I_{D1,avg} = \frac{I_O(2 - D)}{(1 - D)} \tag{68}$$

$$I_{D2,avg} = I_{D3,avg} = I_O \tag{69}$$

Calculating the root-mean-square (RMS) currents is essential for assessing the overall power efficiency of the power converter. Hence, the RMS currents for each component are determined as:

$$I_{S1,rms} = \frac{I_O(2D^2 - 4D + 1)}{(1 - D)^2\sqrt{D}} \tag{70}$$

$$I_{S2,rms} = \frac{I_O}{(1 - D)\sqrt{D}} \tag{71}$$

$$I_{D1,rms} = \frac{I_O(2 - D)}{\sqrt{(1 - D)^3}} \tag{72}$$

$$I_{D2,rms} = \frac{I_O}{\sqrt{D}} \tag{73}$$

$$I_{D3,rms} = \frac{I_O}{\sqrt{1 - D}} \tag{74}$$

$$I_{C1,rms} = -\frac{I_O(2 - D)\sqrt{D}}{(1 - D)} + \frac{DI_O(2 - D)}{\sqrt{(1 - D)^3}} \tag{75}$$

$$I_{C2,rms} = -\frac{I_O(1 - D)}{\sqrt{D}} + I_O\sqrt{1 - D} \tag{76}$$

$$I_{C3,rms} = \frac{I_O}{\sqrt{D}} - \frac{I_O}{\sqrt{1 - D}} \tag{77}$$

$$I_{CO,rms} = -I_O\sqrt{D} + \frac{DI_O}{\sqrt{1 - D}} \tag{78}$$

Design and efficiency

Design approach

The high-performance design is resulted by considering all of voltage and current constraints [30–32]. To this aim, inductance and capacitor values are calculated by considering current and voltage ripple equations as follows:

$$L_1 = L_2 = L_3 \geq \frac{D \times V_i^2}{0.1 \times P_o \times f} = \frac{0.6 \times 20^2}{0.1 \times 200 \times 50 \times 10^3} = 24(\mu H) \tag{79}$$

$$C \geq \frac{D \times V_o}{\Delta V \times R \times f} = \frac{0.6 \times 240}{4 \times 100 \times 50 \times 10^3} = 7.2(\mu F) \tag{80}$$

Calculating efficiency of the proposed converter

The real form of proposed converter with considering parasitic resistance of elements is used to calculate its efficiency [33, 34]. $R_{DS\text{-}ON}$, $R_{(D1, D2, D3)}$, $R_{(L1, L2, L3)}$, $R_{(C1, C2, C3)}$ are resistance of power switch, ESR of diodes, ESR of inductors, and ESR of capacitors, respectively.

$$Power_{Loss} = Loss_{Switches} + Loss_{Diodes} + Loss_{Capacitors} + Loss_{inductors} \tag{81}$$

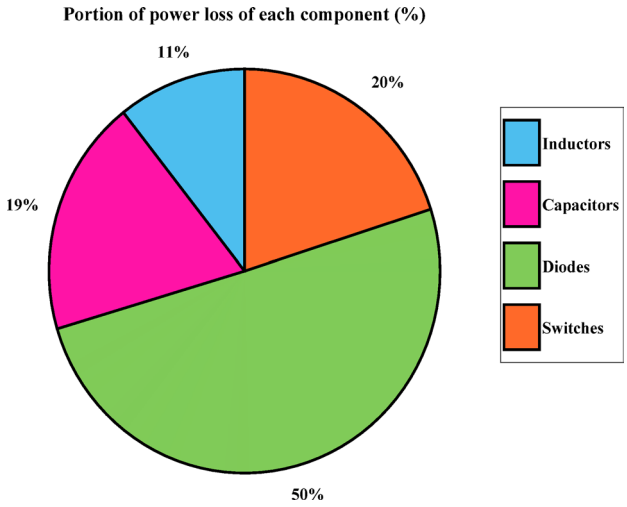


Fig. 6. Power loss of each component per total power loss.

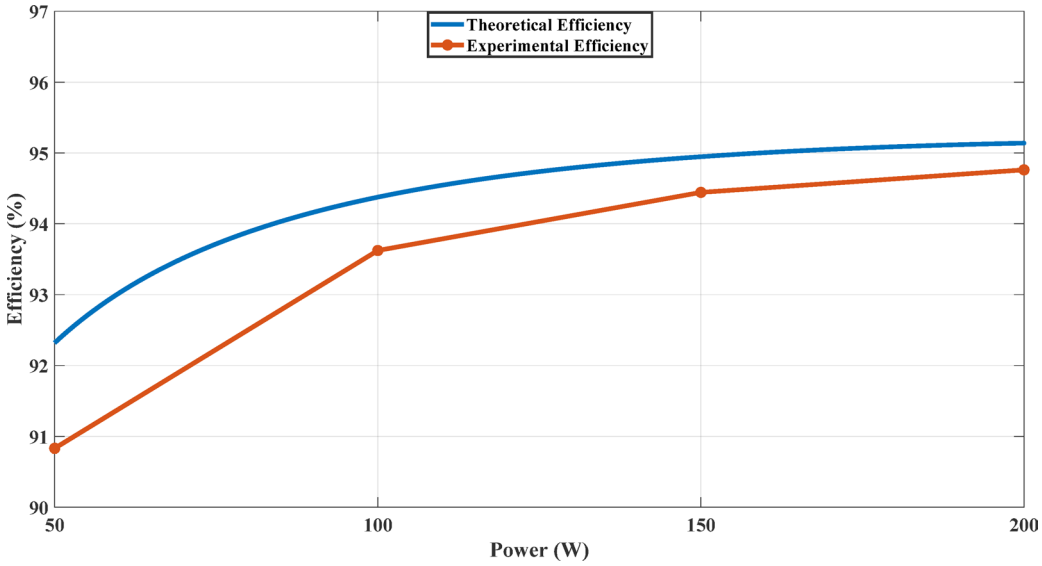


Fig. 7. The theoretical and experimental efficiency of the proposed topology in relation to the output power.

$$Loss_{switches} = Loss_{Conducting} + Loss_{Switching} = R_{DS\_on}(I_G^{rms})^2 + \frac{1}{2} f_s (t_r + t_f) I_G^{ave} V_G \tag{82}$$

$$Loss_{Diodes} = \sum_{i=1}^{Num.\,diodes} (Loss_{Conduction} + Loss_{Forward}) = \sum_{i=1}^{Num.\,diodes} \left[r_{D_i} \left(I_{D_i}^{RMS} \right)^2 + V_{D_i} I_{D_i}^{avg} \right] \tag{83}$$

$$Loss_{Capacitors} = \sum_{i=1}^{Num.\,capacitors} \left[r_{C_i} \left(I_{C_i}^{RMS} \right)^2 \right] \tag{84}$$

$$Loss_{inductors} = \sum_{i=1}^{Num-inductors} [r_{Li} (I_{Li}^{RMS})^2] \tag{85}$$

$$I_{G1}^{rms} = \sqrt{2 \left(\frac{2 - D^2}{(1 - D)^2} \right)} I_O \tag{86}$$

Topologies	Number of Elements				Total Number of Elements	Voltage Gain	Max. Volt. Stress On Switches	Max. Volt. Stress On Diodes	I.R*	E*(%)
	S	D	C	L						
[15]	2	2	2	2	8	*(2)/(1-D)*	*1/2*	*1/2*	High	95
[16]	2	5	4	3	14	*(3-D)/(1-D)*	*2/(3-D)*	*2/(3-D)*	High	95.02
[17]	1	2	3	2	8	*2D/(1-D)*	*1/2D*	*1/2D*	High	93.8
[18]	1	4	4	1	10	*[2 + (2-D) N]/(1-D)*	*1/[2 + (2-D) N]*	*(N + 1)/[2 + (2-D) N]*	High	88.4
[19]	1	5	6	2	13	*3/(1-D)*	*1/3*	*1/3*	High	96
[20]	1	3	4	2	10	(2 + N)/(1-D)	1/(2 + N)	(1 + N)/(2 + N)	Low	94.5
[21]	1	3	4	2	10	*(1 + N)/(1-D)*	*1/(1 + N)*	*N/(1 + N)*	Low	91.2
[22]	1	4	5	2	12	*[N(2-D) + (1 + D)]/(1-D)*	*1/[N(2-D) + (1 + D)]*	*(1 + N)/[N(2-D) + (1 + D)]*	Low	92.1
[23]	1	3	4	2	10	*(1 + N)/(1-D)*	*1/(1 + N)*	*N/(1 + N)*	Low	95.45
[24]	2	2	3	2	9	*N/(1-D)*	*1/N*	*1*	Low	94.2
[25]	1	4	3	2	10	*(DN + 1)/(1-D)*	*1/(DN + 1)*	*N/(DN + 1)*	High	-
[26]	1	3	4	2	10	*(2 + N)/(1-D)*	*1/(2 + N)*	*(1 + N)/(2 + N)*	Low	95.9
[27]	2	5	3	1	11	*[(2-D) N]/(1-D)*	*1/[(2-D)2N]*	*1/(2-D)*	High	94.1
Proposed	2	3	4	3	12	*$(2\text{-}D^{2})/(1\text{-}D)^{2}$*	*1/(1-D)*	*(D + 1)/(1-D)*	Low	95.1

Table 1. Comparison designing features of proposed converter with others. I.R*, Input Ripple; E*, Efficiency.

$$I_{G2}^{rms} = \sqrt{2(\frac{1 - D^2 + D}{1 - D})}\, I_O \tag{87}$$

By implementing Eqs. (81–87) numerical power loss values of each component are calculated as follows:

$$Loss_{L1} = 0.01 \times 2.08^2 = 0.43\, w \tag{88}$$

$$Loss_{L2} = 0.01 \times 0.044^2 = 0.00002w \tag{89}$$

$$Loss_{L3} = 0.01 \times 3 \times 0.044 = 0.0013\, w \tag{90}$$

$$Loss_{C1} = 0.01 \times 7.01^2 = 0.49w \tag{91}$$

$$Loss_{C2} = 0.01 \times 3.45^2 = 0.119w \tag{92}$$

$$Loss_{C3} = 0.01 \times 3.9^2 = 0.16w$$

$$Loss_{D1} = (0.7 \times 0.83) + (0.02 \times 0.017) = 0.5844\, w \tag{93}$$

$$Loss_{D2,3} = 2 \times ((0.7 \times 0.52) + (0.02 \times 0.1102) = 0.7324w \tag{94}$$

$$Loss_{G1} = [0.5 \times 50000 \times (60 + 48) \times 10^{-9} \times 1.25 \times 60] + [0.04 \times 0.9375] = 0.24w \tag{95}$$

$$Loss_{G2} = [0.5 \times 50000 \times (60 + 48) \times 10^{-9} \times 0.6458 \times 323] + [0.04 \times 0.25] = 0.573w \tag{96}$$

$$Total - Loss = 2.91w \tag{97}$$

$$\eta\% = \frac{P^{out}}{P^{out} + P^{Loss}} \times 100 = \frac{50}{50 + 2.91} \times 100 = 92.63\% \tag{98}$$

Figure 6 illustrates the portion of each component in total power loss of the proposed converter. As it could be seen clearly, Diodes total loss are more than other elements. To have a comprehensive study, change of converter's efficiency versus output power change is depicted as Fig. 7.

To have a calculation approximately near to the real, inductor core losses are considered in all of calculations as follows:

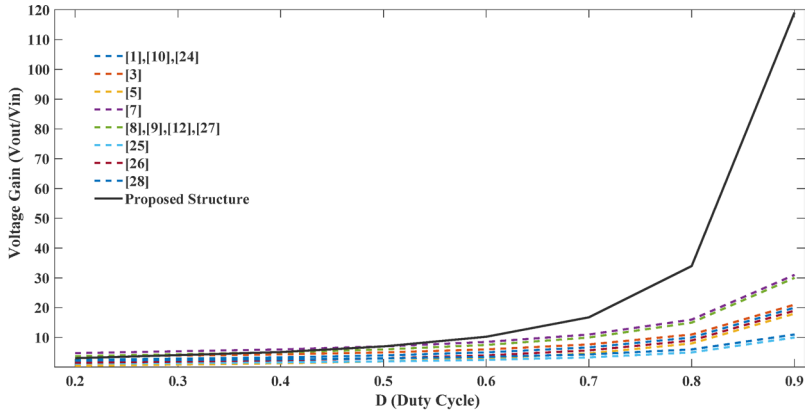
$$P_{core} = k f_s^a B_m^b M \tag{99}$$

$$P_{core} = k f_s^a (\frac{L_i I_{Li}}{N A_c})^b M \tag{100}$$

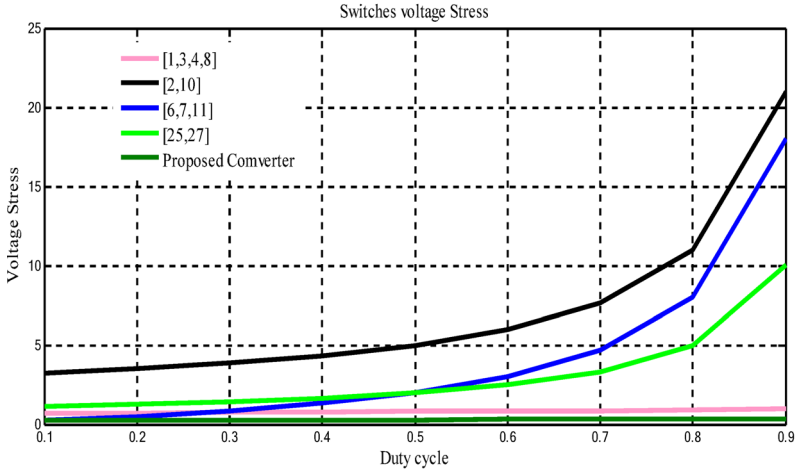
$$P_{core}^{L1} = 1.04w \tag{101}$$

$$P_{core}^{L2} = 0.0072w \tag{102}$$

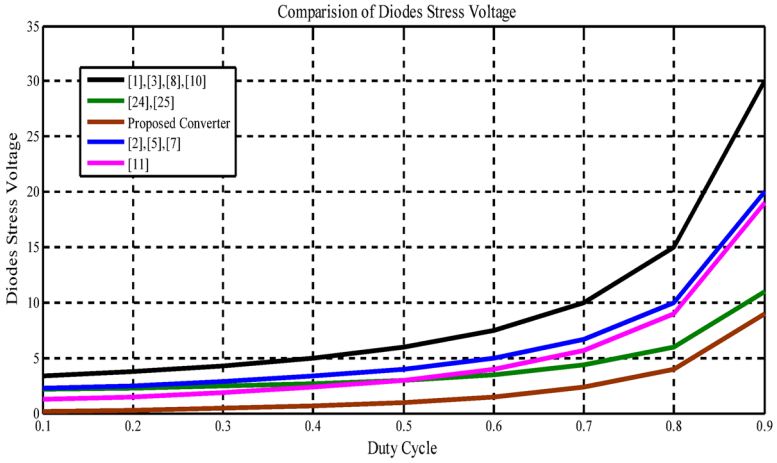
$$P_{core}^{L3} = 0.021w \tag{103}$$



(a)



(b)



(c)

Fig. 8. Comparison curves. (**a**) comparison of voltage gain of proposed converter with others, (**b**) Switches stress voltage, (**c**) diodes blocking voltages.

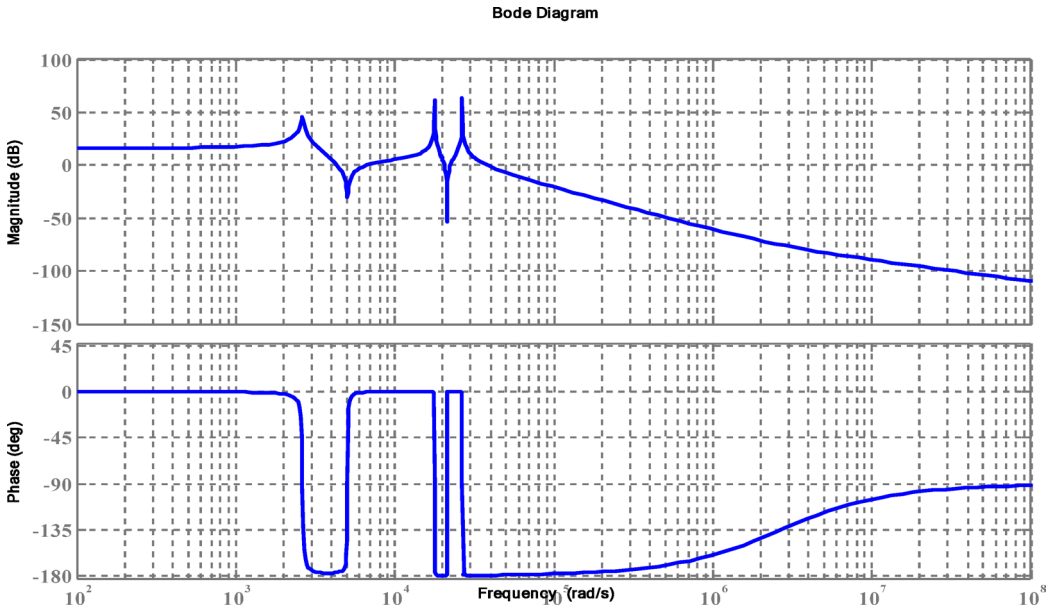


Fig. 9. Phase and gain margin of proposed converter transfer function.

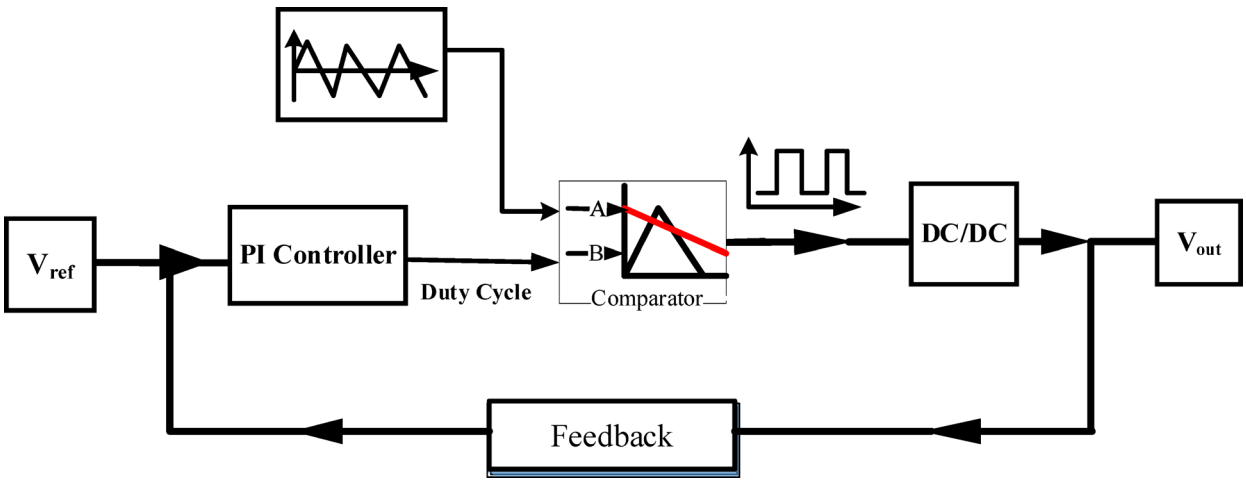


Fig. 10. Close loop block diagram.

$$Total - Loss = 3.98w \tag{104}$$

$$\eta\% = \frac{P^{out}}{P^{out} + P^{Loss}} \times 100 = \frac{50}{50 + 3.98} \times 100 = 91.63\% \tag{105}$$

Comparison Study

To assess the effectiveness of the proposed high-gain DC–DC converter, an extensive benchmark study was carried out against several existing topologies. Table 1 summarizes the main attributes of the suggested design and compares them with converters reported in [15–27]. The comparison considers aspects such as the number of components, overall device count, voltage gain, peak stress across switches and diodes, nominal power capacity, and input current ripple. In the voltage gain expressions of converters that utilize a coupled inductor, the parameter N denotes the turns ratio between the secondary and primary windings. This factor significantly impacts voltage gain performance. By contrast, the proposed topology is transformerless and does not rely on N, thereby avoiding leakage inductance, EMI, and additional losses typically associated with coupled-inductor-based converters. Figure 8a presents the voltage gain profile of the proposed topology in relation to other boost converters. The results indicate that the proposed design delivers a substantially higher voltage gain. This characteristic is particularly advantageous, as it enables the converter to achieve the required output at relatively low duty cycles. Operating at lower duty ratios reduces conduction losses and, consequently, enhances efficiency. Figure 8b compares the maximum voltage stress on the switches. The proposed converter

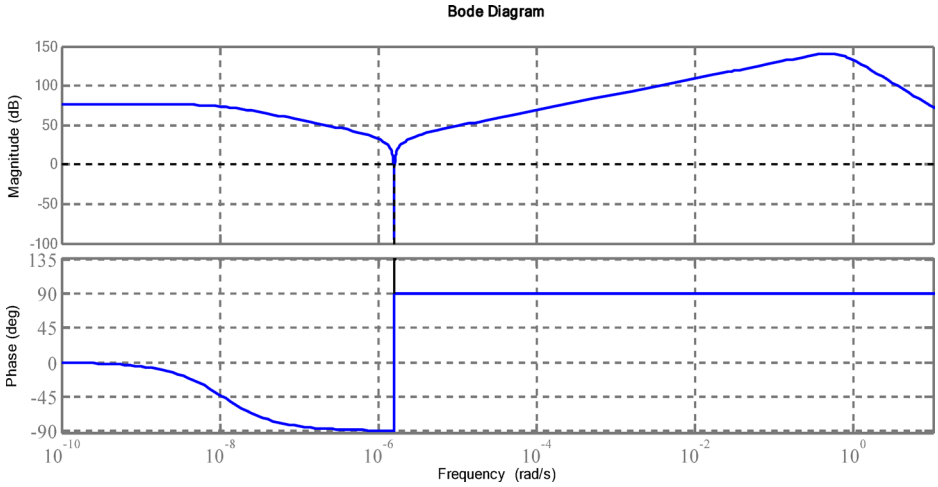


Fig. 11. Closed-loop bode diagram.

Parameters and Components	Value	Parameters and Components	Type or Value
V_o	200 V	*Switch* S_1,S_2	*IRFP* 260n
P_o	200 W	D_1	*MUR* 1560G
V_{in}	20 V	D_2	*MUR* 1560G
f_s	50 kHz	D_3	*MUR* 1560G
L_{in}	150 µH	D_4	*MUR* 1560G
C_1	10 µF/ 350 V	C_2	10 µF/ 200 V
C_3	10 µF/ 200 V	C_O	470 µF/ 450 V
L_2	150 µH	L_3	150 µH

Table 2. Experimental data of laboratory prototype.

demonstrates lower stress levels compared to its counterparts, allowing the use of more affordable power switches. Furthermore, minimizing switch stress directly contributes to reducing power dissipation, thereby improving overall performance. Similarly, Fig. 8c examines the voltage stress imposed on diodes. The proposed design again exhibits considerably lower stress, ensuring both cost reduction and efficiency improvement by lowering conduction and switching losses. Another critical factor considered is the input current ripple. A low input ripple is vital for renewable energy systems and other sensitive applications, as it ensures stable and reliable operation. Converters in [15–19, 25], and [27], listed in the comparison table, exhibit relatively high ripple levels, which restricts their suitability for such applications. The results confirm that the proposed converter delivers superior efficiency in comparison to most of the existing designs, with the exception of the configurations in [19, 23], and [26], which demonstrate slightly higher performance. In conclusion, the comparative analysis demonstrates that the proposed converter outperforms conventional designs by offering higher voltage gain, reduced stress on switching devices, and lower input current ripple. These features establish it as a strong candidate for high step-up power conversion applications.

Dynamic performance

In this section, average-state- space method has been used to give the transfer function. By employing Kirchhoff's voltage and current law, the function includes: state, input and control variable are formulated as an equation of the output and state variables. All assumptions to write state-space equations are listed as follows:

- The value of input voltage source of the proposed converter is adjusted in the constant value.
- All of utilized inductors and series resistance of them are considered equal to L_1=L_2=L_3=L and r_l, respectively
- All of utilized capacitors and series resistance of them are considered equal to C_1=C_2=C_3=C and r_c

By considering these conditions, there are 6 independent state variables. Equation (79) show the state-space form of the output variables.

$$\begin{aligned}[\dot{x}_i(t)] &= [A][\widehat{x}_i(t)] + [B][\widehat{u}_i(t)] \\ [\widehat{y}_i(t)] &= [C][\widehat{x}_i(t)] + [D][\widehat{u}_i(t)]\end{aligned} \tag{106}$$

Equations (79) illustrates the state variables and input variables vectors.

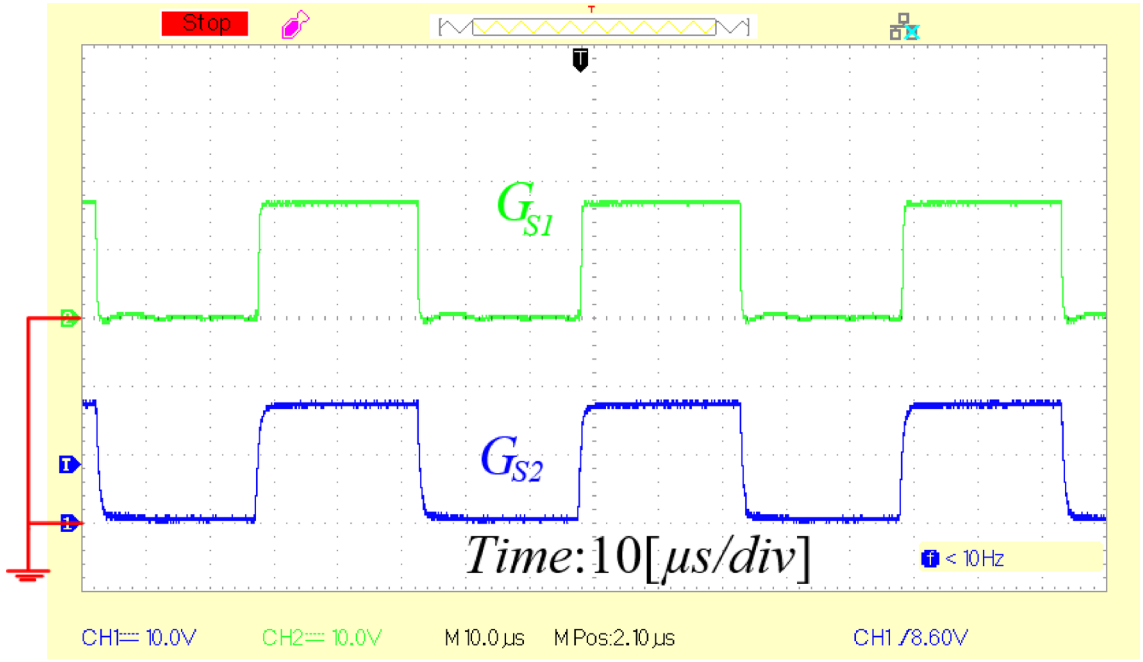


Fig. 12. switching pattern of G_1 and G_2.

$$\begin{aligned}[\widehat{x}] &= [\widehat{i}_{L1}\ \widehat{i}_{L2}\ \widehat{i}_{L3}\ \widehat{v}_{C1}\ \widehat{v}_{C2}\ \widehat{v}_{C3}]\\ [\widehat{u}] &= [v_{in}]\\ [\widehat{y}] &= [\widehat{i}_{in}\ \widehat{v}_o]\end{aligned} \tag{107}$$

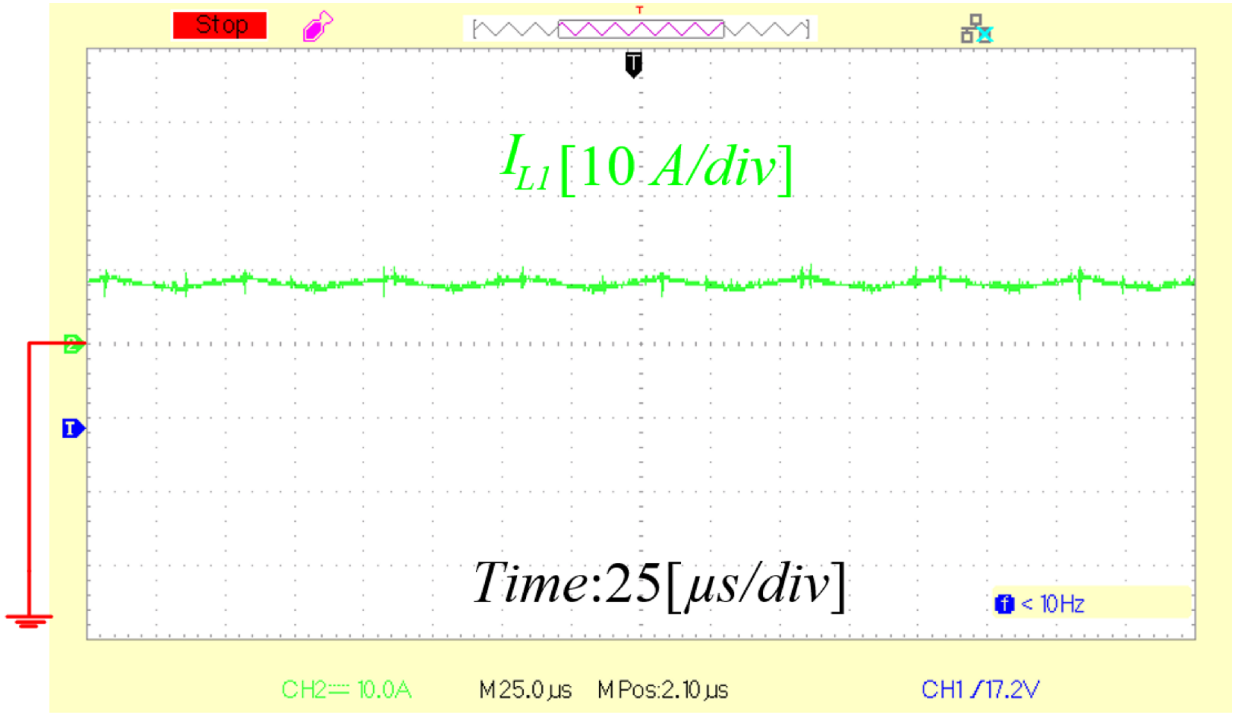
Steady state equations in intervals $(0 \le t \le (D)\,T)$ which both of S_1 and S_2 are on, are written as follows:

$$\begin{pmatrix} i'_{l1}\\ i'_{l2}\\ i'_{l3}\\ v'_{c1}\\ v'_{c2}\\ v'_{c3}\end{pmatrix} = \begin{bmatrix} -\frac{r_l}{l_1} & 0 & 0 & 0 & 0 & 0\\ 0 & -\frac{r_l}{l_2} & \frac{r_c}{l_2} & \frac{1}{l_2} & -\frac{1}{l_2} & 0\\ 0 & \frac{r_c}{l_3} & \frac{r_c}{l_3} & \frac{1}{l_3} & 0 & 0\\ 0 & -\frac{1}{c1} & -\frac{1}{c1} & 0 & 0 & 0\\ 0 & \frac{1}{c2} & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0 & 0\end{bmatrix} \times \begin{pmatrix} i_{l1}\\ i_{l2}\\ i_{l3}\\ v_{c1}\\ v_{c2}\\ v_{c3}\end{pmatrix} + \begin{pmatrix} \frac{1}{l}\\ 0\\ 0\\ 0\\ 0\\ 0\end{pmatrix} v_{in} \tag{108}$$

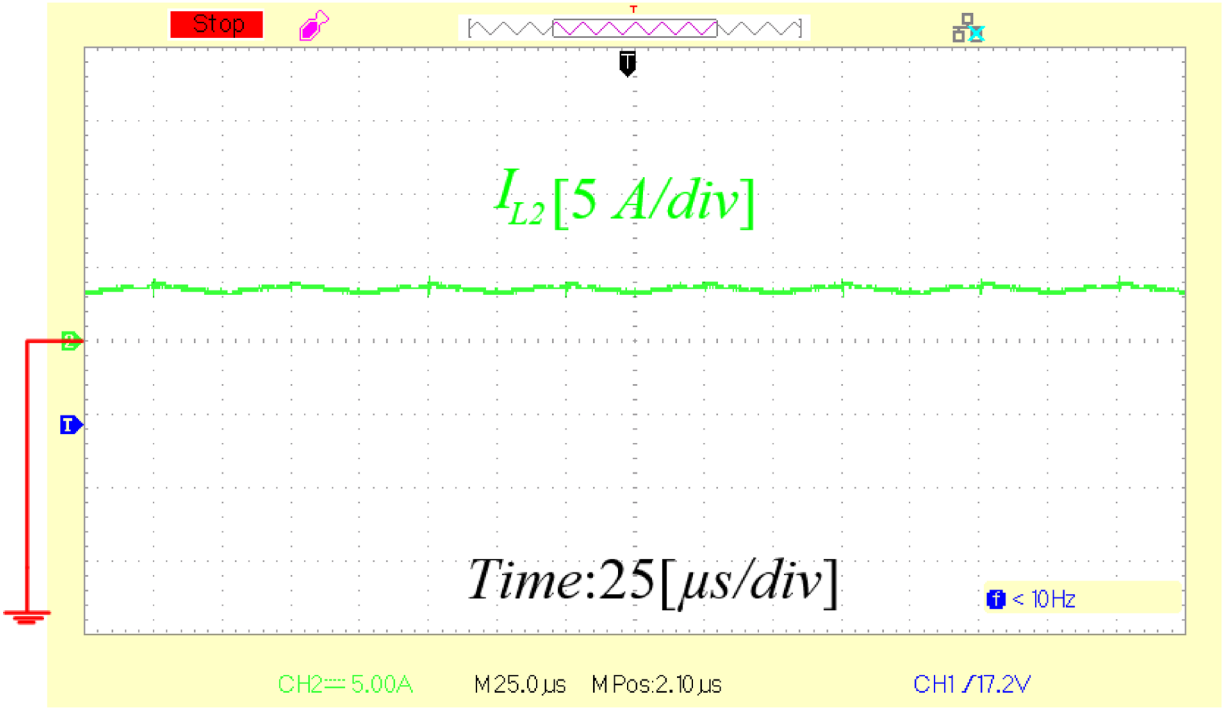
The mentioned equations in interval $(DT \le t \le T)$ which G_2 is on, is written as follows:

$$\begin{pmatrix} i'_{l1}\\ i'_{l2}\\ i'_{l3}\\ v'_{c1}\\ v'_{c2}\\ v'_{c3}\end{pmatrix} = \begin{bmatrix} -\frac{r_l+r_c}{l_1} & 0 & \frac{2r_c}{l1} & \frac{-1}{l1} & 0 & 0\\ 0 & -\frac{r_l+r_c}{l_2} & \frac{r_c}{l_2} & 0 & -\frac{1}{l_2} & 0\\ \frac{r_c}{l3} & 0 & -\frac{2r_c+r_l}{l_3} & \frac{1}{l_3} & 0 & 0\\ \frac{1}{c1} & 0 & -\frac{2}{c1} & 0 & 0 & 0\\ 0 & \frac{1}{c2} & -\frac{1}{c2} & 0 & 0 & 0\\ 0 & 0 & \frac{1}{c3} & 0 & 0 & 0\end{bmatrix} \times \begin{pmatrix} i_{l1}\\ i_{l2}\\ i_{l3}\\ v_{c1}\\ v_{c2}\\ v_{c3}\end{pmatrix} + \begin{pmatrix} \frac{1}{l}\\ 0\\ 0\\ 0\\ 0\\ 0\end{pmatrix} v_{in} \tag{109}$$

by considering Eq. (84), transfer function of the proposed converter is achieved as;

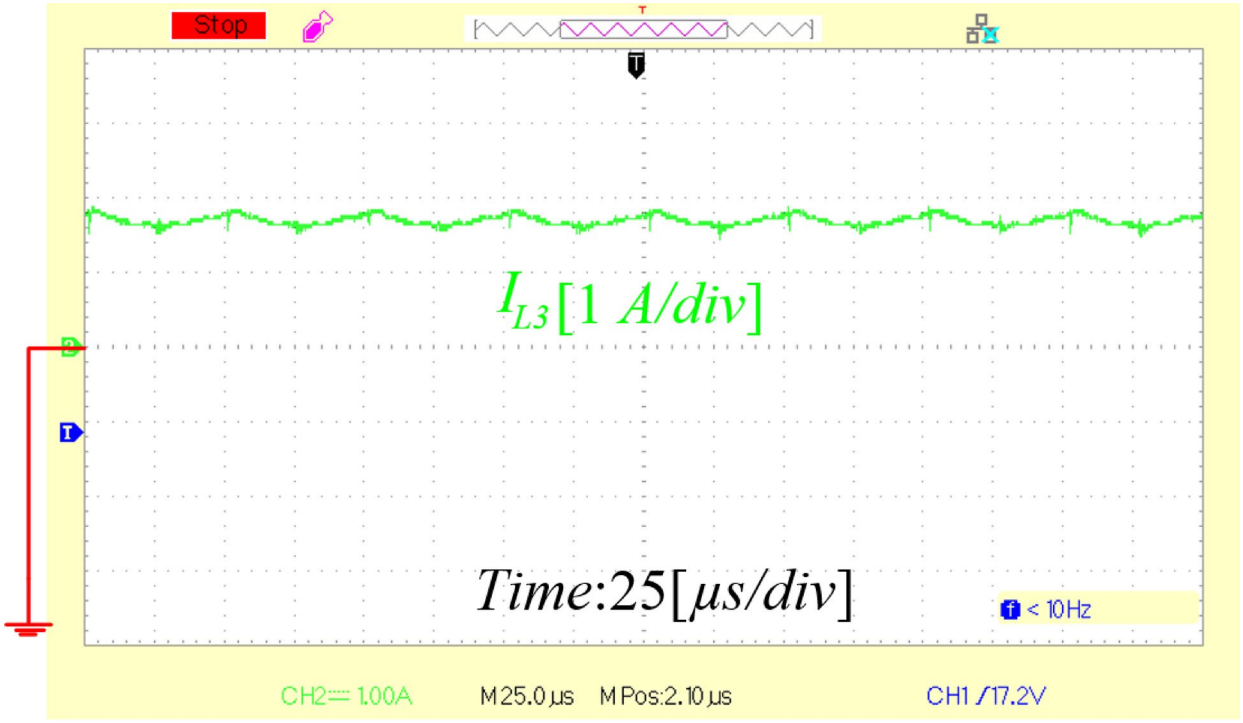


(a)



(b)

Fig. 13. Experimental Results. (**a**) current waveform of L_1, (**b**) current waveform of L_2, (**c**) current waveform of L_3.



(c)

Fig. 13. (continued)

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{328s^5 + 8.7E8s^4 + 2E11s^3 + 4.18E17s^2 + 2.6E19s + 1E25}{s^6 + 93.3s^5 + 1.03E9s^4 + 8E10s^3 + 2.3E17s^2 + 1.4E19s + 1.5E24} \tag{110}$$

Figure 9 illustrates the phase and gain margin of Eq. (84).

To make a stability discussion, close-loop model and diagram are figured as Fig. 10.

To improve stability of close-loop model, by PID controller is used. Pole placement technique is used to equivalent model poles. To adjust PID controller, Ziegler and Nichols, tuning technique is used as follows [29]:

$$C(s) = Kp \times (1 + \frac{1}{T_i S} + T_d s) \tag{111}$$

where: $T_i = 4 \times T_d$

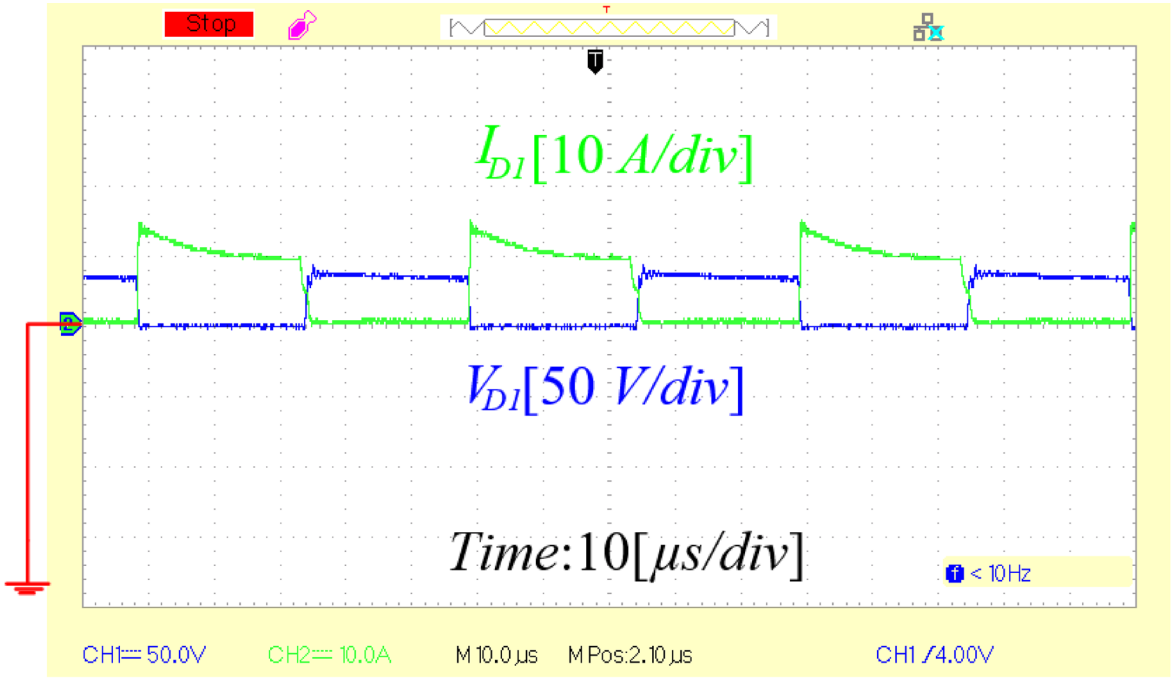
To improve phase margin with utilizing PID controller, the new transfer function is achieved as follows:

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{51s^5 + 8.7E4s^4 + 48E6s^2 + 23.4E7s + 1E12}{s^6 + 83.6s^5 + 1.03E3s^4 + 8E4s^3 + 1.4E19s + 2.8E24} \tag{112}$$

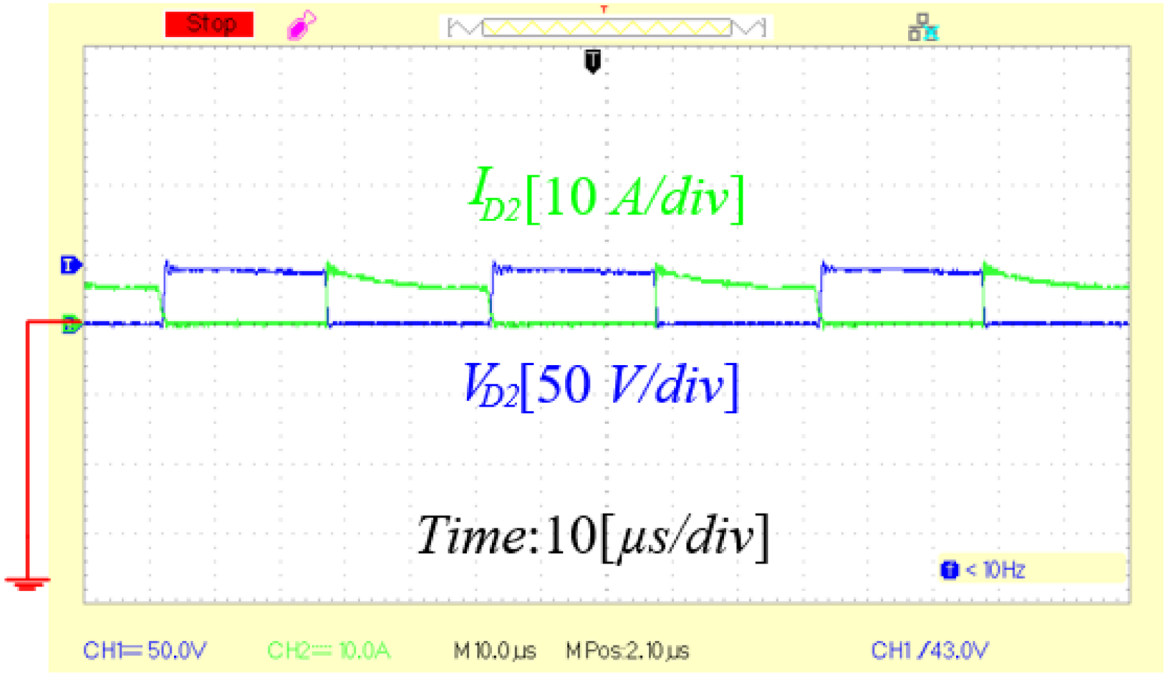
Figure 11 illustrates the bode diagram of close loop model with adjusted PID controller.

Experimental results

To validate the theoretical analysis and demonstrate the practical applicability of the proposed high-gain converter, a 200 W experimental prototype was developed. The key design specifications are provided in Table 2. Figure 12 presents the gating signals applied to switches S_1 and S_2. The measured inductor currents, displayed in Fig. 13a–c, closely follow the values derived from Eqs. (63–65), confirming the accuracy of the analytical model.

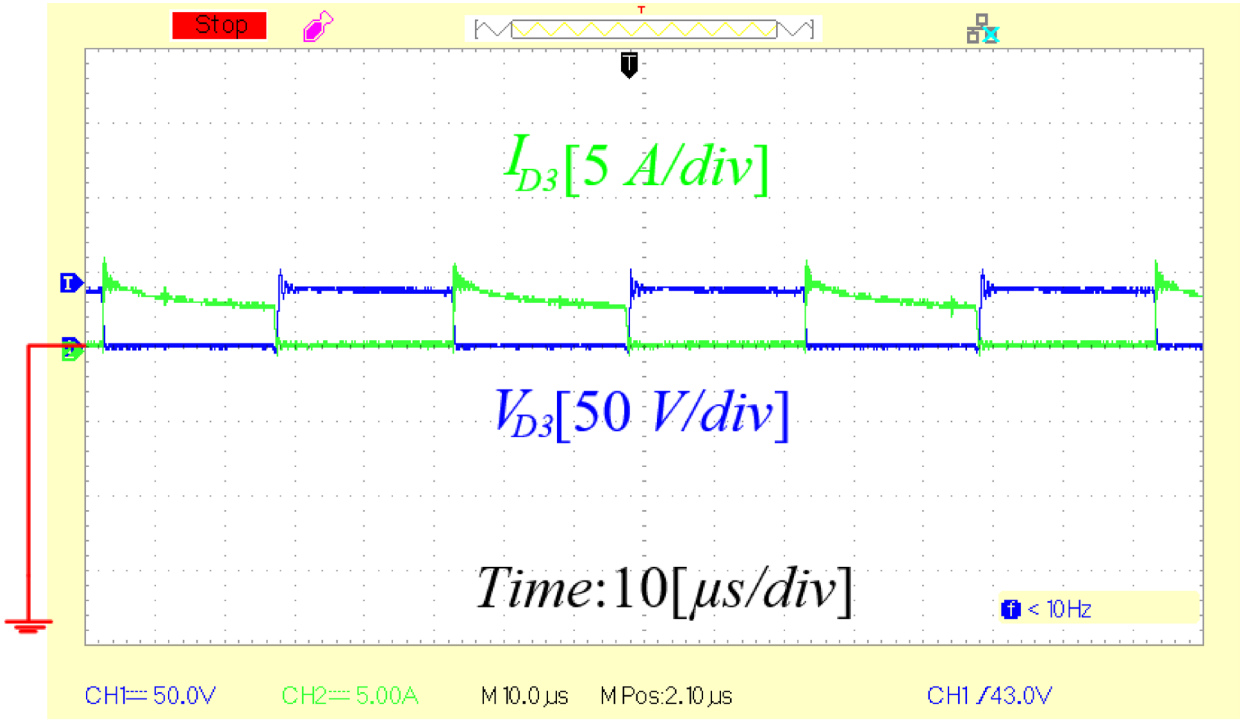


(a)



(b)

Fig. 14. Experimental Results for diodes, (**a**) Voltage and current waveform of D_1, (**b**) Voltage and current waveform of D_2, (**c**) Voltage and current waveform of D_3.



(c)

Fig. 14. (continued)

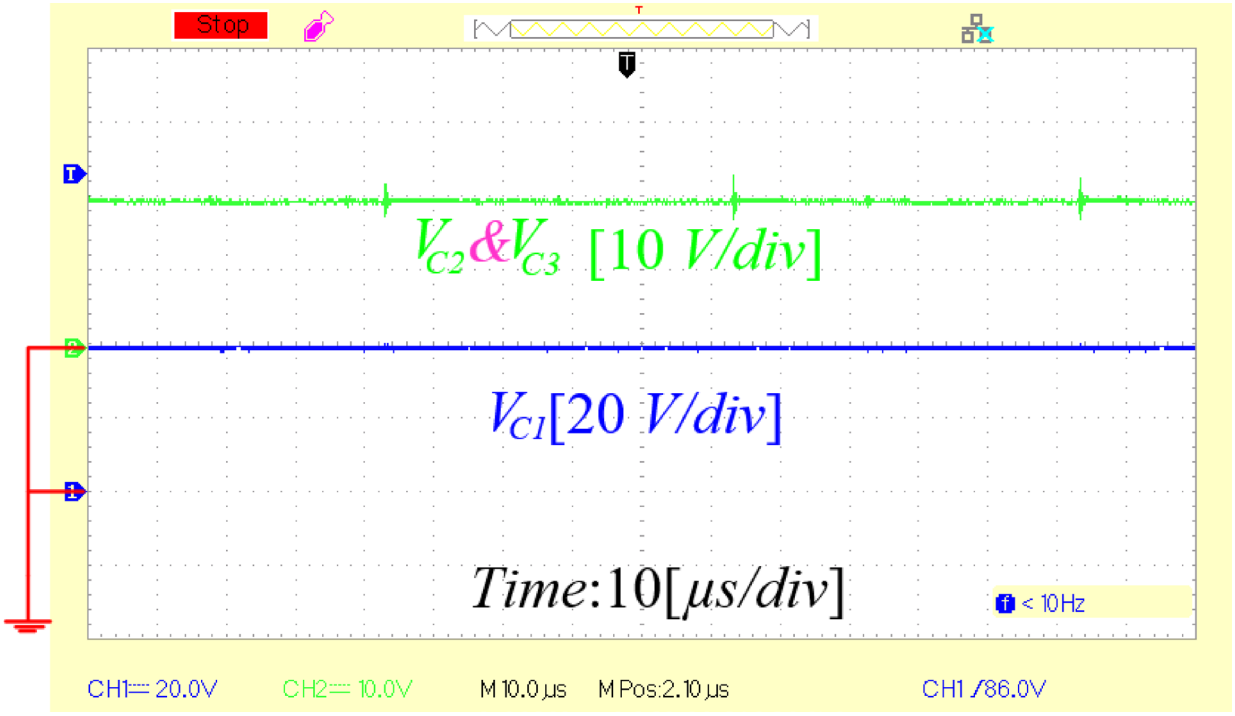


Fig. 15. Capacitor's voltages.

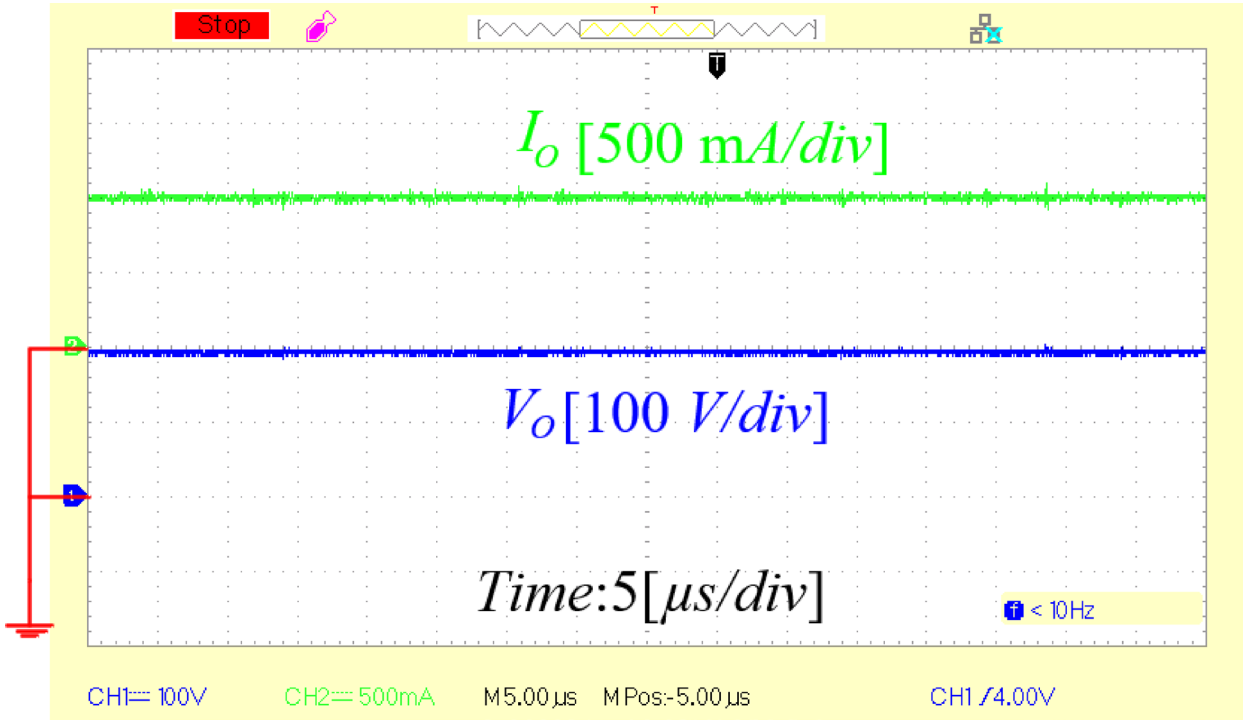


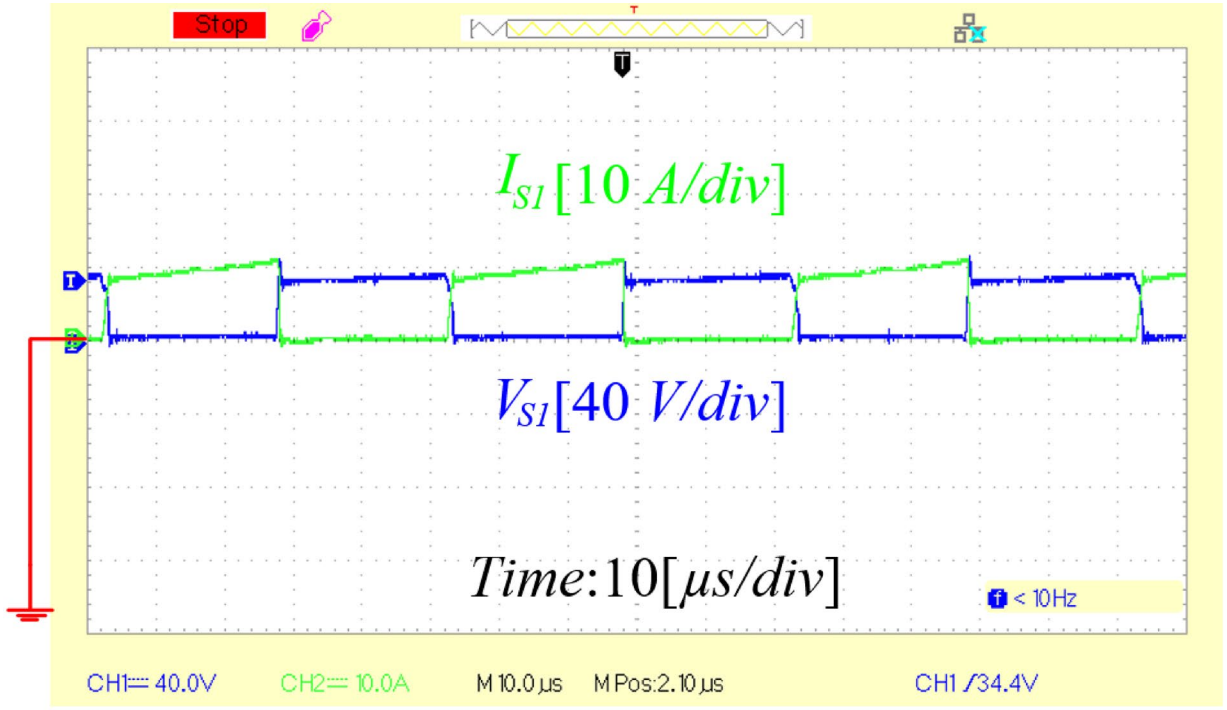
Fig. 16. Output voltage and current.

Experimental results also verify the current and voltage stresses on the diodes. As shown in Fig. 14a, diode D_1 conducts 13 A at 37 V. Diode D_2 sustains 38 V and 9 A [Fig. 14b], while D_3 operates at 38 V and 5 A [Fig. 14c]. Capacitor voltages are consistent with theoretical predictions as well: Fig. 15 records 37 V across C_1 compared to the calculated 40 V from Eq. (11), and around 19 V across C_2 and C_3, which is close to the expected values from Eqs. (13) and (15). The prototype also delivers an output voltage of 195 V with a current of 1 A, as indicated in Fig. 16. These values are in strong agreement with the predicted 200 V from Eq. (16). Switching device stresses were further examined: Fig. 17a shows that S_1 is subjected to a maximum of 36 V and 10 A, while Fig. 17b indicates that S_2 withstands 75 V and 14 A. Both sets of measurements are consistent with the calculated results. In summary, the strong correlation between the analytical expectations and the experimental observations across Figs. 13–17 confirms the correctness of the theoretical analysis and validates the high performance of the proposed converter.

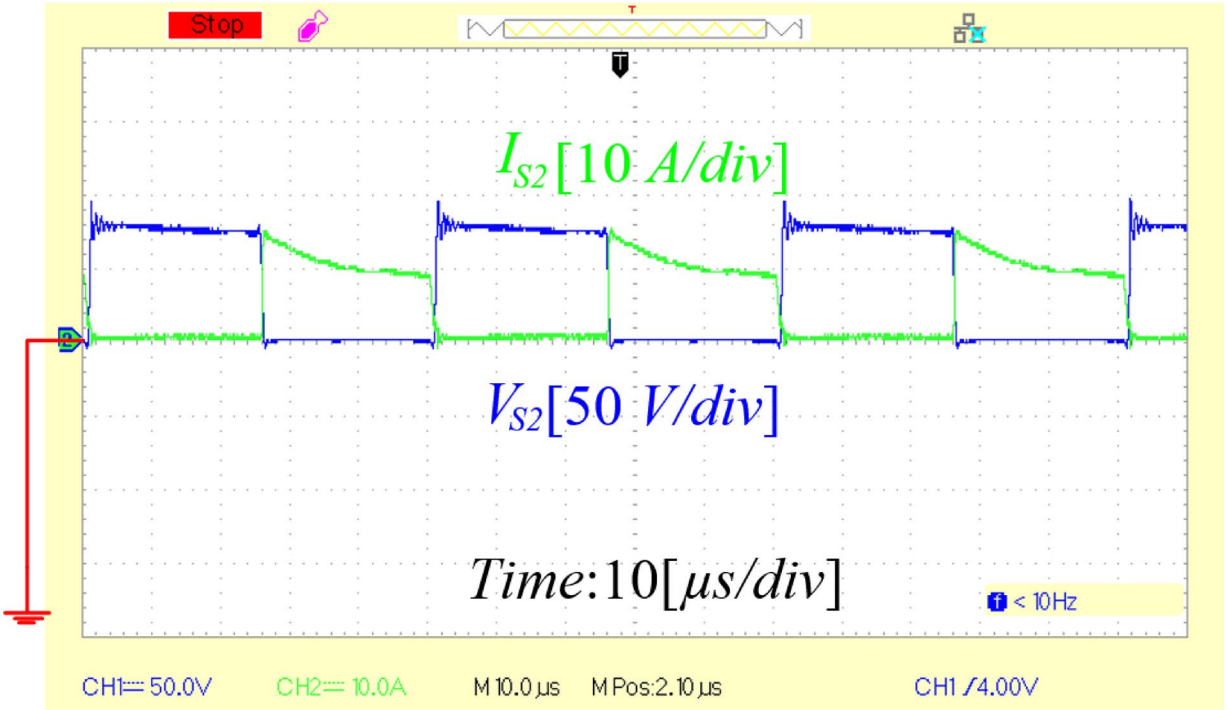
The proposed converter was tested under various load conditions and input values. In Fig. 18a, the output voltage of the converter initially registers around 96 V with a power output of about 200 W. When the load is suddenly altered and the output power is adjusted to 300 W, the output voltage remains relatively stable after brief transient fluctuations. The output voltage deviates only slightly from the reference value, demonstrating the stability of the closed-loop system in maintaining the output voltage close to the target. Figure 18b depicts the output voltage response when the input voltage suddenly drops from 20 to 15 V. It is evident from Fig. 18b that the output voltage shows minimal variation in response to the input change. Figure 19 illustrates the prototype of the proposed step-up converter.

Conclusion

This paper introduces a quadratic high step-up topology designed to minimize input current ripple, specifically tailored for DC microgrid applications. Low-power and low-voltage implementations of this topology typically support output ranges from a few watts to several tens of watts, with voltage levels spanning from 12 to 100V. The proposed converter is particularly well-suited for powering small-scale systems, including sensors, communication devices, and low-power appliances such as LED lighting. Additionally, it plays a major role in regulating the output of residential fuel cells (typically between 24 and 100V) to align with the operating voltage requirements of the microgrid. The suggested topology provides several notable advantages, such as increased voltage gains, lower voltage stress on switching components, continuous input current, a shared ground between the input and output, high efficiency, and synchronized switch operation. The adaptability of this topology makes it ideal for a wide range of applications, including robotics and switch-mode power supplies. In industrial environments, it effectively regulates DC motor speeds in assembly lines by controlling the DC link voltage.

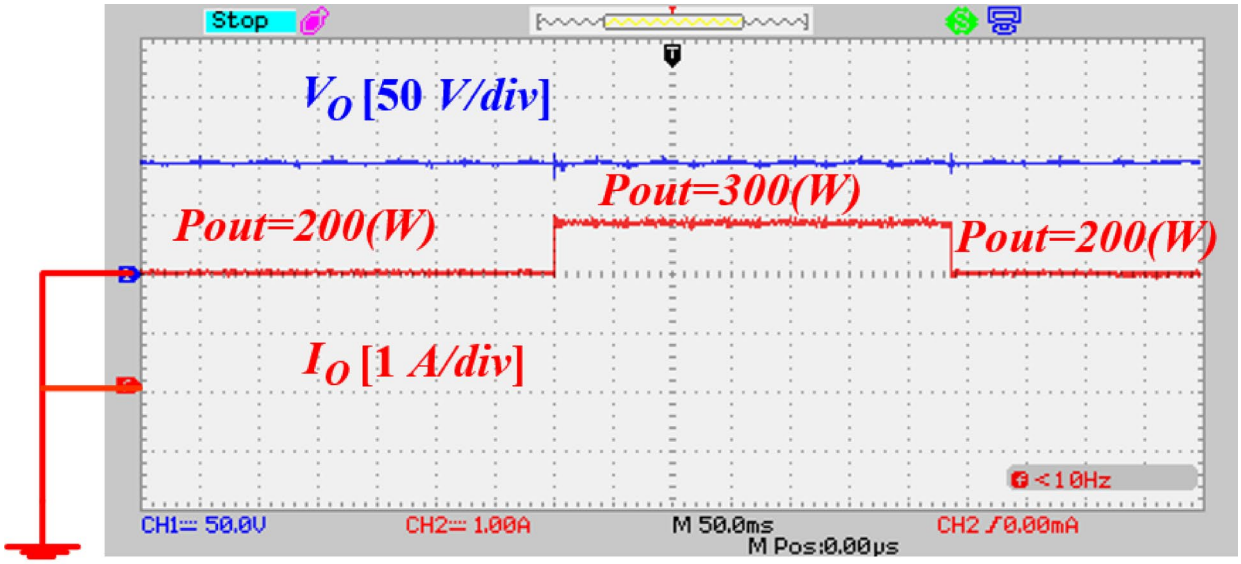


(a)

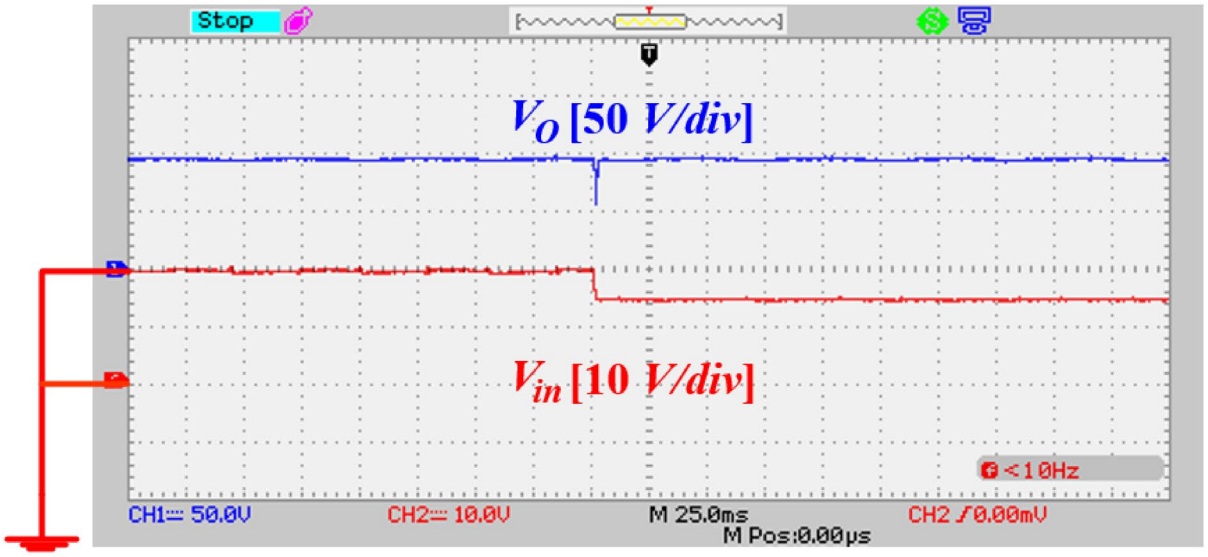


(b)

Fig. 17. Experimental Results for the power switches. (**a**) voltage and current of switch S_1, (**b**) voltage and current of switch S_2.



(a)



(b)

Fig. 18. Dynamic response of the proposed converter, (**a**) step change of the load, (**b**) step change of the input voltage.

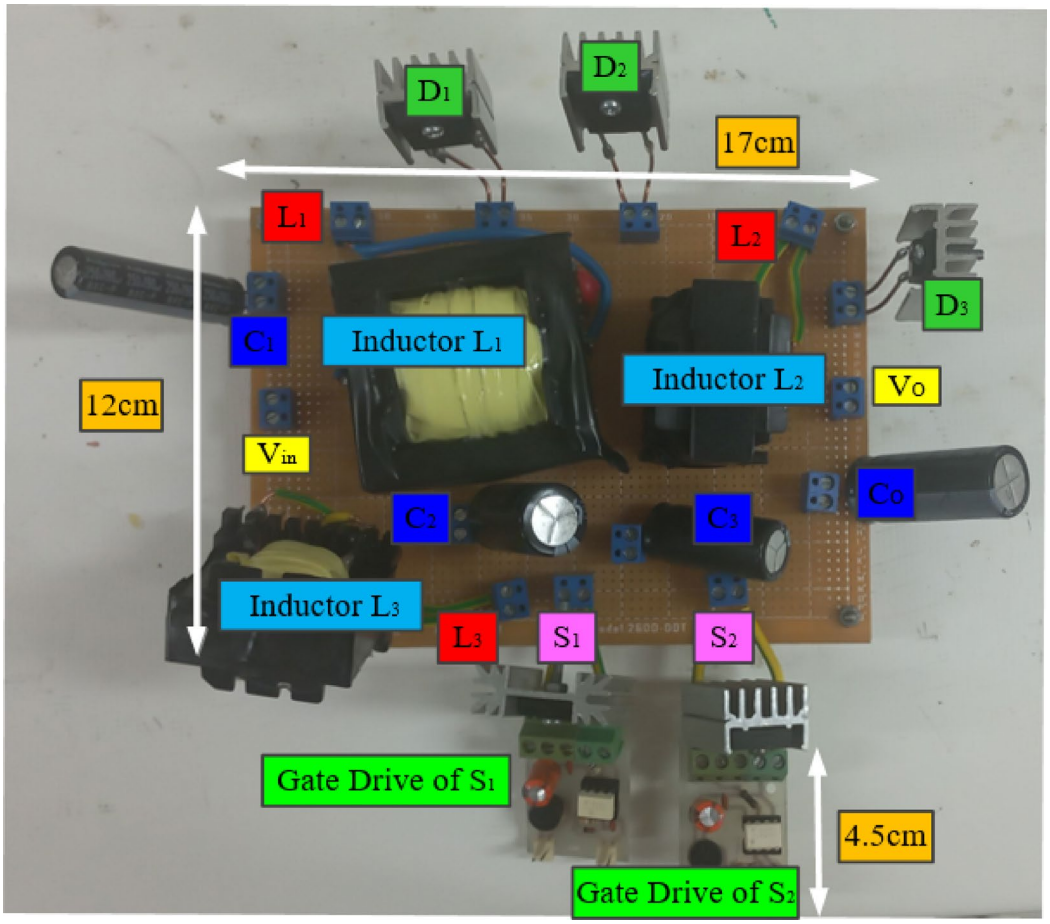


Fig. 19. Experimental model.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Received: 26 June 2025; Accepted: 30 October 2025
Published online: 11 December 2025

References

1. Jia, P. & Yuan, Y. Analysis and design of an isolated high step-up converter based on the secondary side quasi-resonant loops. *IET Power Electr.* **13**, 1129–1143 (2020).
2. Jia, P. et al. An isolated high step-up converter based on the active secondary-side Quasi-resonant loops. *IEEE Trans. Power Electr.* **37**, 659–673 (2021).
3. Jin, T. et al. A New Three-Winding Coupled Inductor High Step-Up DC-DC Converter Integrating with Switched-Capacitor Technique. IEEE Transactions on Power Electronics, 2023.
4. Alghaythi, M. L. et al. A high step-up interleaved DC-DC converter with voltage multiplier and coupled inductors for renewable energy systems. *IEEE Access* **8**, 123165–123174 (2020).
5. Seo, S.-W., Lim, D.-K. & Choi, H. H. High step-up interleaved converter mixed with magnetic coupling and voltage lift. *IEEE Access* **8**, 72768–72780 (2020).
6. Mohammadi, F. Khorsandi, A. Dual- input single- output high step- up DC–DC converter for renewable energy applications. IET Power Electronics, 2024.
7. Kumar, C. & Raj, T. D. A new non-isolated high-step-up DC–DC converter topology with high voltage gain using voltage multiplier cell circuit for solar photovoltaic system applications. *J. Circuits Syst. Comput.* **30**, 2150014 (2021).
8. Nadermohammadi, A. et al. Cost-effective soft-switching ultra-high step-up DC–DC converter with high power density for DC microgrid application. *Sci Rep* **14**, 20407. https://doi.org/10.1038/s41598-024-71436-w (2024).
9. Xu, P. et al. non-isolated switching-capacitor-integrated three-port converters with seamless PWM/PFM modulation. *Sol. Energy* **224**, 160–174 (2021).
10. Paramasivam, SK, et al. Solar photovoltaic based dynamic voltage restorer with DC-DC boost converter for mitigating power quality issues in single phase grid. Energy Sources, Part A: Recovery, Utilization, and Environmental Effects, 2021, 1–25.
11. Lagudu, J. V. & Vulasala, G. Maximum energy harvesting in solar photovoltaic system using fuzzy logic technique. *Int. J. Ambient Energy* **42**, 131–139 (2021).
12. Banaei, M. R. & Bonab, H. A. F. A high efficiency nonisolated buck–boost converter based on ZETA converter. *IEEE Trans. Industrial Electr.* **67**, 1991–1998 (2019).

13. Nanda, H., Sharma, H., Yadav, A. Design and Implementation of a High-gain Switched-capacitor Step-up Multi-level Inverter with Reduced Components Count. Electric Power Components and Systems, 2024, 1–12.
14. Kariyat, V. K. P. & Janardhanan, J. J. Design and development of modified highly efficient high gain DC-DC converter for SPV standalone systems. *Int. J. Power Electr. Drive Syst. (IJPEDS)* **14**, 1562–1576 (2023).
15. Radmanesh, H., Jashnani, H., Pourjafar, S. & Maalandish, M. A dual-output single-input non-isolated DC-DC converter with reduced semiconductors stress. *Int J. Circ. Theor Appl.* **51**(2), 594–610 (2023).
16. Jalilzadeh, TBE. Maalandish, M, "Generalized Non-isolated High Step-Up DC-DC Converter with ReducedVoltage Stress on Devices", International Journal of Circuit TheoryandApplications. https://doi.org/10.1002/cta.2506.
17. Zhang, Y., Zhou, L., Sumner, M. & Wang, P. Single-switch, wide voltage-gain range, boost DC–DC converter for fuel cell vehicles. *IEEE Trans. Veh. Technol.* **67**(1), 134–145. https://doi.org/10.1109/TVT.2017.2772087 (2018).
18. Zhu, B., Wang, H., Vilathgamuwa, M. "Single Switch High Step-up Boost Converter Based on a Novel Voltage Multiplier," IET Power Electronics. https://doi.org/10.1049/iet-pel.2019.0567.
19. Banaei, M. R. & Bonab, H. A. F. A Novel Structure for SingleSwitch Nonisolated Transformerless Buck-Boost DC-DC converter. *IEEE Trans. Industr. Electron.* **64**(1), 198–205. https://doi.org/10.1109/TIE.2016.2608321 (2017).
20. Elsayad, N., Moradisizkoohi, H. & Mohammed, O. A. A SingleSwitch Transformerless DC–DC Converter With Universal Input Voltage for Fuel Cell Vehicles: Analysis and Design. *IEEE Trans. Veh. Technol.* **68**(5), 4537–4549. https://doi.org/10.1109/TVT.2019.2905583 (2019).
21. Tang, Y., Fu, D., Wang, T. & Xu, Z. Hybrid switched-inductor converters for high step-up conversion. *IEEE Trans. Industr. Electron.* **62**(3), 1480–1490 (2014).
22. Tang, Y., Wang, T. & He, Y. A switched-capacitor-based activenetwork converter with high voltage gain. *IEEE Trans. Power Electron.* **29**(6), 2959–2968 (2013).
23. Sharifiyana, O. et al. Presenting a new high gain boost converter with inductive coupling energy recovery snubber for renewable energy systems-simulation, design and construction. *J. Solar Energy Res.* **8**, 1417–1436 (2023).
24. Hu, R. et al. A non-isolated bidirectional DC–DC converter with high voltage conversion ratio based on coupled inductor and switched capacitor. *IEEE Trans. Industrial Electr.* **68**, 1155–1165 (2020).
25. Sanjeevikumar, P. et al. non-isolated sextuple output hybrid triad converter configurations for high step-up renewable energy applications. In: *Advances in Power Systems and Energy Management*. Springer, Singapore, 2018. p. 1–12.
26. Spiazzi, G. et al. non-isolated high-step-up DC–DC converter with minimum switch voltage stress. *IEEE Transactions on Power Electronics*, 2018, 34.2: 1470–1480.
27. Kurdkandi, N. V. & Nouri, T. Analysis of an efficient interleaved ultra-large gain DC–DC converter for DC microgrid applications. *IET Power Electronics* **13**(10), 2008–2018 (2020).
28. Zaoskoufis, K. & Tatakis, E. C. Isolated ZVS-ZCS DC–DC High Step-Up Converter With Low-Ripple Input Current. *IEEE Journal of Emerging and Selected Topics in Industrial Electronics* **2**(4), 464–480 (2021).
29. Nouri, T. & Shaneh, M. A new interleaved ultra-large gain converter for sustainable energy systems. *IET Power Electronics* **14**(1), 90–105 (2021).
30. Tarzamni, H. et al. non-isolated high step-up dc-dc converters: comparative review and metrics applicability. IEEE Transactions on Power Electronics, 2023.
31. Farahani, H. J., Rezvanyvardom, M. & Mirzaei, A. Non-isolated high step-up DC–DC converter based on switched-inductor switched-capacitor network for photovoltaic application. *IET Generation, Trans. Distribution* **17**, 716–729 (2023).
32. Zamani, M. et al. Design and Implementation of Non-isolated High Step-Up DC-DC Converter. International Transactions on Electrical Energy Systems, 2023.
33. Rajabi, A. et al. A non-isolated high step-up DC-DC converter using voltage lift technique: analysis, design, and implementation. *IEEE Access* **10**, 6338–6347 (2022).
34. Karimi Hajiabadi, M. et al. Non-isolated high step-up DC/DC converter for low-voltage distributed power systems based on the quadratic boost converter. *Int. J. Circuit Theory Appl.* **50**(6), 1946–1964 (2022).
35. Dastgiri, A., Hosseinpour, M. & Poulad, A. A high step-up non-isolated DC-DC converter with active switched-inductor and switched-capacitor networks. *Int. J. Model. Simulation* **43**(4), 462–473 (2023).
36. Nadermohammadi, A. et al. A non-isolated single-switch ultra-high step-up DC–DC converter with coupled inductor and low-voltage stress on switch. *IET Power Electron.* **17**, 251–265 (2024).
37. Taheri, D., Shahgholian, G. & Mirtalaei, M. M. Analysis, design and implementation of a high step-up multi-port non-isolated converter with coupled inductor and soft switching for photovoltaic applications. *IET Generation, Trans. Distrib.* **16**(17), 3473–3497 (2022).

Funding

The authors declare that no funds, grants, or other support were received during the preparation of this manuscript.

Declarations

Competing interests

The authors have no relevant financial or non-financial interests to disclose.

Additional information

Correspondence and requests for materials should be addressed to R.R.

Reprints and permissions information is available at www.nature.com/reprints.

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.