



OPEN Low power and high-speed quadrate node upset tolerant latch design using CNTFET

Shaik Asiya^{1,3} & Satheesh Kumar S^{2,3}✉

Scalability, leakage, short-channel effects, and reliability problems are some of the difficulties facing the semiconductor industry as it continues to experience a reduction in size. Heavy charged particles striking an integrated circuit (IC) cause a Single Event Upset (SEU). As devices are scaled down, it usually causes Single and Multiple Node Upset. To overcome the upsets, device and CMOS circuit radiation hardening by design (RHBD) techniques are adopted. In the recent times, Carbon nanotubes have emerged as a feasible technology capable of addressing CMOS problems while maintaining performance and reliability. This manuscript proposes a Low power High speed Quadrate Node Upset Carbon Nanotube latch (LHCNT). The LHCNT latch contains three Dual Interlocked cells with a delta interconnection design, supplying enough redundant nodes to ensure robustness to Multi Node Upsets due to charge sharing. The investigation includes simulation, and performance comparison of a LHCNT latch with an existing hardened latch. The LHCNT latch obtained the power, delay, PDP and APDP as 4.4 μ W, 1.23 ps, 5.41e-18 and 5.19e-2 respectively with a supply voltage of 1 V. Results from simulations show that the proposed LHCNT latch archives low power, delay, and APDP of any latch with a comparable soft error tolerance level.

Keywords Radiation hardening, Soft errors, Single event upset, Carbon nano tubes, Delta DICE

Radiation-induced soft errors, including SEU and MNU, present major reliability concerns in nano electronic circuits. CNTFET have gained attention as a viable replacement for CMOS technology due to their high carrier mobility, energy efficiency, and robustness against process variations. However, like MOSFETs, CNTFETs remain vulnerable to radiation-induced charge increase, necessitating the use of enhanced hardening strategies to mitigate these effects.

Radiation hardening

Reliability is essential for safe and vital electronic systems. Space-related integrated circuits (ICs) are vulnerable to alpha particles from packaging materials and heavy charged particles from cosmic rays^{1,2}. When radiation particles affect a sensitive node, they create several electron-hole pairs. Single-Node-Upset (SNU) occurs when a node's total free charge exceeds its critical charge³. Multiple-Node-Upset (MNU) happens whenever a high-energy particle strikes multiple critical nodes simultaneously due to the charge sharing event⁴. To limit the destructive effects of radiation exposure on semiconductor devices, researchers modified process technologies, layout, and circuit design to create radiation-hardened circuit structures. Circuit-level hardening technology, known to be efficient and convenient, is gaining much interest and research in radiation hardening due to the high cost and complexity of advanced techniques and designs^{5,6}.

The latch is an essential memory component in the logic circuit. To solve MNU complications, the latch circuit adopts RHBD techniques with Muller C-elements (MCE) and radiation hardening materials at the device and layout levels^{7,8}. The basic modules of the various MCEs⁹ are presented in Fig. 1. By employing redundant designs, the MCE are meant to prevent the spread of faults or restore circuit state. RHBD latches with MCE and/or DICE are capable of resisting SEU, despite also occupying up a significant amount of space, especially with MNU. Lowering the technology of CMOS transistors to 32 nm is challenging because of small channels, increased high leakage powers, and susceptibility to process modifications. As the size of transistors shrinks, the development of reliable and resilient CMOS circuitry becomes increasingly difficult and critical^{10,11}. Advanced technologies are desperately needed to enhance scalability above the 22/18 nm semiconductor nodes and outperform conventional CMOS.

¹School of Electronics Engineering, Vellore Institute of Technology (VIT), Vellore 632014, Tamil Nadu, India. ²School of Electronics Engineering, VIT-AP University, Amaravati 522241, Andhra Pradesh, India. ³Shaik Asiya and Satheesh Kumar S contributed equally to this work. ✉email: satheeshkumar.s@vitap.ac.in

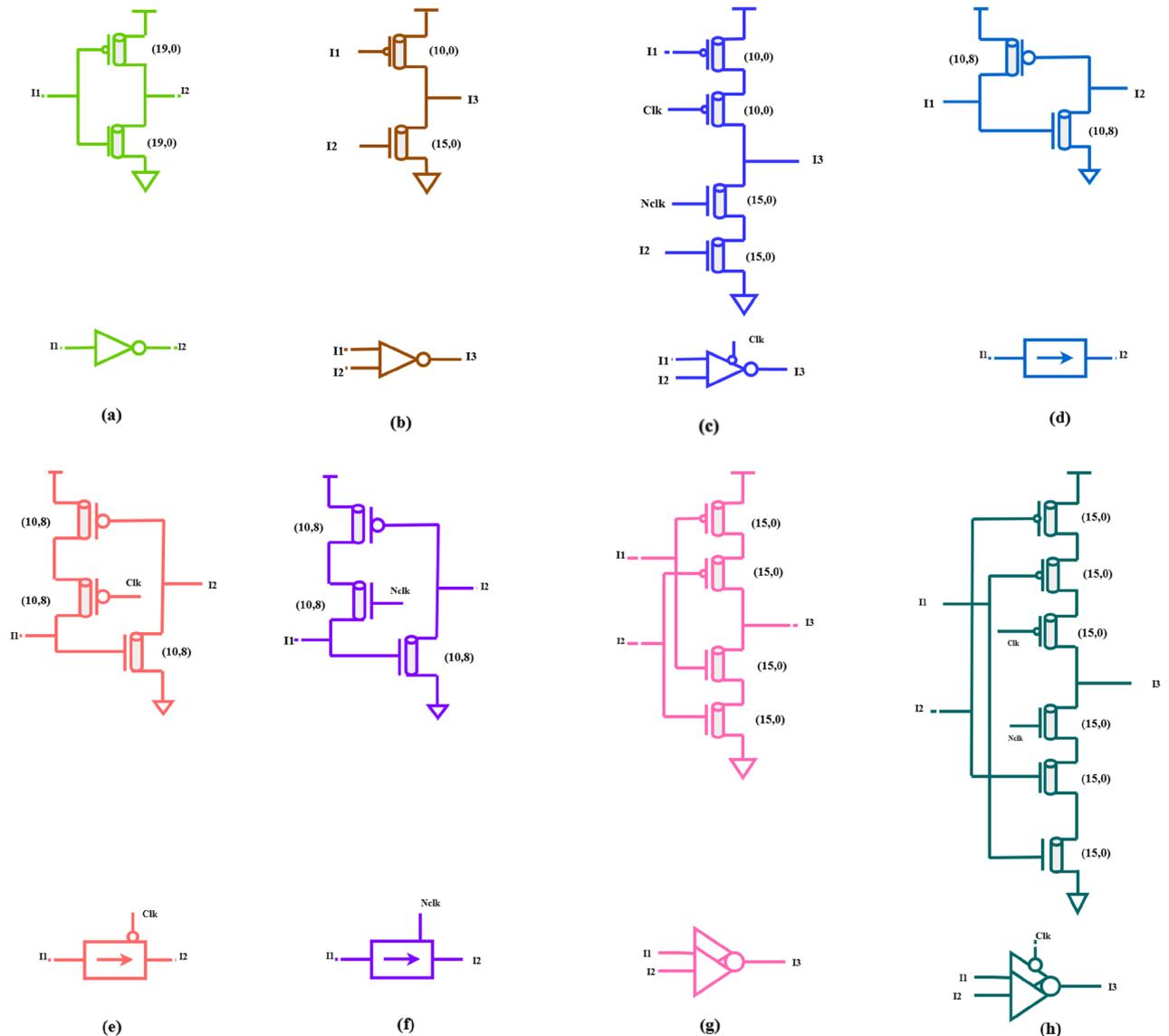


Fig. 1. CNTFET-based logic circuits and their corresponding circuit symbols: (a) Inverter, (b) Two-Input Inverter, (c) Clocked two -Input Inverter, (d) Cross Coupled inverter, (e) & (f) Positive & negative clock Cross Coupled Inverter, (g) C-element, (h) Clocked C-element.

As a result, developing the different methods in transistor technology is essential for overcoming obstacles. Carbon nanotube Field-effect transistors (CNTFETs) have attracted a lot of interest due to their similarities to MOSFETs and their potential for improved performance and energy efficiency. Because of their unique electrical characteristics, CNTFETs are very attractive to researchers studying nanoscale circuits and systems¹².

Carbon nano tube FET (CNTFET)

The best substitute for silicon transistors with respect to performance improvement and power consumption reduction is CNTFET^{13,14}. Plastic waste materials, which are currently exceeding 500,000 tons per year, are a major ecological problem. Out of these, 19% are polypropylene (PP). Particularly, PP plastic debris encompasses 86.7% carbon. Researchers can make advantage of substantial carbon sources to create carbon nanotubes¹⁵. CNTs exhibit incredible physical and chemical properties, making them an excellent substance for possible applications^{16,17}. The graphite sheets were then shaped into cylindrical structures that differ in diameter from less than one nanometer to 50 nanometers and lengths of a few micrometers. Carbon nanotubes (CNTs) have unique chemical, electrical, mechanical, thermal, and visual characteristics based on their proportional arrangement. These substances have outstanding field output characteristics and can contain a current density of 109 A/cm². They also have higher thermal conductivity than diamond, which is generally stated to be the most effective thermal conductor. They are also 100 times stronger than steel in terms of tensile strength¹⁸. Carbon nanotubes are divided into two categories.

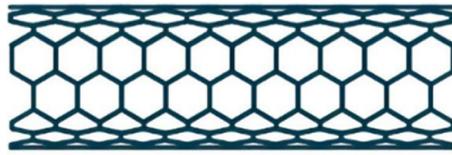


Fig. 2. Single-walled carbon nanotube (SWCNT)¹⁹.

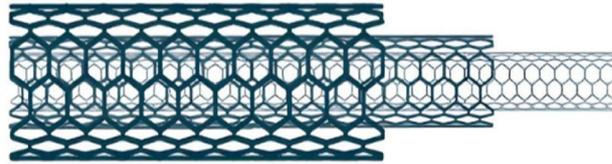


Fig. 3. Multi-walled carbon nanotube (MWCNT)¹⁹.

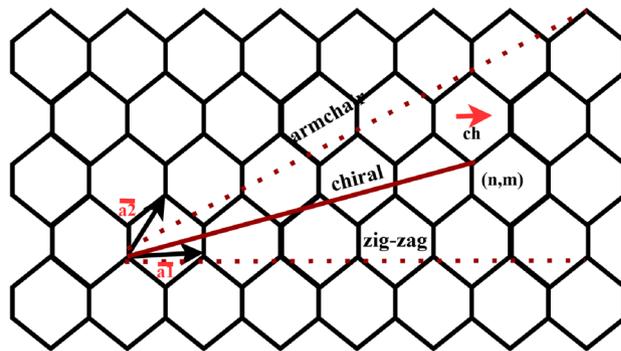


Fig. 4. Chirality Vector of graphene sheet in CNTFET³³.

1. Single walled -based carbon nanotubes (SWCNT).
2. Multi walled -based carbon nanotubes (MWCNT).

Figures 2 and 3 shows a tubular structure made up of two concentric, nested tubes. The principal object is a graphite monolayer comprising a thickness of one atom. The object is then subsequently rolled up until its outside edges are hidden, resulting in an idyllic cylindrical shape as shown in Figs. 2 and 3 respectively. An SWCNT’s chirality (Ch) determines whether it is metallic or semi-conductive. Chirality is the specific direction in which the graphene sheet originally rolled. Equations (1) and (2) provide numerical values for evaluating the correlation between carbon nanotube diameters. The n and m in Eq. (1) are positive integers and denote the tube chirality constants²⁰. DCNT in Eq. (2) represents the diameter of carbon nanotubes illustrated in Fig. 4.

$$Ch = a\sqrt{n^2 + m^2 + nm} \tag{1}$$

$$DCNT = \frac{Ch}{p} \tag{2}$$

Here “ $a = 2.4595$ ” which represents the graphite sheet lattice constant.

Equation (3) determines the width of CNTFET

$$W = (N - 1) S + DCNT \tag{3}$$

where,

N—nano scale carbon tubes count in the CNTFET. S—spacing between inter-nanotubes. W—CNTFET width.

The threshold voltage (v_{TH}) of a CNTFET is determined based on the diameter of the carbon nanotubes in the channel region, using the following formula.

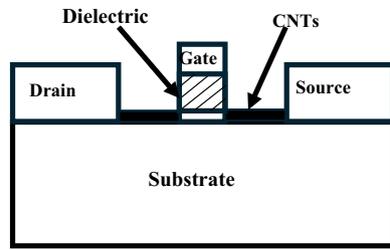


Fig. 5. Cross sectional view of a CNTFET.

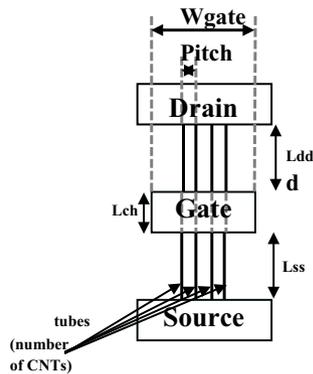


Fig. 6. Top view of a CNFET³³.

$$v_{TH} = \frac{aV_{\pi}}{eDCNT} \quad (4)$$

In the tight bonding model, $V_{\pi} = 3.033$ eV reflects the energy of the carbon 180° to 180° bond. By changing the diameter of the DCNT in Eq. (2), the CNTFET's v_{TH} value can be manually adjusted to the essential level. SWCNTs are suitable for use in photovoltaic devices including solar cells and molecular electronics, due to their exceptional electrical and optical characteristics²¹. CNTFET and CMOSFET devices are identical in function and structure. CNTFET technology has been suggested for usage in a variety of circuits, including digital and analog systems^{16–21}. A CNTFET operates similarly to a MOSFET, but it uses semiconducting carbon nanotubes in place of the conventional MOS transistor channel. The CNTFET's top and cross-sectional views are shown in Figs. 5 and 6.

According to Fig. 5, $DCNT$ is the diameter of the CNT, N represents the count of CNTs, and Pitch represents the centre-to-centre distance between two neighbouring CNTs in the channel region. The suggested designs employ $N = 1$, Pitch = 20 nm, with varied chirality values of CNTs (n, m) are (8,0), (10,0), (13,0), (15,0), (19,0) and (10,8) and the corresponding DCNT values are 0.63 nm, 0.79 nm, 1.03 nm, 1.18 nm, 1.15 nm and 1.2 nm respectively according to Eq. (2). The CNTFET model specifications that are significant for the simulation are presented in Table 1.

CNTFETs and traditional CMOS transistors are comparable in terms of their carrier transport mechanism and channel material. Ballistic or near-ballistic electron transport is made possible by CNTFETs' use of quasi-one-dimensional semiconducting carbon nanotubes to create the channel, which allows electrons to move across the channel with little to no scattering. However, as devices get smaller, electrons in CMOS transistors which are based on silicon are sensitive to frequent scattering occurrences. In CMOS, this results in elevated dynamic power consumption due to decreased carrier mobility and increased resistive losses. Additionally, CNTFETs have low off-state leakage currents and steep subthreshold slopes (< 60 mV/dec), which enable lower threshold voltages without reducing power efficiency. Since CMOS has short-channel effects and subthreshold leakage, this advantage can be challenging to achieve.

Furthermore, CNTFETs allow for threshold voltage tunability via chirality and nanotube diameter, providing fine control over power-performance trade-offs. In contrast, CMOS threshold tuning involves intricate doping and is more vulnerable to process variability. All these properties interact to give CNTFET-based circuits higher energy efficiency, especially at nanoscale nodes (less than 10 nm), where CMOS has serious scaling and leakage control issues. For contemporary ultra-low-power, high-performance digital circuits, CNTFETs provide a radically innovative and more effective route.

Parameter	Description	Value
L_{ch}	The channel's total length	32 nm
L_{geff}	The average free path that results caused from the intrinsic CNT channel region's non-optimal elastic scattering	100 nm
L_{ss}	The length of the doped CNT extension region on the source side	32 nm
L_{dd}	The length of the doped CNT extension region on the drain side	32 nm
E_{fi}	The doped source/drain CNT's Fermi level	0.6 eV
K_{gate}	The dielectric constant for HfO_2 (planar gate), a high-k substance utilized as the top gate dielectric	16
T_{ox}	The HfO_2 high-k top gate dielectric material's thickness in a planar gate setup	4 nm
VDD	Supply Voltage	1 V
	Features of CNTs applied in the channel area of CNTFETs	
Pitch	The separation among two neighbouring CNT centres inside the same device	20 nm
Tubes	CNTFET's channel region's amount of each form of CNT	1
(n, m)	CNT chirality values applied in the proposed designs	(8,0), (10,0), (13,0), (19,0)

Table 1. CNTFET model specifications are significant for the simulation.

Background

This section describes the radiation-hardening process that enhances latch designs against soft errors. The advantages and disadvantages/limitations of existing radiation-hardened latches are discussed. Finally, an overview of the proposed latch design is given to enhance fault tolerance, and power, delay, and space efficiency optimizations.

Upset mechanism in CNTFET inverter

Radiation upset in CNTFET electronics happens when intense particles strike sensitive locations. The reverse-biased electric field influences the collection of additional electron-hole pairs in the depletion layer after the striking. In this area, electrons are captured by NCNTFET transistors and holes by PCNTFET transistors²². Figure 7 illustrates the charge-collection process using an inverter, as described in^{10,11}, and²². A reverse-biased electric field affects the polarity of radiation-induced transient voltages, which varies by transistor type. In an OFF-state PCNTFET transistor, the voltage at the drain changes from '0' to '1' owing to hole accumulation. In the case of an OFF-state NCNTFET transistor, electron concentration drives the voltage at the drain to go from '1' to '0'.

Existing hardened latch design

Several traditional design elements such as Inverter (INV), 2-input inverter, clocked 2-input inverter, cross-coupled inverter, clocked cross-coupled inverter, dual-input C-element (CE), and clocked dual-input C-element (CG-CE) presented in Fig. 1, were included to provide a strong and self-recoverable CNT latch. The basic part of the Delta DICE is the cross-coupled element, as presented in Fig. 1d¹³. Normally, the values of I1 and I2 stay at 1 or 0. If I1 and I2 are equal to 1, any soft errors that occurs due to heavy ion particle being applied to any of them do not spread to other nodes. A positive pulse at I1 causes the fault to go to I2, where it produces a negative pulse. On the other hand, if I2 experiences a negative pulse, the error spreads to I1, resulting in a positive pulse. The C-element in Fig. 1 (g) functions according to the concept that the output (I3) assumes the opposite value when two inputs (I1 and I2) are equal. I3 maintains its initial logic value while going into a high-impedance state when there are different inputs present.

In Fig. 1 (b), a typical inverter's single input can be splitting to create a dual-input inverter. To assure PCNTFET driving capabilities, the dual-input inverter CNT will set the NCNTFET tube chirality as (15, 0) and the PCNTFET tube chirality as (10, 0). The truth table of Dual-input inverter circuit is presented in Table 2. The symbol Z represents a high impedance state. In the absence of SEU, the dual-input inverter circuit operate normally, synchronizing with the NCNTFET/PCNTFET inputs. When there is a SEU, its input-output connection shows that the output logic state changes only when both the NCNTFET/PCNTFET inputs transition from 0 to a phase in which the PCNTFET input is 0 and the NCNTFET input is 1. The NCNTFET and PCNTFET transistors are both activated at the same time in this case. NCNTFET tubes have a stronger driving ability than PCNTFET tubes. As a result, the output is disrupted, switching from 1 to 0. The response of the dual-input

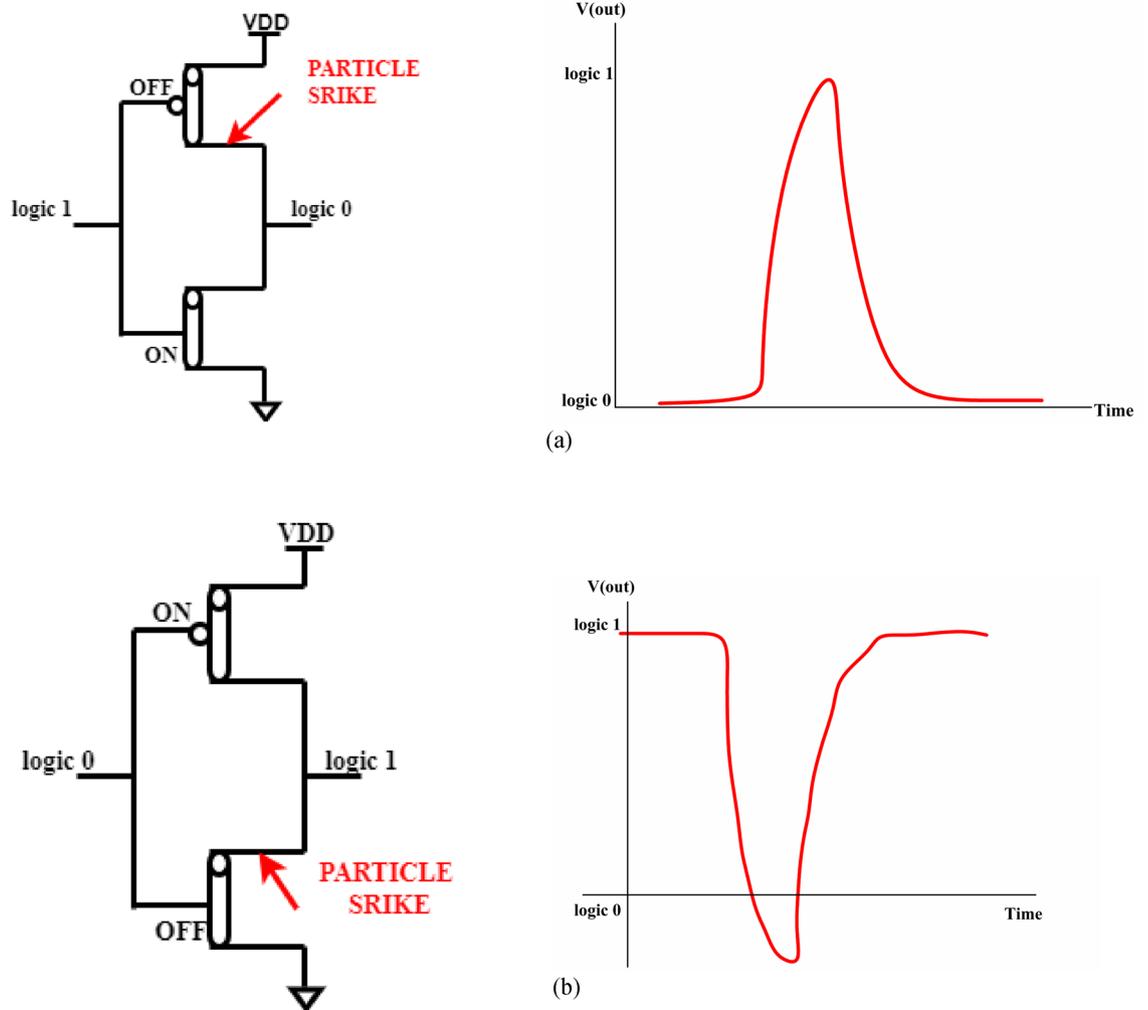


Fig. 7. Upset mechanism in: (a) p-CNTFET, (b) n-CNTFET.

I1	I2	I3 (output)
1	1	0
0	0	1
1	0	Z
0	1	0

Table 2. Truth table of dual-input inverter.

inverter remains constant in other operating modes due to the isolation of defects at a specific node. NCNTFET defects influence the inverter's output only during a SEU.

The latch, depicted in Fig. 8(a) and built by Shakeel et al.²³, has SNU self-recovery capabilities while consuming less power and area. If the logic values of two nodes are upset simultaneously, the latch may generate an incorrect output. The Delta DICE latch, on the other hand, is made to recover from DNU. The triangle architecture of its three DICE units provides a small design with minimal area overhead. The absence of a clock-controlled element, however, causes a larger delay and higher power consumption. The Delta DICE latch consists of three DICE cells with cross-coupled inverters placed in a delta topology, which provides tolerance to both single and double node upsets⁹. In a similar vein, TNURL utilizes seven SIMs to improve TNU recoverability, but its non-existence of QNU tolerance means it remains susceptible to quasi-node interruptions, which increases the power and area overhead. The IHTRL latch's use in high-speed circuits is restricted by its high propagation delay (D-Q) and further area overhead caused by its 4 × 4 array structure.

The HTNURE latch is unreliable for high-speed applications because of its longer TNU recovery intervals and substantial power consumption from complex feedback loops. Comparable to this, the LTNUT latch's use of

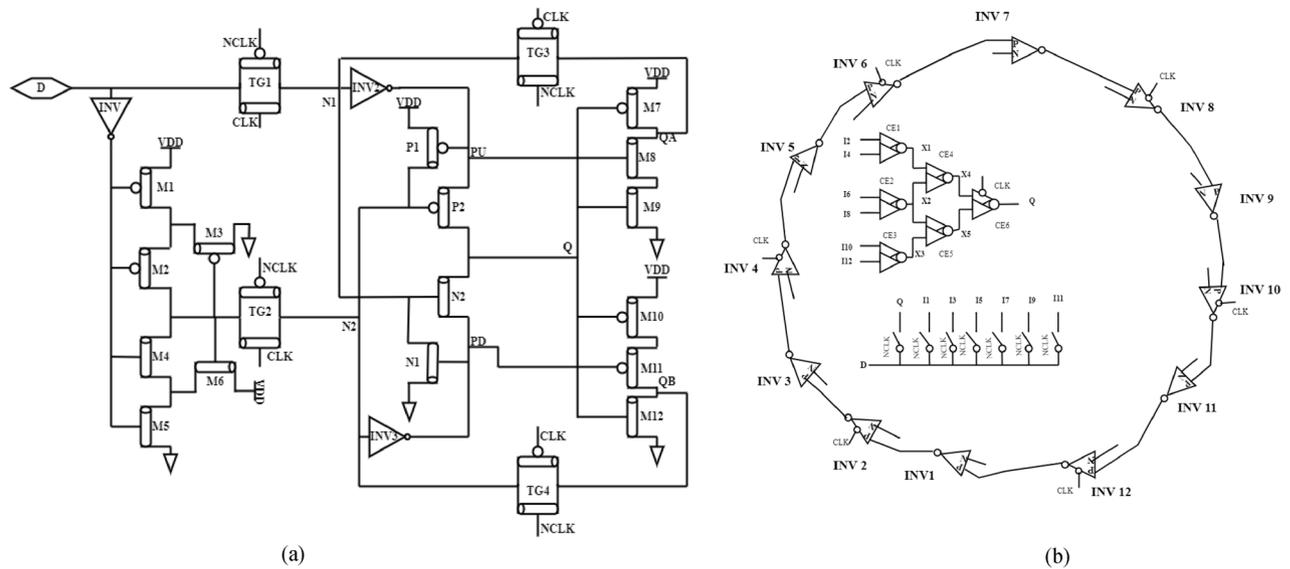


Fig. 8. Existing circuit implementations: (a) CNTFET-based design²³ (b) CMOS-based LCQNUT³³.

multi-level C-elements leads to significant power consumption and a more complex design. Although QNUTL fails to complete QNU self-recovery and optimized for QNU tolerance using a triple-level Soft-Error-Interceptive Module (SIM) and three DICE cells, it is vulnerable to latch in a fault in extreme conditions. It additionally increases circuit complexity and power consumption. While the HLTNURL latch provides TNU reliability, its feasibility in density nanoelectronics circuits has limitations due to its high-power consumption and significant silicon area overhead. The LCTNUCR latch design, a multiple clocked four-input C-elements (CEs), exhibits a substantial area overhead, which increases complexity and degrades performance in large-scale applications.

ADTRL has a larger area and longer delay time than the other design, but it consumes less power than other TNU-resilient latches. Designing the circuit is also more complicated by its modified DICE structure. The TSRL latch's quadrilateral regaining and its structure increase more transistors and complexity to the design, and its widespread usage of dual-input CEs causes a significant area overhead. A three-stage blocking module and two input inverters integrated with interlocked modules are features of the D-latch design (LCQNUT), which is shown in Fig. 8(b). The latch is resistant to Quadrate Node Upset QNU because of the efficient prevention of soft errors provided by these LCQNUT and blocking modules³³. However, using redundant modules a lot leads to higher power consumption and larger delays. Although QNUTL fails complete QNU self-recovery and optimized for QNU tolerance using a triple-level Soft-Error-Interceptive Module (SIM) and three DICE cells, it is vulnerable to latch in a fault in extreme condition. It additionally increases circuit complexity and power consumption. Even though many latch designs currently in use have the versatility of withstanding MNU, they frequently fail to provide full self-recovery and require trade-offs between power, area, and delay. Table 3 illustrates all the existing hardened latches, along with their methodologies, key features and challenges.

Proposed low power high speed quadrate node upset tolerant CNTFET latch(LHCNT)

This work proposes a novel LHCNT tolerant latch, specifically addressing the minimum delay and power constraints associated with the existing latch designs. The proposed LHCNT latch's schematic diagram is shown in Fig. 9. The LHCNT latch is designed with Seven transmission gates, a Delta DICE unit, twelve dual-input inverters (INV1 to INV12), and one inverter (INV). The twelve dual-input inverters exert complemented inputs and outputs to latch the data. Delta DICE is based on three DICE cells connected in a delta topology. The Delta DICE latch maintains dual interlocking's excellent DICE resilience against SNUs. In DNUs, the two possible outcomes nodes X1, X2, and X3 are constantly driven by two ON states ($N4=0$, $X2=1$) cross-coupled elements. The Delta DICE latch is insensitive to DNUs due to the realization that all three DICE cells have two nodes controlled by two ON cross-coupled components apiece. The Delta DICE latch retains the remarkable DICE robustness of dual interlocking against SNUs. The LHCNT has D and Q as input and output, as well as CLK and NCLK are system clocks. Internal nodes of the LHCNT latch include N1 through N12 and X1 through X3. When CLK is set to 1, all transmission gates (TGs) are ON, causing the latch to enter its transparent phase. And then odd nodes use dual input inverters to transfer data to even nodes, whereas even nodes use Delta DICE to send data to output node Q. Initialization can be completed by all nodes. Throughout the transparent phase, the Delta DICE-based feedback loop and INV2N ($N=1, 2, \dots, 6$) do not perform.

The latch is said to have entered its latch phase when all transmission gates (TGs) are turned off and NCLK is set to 1 and CLK becomes 0. Feedback loops between modules guarantee that the latch functions properly in this mode, while INV2N ($N=1, 2, \dots, 6$) and the Delta DICE are active. To thoroughly explain the QNU tolerance concept of the proposed latch, specific values are assigned with the assumption that $D=0$. In this case, consider the nodes Q, N1, N3, N5, N7, N9, and N11 are set to 0, while N2, N4, N6, N8, N10, and N12 are set to 1. The primary focus is generally on the latch mode operation. Initially, the analysis begins with an SEU scenario. If a

Design name	Author	Circuit description	Advantages	Limitations
Delta DICE ⁹	Eftaxiopoulos, N. et al., (2015)	Data is maintained on three interconnected DICEs, with shared nodes to improve error recovery	DNU self-recovery is provided, and the D-Q delay is reduced utilizing an inverter	TNU cannot be tolerated, and the various feedback loops result in high power consumption
TNURL ²⁴	A. Yan et al.(2020)	Employs seven SIMs to improve TNU recoverability through redundant data storage	By using interconnected SIMs, it assures reliability of data and exhibits strong resilience	Significant area overhead and power consumption; it is vulnerable to quasi-node disruptions because of its lack of QNU tolerance
IHTRL ²⁵	Huang Z, et al., (2021)	Enhance stability by integrating a 4 × 4 C-element array, four clock-gated CEs, and four transmission gates	Exhibits high error tolerance and lower delay	Its complex matrix design results in a significant area overhead, and the significance for high-speed applications is limited by its propagation delay (D-Q)
HTNURE ²⁶	Xu H., et al., (2021)	Comprises twelve 2-input CEs and six pass gates, design with a three-loop interlocked feedback system	Maintains precise data inputs by using feedback loops that are interconnected	Multiple feedback loops result in significant power consumption; a long recovery stage reduces effectiveness in real-time applications
LTNUT ²⁷	. Lu Y, et al., (2022)	Enhances SEU protection through the combination of an ISEHL latch with multi-level C-elements	Extremely efficient for space applications, which provides total defence against SEU for all nodes within including output	Multiple error-filtering stages result in significant power consumption, and the complex circuit design causes fabrication to be more difficult
QNUTL ²⁸	A. Yan, et al., (2022)	QNU tolerance can be obtained by using a triple-level Soft-Error-Interceptive Module (SIM) and three DICE cells	Can maintain QNU events while enhancing the reliability in radiation conditions	Higher power consumption and circuit complexity; incomplete QNU self-recovery, which could result in latching problems in extreme cases
HLTNURL ²⁹	Y. Dai., et al., (2022)	Increases TNU resilience by using a timing clock-gating method and feedback system	Provides strong TNU protection while maintaining data integrity under fault conditions caused on by radiation	Complex feedback as well as recovery connects lead to high power consumption; integration in small nano electronic systems is limited by a large silicon area
LCTNUCR ³⁰	S. Cai, et al., (2023)	It utilizes multiple clocked four-input C-elements to improve upset recovery	Achieves TNU self-recovery and provides strong fault tolerance in radiation-sensitive environments	A high transistor counts results in excessive area overhead making integration into large-scale circuits is challenging due to complex design
ADTRL ³¹	A. Yan, et al., (2023)	Uses three modified DICE cells and six transmission gates are employed to improve fault tolerance	Reduces power consumption compared to other TNU-resilient latches while offering robust node-upset resilience	The modified DICE structure increases design complexity, eventually resulting in greater area and minimum delay
TSRL ³²	Y. Bai, et al., (2024)	A quadrilateral recovery structure which includes four clock-gated dual-input CEs and twelve dual-input CEs	Recoverable from any possible TNUs with a robust error correction system	The use of several dual-input CEs results in a large area overhead and prolonged recovery periods for TNU faults

Table 3. Summary of various existing hardened latch designs.

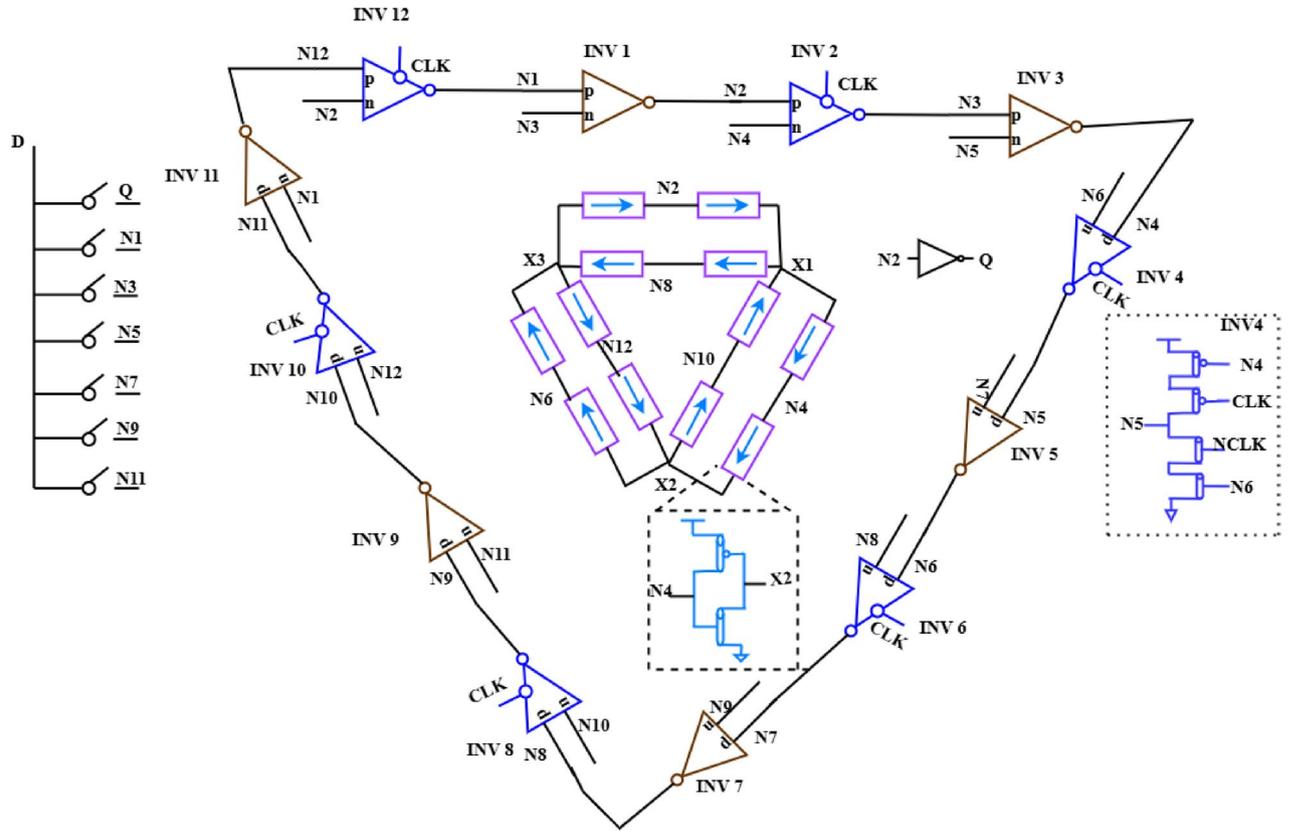


Fig. 9. Proposed low power high speed quadrate node upset carbon nanotube (LHCNT).

fault occurs, an NCNTFET malfunction affecting the output of dual-input inverters may result in one of three possible outcomes, as outlined in Table 2.

Single node upset analysis

Case 1: Consider N4 as an illustration of an even node that has been flipped in the storage module. Although CNTFET tubes in INV4 are conducting, N4 is flipped from 1 to 0. However, the N5 output node is not affected. No other nodes are impacted, and the output Q remains unchanged.

Case 2: Consider node N11 as an example of an odd node flipped in the storage module. When N11 changes from 0 to 1, both of INV11’s transistors conduct. As NCNTFET is more capable of driving than PCNTFET, node N12 is driven to zero. The issue spreads to INV12, although it is essentially stopped. INV11 finally sets N11 back to 0.

Case 3: An issue occurred in the Delta DICE module. The delta interconnection topology module nodes retain their logical states, while the faulty nodes within the interception module can be easily repaired using the nodes from the interconnection nodes.

Dual node upset analysis

Case 1: The analysis indicates that both the Delta DICE and the intercepting modules can self-recover from node upset if an error happens in both.

Case 2: If double node upsets originate inside the interception module. Considering the event of a failure at node pair <N3, N5>. When nodes N3 and N5 are flipped from 0 to 1, INV3 and INV5’s NCNTFET transistors turn on, resulting nodes N2 and N4 to zero. INV8’s node N6 is stable in the meantime and will restore N5. The output Q remains unchanged due to no changes in the remaining nodes.

Case 3: Consider the double node upset in the Delta DICE module. The output Q can be maintained while the error nodes in this module are quickly restored due to the Delta DICE nodes.

Triple node upset analysis

Case 1: An upset occurring on any three nodes of the Delta DICE, will be restored by the interception module.

Case 2: Triple node upset occurring in interception module. Consider the node pair N7, N9, and N11 flipped from 0 to 1; the NCNTFET transistors in INV5, INV7, and INV9 turn on, resulting nodes N6, N8, and N10 to 0. While node N12 in INV10 is still stable and may restore N11. The remaining nodes are unchanged and are set to have a minimal effect on the output node Q.

Case 3: Consider the two upsets that occurred in the Delta DICE module and a single upset happen in the intercepting module. As per case 3 in SNU and case 3 in DNU, the node pairs, which upset N2, N4, and N6. X2 and X3 remain unchanged, and Q can be recovered.

Case 4: Consider the two upsets that occurred in the interception module and one inside the Delta DICE module. Since the Delta DICE module exists as self-recoverable and fix errors in the interception module without affecting the output Q.

Quadruple node upset analysis

Case 1: The Delta DICE module with four node upsets simultaneously cause an upset in the output Q. However, the output recovers from the faults occurring on Delta DICE in the subsequent clock cycle.

Case 2: All the four upsets happen within the interception module. Consider node pairs N5, N7, N9, and N11 flip from 0 to 1. The NCNTFETs of INV3, INV5, INV7, and INV9 that conduct, which causes nodes N4, N6, N8, and N10 to flip from 1 to 0. As a result, nodes X2 upsets, but X1 and X3 remains unchanged through N2 and N12 nodes. Due to the INV2 and INV10 inputs of NCNTFET, the nodes N3 and N11 will be restored. Simultaneously, the other nodes don't change, and output Q remain the same.

Case 3: Three upsets happen in the interception module and one occurring in Delta DICE module. The Delta DICE module enables self-recovery by correcting flipped faults in the interception module while ensuring that the output Q remains unchanged.

Case 4: Two double node faults occur: one exists in the Interception module, and the other is in the Delta DICE module. Consider inputs nodes N3, N5 of INV3 and INV5 respectively flipped from 0 to 1, this upset cause N4 and N6 nodes to flip to 0. As a result, INV 4 and INV 6 NCNTFET turn on and restores the N5 and N7 nodes. Meanwhile, X1 and X2 are flipped from 1 to 0, but due to the X3 node, the Q output remains unchanged. Hence, the proposed LHQCNT latch can handle all SNUs, DNU, TNU, and QNU.

Results and discussion

The simulation results for the LHQCNT latch are thoroughly examined in this section. In comparison with existing latch topologies, the performance metrics—such as power consumption, delay, and reliability—are assessed. The comparison demonstrates the benefits and drawbacks of LHQCNT about effectiveness, durability, and suitability for radiation-hardened applications.

Simulation method

The 32 nm CNT-based FET Verilog-A structure³⁴ from Stanford University is utilized for design to simulate the LHQCNT latch circuit shown in Fig. 9. Verilog-A code is used in cadence virtuoso tools to create symbols of PCNTFET and NCNTFET to construct a latch circuit at room temperature (27° C) along with supply voltage VDD = 1 V, with a clock frequency of 500 MHz. This paper's structure is based on standard simulation dimensions, such as the chirality vector of the PCNTFET setup ratio as (10, 0) and the NCNTFET setup ratio as (15, 0), apart from transistor dimensions specified in Table 1 using in two input inverter and Delta DICE. The chirality vector of PCNTFET and NCTFET set up ratio as (8, 0); similarly, the inverter chirality is P/NCNTFET setup ratio as (13, 0). Table 1 indicates key model parameters, and their respective values used in the simulation.

This section explains the output waveforms illustrated in Fig. 10, which corresponds to the input waveforms supplied into the LHQCNT. Simulation results are accurately provided for average power, maximum propagation delays, PDP and APDP. The LHQCNT design is then compared to the existing designs in terms of PDP, maximum propagation delay, average power, APDP and transistor count.

The simulation utilizes the double-exponential current source model outlined in Eqs. (5) and (6) to simulate fault injections³⁵. The raise ($\tau\alpha$) and fall ($\tau\beta$) time constants used for the current pulse are 0.1ps and 3ps respectively. For the simulation purpose, the maximum injected charge per node is considered as 48fC, which is adequate to assess the circuit performance in the presence of extreme SNU, DNU, TNU, and QNU events that might compromise node stability.

$$I_{inj} = I_0 \left(e^{-\frac{t}{\tau\alpha}} - e^{-\frac{t}{\tau\beta}} \right) \quad (5)$$

$$I_0 = \frac{Q_{inj}}{T_\alpha - T_\beta} \quad (6)$$

where,

I_0 = initial current. Q_{inj} = the charge collected at time t, I_{inj} = the injected current impulse, and

$\tau\alpha$ and $\tau\beta$ represents the amount of accumulation and particle motion pattern formation time constants, respectively. Simulation results of the LHQCNT Latch for SNUs, DNU, and TNU fault injections shown in Fig. 11. Four SNU possibilities are simulated, each inserting a fault within the nodes N1, N4, X1, and Q between 0 and 12 ns. Between 14 and 24 ns, six DNU possibilities are simulated, inserting faults within the node pairs <N3, N5>, <N6, N8>, <N7, N10>, <Q, X1> <X2, X3>, and <Q, N2>. Similarly, between 24 and 32 ns, six TNU possibilities are simulated, injecting faults into node pairs <N7, N9, N11>, <X1, X2, Q>, <N1, N4, Q>, <N2, N4, N6>, <N2, X1, X2> and <N8, N9, X1>. The simulation results demonstrate that the LHQCNT latch is effective in contrast to SNUs, DNU, and TNU.

$\tau\alpha$ and $\tau\beta$ represents the amount of accumulation and particle motion pattern formation time constants, respectively. Simulation results of the LHQCNT Latch for SNUs, DNU, and TNU fault injections shown in Fig. 11. Four SNU possibilities are simulated, each inserting a fault within the nodes N1, N4, X1, and Q between 0 and 12 ns. Between 14 and 24 ns, six DNU possibilities are simulated, inserting faults within the node pairs

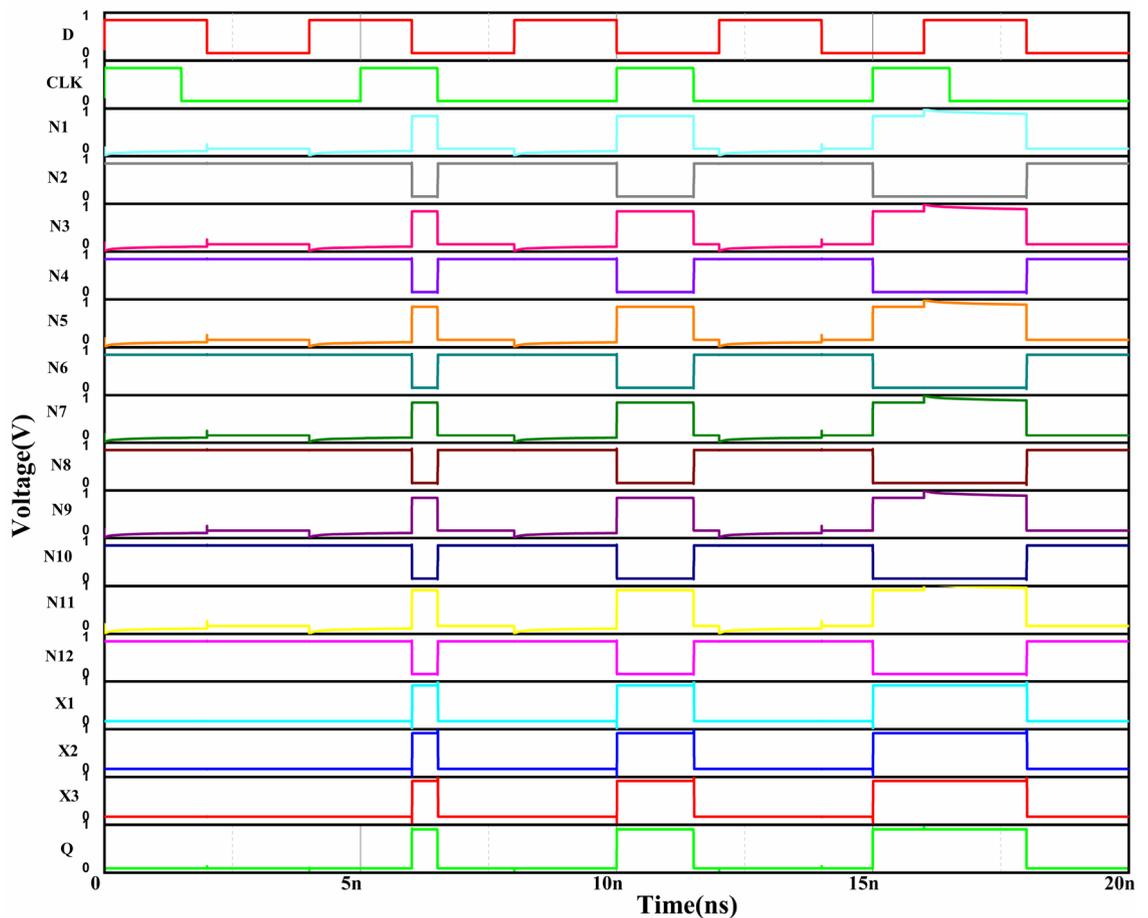


Fig. 10. Simulation output of the LHQCNT Latch.

< N3, N5>, < N6, N8>, < N7, N10>, < Q, X1> < X2, X3>, and < Q, N2>. Similarly, between 24 and 32 ns, six TNU possibilities are simulated, injecting faults into node pairs < N7, N9, N11>, < X1, X2, Q>, < N1, N4, Q>, < N2, N4, N6>, < N2, X1, X2> and < N8, N9, X1>. The simulation results demonstrate that the LHQCNT latch is effective in contrast to SNUs, DNUs, and TNUs.

The simulation waveforms for the LHQCNT latch against QNU fault injections are illustrated in Fig. 12. QNU possibilities are examined by inserting faults into node pairs < N4, N5, N9, N11>, < N2, N4, N6, N8>, < N1, N3, N10, N12>, < N1, N3, X1, X3>, < N8, X2, X3, Q>, < N5, X2, X3, Q>, < N2, X1, X2, X3>, < N3, X1, X2, X3>, and < X1, X2 × 3, Q> between 0 to 40 ns. The simulation results indicate that the latch can withstand QNUs.

Comparative analysis

Table 4 compares the reliability of the LHQCNT latch to previous latch designs with^{9,22,34}. Table 4 shows that the latch²² is an SNU self-recoverable, but it cannot tolerate DNU, TNU, and QNU. The Delta DICE latch in⁹ is resistant to DNU upsets, whereas it cannot tolerate TNU and QNU upsets. The second column is used to indicate the design's technology. The third column indicates the tolerance of SNU, DNU, TNU, and DNU, and the fourth column indicates the critical charge, respectively. The fifth and sixth columns indicate setup and hold times, respectively. Contrasted to existing latches with similar soft errors, the LHQCNT latch achieves the minimum setup time, the lowest power, and minimum delay. The low power consumption and minimum delay of the LHQCNT latch allow it to achieve the minimum APDP. The size of the area is proportional to the number of transistors. All transistors' width-to-length ratios are added together to determine the area by using Eq. (7)¹⁸.

$$UST = \sum_n^{i=1} (w|L)_i \quad (7)$$

The results suggest that LHQCNT latches have an advantage over SNU, DNU, TNU and QNU-tolerant latches. The LHQCNT latch outperforms the compared latches in terms of area, power, PDP, and APDP, with Δ power, Δ delay, Δ area, and Δ APDP determined by Eq. (8).

$$\Delta = (Proposed\ Latch - Compare\ Latch) / Compare\ Latch \quad (8)$$

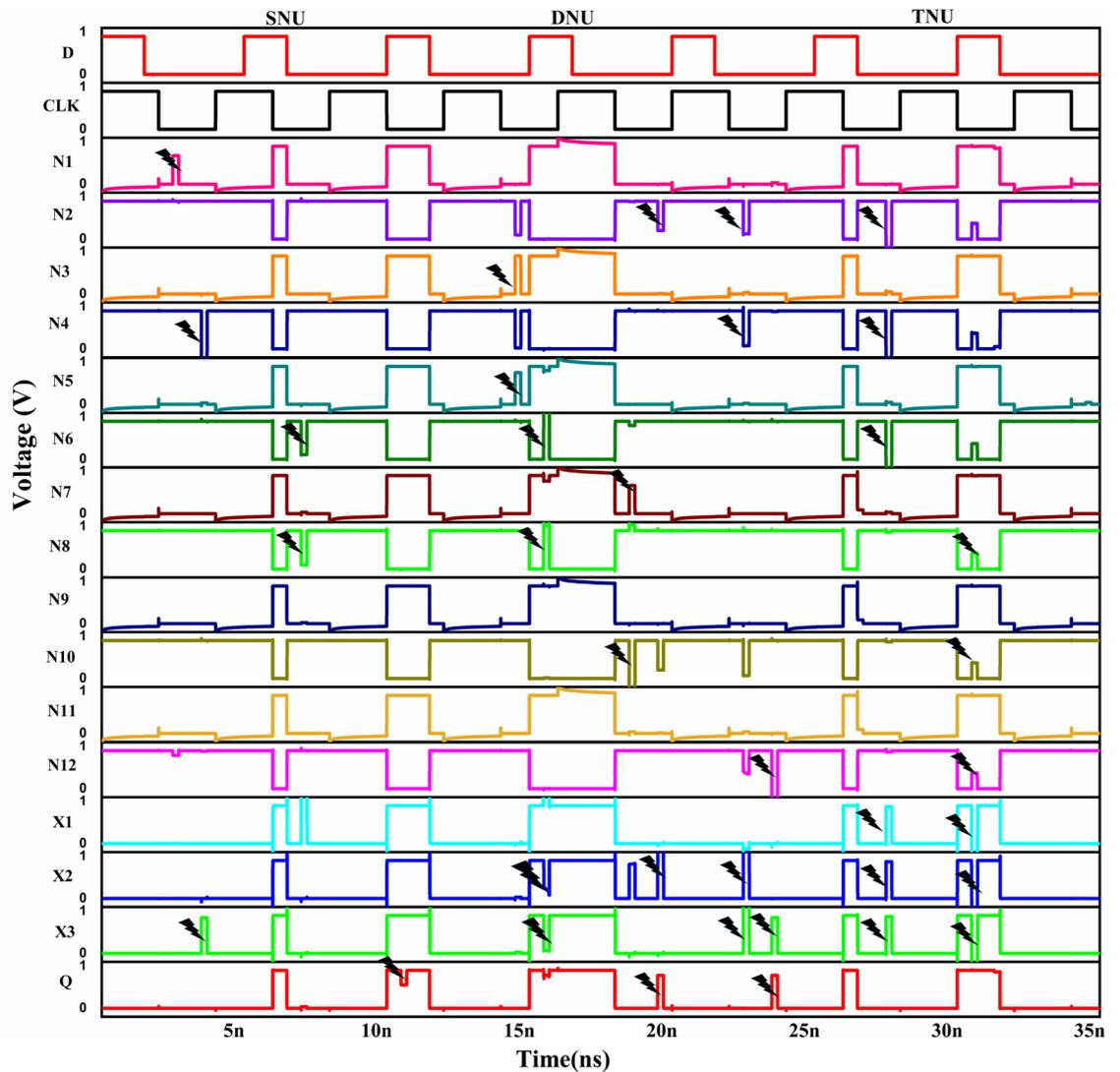


Fig. 11. Output characteristics of the LHCNT Latch under SNU, DNU and TNU fault conditions.

In terms of delay, the LHCNT achieves 1.06 ps, which is 11.47 times faster than LCQNUT (18.52 ps) and 16.47 times faster than Shakeel et al. (13.22 ps). In terms of average power consumption, the LHCNT attains 0.12 μW , which is 69.23% less than LCQNUT (0.39 μW). However, Shakeel et al. (0.087 μW) consumed 27.5% less power than LHCNT due to a lower transistor count. Figure 13 represents the graphical representation of the proposed latch with other existing latches.

Impact analysis of process, voltage and temperature variations

The performance and dependability of circuits are greatly impacted by changes in Process, Voltage, and Temperature (PVT). Variations in the power supply and variations in the room temperature are the causes of these differences. To ensure the robustness and stable operation of the latch design, it is essential to evaluate it under various PVT issues.

Process variations

CNT fabrication results in unavoidable variation in certain characteristics. The most critical parameters affecting CNTFET performance are (i) the diameter of CNTs, (ii) the value of CNT pitch, and (iii) the quantity of CNTs present in the channel. The Eq. (2) shows a direct relationship between CNT diameter and CNTFET threshold voltage (v_{TH}). Large diameter variations may have an impact on the CNTFET's v_{TH} in the design. The width of the CNTFET can be calculated by the CNT pitch value and number of CNTs in the channel region using Eq. (3). Tables 5, 6 and 7 presents the power and delay values corresponding to variation in CNT diameter, CNT pitch and CNTs position.

To assess the impact of parameter variations on circuit performance, PVT analysis was conducted for the proposed LHCNT with 30 iterations. Consistent with typical practices, the variables taken into consideration comprised CNT diameter and pitch values that changed by 5%, 10%, 15%, and 20%^{36,37}. In the LHCNT, the

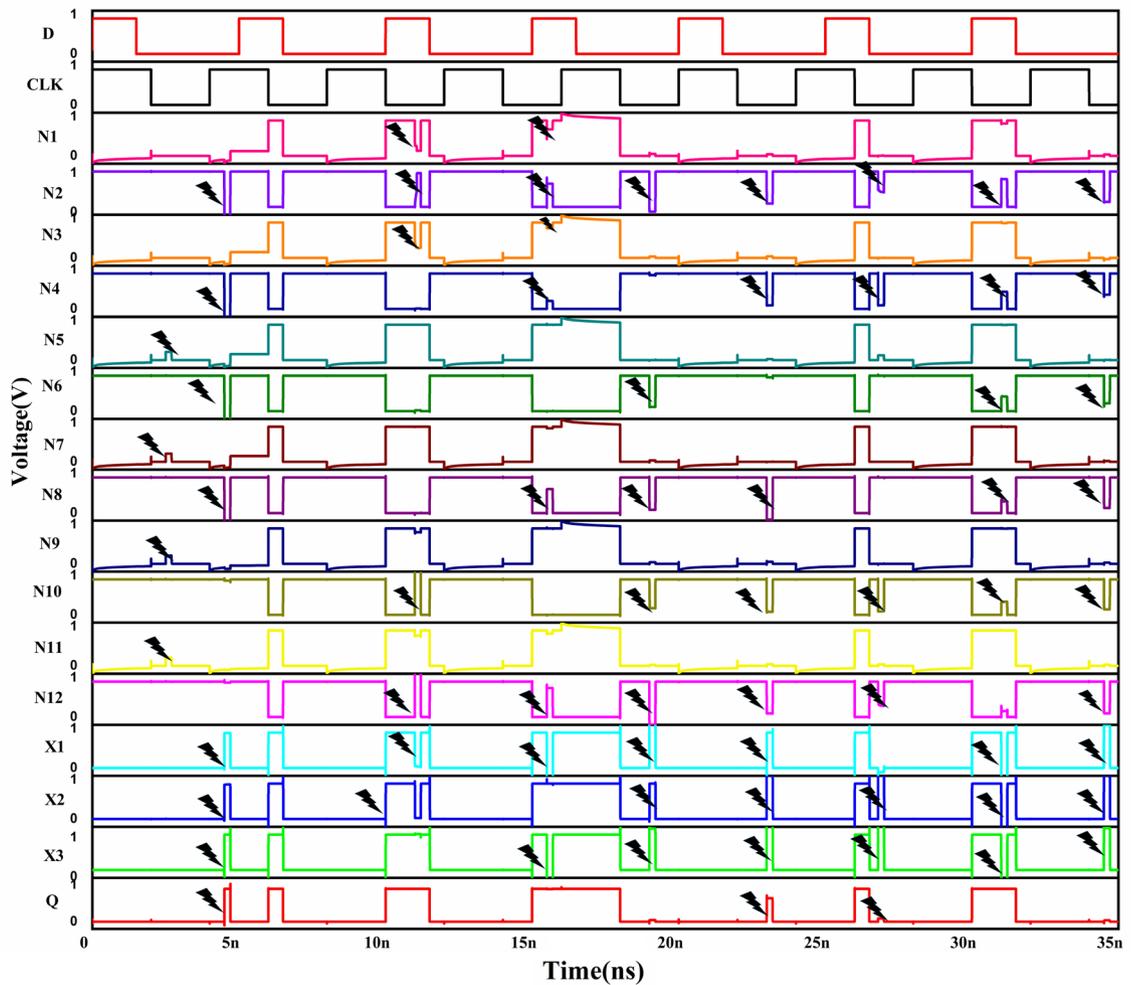


Fig. 12. Output characteristics of the LHQCNT latch under QNU fault conditions.

Latch	Technology	Tolerance				Q_{crit} (fC)	Setup time (ps)	Hold time (ps)	Area (UST)	Delay (D-Q) ps	Delay (C-Q) ps	Power (μ W)	PDP (10^{-18})	APDP (10^{-2})
		SNU	DNU	TNU	QNU									
Delta DICE ⁹	CMOS (32 nm)	Yes	Yes	No	No	42	34.83	15.83	60	71.58	65.80	1.82	130.27	78.16
Shakeel et al ²³	CNTFET (16 nm)	Yes	No	No	No	--	--	--	32	13.22	10.91	0.087	1.15	0.36
LCQNT ³³	CMOS (32 nm)	Yes	yes	Yes	Yes	45	10.57	10.16	96	18.52	14.67	0.39	7.22	0.69
LHQCNT	CNTFET (32 nm)	Yes	Yes	Yes	Yes	48	0.32	3.4	96	1.06	0.98	0.12	0.12	0.11

Table 4. Comparative analysis of LHQCNT latch with existing Latches.

quantity of CNTs in the CNTFET channel region was also altered by ± 1 and ± 2 . With the use of two-dimensional graphs. Figure 16 shows how these differences affect average power and maximum propagation delay.

According to Fig. 14 that differences in CNT diameters have the greatest impact on the performance of the proposed LHQCNT. Variation leads to a considerable rise in average power and maximum propagation delay. An increase in CNTs moderately affects the performance of the proposed design, leading to a slight rise in both average power consumption and propagation delay as variations escalate. Conversely, variations in pitch value have minimal to no impact, as both average power consumption and propagation delay stay nearly constant despite increasing variation.

Supply voltage variations

The proposed design LHQCNT is simulated using three alternative supply voltages (0.9 V, 1 V and 1.1 V) simultaneously at the same node for fault injection. Figures 15 and 16 displays the simulation results graphically.

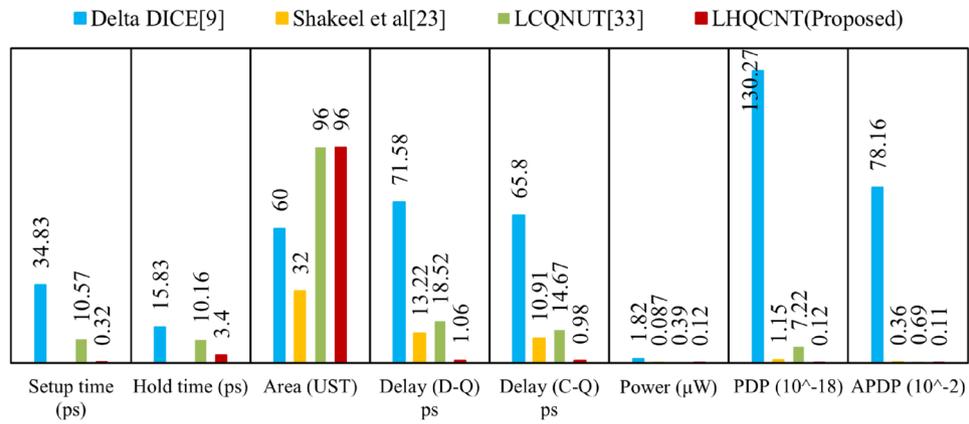


Fig. 13. Graphical representation of the proposed LHCNT latch with other existing Latches.

CNT diameter	8	8.4	8.8	9.2	9.6
Power (µW)	4.395	4.394	4.393	4.39	4.388
Delay (D-Q) ps	1.229	1.229	1.228	1.227	1.227

Table 5. Power and delay values corresponding to variations in CNT diameters.

CNT pitch value (nm)	20	21	22	23	24
Power (µW)	4.395	4.395	4.395	4.395	4.395
Delay (D-Q) ps	1.228	1.228	1.228	1.228	1.228

Table 6. Power and delay values corresponding to variations in CNT pitch values.

CNT Pos	-2	-1	0	1	2
Power (µW)	4.394	4.394	4.395	4.395	4.395
Delay (D-Q)ps	1.227	1.227	1.227	1.228	1.288

Table 7. Power and delay values corresponding to variations in CNT positions.

As the supply voltage increases, the injected pulse’s amplitude and average power increases as shown in Table 8. However, the propagation delay reduces slightly, permitting the circuit to respond faster.

Temperature variations

The simulation was conducted at temperatures of -30 °C, 0 °C, 30 °C, 60 °C, and 90 °C, while maintaining the same node and timing for fault injection. The results, illustrated in Fig. 17, show that variations in temperature have no significant impact on the average power and propagation delay.

Conclusion

This manuscript presents an LHCNT latch that uses a CNTFET to mitigate the impact of MNUs caused by adverse radiation conditions and enhance circuit reliability. A comparative analysis was undertaken to evaluate the challenges and opportunities of adopting Nano electronic circuits that are developed with CNTFET technology as an alternative to CMOS technology. In comparison to LCQNUT’s CMOS variant with a 0.9 V supply voltage, the LHCNT reduces power consumption by 69.23%, decreases delays by 16.47 times, and reduces the power-delay product (PDP) by 98%.Based on the data presented in Table 5. Therefore, it can be concluded that CNTFET serves as a promising substitute for CMOS in the development of nanoelectronic circuits. Simulation results confirmed that the LHCNT latch achieves low power, and lesser delay, while PVT analysis revealed moderate stability.

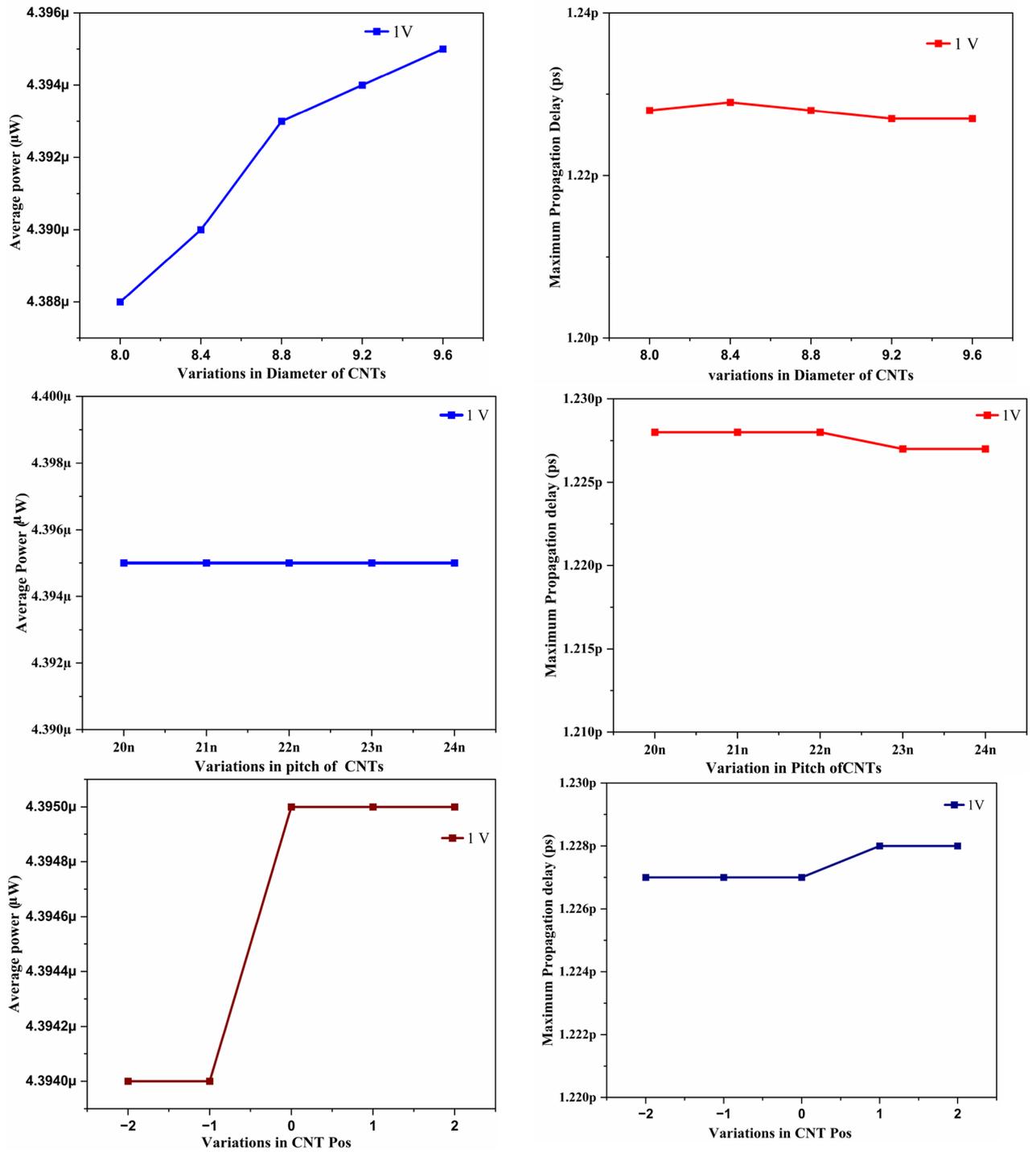


Fig. 14. Effect of process variations in CNT diameter, pitch, and position on power and delay.

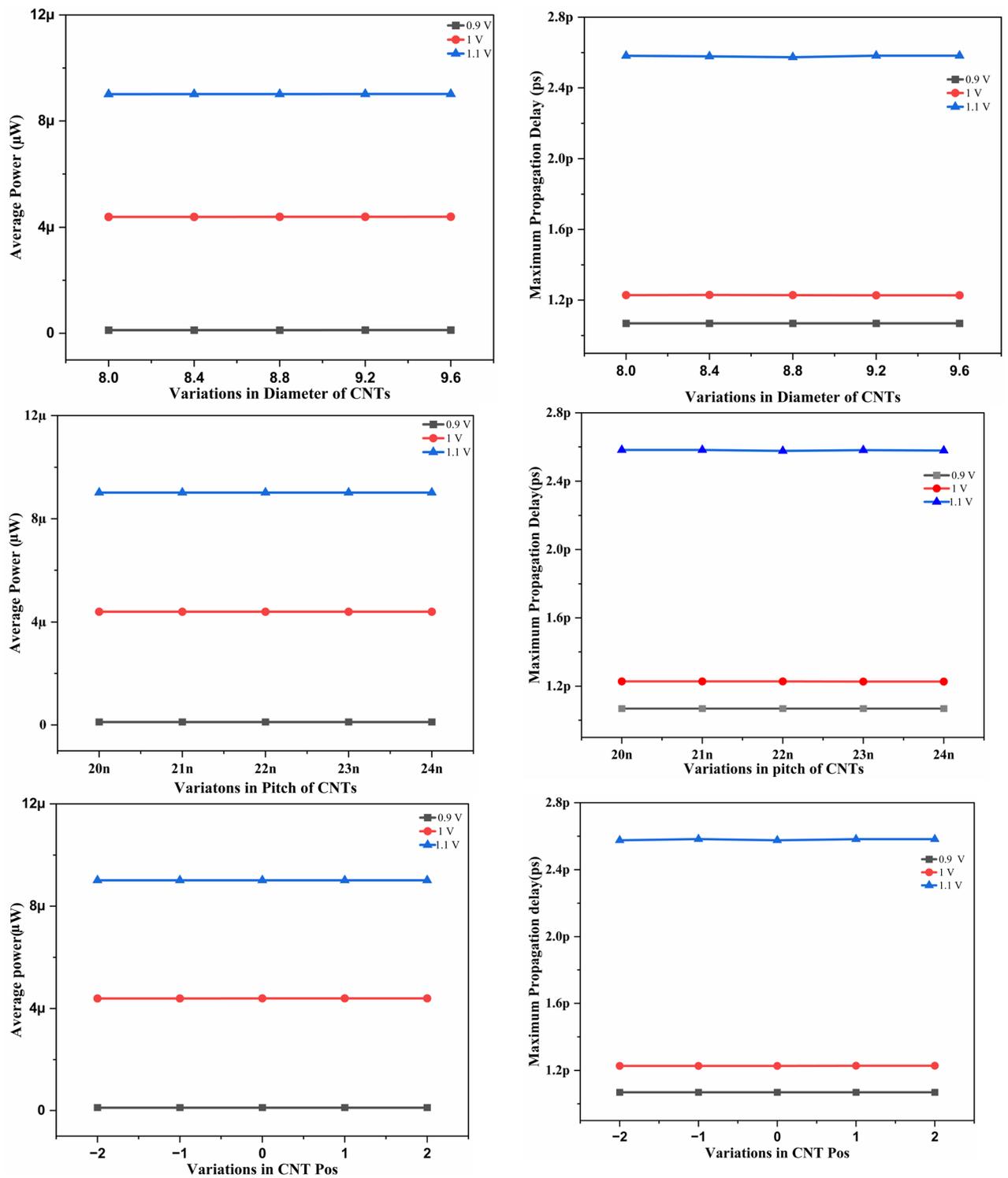


Fig. 15. Various voltage variations in CNT diameter, pitch, and position affecting power and delay.

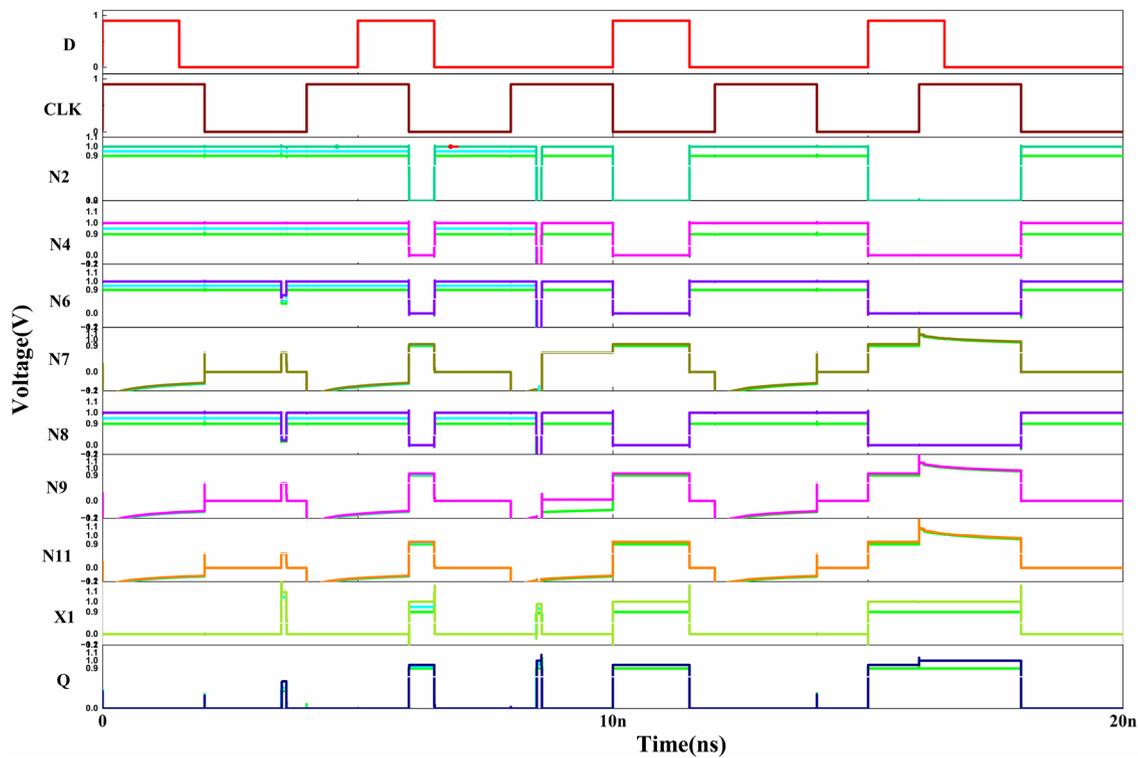


Fig. 16. Output characteristics of the LHCNT under varying supply voltage conditions.

Voltage (V)	Power(μ W)	Delay(D-Q) ps
0.9	0.12	1.06
1	4.53	1.22
1.1	9.01	2.58

Table 8. LHCNT at various voltages with power and Delay.

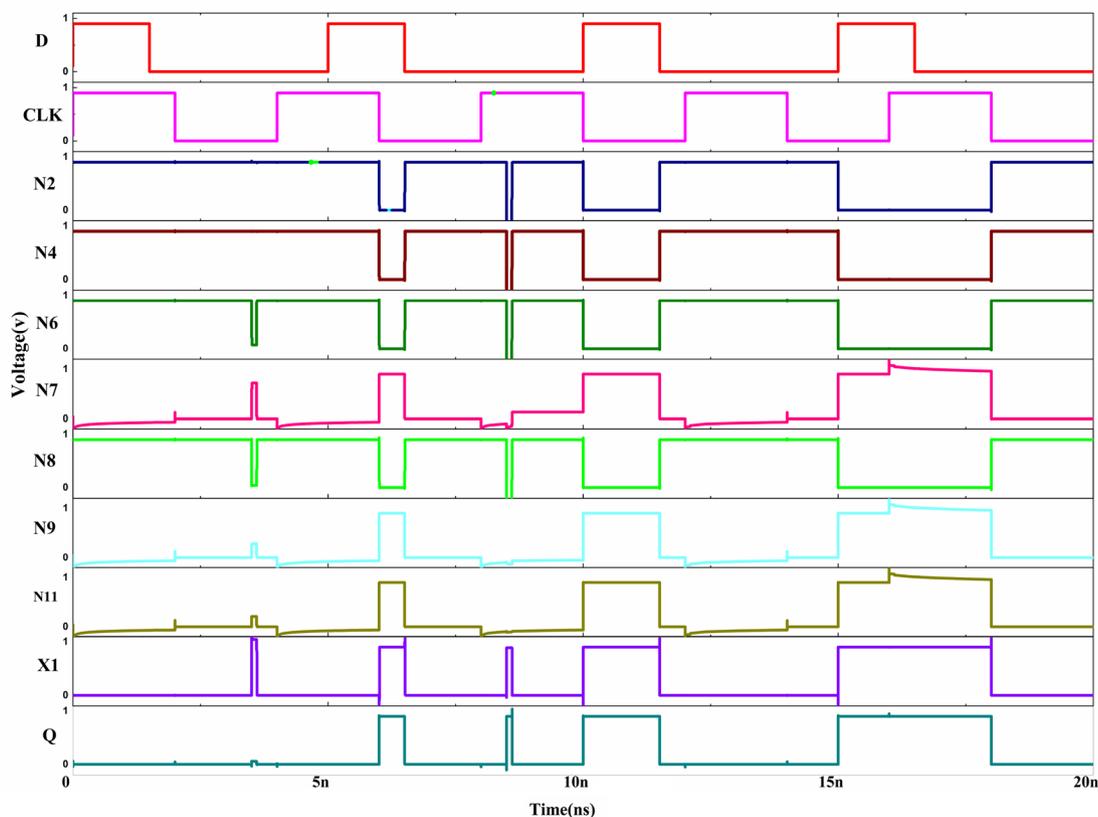


Fig. 17. Output characteristics of the LHQCNT latch under varying temperature conditions.

Data availability

Data availability Statement: All relevant data are within the manuscript.

Received: 11 April 2025; Accepted: 10 November 2025

Published online: 22 December 2025

References

- Zick, K. M. & John P. H. High-level vulnerability over space and time to insidious soft errors. In *2008 IEEE International High Level Design Validation and Test Workshop* (IEEE, 2008).
- Schwank, J. R., Marty, R. & Snd Paul, E. D. Radiation hardness assurance testing of microelectronic devices and integrated circuits: radiation environments, physical mechanisms, and foundations for hardness assurance. *IEEE Trans. Nucl. Sci.* **60** (3), 2074–2100 (2013).
- Ferlet-Cavrois, V. & Lloyd, W. M. Single event transients in digital CMOS—a review. *IEEE Trans. Nucl. Sci.* **60** (3), 1767–1790 (2013).
- Kaupilla, A. V. et al. Impact of process variations and charge sharing on the single-event-upset response of flip-flops. *IEEE Trans. Nucl. Sci.* **58**, 2658–2663 (2011).
- Qi, C. et al. A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets. *IEEE Trans. Device Mater. Reliab.* **16** (3), 388–395 (2016).
- Wang, H-B. et al. An SEU-tolerant DICE latch design with feedback transistors. *IEEE Trans. Nucl. Sci.* **62** (2), 548–554 (2015).
- Kumaravel, S. Design and analysis of SEU hardened latch for low power and high speed applications. *J. Low Power Electron. Appl.* **9** (3), 21 (2019).
- Black, J. D. et al. DFF layout variations in CMOS SOI—analysis of hardening by design options. *IEEE Trans. Nucl. Sci.* **67**, 1125–1132 (2020).
- Kumar, S. S., Sundaram, K., Padmanaban, S., Holm-Nielsen, J. B. & Blaabjerg, F. A low power and soft error resilience guard-gated Quartro-based flip-flop in 45 nm CMOS technology. *IET Circuits Devices Syst.* **15** (6), 571–580 (2021).
- Kim, Y-B. Integrated circuit design based on carbon nanotube field effect transistor. *Trans. Electr. Electron. Mater.* **12.5**, 175–188 (2011).
- Sachdeva, A., Deepak, K. & Erfan, A. A carbon nano-tube field effect transistor based stable, low-power 8T static random access memory cell with improved write access time. *AEU-Int. J. Electron. Commun.* **162**, 154565 (2023).
- Mani, E. et al. Design of high stability, low power and high speed 12 T SRAM cell in 32-nm CNTFET technology. *AEU-Int. J. Electron. Commun.* **154**, 154308 (2022).
- Zahoor, F. et al. Carbon nanotube field effect transistor (cntfet) and resistive random-access memory (rram) based ternary combinational logic circuits. *Electronics* **10.1**, 79 (2021).
- Prakash, P., Mohana, K., Bennet, M. A. & S, and A review on carbon nanotube field effect transistors (CNTFETs) for ultra-low power applications. *Renew. Sustain. Energy Rev.* **89**, 194–203 (2018).
- Obite, F., Geoffrey, I. & Joseph, S. B. Carbon nanotube field effect transistors: toward future nanoscale electronics. *Int. J. Comput. Appl.* **41** (2), 149–164 (2019).

16. Zakaria, M. R. et al. Study of carbon nanotubes stability in different types of solvents for electrospray deposition method 538–543 (2020).
17. Hamzah, N. et al. Identification of CNT growth region and optimum time for catalyst oxidation: experimental and modelling studies of flame synthesis. *Macromol* **2019**, 85–91 (2019).
18. Díez-Pascual, A. M. Chemical functionalization of carbon nanotubes with polymers: a brief overview. *Macromol* **2**, 64–83 (2021).
19. Díez-Pascual, A. M. Chemical functionalization of carbon nanotubes with polymers: a brief overview. *Macromol* **1** (2), 64–83 (2021).
20. Eatemadi, A. et al. Carbon nanotubes: properties, synthesis, purification, and medical applications. *Nanoscale Res. Lett.* **9**, 1–13 (2014).
21. Jamal, G. R. A. & Sharif, M. M. Calculating optical transition energies in semiconducting zigzag SWCNTs. In *International Conference on Advanced Mechatronics, Intelligent Manufacture, and Industrial Automation (ICAMIMIA)* (IEEE, 2017).
22. Yan, A. et al. Quadruple cross-coupled dual-interlocked-storage-cells-based multiple-node-upset-tolerant latch designs. *IEEE Trans. Circuits Syst. I Regul. Pap.* **67** (3), 879–890 (2020).
23. Shakeel, S. & Naushad, A. CNTFET based radiation hardened latch. *Australian J. Electr. Electron. Eng.* **18** (3), 199–208 (2021).
24. Yan, A. et al. Design of a triple-node-upset self-recoverable latch for aerospace applications in harsh radiation environments. *IEEE Trans. Aerospace Electron. Syst.* **56** (2), 1163–1171 (2019).
25. Huang, Z. et al. A high-speed and triple-node-upset recovery latch with heterogeneous interconnection. *Microelectron. J.* **118**, 105290 (2021).
26. Xu, H., Sun, C., Zhou, L., Liang, H. & Huang, Z. Design of a highly robust triple-node-upset self-recoverable latch. *IEEE Access.* **9**, 113622–113630 (2021).
27. Lu, Y. et al. A low power-consumption triple-node-upset-tolerant latch design. *J. Electron. Test.* **38** (1), 63–76 (2022).
28. Yan, A. et al. Novel quadruple-node-upset-tolerant latch designs with optimized overhead for reliable computing in harsh radiation environments. *IEEE Trans. Emerg. Top. Comput.* **10** (1), 404–413 (2020).
29. Dai, Y. et al. A high performance and low power triple-node-upset self-recoverable latch design. *Electronics* **11** (21), 3606 (2022).
30. Cai, S. et al. Four-input-C-element-based multiple-node-upset-self-recoverable latch designs. *Integration* **90**, 11–21 (2023).
31. Yan, A. et al. Advanced DICE based triple-node-upset recovery latch with optimized overhead for space applications. In *2023 IEEE 32nd Asian Test Symposium (ATS)* 1–5 (IEEE, 2023).
32. Bai, Y., Chen, X., Yang, Y., Zhou, X. & Zhang, Y. Triple-node-upset self-recoverable latch design for aerospace applications. *Microelectron. Reliab.* **154**, 115338 (2024).
33. Xu, H. et al. A highly reliable and low-overhead quadruple-node-upset tolerant latch design. *Microelectron. Reliab.* **157**, 115413 (2024).
34. Deng, J. & Philip Wong, H-S. A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—part I: model of the intrinsic channel region. *IEEE Trans. Electron. Devices.* **54** (12), 3186–3194 (2007).
35. Sharma, T. & Laxmi, K. Design of unbalanced ternary counters using shifting literals-based D-Flip-Flops in carbon nanotube technology. *Comput. Electr. Eng.* **93**, 107249 (2021).
36. Moaiyeri, M. H., Akbar, D. & Keivan, N. Design of energy-efficient and robust ternary circuits for nanotechnology. *IET Circuits Devices Syst.* **5** (4), 285–296 (2011).
37. Paul, A. & Buddhadev, P. Design of ternary and quaternary asynchronous Up/Down counter using CNTFET. *AEU-Int. J. Electron. Commun.* **179**, 155323 (2024).

Acknowledgements

We are thankful to the Management of Vellore Institute of Technology for providing the opportunity for carrying out the research.

Author contributions

The authors declare that they have all contributed equally to the conception, design, execution, and writing of this paper.

Funding

The authors received no specific funding for this work.

Competing interests

The authors declare no competing interests.

Ethical approval

No participation of humans takes place in this implementation process.

Human and animal rights

No violation of Human and Animal Rights is involved.

Additional information

Supplementary Information The online version contains supplementary material available at <https://doi.org/10.1038/s41598-025-28311-z>.

Correspondence and requests for materials should be addressed to S.K.S.

Reprints and permissions information is available at www.nature.com/reprints.

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Open Access This article is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International License, which permits any non-commercial use, sharing, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if you modified the licensed material. You do not have permission under this licence to share adapted material derived from this article or parts of it. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit <http://creativecommons.org/licenses/by-nc-nd/4.0/>.

© The Author(s) 2025