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High-step-up quadratic DC–DC converter based on switched capacitor and coupled inductor techniques

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This paper proposes a non-isolated quadratic high-step-up DC-DC converter. A coupled inductor and a switched capacitor cell are implemented in its structure to increase voltage gain. Balancing the capacitor and the coupled inductor plays the role of the resonant tank, which solves the problem of reverse recovery losses of its diodes. In this structure, soft switching conditions are established for some diodes and MOSFET, which reduces the switching losses of the converter. With a low number of components, the proposed converter achieves a high voltage gain. The diode-capacitor clamp circuit is utilized to reduce the negative effects caused by the leakage inductance and recover the energy stored in it. The performance of the proposed converter is analyzed in the continuous and discontinuous conduction modes. An analysis of design considerations, including inductors and capacitors, is presented. In addition, an analysis of the efficiency of the proposed topology is provided. The proposed topology is compared in terms of voltage gain, voltage/current stress across semiconductor components, and converter efficiency with related topologies. Finally, a 210 W (20 V/420 V) laboratory prototype is presented to verify the proposed converter's mathematical analysis and performance.

The issue of energy conversion has been one of the main challenges in the last decade, and engineers are always looking for new ways to provide the required energy. The most important sources are fossil fuels and renewable energy sources. Unlike renewable energy sources, fossil fuels are limited and produce much pollution[1,2]. As the output voltage of renewable energy systems is limited, power electronic converters are needed to provide high voltage gain. In the design of these converters, the output voltage gain, the voltage stress across the semiconductor elements, the number of elements, and the efficiency are considered[3–5]. In order to increase the output voltage gain, a switched capacitor cell and a coupled inductor can be used. In these types of converters, the capacitors of switched capacitor cells are charged in parallel and discharged in series, which increases the voltage gain of the converter. Of course, in this case, the coupled inductor can be used in the mentioned cell structure to improve the diode reverse recovery problem[6,7]. Also, the coupled inductor gives the converter higher degrees of freedom to increase output voltage gain and reduce voltage stress across the semiconductor elements[8]. In[9–11], a transformer has been used as an isolation technique in those structures. The presence of voltage spikes across semiconductor elements is the main disadvantage of these converters, which is caused by the leakage inductance of the transformer. The number of components used in the structure of the converter is another significant issue for DC-DC converters. The presence of a substantial quantity of components increases the circuit's volume and the construction cost. In addition, each of the elements also includes losses[12].

In[13,14], two symmetrical switched capacitor cells are implemented in order to increase the output voltage gain. In addition, a passive clamp circuit was used to recover the leakage energy and improve the voltage spike across the switch. In[15], a SEPIC DC-DC converter is presented. The structure of this converter includes voltage multiplier cells to increase the output voltage gain. Besides, the passive clamp structure has been used to recover the leakage energy of the coupled inductor. High diode counts and hard switching conditions have reduced converter efficiency.

In[16,17], a diode-capacitor cell and two coupled inductors have been used to increase the output voltage gain. Also, in order to have soft switching conditions, the snubber capacitor is placed parallel to the main power

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switches. A large number of switches and the presence of a snubber capacitor and two coupled inductors increase the size of the structure of these converters. The DC–DC converter suggested in[18] is based on the conventional boost converter. A switched capacitor cell has been used to increase its voltage gain in this structure; however, it has a low voltage gain. One of the methods to improve the efficiency is the quasi-resonant operation, which is utilized by the converters presented in[19,20]. Also, two passive clamp circuits are used in their structure. In[21–24], the voltage lift technique was utilized to increase voltage gain. In this technique, energy storage elements such as capacitors and inductors are implemented in order to increase the output voltage gain and overcome the parasitic effects of the components. In[25–27], the input source and the output terminal do not have a common ground. This method makes these converters unsuitable for PV applications. In some converters, a three-coil coupled inductor has been used to increase the output voltage gain, which has a sizeable magnetic core[27–29]. In the interleaved DC–DC converter presented in[29], two pairs of three-coil inductors and a voltage multiplier cell are utilized to increase the output voltage gain in a cascade structure. Despite the hard switching conditions, the large number of semiconductor elements in this converter has caused an increase in losses and, as a result, a decrease in the converter efficiency.

In this paper, a non-isolated high-step-up DC-DC converter is presented. In order to increase the voltage gain, a coupled inductor and the switched capacitor cell are used in its structure. Due to the presence of the clamp circuit, there is a low voltage stress across the semiconductor components, which increases efficiency and reduces construction costs. The clamp circuit in the proposed structure recovers the leakage energy of the coupled inductor and increases the voltage gain. Additionally, soft switching conditions are established, and the current waveforms flowing through some diodes and MOSFETs are quasi-resonant, which leads to reduced switching losses.

Proposed converter operation principles

Figure 1 shows the structure of the suggested converter. In order to increase the output voltage gain, the coupled inductor and the switched capacitor technique are used. This structure contains two power switches (S_1, S_2), an inductor (L_1), a coupled inductor, four diodes (D_1, D_2, D_3 and D_O) and four capacitors (C_1, C_2, C_3 and C_O). The input source is V_{in}, and the output port is V_O. To simplify the steady-state analysis calculations, the following assumptions are considered:

1) All components of the converter are considered ideal.
2) The coupled inductor is modeled as a leakage inductor (L_K) and a magnetizing inductor (L_m) at the primary side with a coupling coefficient $k = L_m/(L_m + L_k)$ and its turn ratio is $n = n_2/n_1$.

The key waveform of the suggested converter in Continues Conduction Mode (CCM) is shown in Fig. 2. In the CCM condition, the proposed converter has four operation modes, as shown in Fig. 3a–d. Both power switches are turned on and off simultaneously. So, the control structure of the proposed converter is simple.

Mode I ($t_0 < t < t_1$): Regarding Fig. 3a, at the beginning of this time interval, switches S_1 and S_2 are simultaneously turned on, such that the power switch S_2 is turned on under ZCS (Zero Current Switching) conditions. In this transient mode, the output diode D_O is forward bias. Because of the influence of the reflected leakage inductance on the secondary side of the coupled inductor, the current passing through diode D_O drops to zero at the end of this time interval, resulting in a low reverse recovery issue.

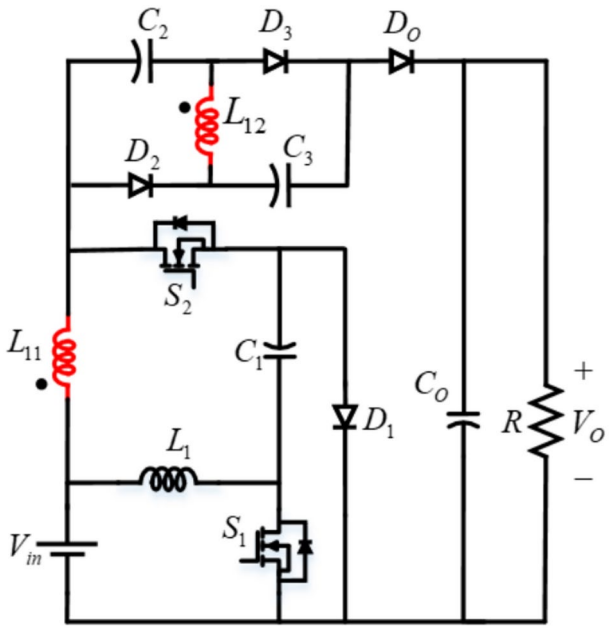

Fig. 1. Power circuit schematic of the proposed converter.

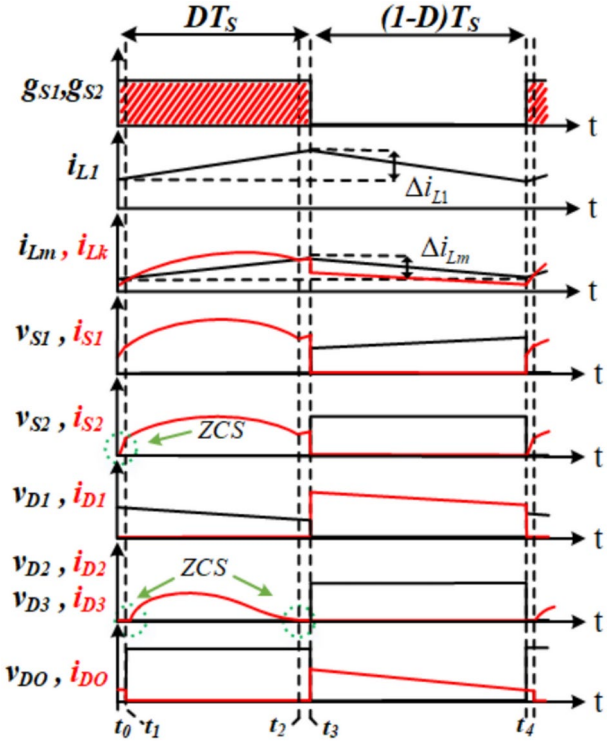

Fig. 2. Key waveform of the proposed converter in CCM.

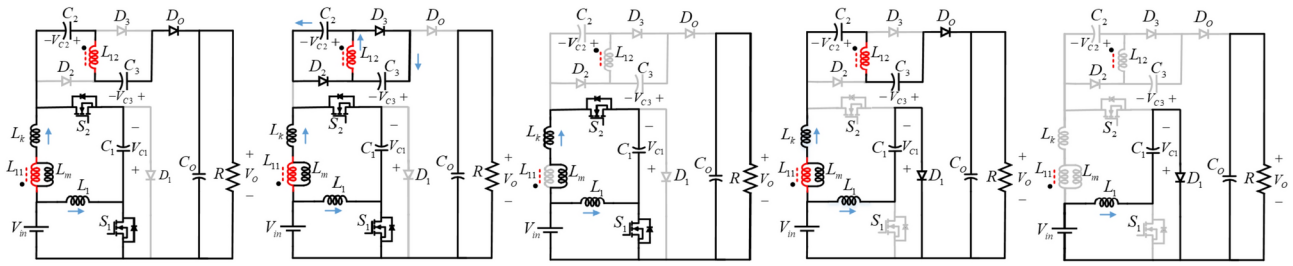

Fig. 3. The equivalent circuits of the operation modes. (**a**) mode I. (**b**) mode II. (**c**) mode III. (**d**) mode IV. (**e**) mode V. (CCM operation includes Figures (**a**–**d**) and DCM operation includes Figures (**a**–**e**)).

Mode II ($t_1 < t < t_2$): In this operation mode, MOSFETs S_1 and S_2 remain in on state from the previous operating mode. Diodes D_2, and D_3 are turned on at ZCS conditions and D_1 and D_O are reversed bias in this mode. The input source charges L_1, and its current level increases linearly. Also, the current of L_{11} is energized by the input source and C_1, and its current increases. C_2 and C_3 are charged through the secondary side of the coupled inductor. This operation mode ends when D_2 and D_3 are turned off at ZCS conditions. A schematic of the converter in this operational mode is illustrated in Fig. 3b. In this operation mode, the following equations are obtained:

$$V_{L1}^{II} = V_{in} \tag{1}$$

$$\frac{V_{Lm}^{II}}{k} = V_{in} + V_{C1} \tag{2}$$

$$nV_{Lm}^{II} = V_{C2} = V_{C3} \tag{3}$$

$$I_{C1}^{II} = I_{Lk} = I_{Lm} + nI_{L12} \tag{4}$$

$$I_{C2}^{II} = I_{C3}^{II} = -\frac{I_{L12}}{2} \tag{5}$$

$$I_{CO}^{II} = I_O \tag{6}$$

$$f_R = \frac{1}{T_R} = \frac{1}{2\pi\sqrt{L_k(C_2||C_3)}} \tag{7}$$

In order to eliminate the reverse recovery loss of D_2 and D_3 as well as reduce the switch turn-off loss, it is mandatory that the resonant time (T_R) be shorter than the turn-on time of the switching period ($T_R < D \times T_s$) as illustrated in Fig. 2.

Mode III ($t_2 < t < t_3$): In this transient operation mode, the power switches are in the on state, and all the diodes are reversed bias. Similar to operation mode II, L_1 is charged by V_{in}, and L_{11} is charged by V_{in} and C_1. In addition, the voltages of C_2 and C_3 remain constant. This operation mode ends when the power switches turn off. A schematic of the converter in this operational mode is shown in Fig. 3c. In this operation mode, the following equations are expressed:

$$V_{L1}^{III} = V_{in} \tag{8}$$

$$\frac{V_{Lm}^{III}}{k} = V_{in} + V_{C1} \tag{9}$$

$$I_{C1}^{III} = I_{Lk} = I_{Lm} \tag{10}$$

$$I_{CO}^{III} = I_O \tag{11}$$

Mode IV ($t_3 < t < t_4$): Regarding Fig. 3d, in this operation mode, D_2, D_3, and the power switches are in off state, and D_1 and D_O are forward biased. C_1 is charged by V_{in} and L_1. L_{11}, C_2, and C_3 are discharged, and the current passing through L_{11} decreases. In addition, the input source, L_{11}, C_2, and C_3 charge C_O and supply the power to the output load. In this operation mode, the following equations are obtained:

$$V_{L1}^{IV} = V_{in} - V_{C1} \tag{12}$$

$$V_O = V_{in} + V_{C2} + V_{C3} - V_{Lm}^{IV}\left(n + \frac{1}{k}\right) \tag{13}$$

$$I_{C1}^{IV} = -I_{L1} \tag{14}$$

$$I_{C2}^{IV} = I_{C3}^{IV} = \frac{I_{Lm}}{n+1} \tag{15}$$

$$I_{CO}^{IV} = I_O - I_{C3}^{IV} \tag{16}$$

Mode V ($t_4 < t < t_5$): This operation mode corresponds to the DCM condition as shows in Figs. 3e and 4. In this case, D_1 is forward bias, and the rest of the semiconductor elements are in off state. C_1 is charged through the input source and L_1. C_O supplies the output load power. For this operation mode, the following equations are expressed:

$$V_{L1}^{V} = V_{in} - V_{C1} \tag{17}$$

$$I_{CO}^{V} = I_O \tag{18}$$

Steady state analysis

Voltage gain in CCM

By applying the volt-second balance principle for L_1 and substituting (1) and (13) into it, the following equation is expressed:

$$V_{C1} = \frac{1}{1-D} V_{in} \tag{19}$$

According to (2) and (19), the following equation is achieved for the voltage across L_m in operation mode II:

$$V_{Lm}^{II} = \frac{k(2-D)}{1-D} V_{in} \tag{20}$$

Using (3) and (20), the following equation is obtained:

$$V_{C2} = V_{C3} = nV_{Lm}^{II} = \frac{nk(2-D)}{1-D} V_{in} \tag{21}$$

By applying the volt-second balance low for L_m and according to (20), the voltage across L_m in operation mode IV is obtained as follows:

$$V_{Lm}^{IV} = -\frac{kD(2-D)}{(1-D)^2} V_{in} \tag{22}$$

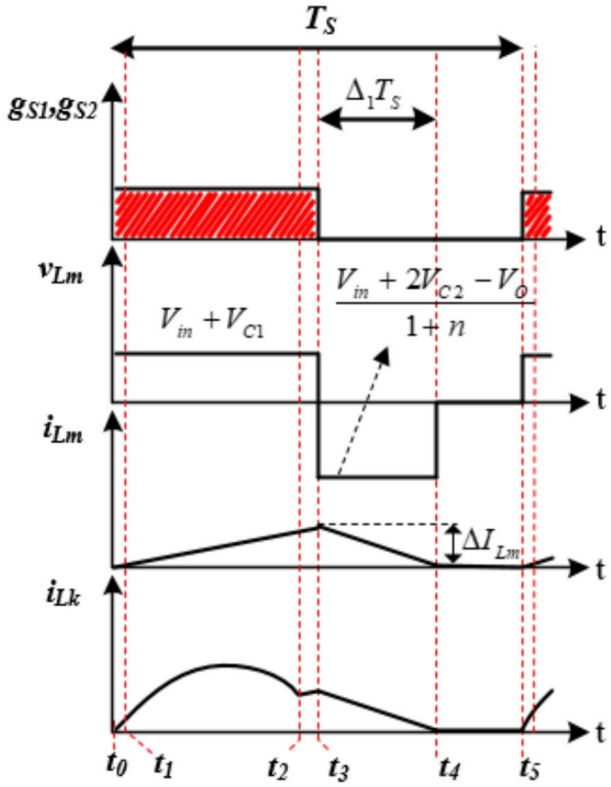

Fig. 4. Key waveforms of the proposed converter in DCM.

By substituting (21) and (22) into (12), the following equation for the voltage gain of the converter in CCM condition is calculated:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{1 + nk(2-D)^2}{(1-D)^2} \tag{23}$$

In the ideal case, assuming $k = 1$, the output voltage gain of the converter is expressed as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{1 + n(2-D)^2}{(1-D)^2} \tag{24}$$

According to (24), the output current can be derived as:

$$I_O = \frac{(1-D)^2}{1 + n(2-D)^2} I_{in} \tag{25}$$

Voltage stress across power semiconductors

Using mode II, the following equations are obtained:

$$V_{D1} = V_{C1} \tag{26}$$

$$V_{DO} = V_O + V_{C1} - V_{C3} \tag{27}$$

According to operation mode IV, the following equations are expressed:

$$V_{S1} = V_{C1} \tag{28}$$

$$V_{S2} = V_{in} - \frac{V_{Lm}^{IV}}{k} \tag{29}$$

$$V_{D2} = V_{D3} = V_{C2} - nV_{Lm}^{IV} \tag{30}$$

According to (19), (22), (26), (28), and (29), the following equations are achieved:

$$V_{D1} = V_{S1} = \frac{1}{1-D} V_{in} \tag{31}$$

$$V_{S2} = \frac{1}{(1-D)^2} V_{in} \tag{32}$$

According to (19), (21), (22), (27), and (30), the following equations can be derived:

$$V_{D2} = V_{D3} = \frac{nk(2-D)}{(1-D)^2} V_{in} \tag{33}$$

$$V_{DO} = \frac{(2-D)(1+nk)}{(1-D)^2} V_{in} \tag{34}$$

Current stress of power semiconductors

By applying the ampere-second balance low for C_O, the following equation for the current passing through C_3 in operation mode IV is achieved:

$$I_{C3}^{IV} = \frac{1}{1-D} I_O \tag{35}$$

Using (15) and (35), the following equation can be written:

$$I_{Lm} = \frac{(1+n)}{1-D} I_O \tag{36}$$

According to (4) and (5), the current passing through C_2 in operation mode II is as follows:

$$I_{C2}^{II} = \frac{I_{Lm} - I_{C1}^{II}}{2n} \tag{37}$$

By applying the ampere-second balance low for C_2 and according to (35) and (37), the following equation for the current passing through the capacitor C_1 in operation mode II can be obtained as:

$$I_{C1}^{II} = I_{Lm} + \frac{2n}{D} I_O \tag{38}$$

Now, by substituting (36) into (38), the current passing through capacitor C_1 in operation mode II is achieved as follows:

$$I_{C1}^{II} = \left(\frac{1+n}{1-D} + \frac{2n}{D} \right) I_O \tag{39}$$

Using (39), the current of C_1 in operation mode IV can be derived as follows:

$$I_{C1}^{IV} = -D \left(\frac{1+n}{(1-D)^2} + \frac{2n}{D(1-D)} \right) I_O \tag{40}$$

According to (36), (37), and (39), the current passing through C_2 in operation mode II is obtained as follows:

$$I_{C2}^{II} = -\frac{1}{D} I_O \tag{41}$$

Using (14) and (40), inductor current L_1 is expressed as:

$$I_{L1} = D \left(\frac{1+n}{(1-D)^2} + \frac{2n}{D(1-D)} \right) I_O \tag{42}$$

According to operation mode II, it can be written:

$$I_{S1} = I_{L1} + I_{C1}^{II} \tag{43}$$

$$I_{S2} = I_{C1}^{II} \tag{44}$$

$$I_{D2} = I_{D3} = -I_{C2}^{II} \tag{45}$$

According to operation mode IV, it can be written:

$$I_{D1} = -I_{C1}^{IV} \tag{46}$$

$$I_{DO} = I_{C3}^{IV} \tag{47}$$

Using (39) and (42) into (43), the current stress of S_1 can be obtained as follows:

$$I_{S1} = \left(\frac{1+n}{(1-D)^2} + \frac{2n}{D(1-D)}\right) I_O \tag{48}$$

Using (39) and (44), current stress of S_2 can be obtained as:

$$I_{S2} = \left(\frac{1+n}{1-D} + \frac{2n}{D}\right) I_O \tag{49}$$

According to (35), (40), (41), (45-47), the following equations are obtained for the current stress of the diodes:

$$I_{D1} = D\left(\frac{1+n}{(1-D)^2} + \frac{2n}{D(1-D)}\right) I_O \tag{50}$$

$$I_{D2} = I_{D3} = \frac{1}{D} I_O \tag{51}$$

$$I_{DO} = \frac{1}{1-D} I_O \tag{52}$$

Voltage gain in DCM

Discontinuous Conduction Mode (DCM) analysis is considered for the condition where the coupled inductor enters the DCM condition. The converter has five operation modes in DCM condition. These operation modes are shown in Fig. 3a-e. Figure 4 shows the key waveform of the suggested converter in DCM condition. According to this figure, by applying the volt-second balance low for L_m, the following equation is achieved:

$$V_{Lm}^{II} D + V_{Lm}^{IV} \Delta_1 = 0 \tag{53}$$

According to (13), (20) and (53), the voltage gain in DCM condition is obtained as:

$$M_{DCM} = 1 + \frac{2nk(2-D)}{1-D} + \frac{D(2-D)(1+n)}{\Delta_1(1-D)} \tag{54}$$

According to Fig. 4, the average value of the current passing through L_m is expressed as:

$$I_{Lm} = \frac{\Delta I_{Lm}}{2} \tag{55}$$

According to (20) and (55), the average current passing through L_m is achieved as follows:

$$I_{Lm} = \frac{kD(2-D)}{2f_S L_m(1-D)} V_{in} \tag{56}$$

By applying the ampere-second balance low for C_O, the following equation is obtained:

$$I_{CO}^{II} D + I_{CO}^{IV} \Delta_1 + I_{CO}^{V}(1 - D - \Delta_1) = 0 \tag{57}$$

According to (6), (16), (18) and (57), the following equation can be written for C_3 in operating mode IV:

$$I_{C3}^{IV} = \frac{1}{\Delta_1} I_O \tag{58}$$

According to (15) and (58), the following equation for the average current through L_m is achieved:

$$I_{Lm} = \frac{1+n}{\Delta_1} I_O \tag{59}$$

By substituting (56) into (59), the following equation for Δ_1 can be obtained:

$$\Delta_1 = \frac{2f_S L_m(1+n)(1-D)}{D(2-D)R} M_{DCM} \tag{60}$$

According to (54) and (60), the output voltage gain of the converter in DCM condition is achieved as:

$$M_{DCM} = \left(\frac{2-D}{1-D}\right)\left(nk + \sqrt{n^2k^2 + \frac{D^2R}{2f_S L_m}}\right) \tag{61}$$

Using (23), (61), and assuming that the normalized input inductor time constant equals $\tau = f_s L_m / R$, where R represents the load resistance, the boundary conditions between CCM and DCM are as follows:

$$\tau_{DCM} = D^2 \Big/ \left(2 \left(\frac{5 - 2D + D^2}{(2 - D)(1 - D)} \right) - 8 \right) \tag{62}$$

According to this equation, the boundary conduction mode (BCM), CCM, and DCM regions for $n = 2$ can be plotted as shown in Fig. 5.

Non-ideal voltage gain in CCM

The deviation of the non-ideal voltage gain of the proposed converter is influenced by parasitic parameters and leakage inductance. In this analysis, the resistances of the components are considered as follows: inductor and coupled inductor (r_{L1}, r_{L11}, r_{L12}); capacitors (r_{C1}, r_{C2}, r_{C3}, r_{CO}); switches ($r_{DS(on)1}$, $r_{DS(on)2}$); diodes (r_{D1}, r_{D2}, r_{D3}, r_{DO}), along with their forward voltage drops (V_{F1}, V_{F2}, V_{F3}, V_{FO}). By applying KVL in the loops containing L_1 and L_m the following equations are derived in the operating mode II:

$$V_{L1}^{II} = V_{in} - r_{L1} I_{L1} - R_{ds1} (I_{L1} + I_{C1}^{II}) \tag{63}$$

$$V_{Lm}^{II} = kV_{in} + kV_{C1} - kI_{C1}^{II} (r_{L11} + r_{C1} + R_{ds1} + R_{ds2}) - kR_{ds1} I_{L1} \tag{64}$$

$$V_{C2} + V_{C3} = 2nV_{Lm}^{II} - V_{F2} - V_{F3} - \frac{V_O}{DR} (r_{C2} + r_{C3} + r_{D2} + r_{D3}) \tag{65}$$

By substituting (65) into (64), it can be written:

$$V_{C2} + V_{C3} = 2n \left[kV_{in} + kV_{C1} - kI_{C1}^{II} (r_{L11} + r_{C1} + R_{ds1} + R_{ds2}) - kR_{ds1} I_{L1} \right] - V_{F2} - V_{F3} - \frac{V_O}{DR} (r_{C2} + r_{C3} + r_{D2} + r_{D3}) \tag{66}$$

By applying KVL in the loops including inductors L_1 and L_m, the following equations are obtained in the operating mode IV:

$$V_{L1}^{IV} = V_{in} - V_{C1} - V_{F1} - I_{L1} (r_{L1} + r_{C1} + r_{D1}) \tag{67}$$

$$V_{Lm}^{IV} = \frac{k}{kn + 1} \left[V_{in} + V_{C2} + V_{C3} - V_{FO} - V_O - I_{Lm} \left(\frac{r_{L11} + r_{L12} + r_{C2} + r_{C3} + r_{DO}}{n + 1} \right) \right] \tag{68}$$

By applying the volt-second balance for L_1, the following equation for the voltage across the capacitor C_1 is obtained:

$$V_{C1} = \frac{V_{in}}{1 - D} - I_{L1} \left(\frac{r_{L1} + DR_{ds1}}{1 - D} + r_{C1} + r_{D1} \right) - \frac{DR_{ds1}}{1 - D} I_{C1}^{II} - V_{F1} \tag{69}$$

By applying the volt-second balance for L_m, the following equation is obtained:

$$\begin{aligned} &V_{in} \left(\frac{knD + 1}{1 - D} \right) + V_{C1} \frac{D(kn + 1)}{1 - D} - I_{C1}^{II} \frac{D(kn + 1)(r_{L11} + r_{C1} + R_{ds1} + R_{ds2})}{1 - D} \\ &- I_{L1} \frac{D(kn + 1) R_{ds1}}{1 - D} + V_{C2} + V_{C3} - V_{FO} - I_{Lm} \left(\frac{r_{L11} + r_{L12} + r_{C2} + r_{C3} + r_{DO}}{n + 1} \right) = V_O \end{aligned} \tag{70}$$

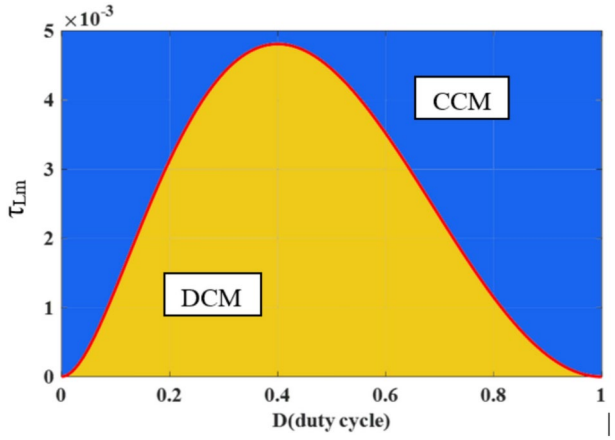

Fig. 5. The proposed converter CCM and DCM regions.

By substituting (66) into (70), it can be written:

$$\begin{aligned}\overbrace{\left[\frac{DR+(r_{C2}+r_{C3}+r_{D2}+r_{D3})}{DR}\right]}^{A_2}V_O &= V_{in}\left(\frac{knD+1}{1-D}+2nk\right)+V_{C1}\left[\frac{D(kn+1)}{1-D}+2nk\right]\\ &-I_{C1}^{II}\left[\frac{D(kn+1)(r_{L11}+r_{C1}+R_{ds1}+R_{ds2})}{1-D}+2nk(r_{L11}+r_{C1}+R_{ds1}+R_{ds2})\right]\\ &-I_{L1}\left[\frac{D(kn+1)R_{ds1}}{1-D}+2nkR_{ds1}\right]-I_{Lm}\overbrace{\left[\frac{r_{L11}+r_{L12}+r_{C2}+r_{C3}+r_{DO}}{n+1}\right]}^{A_1}\\ &-V_{F2}-V_{F3}-V_{FO}\end{aligned} \tag{71}$$

By substituting (69) into (71), the following equation is obtained:

$$\begin{aligned}A_2V_O = V_{in}&\overbrace{\left[\frac{knD+1+2nk}{1-D}+\frac{D(kn+1)}{(1-D)^2}+2nk\right]}^{A_3}\\ -I_{L1}&\overbrace{\left[\frac{D(kn+1)R_{ds1}}{1-D}+2nkR_{ds1}+\left(\frac{D(kn+1)}{1-D}+2nk\right)\left(\frac{r_{L1}+DR_{ds1}}{1-D}+r_{C1}+r_{D1}\right)\right]}^{A_4}\\ -I_{C1}^{II}&\overbrace{\left[\frac{D(kn+1)(r_{L11}+r_{C1}+R_{ds1}+R_{ds2})}{1-D}+2nk(r_{L11}+r_{C1}+R_{ds1}+R_{ds2})+\frac{D^2(kn+1)R_{ds1}}{(1-D)^2}+\frac{2nkDR_{ds1}}{1-D}\right]}^{A_5}\\ -A_1I_{Lm}-V_{F1}&\overbrace{\left[\frac{D(kn+1)}{1-D}+2nk\right]}^{A_6}-V_{F2}-V_{F3}-V_{FO}\end{aligned} \tag{72}$$

By simplifying Eq. (72), it can be written:

$$V_O = \frac{A_3}{A_2}V_{in}-\frac{A_4}{A_2}I_{L1}-\frac{A_5}{A_2}I_{C1}^{II}-\frac{A_1}{A_2}I_{Lm}-\frac{A_6}{A_2}V_{F1}-\frac{1}{A_2}(V_{F2}+V_{F3}+V_{FO}) \tag{73}$$

According to (36), (39), and (42), the following equations are expressed:

$$I_{L1} = D\left(\frac{1+n}{(1-D)^2}+\frac{2n}{D(1-D)}\right)\frac{V_O}{R} \tag{74}$$

$$I_{C1}^{II} = \left(\frac{1+n}{1-D}+\frac{2n}{D}\right)\frac{V_O}{R} \tag{75}$$

$$I_{Lm} = \frac{(1+n)}{1-D}\frac{V_O}{R} \tag{76}$$

By substituting (74-76) into (73), it can be written:

$$\begin{aligned}V_O = \frac{A_3}{A_2}V_{in}&-\frac{A_4D}{A_2}\left[\frac{1+n}{(1-D)^2}+\frac{2n}{D(1-D)}\right]\frac{V_O}{R}-\frac{A_5}{A_2}\left[\frac{1+n}{1-D}+\frac{2n}{D}\right]\frac{V_O}{R}\\ &-\frac{A_1}{A_2}\left[\frac{1+n}{1-D}\right]\frac{V_O}{R}-\frac{A_6}{A_2}V_{F1}-\frac{1}{A_2}(V_{F2}+V_{F3}+V_{FO})\end{aligned} \tag{77}$$

By simplifying (77), the following equation is obtained:

$$\begin{aligned}V_O&\overbrace{\left[1+\frac{A_4D}{A_2R}\left[\frac{1+n}{(1-D)^2}+\frac{2n}{D(1-D)}\right]+\frac{A_5}{A_2R}\left[\frac{1+n}{1-D}+\frac{2n}{D}\right]+\frac{A_1}{A_2R}\left[\frac{1+n}{1-D}\right]\right]}^{A_7}\\ &= \frac{1}{A_2}[A_3V_{in}-A_6V_{F1}-(V_{F2}+V_{F3}+V_{FO})]\end{aligned} \tag{78}$$

By simplifying (78), the non-ideal output voltage of the proposed converter with the influence of leakage inductance and parasitic resistances of the elements is obtained as follows:

$$V_O = \frac{1}{A_2A_7}[A_3V_{in}-A_6V_{F1}-(V_{F2}+V_{F3}+V_{FO})] \tag{79}$$

Considering (79) and according to Table 2, the non-ideal voltage gain versus duty cycle D is illustrated in Fig. 6. This figure shows how voltage gain changes with the duty cycle (D) for both an ideal and a non-ideal power converter. The solid red line represents the ideal theoretical case, while the blue dashed line accounts for non-ideal model, assuming an output power of 210 W. Figure 6 is plotted in $k = 0.985$ and $R = 840\ \Omega$. As can be seen, the effect of leakage inductance and parasitic resistances is less at lower duty cycles leading to a comparatively higher efficiency.

The small inset zooms in on a specific range (around $D = 0.5$) to highlight the gap between the two models. As expected, the non-ideal case results in a lower voltage gain due to practical factors like parasitic resistances and switching losses. Interestingly, the non-ideal gain peaks sharply at high duty cycles before dropping, indicating potential instability or inefficiency in that region.

Design considerations

Inductor design

The voltage across the inductor is proportional to the current that passes through the inductor per unit of time. So, it can be written as:

$$V_L = L\frac{\Delta I_L}{\Delta t} \tag{80}$$

By considering the maximum acceptable current ripple of 20% for inductors L_1 and L_m and according to operation mode II and substituting (1) and (20) into (80), the minimum inductor inductance of L_1 and L_m are obtained from the following equation:

$$L_1 > \frac{DV_{in}}{\Delta I_L f_S} = \frac{DV_{in}}{20\% I_{L1} f_S} = \frac{D(1-D)^2 R}{20\% M\left[D(1+n)+2n(1-D)\right] f_S} \tag{81}$$

$$L_m > \frac{D(2-D)V_{in}}{\Delta I_{Lm}(1-D) f_S} = \frac{D(2-D)V_{in}}{20\% I_{Lm}(1-D) f_S} = \frac{D(2-D)R}{20\% M(1+n) f_S} \tag{82}$$

Capacitor design

The current passing through the capacitor is proportional to the voltage changes across the capacitor per unit of time. So, it can be written as:

$$I_C = C\frac{\Delta V_C}{\Delta t} \tag{83}$$

By considering the maximum acceptable ripple of voltage for capacitors usually 1% of the voltage across capacitor C_1) and according to operation mode II and using (39) and (83), the following equation is obtained:

$$C_1 > \frac{(D+2n-nD)I_O}{\Delta V_{C1}(1-D) f_S} = \frac{(D+2n-nD)P_{out}}{1\% V_{C1}(1-D) V_O f_S} \tag{84}$$

According to (5), the current passing through C_1 and C_2 is equal in operation mode II. By taking into consideration the maximum acceptable voltage ripple for capacitors (usually 1% of the voltage across capacitor C_2, C_3, and C_O).

And by substituting (6) and (41) into (83), the following equations can be written:

$$C_2 > \frac{I_O}{\Delta V_{C2} f_S} = \frac{P_{out}}{1\% V_{C2} V_O f_S} \tag{85}$$

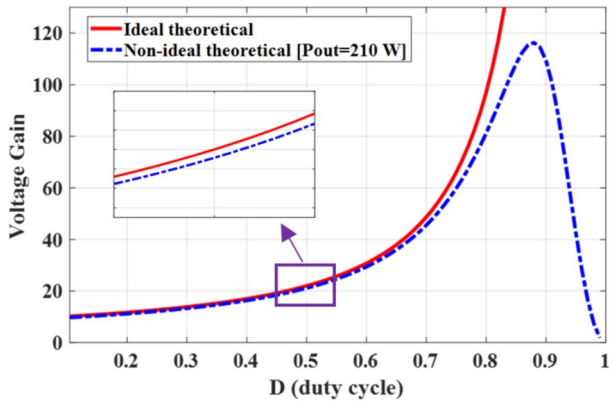

Fig. 6. Effect of the leakage inductance and parasitic components on the output voltage gain.

RMS Values at $V_{in}=20$ V, $P_{out}=210$ W, $f_S=50$ kHz, $n=2$, and $D=0.5$	
$I_{S1}^{RMS}=\left(\frac{1+n}{(1-D)^2}+\frac{2n}{D(1-D)}\right)\frac{V_O\sqrt{D}}{R}=9.78A$	$I_{DO}^{RMS}=\frac{V_O}{R\sqrt{1-D}}=0.7A$
$I_{S2}^{RMS}=\left(\frac{1+n}{1-D}+\frac{2n}{D}\right)\frac{V_O\sqrt{D}}{R}=4.89A$	$I_{CO}^{RMS}=\frac{V_O}{R}\sqrt{\frac{D}{1-D}}=0.49A$
$I_{C2}^{RMS}=I_{C3}^{RMS}=\frac{V_O}{R\sqrt{D(1-D)}}=1A$	$I_{secondary}^{RMS}=\frac{V_O}{R}\sqrt{\frac{4-3D}{D(1-D)}}=1.58A$
$I_{L1}^{RMS}=\frac{DV_O}{R}\left(\frac{1+n}{(1-D)^2}+\frac{2n}{D(1-D)}\right)=7A$	$I_{D2}^{RMS}=I_{D3}^{RMS}=\frac{V_O}{R\sqrt{D}}=0.7A$
$I_{primary}^{RMS}=\frac{V_O}{R}\sqrt{\frac{D+4n^2+n^2D^2+4nD-2nD^2-4n^2D}{D(1-D)^2}}=5A$	
$I_{C1}^{RMS}=I_O\sqrt{\frac{D^2+4n^2+n^2D^2+4nD-2nD^2-4n^2D}{D(1-D)^3}}=6.91A$	
$I_{D1}^{RMS}=D\left(\frac{1+n}{(1-D)^2}+\frac{2n}{D(1-D)}\right)\frac{V_O\sqrt{1-D}}{R}=4.89A$	

Table 1. RMS current values of the components.

Percentage (%)	P_{Loss}[W]	Parameters
28.86%	1.98	Power loss of inductor/coupled inductor
14.14%	0.97	Power loss of MOSFETs
49.56%	3.4	Power loss of diodes
7.44%	0.51	Power loss of capacitors
–	6.86	Total power loss
96.8%	–	Efficiency
$V_{in}=20$ V, $P_{out}=210$ W, $f_S=50$ kHz, $D=0.5$ $r_{L1}=10$ mΩ, $r_{L11}=10$ mΩ, $r_{L12}=22$ mΩ $r_{C1}=0.01$ Ω, $r_{C2}=r_{C3}=0.015$ Ω, $r_{CO}=0.025$Ω S_1,S_2: SE150180GTS $R_{ds}=4.8$mΩ, $t_{d(on)=}$20 ns, $t_{d(off)=}$37 ns D_1,D_2,D_3: SBR10U300CT $r_D=20$mΩ with maximum $V_F=0.64$ V in 5 A D_O: STTH12R06 $r_D=17$mΩ with maximum $V_F=1.4$ in 5 A		

Table 2. Power losses distribution.

$$C_3 > \frac{I_O}{\Delta V_{C3} f_S} = \frac{P_{out}}{1\% V_{C3} V_O f_S} \tag{86}$$

$$C_O > \frac{DI_O}{\Delta V_{CO} f_S} = \frac{DP_{out}}{1\% V_{CO} V_O f_S} \tag{87}$$

Efficiency analysis

In this section, the converter efficiency is investigated by considering the presence of parasitic resistances of the elements. Table 1 shows the RMS values of the current passing through the elements by considering $n=2$, $D=0.5$, and output resistance $R=840$ Ω. Table 2 displays the power loss breakdown across different proposed converter components. In this table, V_F denotes the forward voltage drop of the diode. R_{ds} and r_D are the on-state resistance of the switch and the diode, respectively. Internal resistances of the capacitor and the inductor are represented by r_C and r_L, respectively. In addition, the power semiconductors specification and their part numbers are provided. Figure 7 shows the power loss distributions of the constituent elements of the suggested converter. According to this figure, the highest share of power losses is related to diode losses, and the lowest is related to capacitor losses. The efficiency and voltage gain curves of the converter versus the duty cycle and for $n=2$ are shown in Fig. 8. As shown in this figure, although the voltage gain of the converter increases with the increase of the duty cycle, the efficiency of the converter is acceptable up to a certain range and then decreases. As can be seen, at high-duty cycle ranges, conduction losses increase, and efficiency is reduced.

Inductor losses: The conduction losses of the inductor and coupled inductor are calculated as following equations:

$$\begin{cases} p_{L,Cond}^{loss} = r_L (I_L^{RMS})^2 \\ p_{L1,Cond}^{loss} = 0.01 \times (7)^2 = 0.49W \\ p_{L\_Primary,\,Cond}^{loss} = 0.01 \times (5)^2 = 0.25W \\ p_{L\_Secondary,\,Cond}^{loss} = 0.022 \times (1.58)^2 = 0.05W \end{cases} \tag{88}$$

$$P_{L,Cond\_total}^{loss} = P_{L1,Cond}^{loss} + P_{L\_Primary,Cond}^{loss} + P_{L\_Secondary,Cond}^{loss} = 0.79\,W \tag{89}$$

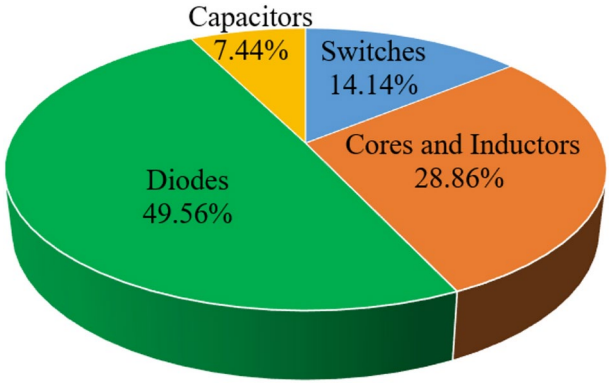

Fig. 7. Power loss distributions of the proposed topology at 210 W output power.

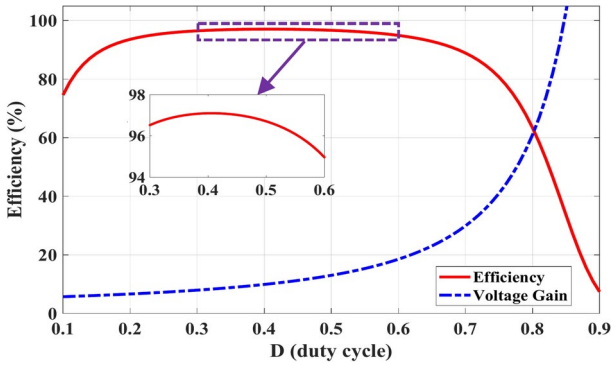

Fig. 8. Efficiency and voltage gain curves versus duty cycle.

The core power losses related to the inductors is calculated as[30]:

$$P_C = k f_s^{\alpha} B_m^{\beta} \tag{90}$$

The power loss (P_C) is expressed in unit W/kg. The parameters α, β and k known as the Steinmetz coefficients, are typically specified by manufacturers for various core materials. For ferrite materials, the values of α can vary from 1 to 2, ($1 \le \alpha \le 2$). Based on Faraday's Law, it can be written:

$$V_L = N\frac{d\varphi(t)}{dt} = NA_c\frac{dB(t)}{dt} \tag{91}$$

The parameter A_c represents the core area as specified by manufacturers for various types of magnetic cores. N is the turns of inductor's windings. Hence, the peak flux density of ΔB for the inductor and the coupled inductor, can be determined as follows:

$$\begin{cases} \Delta B_{L1} = \dfrac{1}{N_{L1}A_{C\_L1}}\displaystyle\int_0^{DT_s} V_{L1}dt = \frac{V_{L1}DT_s}{N_{L1}A_{C\_L1}} = \frac{V_{L1}D}{N_{L1}A_{C\_L1}f_s} \\ \Delta B_{L\_Primary} = \dfrac{1}{N_{L\_Primary}A_{C\_CL}}\displaystyle\int_0^{DT_s} V_{L\_Primary}dt = \frac{V_{L\_Primary}DT_s}{N_{L\_Primary}A_{C\_CL}} = \frac{V_{L\_Primary}D}{N_{L\_Primary}A_{C\_CL}f_s} \\ \Delta B_{L\_Secondary} = \dfrac{1}{N_{L\_Secondary}A_{C\_CL}}\displaystyle\int_0^{DT_s} V_{L\_Secondary}dt = \frac{V_{L\_Secondary}DT_s}{N_{L\_Secondary}A_{C\_CL}} = \frac{V_{L\_Secondary}D}{N_{L\_Secondary}A_{C\_CL}f_s} \end{cases} \tag{92}$$

The core loss in both inductor and coupled inductor can be expressed as $P_{Core} = P_C M$, where M represents the mass of the core. Therefore, considering $B_m = \Delta B/2$, the core loss of inductor and coupled inductor is calculated as:

$$\begin{aligned} P_{Core}^{loos} &= kf_s^{\alpha}B_{m1}^{\beta}M_{L1} + kf_s^{\alpha}B_{m\_Primary}^{\beta}M_{CL} + kf_s^{\alpha}B_{m\_Secondary}^{\beta}M_{CL} \\ &= kf_s^{\alpha}\left[B_{m1}^{\beta}M_{L1} + \left(B_{m\_Primary}^{\beta} + B_{m\_Secondary}^{\beta}\right)M_{CL}\right] \\ = kf_s^{\alpha}\left[\left(\frac{V_{L1}D}{2N_{L1}A_{C\_L1}f_s}\right)^{\beta}M_{L1} + \left(\left(\frac{V_{L\_Primary}D}{2N_{L\_Primary}A_{C\_CL}f_s}\right)^{\beta} + \left(\frac{V_{L\_Secondary}D}{2N_{L\_Secondary}A_{C\_CL}f_s}\right)^{\beta}\right)M_{CL}\right] \\ &= 5.597\ \times\ 10^{-4} \times (50\times10^3)^{1.43} \times \left[(0.05618)^{2.85} \times 0.089 + \left((0.08498)^{2.85} + (0.08498)^{2.85}\right) \times 0.215\right] \\ &= 2934.15 \times [0.000025 + 0.00019 + 0.00019] = 1.19\,W \end{aligned} \tag{93}$$

The parameters utilized for the calculation of the core losses are as:
$k = 5.597\times10^{-4}$, $\alpha = 1.43$, $\beta = 2.85$, $M_{L1} = 0.089$ kg, $M_{CL} = 0.215$, $A_{C\_L1} = 178\text{mm}^2$, $A_{c\_CL} = 353\text{mm}^2$ fs = 50 kHz.
The total power loss of inductors is obtained as follows:

$$P_{L\_total}^{loss} = P_{L,Cond\_total} + P_{Core} = 0.79 + 1.19 = 1.98W \tag{94}$$

Switch losses: The power losses of the switches are determined as:

$$\begin{cases} P_{SW}^{loss} = R_{ds}(I_S^{RMS})^2 + \dfrac{1}{2T_S}\left[I_{ds(on)}V_{ds}t_{(on)} + I_{ds(off)}V_{ds}t_{(off)}\right] \\ P_{SW1}^{loss} = 0.0048 \times (9.78)^2 + 25\times10^3\left[5.5\times23\times20\times10^{-9} + 6\times17\times37\times10^{-9}\right] = 0.62W \\ P_{SW2}^{loss} = 0.0048 \times (4.89)^2 + 25\times10^3\left[2.5\times35\times20\times10^{-9} + 2.5\times35\times37\times10^{-9}\right] = 0.25W \end{cases} \tag{95}$$

C_{OSS} is the parasitic capacitor of the switch. P_{Coss} is obtained as follows[31]:

$$\begin{cases} P_{Coss} = \dfrac{1}{2}f_S Coss V_{DS}^2 \\ P_{Coss,S1} = \dfrac{1}{2}f_S C_{OSS,S1}\left(\dfrac{V_{in1}}{1-D}\right)^2 = \dfrac{1}{2}\times50000\times476\times10^{-12}\left(\dfrac{20}{1-0.5}\right)^2 = 0.02W \\ P_{Coss,S2} = \dfrac{1}{2}f_S C_{OSS,S2}\left(\dfrac{V_{in1}}{(1-D)^2}\right)^2 = \dfrac{1}{2}\times50000\times476\times10^{-12}\left(\dfrac{20}{(1-0.5)^2}\right)^2 = 0.08W \end{cases} \tag{96}$$

The total power loss of the switches is obtained from the following equation:

$$P_{SW\_total}^{loss} = P_{SW1}^{loss} + P_{SW2}^{loss} + P_{Coss,S1} + P_{Coss,S2} = 0.62 + 0.25 + 0.02 + 0.08 = 0.97W \tag{97}$$

Diode losses: The power losses of the diodes are determined as:

$$\begin{cases} P_D^{loss} = V_F I_{D\_avg} + (I_D^{RMS})^2 r_D \\ P_{D1}^{loss} = 0.6\times3.45 + (4.89)^2\times0.02 = 2.55W \\ P_{D2}^{loss} = 0.5\times0.49 + (0.7)^2\times0.02 = 0.25W \\ P_{D3}^{loss} = 0.5\times0.49 + (0.7)^2\times0.02 = 0.25W \\ P_{Do}^{loss} = 0.7\times0.49 + (0.7)^2\times0.017 = 0.35W \end{cases} \tag{98}$$

The total power loss of the diodes is obtained from the following equation:

$$P_{D\_total}^{loss} = P_{D1}^{loss} + P_{D2}^{loss} + P_{D3}^{loss} + P_{Do}^{loss} = 3.4W \tag{99}$$

Capacitor losses: Losses of the capacitors are determined as follows:

$$\begin{cases} P_C^{loss} = (I_C^{RMS})^2 \times ESR \\ P_{C1}^{loss} = (6.91)^2\times0.01 = 0.48W \\ P_{C2}^{loss} = (1)^2\times0.015 = 0.015W \\ P_{C3}^{loss} = (1)^2\times0.015 = 0.015W \\ P_{CO}^{loss} = (0.49)^2\times0.025 = 0.006W \end{cases} \tag{100}$$

The total power loss of the capacitors is obtained as the following equation:

$$P_{C\_total}^{loss} = P_{C1}^{loss} + P_{C2}^{loss} + P_{C3}^{loss} + P_{CO}^{loss} = 0.51W \tag{101}$$

Therefore, the total power losses P_{Loss} is written as:

$$P_{total}^{loss} = P_{L\_total}^{loss} + P_{SW\_total}^{loss} + P_{D\_total}^{loss} + P_{C\_total}^{loss} = 6.86W \tag{102}$$

Consequently, the total efficiency of the proposed converter can be calculated as:

$$\eta_{Converter} = \frac{P_o}{P_o + P_{total}^{loss}} \times 100\% = \frac{210}{210 + 6.86} \times 100\% = 96.8\% \tag{103}$$

Dynamic model and control method

The proposed topology consists of six storage elements, where the voltage and current of the components can be derived as follows:

First stage:

$$V_{L1}^{II} = V_{in} \Rightarrow \frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} \tag{104}$$

$$V_{Lm}^{II} = k\left(V_{in} + V_{C1}\right) \Rightarrow \frac{di_{Lm}}{dt} = \frac{k\left(V_{in} + V_{C1}\right)}{L_m} \tag{105}$$

$$i_{C1}^{II} = i_{Lm} + \frac{2n}{D} I_O \Rightarrow \frac{dv_{C1}}{dt} = \frac{i_{Lm}}{C_1} + \frac{2n}{DC_1} I_O \tag{106}$$

$$i_{C2}^{II} = -\frac{I_O}{D} \Rightarrow \frac{dv_{C2}}{dt} = -\frac{I_O}{DC_2} \tag{107}$$

$$i_{C3}^{II} = -\frac{I_O}{D} \Rightarrow \frac{dv_{C3}}{dt} = -\frac{I_O}{DC_3} \tag{108}$$

$$i_{CO}^{II} = I_O \Rightarrow \frac{dv_{CO}}{dt} = \frac{I_O}{C_O} \tag{109}$$

Second stage:

$$V_{L1}^{IV} = V_{in} - V_{C1} \Rightarrow \frac{di_{L1}}{dt} = \frac{V_{in} - V_{C1}}{L_1} \tag{110}$$

$$V_{Lm}^{IV} = \frac{k\left(V_O - V_{in} - V_{C2} - V_{C3}\right)}{n+1} \Rightarrow \frac{di_{Lm}}{dt} = -\frac{k\left(V_O - V_{in} - V_{C2} - V_{C3}\right)}{\left(n+1\right) L_m} \tag{111}$$

$$i_{C1}^{IV} = -i_{L1} \Rightarrow \frac{dv_{C1}}{dt} = -\frac{i_{L1}}{C_1} \tag{112}$$

$$i_{C2}^{IV} = \frac{i_{Lm}}{n+1} \Rightarrow \frac{dv_{C2}}{dt} = \frac{i_{Lm}}{\left(n+1\right) C_2} \tag{113}$$

$$i_{C3}^{IV} = \frac{i_{Lm}}{n+1} \Rightarrow \frac{dv_{C3}}{dt} = \frac{i_{Lm}}{\left(n+1\right) C_3} \tag{114}$$

$$i_{CO}^{IV} = -i_{C3}^{IV} + I_O \Rightarrow \frac{dv_{CO}}{dt} = -\frac{i_{Lm}}{\left(n+1\right) C_O} + \frac{I_O}{C_O} \tag{115}$$

To derived state space vectors, these equations can be rewritten as follows:

$$\frac{dx}{dt} = X^{II} D + X^{IV}\left(1 - D\right) \tag{116}$$

Therefore, the achieved equations can be stated as follows:

$$\frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} - \frac{\left(1 - D\right) V_{C1}}{L_1} \tag{117}$$

$$\frac{di_{Lm}}{dt} = \frac{k}{L_m}\left[\frac{1 + nD}{n+1} V_{in} + V_{C1} D + \frac{1 - D}{n+1}\left(V_{C2} + V_{C3} - V_{Co}\right)\right] \tag{118}$$

$$\frac{dv_{C1}}{dt} = \frac{D}{C_1} i_{Lm} + \frac{2nV_{Co}}{R_O C_1} - \frac{1 - D}{C_1} i_{L1} \tag{119}$$

$$\frac{dv_{C2}}{dt} = -\frac{V_O}{DR_O C_2} D + \frac{\left(1 - D\right)}{\left(n+1\right) C_2} i_{Lm} \Rightarrow \frac{dv_{C2}}{dt} = -\frac{V_O}{R_O C_2} + \frac{\left(1 - D\right)}{\left(n+1\right) C_2} i_{Lm} \tag{120}$$

$$\frac{dv_{C3}}{dt} = -\frac{V_O}{DR_O C_3} D + \frac{\left(1 - D\right)}{\left(n+1\right) C_3} i_{Lm} \Rightarrow \frac{dv_{C3}}{dt} = -\frac{V_O}{R_O C_3} + \frac{\left(1 - D\right)}{\left(n+1\right) C_3} i_{Lm} \tag{121}$$

$$\frac{dv_{Co}}{dt} = \frac{V_{Co}}{R_O C_O} D + \left(-\frac{i_{Lm}}{(n+1)\, C_O} + \frac{V_O}{R_O C_O} \right) (1-D) \Rightarrow \frac{dv_{Co}}{dt} = \frac{V_{Co}}{R_O C_O} + \frac{(1-D)}{(n+1)\, C_o} i_{Lm} \quad (122)$$

Dynamic modeling of the proposed converter

For dynamic response analysis, independent storage elements are considered as state variables vector (x). Given that the voltage equations for capacitors C_2 and C_3 are identical, one of them can be excluded to simplify the analysis. In this converter, L_1 , L_m, C_1, C_2, and C_o are selected as state variables. The state variables vector (x), input vector (u), and output vector (y) are considered as follows:

$$\begin{cases} x^T = [\quad i_{L1} \quad i_{Lm} \quad v_{C1} \quad v_{C2} \quad v_{Co} \ ] \\ u = [V_{in}] \\ y^T = [V_o] \end{cases} \quad (123)$$

The average state space of the overall system can be displayed as follows

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases} \quad (124)$$

Equation (124) can be expressed as:

$$\dot{x} = \begin{bmatrix} 0 & 0 & -\frac{(1-D)}{L_1} & 0 & 0 \\ 0 & 0 & \frac{kD}{L_m} & \frac{k(1-D)}{L_m(n+1)} & -\frac{k(1-D)}{L_m(n+1)} \\ -\frac{1-D}{C_1} & \frac{D}{C_1} & 0 & 0 & \frac{2n}{R_O C_1} \\ 0 & \frac{(1-D)}{(n+1)C_2} & 0 & 0 & -\frac{1}{R_O C_2} \\ 0 & \frac{(1-D)}{(n+1)C_o} & 0 & 0 & \frac{1}{R_o C_o} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{Lm} \\ V_{C1} \\ V_{C2} \\ V_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{k(1+nD)}{L_m(n+1)} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in} \quad (125)$$

$$y = [\ 0 \quad 0 \quad 0 \quad 0 \quad 1 \ ] \begin{bmatrix} i_{L1} \\ i_{Lm} \\ V_{C1} \\ V_{C2} \\ V_{Co} \end{bmatrix} + [0]\, V_{in} \quad (126)$$

In this case, A, B, C, and D can be written as:

$$A = \begin{bmatrix} 0 & 0 & -\frac{(1-D)}{L_1} & 0 & 0 \\ 0 & 0 & \frac{kD}{L_m} & \frac{k(1-D)}{L_m(n+1)} & -\frac{k(1-D)}{L_m(n+1)} \\ -\frac{1-D}{C_1} & \frac{D}{C_1} & 0 & 0 & \frac{2n}{R_O C_1} \\ 0 & \frac{(1-D)}{(n+1)C_2} & 0 & 0 & -\frac{1}{R_O C_2} \\ 0 & \frac{(1-D)}{(n+1)C_o} & 0 & 0 & \frac{1}{R_o C_o} \end{bmatrix} \quad (127)$$

$$B = \begin{bmatrix} \frac{1}{L_1} \\ \frac{k(1+nD)}{L_m(n+1)} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (128)$$

$$C = [\ 0 \quad 0 \quad 0 \quad 0 \quad 1 \ ] \quad (129)$$

$$D = [0] \quad (130)$$

According to the small signal modeling method, state variables, duty cycles, input and output voltages consist of two segments, a DC ($\overline{X}$, $\overline{Y}$, $\overline{U}$, $\overline{D}$) part and an AC ($\tilde{x}$, $\tilde{y}$, $\tilde{u}$, $\tilde{d}$) part.

$$\begin{cases} x = \overline{X} + \tilde{x} \\ y = \overline{Y} + \tilde{y} \\ u = \overline{U} + \tilde{u} \\ d = \overline{D} + \tilde{d} \end{cases} \quad (131)$$

It is supposed that the AC values are significantly smaller than the DC values ($\overline{X} >> \tilde{x}$, $\overline{Y} >> \tilde{y}$, $\overline{U} >> \tilde{u}$, $\overline{D} >> \tilde{d}$) and do not change considerably during one period. Therefore, the small signal model can be displayed as follows:

$$\begin{cases} \dot{\tilde{x}} = A'\tilde{x} + B'\tilde{u} + E'\tilde{D} \\ \hat{y} = C'\tilde{x} + D'\tilde{u} + F'\tilde{D} \end{cases} \tag{132}$$

In the small signal analysis, input voltage is short circuited. In (132), $\dot{x}$, $\tilde{u}$ and $\dot{y}$ are the state variables vector, control signals, and output signals, respectively. The new state space vector based on these definitions can be rewrite as follows:

$$\dot{x} = \begin{bmatrix} 0 & 0 & -\frac{(1-\overline{D})}{L_1} & 0 & 0 \\ 0 & 0 & \frac{k\overline{D}}{L_m} & \frac{k(1-\overline{D})}{L_m(n+1)} & -\frac{k(1-\overline{D})}{L_m(n+1)} \\ -\frac{1-\overline{D}}{C_1} & \frac{\overline{D}}{C_1} & 0 & 0 & \frac{2n}{R_O C_1} \\ 0 & \frac{(1-\overline{D})}{(n+1)C_2} & 0 & 0 & -\frac{1}{R_O C_2} \\ 0 & \frac{(1-\overline{D})}{(n+1)C_o} & 0 & 0 & \frac{1}{R_o C_o} \end{bmatrix} \begin{bmatrix} \tilde{i}_{L1} \\ \tilde{i}_{Lm} \\ \tilde{V}_{C1} \\ \tilde{V}_{C2} \\ \tilde{V}_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{k(1+n\overline{D})}{L_m(n+1)} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tilde{V}_{in} + \begin{bmatrix} \frac{\overline{I}_{L1}}{L_1} \\ \frac{k\overline{V}_{C1}}{L_m} - \frac{k\overline{V}_{C2}}{L_m(n+1)} + \frac{k\overline{V}_{Co}}{L_m(n+1)} \\ \frac{\overline{I}_{L1}}{L_1} + \frac{\overline{I}_{Lm}}{C_1} \\ -\frac{\overline{I}_{Lm}}{(n+1)C_2} \\ -\frac{\overline{I}_{Lm}}{(n+1)C_O} \end{bmatrix} \tilde{D} \tag{133}$$

$$y = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \tilde{i}_{L1} \\ \tilde{i}_{Lm} \\ \tilde{V}_{C1} \\ \tilde{V}_{C2} \\ \tilde{V}_{Co} \end{bmatrix} + [0]\,\tilde{V}_{in} + [0]\,\tilde{D} \tag{134}$$

where A$\prime$($n \times n$ fixed matrix), E$\prime$($n \times n$ fixed matrix), and C$\prime$($m \times n$ fixed matrix) are calculated as follows:

$$A' = \begin{bmatrix} 0 & 0 & -\frac{(1-\overline{D})}{L_1} & 0 & 0 \\ 0 & 0 & \frac{k\overline{D}}{L_m} & \frac{k(1-\overline{D})}{L_m(n+1)} & -\frac{k(1-\overline{D})}{L_m(n+1)} \\ -\frac{1-\overline{D}}{C_1} & \frac{\overline{D}}{C_1} & 0 & 0 & \frac{2n}{R_O C_1} \\ 0 & \frac{(1-\overline{D})}{(n+1)C_2} & 0 & 0 & -\frac{1}{R_O C_2} \\ 0 & \frac{(1-\overline{D})}{(n+1)C_o} & 0 & 0 & \frac{1}{R_o C_o} \end{bmatrix} \tag{135}$$

$$B' = \begin{bmatrix} \frac{1}{L_1} \\ \frac{k(1+n\overline{D})}{L_m(n+1)} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{136}$$

$$E' = \begin{bmatrix} \frac{\overline{I}_{L1}}{L_1} \\ \frac{k\overline{V}_{C1}}{L_m} - \frac{k\overline{V}_{C2}}{L_m(n+1)} + \frac{k\overline{V}_{Co}}{L_m(n+1)} \\ \frac{\overline{I}_{L1}}{L_1} + \frac{\overline{I}_{Lm}}{C_1} \\ -\frac{\overline{I}_{Lm}}{(n+1)C_2} \\ -\frac{\overline{I}_{Lm}}{(n+1)C_O} \end{bmatrix} \tag{137}$$

$$C' = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{138}$$

Transfer function of this state-space vector can be expressed as:

$$G(s) = \frac{V_{Co}(s)}{D(s)} = \frac{8.409e04s^3 + 1.989e-07s^2 + 1.044e14s + 42.65}{s^5 - 361.8s^4 - 2.164e08s^3 + 7.794e10s^2 - 6.994e15s + 2.531e18} \tag{139}$$

For this system, by using parameters' values from Table 3, the step response can be modeled in MATLAB. The step-response is shown in Fig. 9. The step response shown in the figure indicates that the system is highly unstable. Initially, the output remains close to zero, but as time progresses, it exhibits an exponential divergence, rapidly growing to an extremely large value (on the order of 10^{23}). This behavior suggests that the system has at least one unstable pole with a positive real part, leading to an unbounded response. Such instability can arise from inherently unstable open-loop system. To address this issue, a stability analysis should be conducted by examining the system's poles and adjusting the controller parameters potentially through modifying the pole placement strategy to ensure all poles have negative real parts, leading to a stable response.

Pole placement control description

Since the proposed topology is unstable it is required to apply pole-placement strategy, in this case, control diagram is illustrated in Fig. 10. This block diagram represents a state-space control system designed to regulate the output voltage V_{CO}. The reference input $V_{CO,ref}$ is processed through an integrator to eliminate steady-state error, with feedback gains k_q and k_x adjusting the control input. Matrices A', C', D, and E' define the system dynamics, ensuring stability and desired performance. The control law combines integral and state feedback

Components	Values
Input voltages	$V_{in} = 20$ V
Output voltages	$V_{out} = 420$ V
Duty cycles	$D = 0.5$
Turn ratio	$n = 2$
Output power	*300 W*
Inductors	$L_1 = 300\ \mu H$ *and* $L_m = 150uH$
Capacitor	$C_1 = C_2 = C_3 = 4.7\ \mu F$ *and* $C_O = 220\ \mu F$

Table 3. Components' values.

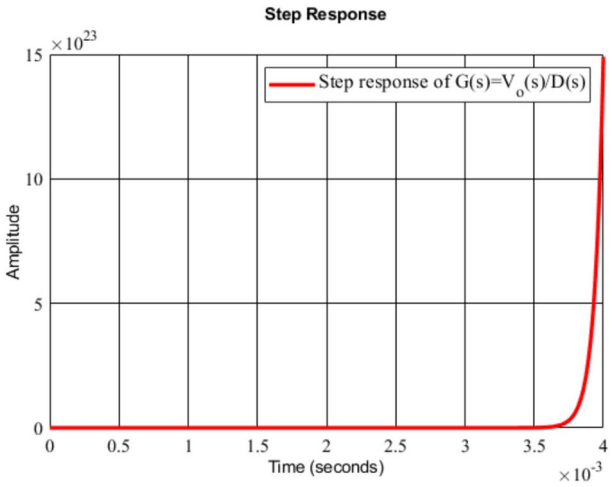

Fig. 9. Step-response of the proposed topology before pole placement strategy.

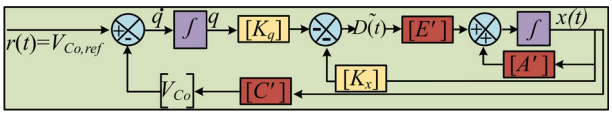

Fig. 10. Schematic of the close-loop control method.

to achieve accurate voltage regulation. This structure suggests a pole placement control approach for enhanced system response.

Based on Fig. 10, the following equations can be written:

$$\tilde{d} = -k_x \tilde{x} - k_q q \tag{140}$$

$$\dot{q} = r - y = r - C' \tilde{x} \tag{141}$$

where q is the integrator output and r is the reference signals vector for the output variable. The vector r can be expressed as:

$$r(t)^T = [V_{Co,ref}] \tag{142}$$

It can be simplified as follows:

$$\dot{\underset{1}{q}}(t) = V_{Co,ref} - V_{Co}(t) \tag{143}$$

In this method, if the control system is complete state controllable, it can be located the closed-loop poles to any suitable location with proper design of the state feedback gain matrix. The controllability matrix of this system is defined as follows:

$$\Phi_c = \left[E' \middle| A'E' \middle| A'^2 E' \middle| \ldots \middle| A'^{n-1} E' \right] = \left[E' \middle| A'E' \right] \tag{144}$$

For this system, if the rank of the controllability matrix $\emptyset_c$ is complete, then the system is completely controllable.

$$rank(\Phi_c) = n = 2 \tag{145}$$

Using Fig. 10 and Eqs. (135), (136), and (137), the open-loop state matrixes change to the matrixes $\tilde{A}'$ and $\tilde{E}'$ as follows:

$$\begin{cases} \begin{bmatrix} \dot{\tilde{x}}(t) \\ \dot{q}(t) \end{bmatrix} = \begin{bmatrix} A' & 0 \\ -C' & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} + \begin{bmatrix} E' \\ 0 \end{bmatrix} \tilde{D}(t) + \begin{bmatrix} 0 \\ I \end{bmatrix} r(t) \\ y(t) = \begin{bmatrix} C' & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} \end{cases} \tag{146}$$

$$\tilde{A}' = \begin{bmatrix} A' & 0 \\ -C' & 0 \end{bmatrix}, \tilde{E}' = \begin{bmatrix} E' \\ 0 \end{bmatrix} \tag{147}$$

Now, the new controllability matrix $\overline{\Phi_c}$ is assumed as follows:

$$\overline{\Phi_c} = \left[\hat{E}' \middle| \tilde{A}'\tilde{E}' \middle| \tilde{A}'^2\tilde{E}' \middle| \ldots \middle| \tilde{A}'^{n-1}\tilde{E}'\right] = \left[\tilde{E}' \middle| \tilde{A}'\tilde{E}'\right] \tag{148}$$

Then, the $\overline{\Phi_c}$ can be written as follows:

$$\overline{\Phi_c} = \underbrace{\begin{bmatrix} E' & A' \\ 0 & -C' \end{bmatrix}}_{M} \begin{bmatrix} I & 0 \\ 0 & \Phi_c \end{bmatrix} \tag{149}$$

If the following matrix rank is equal to $n+m$, the defined system will be completely state controlled.

$$rank(M) = n + m = 7 \tag{150}$$

The fourth eigenvalues of the matrix $\tilde{A}'$ are obtained as follows:

$$eig(\tilde{A}') = \widehat{\lambda} = 1.0e+04 \times \begin{cases} 0.0000 + 0.0000i \\ 1.5651 + 0.0000i \\ -1.5650 + 0.0000i \\ -0.0001 + 0.5343i \\ -0.0001 - 0.5343i \\ 0.0002 + 0.0000 \end{cases} \tag{151}$$

As can be seen, two eigenvalues have positive real part. These eigenvalues should be sufficiently shifted to the left side of the *jw* axis in order to reach the desired location of the converter closed-loop eigenvalues and achieve desired phase margin ($PM \geq 80$) and gain margin ($GM \geq 10$). The new eigenvalues are determined as follows:

$$eig(\tilde{A}') = \widehat{\lambda} = 1.0e+05 \times \begin{cases} 0.0000 + 0.0000i \\ -0.1435 + 0.0000i \\ -0.4565 + 0.0000i \\ -0.0330 + 0.0534i \\ -0.0330 - 0.0534i \\ -8.8000 + 0.0000 \end{cases} \tag{152}$$

Using the formula in MATLAB for placing the eigenvalues by importing the matrixes ($\tilde{A}'$ and $\tilde{E}'$), and considering the designed places for the closed-loop eigenvalues, this relation can be written:

$$k = [k_x, k_q] = place(\tilde{A}', \tilde{E}', \lambda') \tag{153}$$

The control coefficients matrixes k_x and k_q are obtained as follows:

$$k_x = \begin{bmatrix} -2.7238 & 1.1290 & 0.2140 & 0.0665 & 381.1460 \end{bmatrix} \tag{154}$$

$$k_q = [-1.6225e+06] \tag{155}$$

Also, after this control method, the transfer functions are obtained as follows:

$$G(s) = \frac{V_{Co}(s)}{D(s)} = \frac{-1.054e09s^4 + 1.201e14s^3 + 5.733e17s^2 + 2.274e22s - 4.807e10}{s^6 + 9.466e05s^5 + 5.97e10s^4 + 9.664e14s^3 + 5.914e18s^2 + 2.274e22s - 2.232e09} \tag{156}$$

By importing (21) and (22) in (28), the state equations of the control system are written as follows

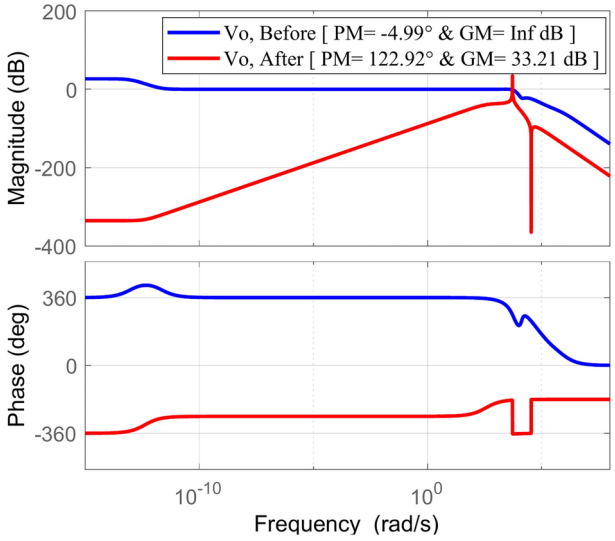

Fig. 11. Bode plot comparison of the system before and after control implementation. The phase margin (PM) and gain margin (GM) improvements indicate enhanced stability and robustness after applying the control strategy.

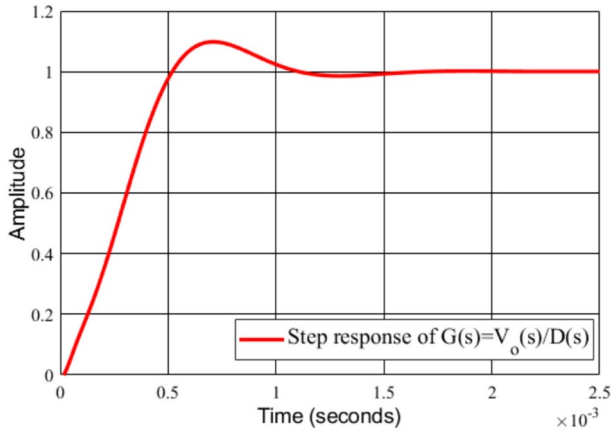

Fig. 12. Step response of the controlled system, showing a smooth transient with minimal overshoot and a fast settling time, demonstrating effective voltage regulation.

$$\begin{cases} \begin{bmatrix} \dot{\tilde{x}}(t) \\ \dot{q}(t) \end{bmatrix} = \begin{bmatrix} A' - E'k_x & -E'k_q \\ -C' & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} + \begin{bmatrix} 0 \\ I \end{bmatrix} r(t) \\ y(t) = \begin{bmatrix} C' & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} \end{cases} \tag{157}$$

The bode diagram illustrates the frequency response of the system before and after applying the control strategy in Fig. 11. The magnitude plot (top) shows how the system gain varies with frequency, while the phase plot (bottom) depicts the phase shift across different frequencies. Before control (blue line), the phase response and the phase margin was negative (-4.99°), confirming that the system was unstable. The gain margin was infinite, suggesting no gain crossover point, further emphasizing instability. After applying control (red line), the magnitude response was significantly improved, leading to a more stable frequency response. The phase response also became smoother, reducing abrupt shifts. The phase margin increased to 122.92°, and the gain margin became 33.21 dB, ensuring system stability and robustness. Overall, the applied control strategy effectively stabilizes the system by improving margins, leading to a well-conditioned and reliable design.

Furthermore, the step response of the utilized control strategy is depicted at Fig. 12. This figure shows the step response of the system, which represents how the system's output $V_O(s)$ responds to a step input in $D(s)$. The output starts at zero and rises quickly, indicating a fast transient response. The system overshoots above the final steady-state value (around 1.2 before settling back to 1). Overshoot occurs due to the system's dynamics and can indicate underdamping. The system stabilizes at around 1.5 ms. This suggests a fast response time, which

is ideal in many control applications. After the transient response, the output remains close to 1, indicating no steady-state error.

Comprehensive comparison

In this section, the proposed converter is compared with some other converters. In Table 4, the voltage gain, the number of elements, normalized voltage stress (NVS) across the main power switch, input and output common ground feature, and the efficiency of the converters at 210 W are gathered and tabulated. In order to make a fair comparison, the value of $n=2$ is considered for the turn ratio of all converters. Figure 13a shows the curves of the output voltage gain versus the duty cycle of the suggested structure and other compared converters. Based on this figure, the voltage gain of the suggested converter is higher than the voltage gain of other compared converters for all duty cycle values. Therefore, it can be said that the suggested topology is an high-step-up converter. Figure 13b shows the output voltage gain per the number of elements (Gain/TCC) versus the duty cycle. According to this figure, the output voltage gain of the proposed converter is higher than other converters. Therefore, it can be said that the proposed converter provides a high output voltage gain for a low number of components compared to other references. On the other hand, it can be concluded that the proposed topology components are structured better than the other topologies to provide higher voltage gains. Figure 13c shows the normalized voltage stress across the main power switch. As shown in this figure, the normalized voltage stress across the main power switch of the proposed converter has the lowest value compared to other structures for all duty cycle values.

Furthermore, with an increase in the duty cycle, the normalized voltage stress across the main power switch of the suggested converter decreases. This highlights the superiority of the proposed converter, as the reduction in voltage stress is evident when the duty cycle is raised in relation to the output voltage. As a result, a power switch with low power specifications and low $R_{ds(on)}$ can be used, which reduces the cost and increases the efficiency. The total normalized voltage stress across the semiconductor elements is shown in Fig. 13d. According to this figure, the total normalized voltage stress of the proposed converter is lower than the structures in[14,16,17,19,27,28] for all duty cycle values. Furthermore, for $D<0.65$, the total normalized voltage stress of the proposed converter is lower than the structures in[24,29]. It should be noted that when $D>0.65$, conduction losses increase. Moreover, the converter presented in[18] has the lowest total normalized voltage stress compared to the other converters. According to {R2-6} Table 4, the number of components of the proposed converter is equal to the number of components of the structures presented in[13,18,19]. Other compared structures have more components than the proposed converter. Another notable advantage of the proposed topology is the establishment of a common ground for both input and output, resulting in reduced electromagnetic interference (EMI) issues. Furthermore, the experimental efficiency of the proposed converter in the output power of 210 W is lower than the efficiency of[25] and higher than the efficiency of all other compared converters.

Experimental Results

In this section, to verify the theoretical analysis, the experimental results of the prototype of the suggested converter are presented. The prototype of the proposed converter is shown in Fig. 14. The specifications of the prototype are listed in Table 2. The goal is to convert the input voltage $V_{in}=20$ V to the output voltage $V_{out}=440$ V until the converter delivers 210 W output power. For this purpose, by setting $n=2$ and according

Ref	Voltage gain (M_{CCM})	No. of elements				NVS across main switch	Gain/TCC	Total NVS across components	Common ground	Eff(%) 210W
		S	D	C	L+CL					
[13]	$\frac{2n+3}{1-D}$	1	5	5	$0+1^{2w}$	$\frac{1}{2n+3}$	$\frac{M_{CCM}}{12}$	$\frac{4n+6}{2n+3}$	✓	96.2
[14]	$\frac{2+nD}{1-D}$	2	6	3	$0+2^{2w}$	$\frac{1}{2+nD}$	$\frac{M_{CCM}}{13}$	$\frac{8+4nD}{2+nD}$	✓	94.7
[15]	$\frac{3+2n+nD}{1-D}$	1	6	6	$0+1^{2w}$	$\frac{1}{3+2n+nD}$	$\frac{M_{CCM}}{14}$	$\frac{5n+6}{3+2n+nD}$	✓	93.2
[16]	$\frac{n(2-D)^2+(1-D)}{(1-D)^2}$	3	4	5	$0+2^{2w}$	$\frac{1-D}{1-D+n(2-D)^2}$	$\frac{M_{CCM}}{14}$	$\frac{2+8n-4D}{1-D+n(2-D)^2}$	✓	96.1
[17]	$\frac{n(2-D)+(1-D)^2}{(1-D)^2}$	4	4	5	$0+2^{2w}$	$\frac{1-D}{n(2-D)+(1-D)^2}$	$\frac{M_{CCM}}{15}$	$\frac{3+3n-D}{n(2-D)+(1-D)^2}$	✓	91
[18]	$\frac{3+n}{1-D}$	1	5	5	$0+1^{2w}$	$\frac{1}{3+n}$	$\frac{M_{CCM}}{12}$	$\frac{n+6}{n+3}$	✓	96.1
[19]	$\frac{1+D+2n(1-D)}{(1-D)^2}$	2	4	4	$1+1^{2w}$	$\frac{1-D}{1+D+2n(1-D)}$	$\frac{M_{CCM}}{12}$	$\frac{6+2n-2D}{1+D+2n(1-D)}$	✓	93.7
[24]	$\frac{2n+3}{1-D}$	2	6	6	$0+2^{2w}$	$\frac{1}{2n+3}$	$\frac{M_{CCM}}{16}$	$\frac{6+6n-nD}{2n+3}$	✓	95.2
[25]	$\frac{2n+2}{1-D}$	2	6	6	$0+2^{2w}$	$\frac{1}{2+2n}$	$\frac{M_{CCM}}{16}$	$\frac{4n+5}{2n+2}$	×	96.8
[27]	$\frac{2n+4}{1-D}$	3	6	4	$0+2^{3w}$	$\frac{1}{2n+4}$	$\frac{M_{CCM}}{15}$	$\frac{7n+10}{2n+4}$	×	96.2
[28]	$\frac{2n+2}{1-D}$	4	6	7	$2+2^{3w}$	$\frac{1}{2+2n}$	$\frac{M_{CCM}}{21}$	$\frac{5n+4}{1+n}$	✓	96
[29]	$\frac{3n+2+D(2n-1)}{1-D}$	2	9	8	$0+2^{3w}$	$\frac{1}{3n+2+D(2n-1)}$	$\frac{M_{CCM}}{21}$	$\frac{9n+6}{2+3n+(2n-1)D}$	✓	90
Proposed	$\frac{1+n(2-D)^2}{(1-D)^2}$	2	4	4	$1+1^{2w}$	$\frac{1-D}{1+n(2-D)^2}$	$\frac{M_{CCM}}{12}$	$\frac{5+6n-3D(n+1)}{1+n(2-D)^2}$	✓	96.3

Table 4. Comparison of the proposed converter with different relevant step-Up DC-DC converters.

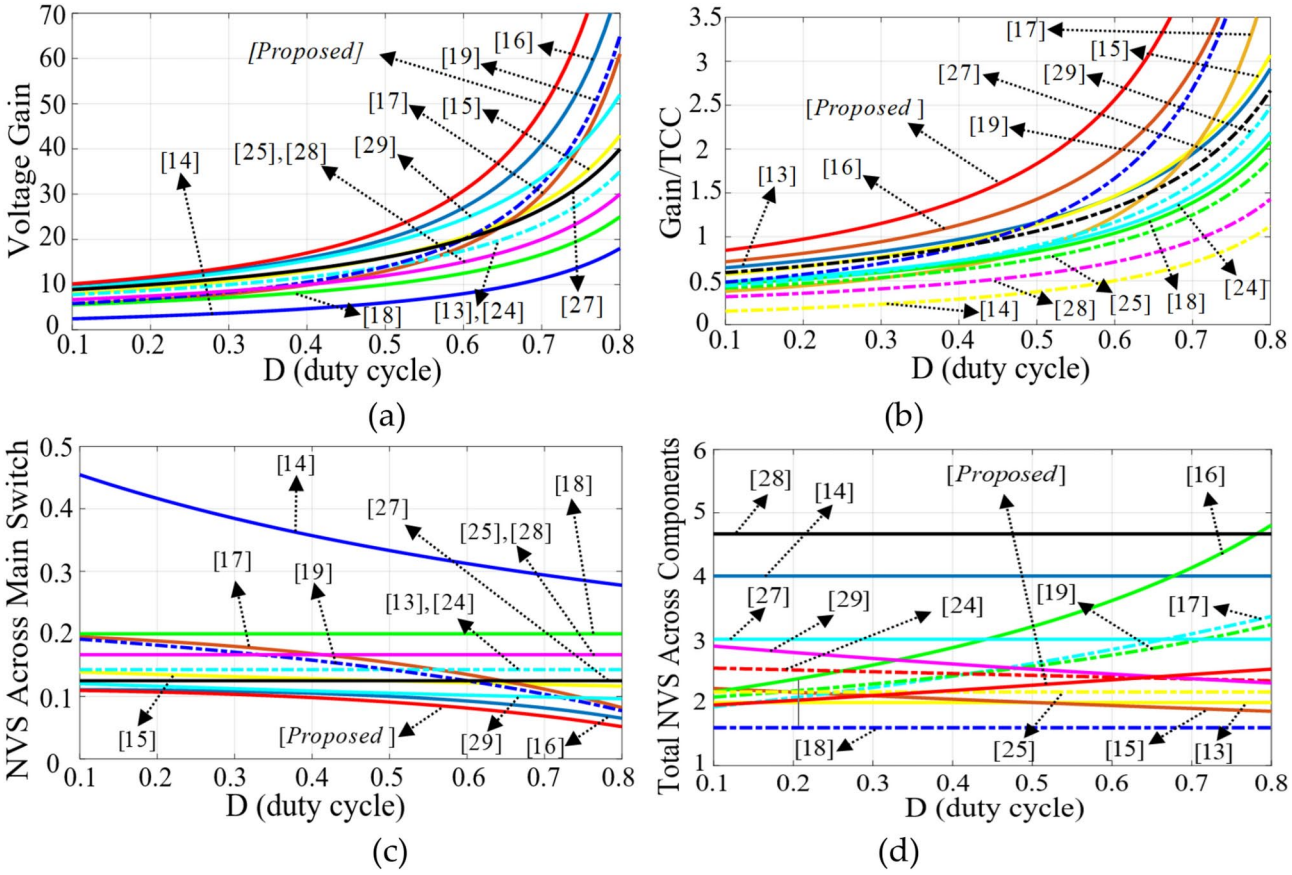

Fig. 13. Comparison of the proposed converter with converters mentioned in {R2-6} Table 4 in terms of (**a**) output voltage gain, (**b**) Gain/TCC, (**c**) normalized voltage stress (NVS) across the main power switch, (**d**) normalized total voltage standing (NTVS).

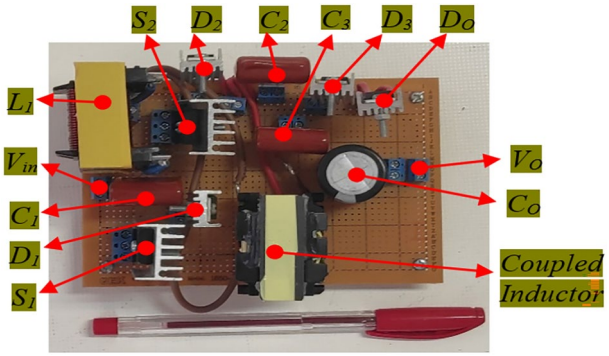

Fig. 14. Laboratory prototype of the proposed converter.

to (24), the converter's duty cycle should be considered equal to $D=0.5$. The switching frequency is considered equal to $f_S=50$ kHz. An 840 Ω load is placed on the output port. By considering $\Delta I_{L1}=1$ A and $\Delta I_{Lm}=4.25$ A and according to (81) and (82), the minimum inductance values of L_1 and L_m are equal to 200 µH and 140 µH, respectively. Therefore, the inductance values of L_1 and L_m in the prototype are considered equal to 300 µH and 150 µH, respectively. By considering $\Delta V_{C1}=8$ V, $\Delta V_{C2}=\Delta V_{C3}=3$ V, and $\Delta V_{CO}=0.03$ V and according to (84)-(87), the minimum capacity values of C_1, C_2, C_3, and C_O are equal to 4.3 µF, 3.3 µF, 3.3 µF and 166 µF, respectively. So, the capacity values of C_1, C_2, and C_3 are considered equal to 4.7 µF, and the capacitance value of C_O is considered equal to 220 µF. Figure 15a shows the output current and voltage waveforms obtained from the laboratory prototype. It is shown in this figure that the output voltage is equal to 420 V, which proves the statement (24), and the current passing through the output load is equal to 0.5 A. 10 (b) shows the current waveform of L_1. According to this figure, the average current value of L_1 equals 6.96 A, which corresponds to (42). Figure 16

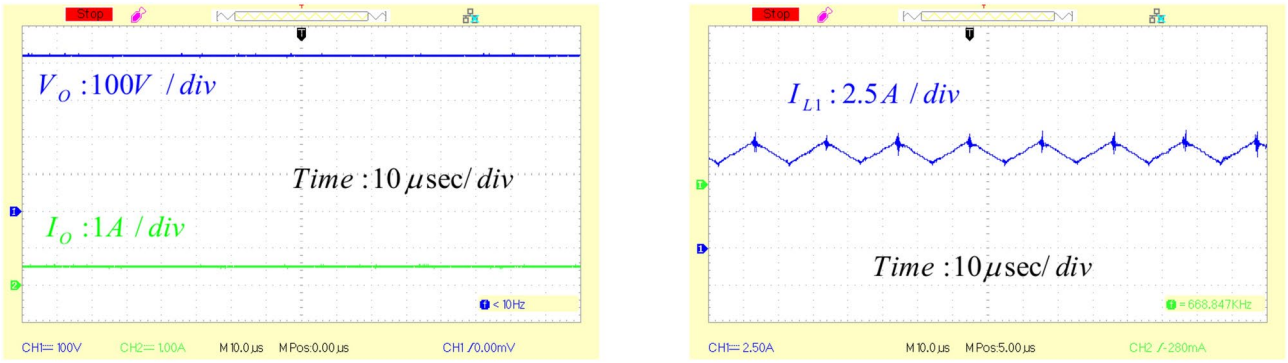

Fig. 15. Experimental results: (**a**) Voltage and current waveforms of the output load. (**b**) waveform of the current passing through L_1.

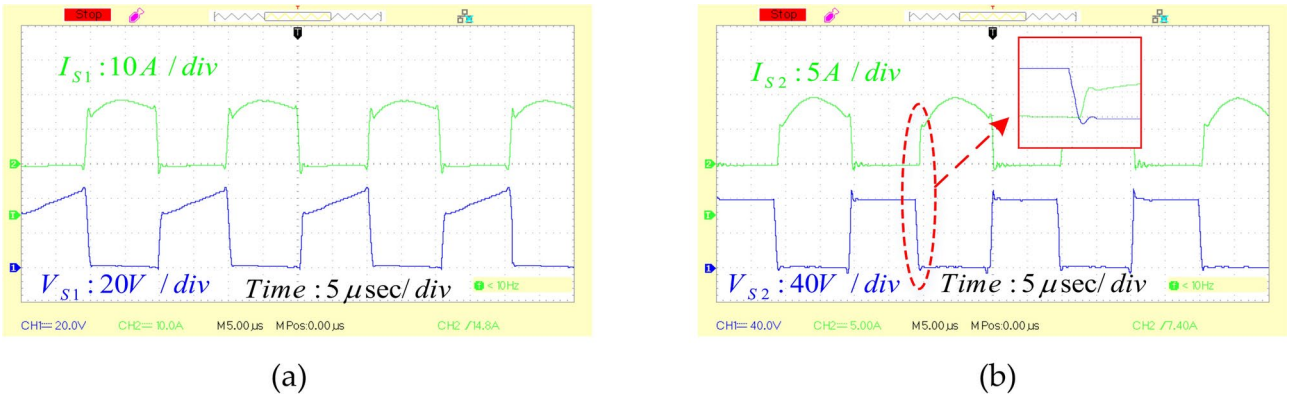

Fig. 16. Voltage and current experimental waveforms of. (**a**) S_1. (**b**) S_2.

shows the current and voltage waveforms of S_1 and S_2. According to Fig. 16a, the voltage stress of S_1 is equal to 38.5 V. In addition, the waveform of the current passing through it is quasi-resonant. Also, according to Fig. 16b, the voltage stress of S_2 equals 78 V. In addition, as can be seen in this figure, S_2 turns on under ZCS conditions, and the waveform of the current passing through this power switch is also quasi-resonant.

Figure 17 shows the voltage and current waveforms of D_1, D_2, D_3, and D_O. According to Fig. 17a, the voltage stress of D_1 is equal to 38 V. As shown in Fig. 17b and c, the voltage stress of D_2 and D_3 is equal to 230 V. As evident from the observation, the current waveforms of these diodes reach zero before experiencing reversed or forward biases. This observation substantiates these diodes' ZCS condition. Figure 17d illustrates voltage and current stress across D_O, which is 348 V, and proves the provided mathematical analysis. Figure 18 shows the voltage waveforms of C_1, C_2, and C_3. As shown in this figure, the voltage across C_1, C_2, and C_3 are equal to 39 V, 117 V, and 117 V, respectively.

The control strategy was successfully implemented in an experimental setup to evaluate its performance under varying conditions. Figure 19a illustrates the system's response to input voltage variations, demonstrating a rapid transient response with minimal overshoot. This confirms the controller's effectiveness in maintaining stability.

Figure 19b presents the system's dynamic response to a load variation. Initially, the load resistance is set at 840Ω, and at a certain instant, it is increased to 1000 Ω. The transient region, highlighted in the middle of the figure, shows the system's reaction to this change. The output current (i_O) decreases as expected due to the reduced load current demand, while the output voltage (V_O) remains stable with minimal deviation, confirming the effectiveness of the applied control strategy. The system successfully regulates the voltage despite the load variation, demonstrating the robustness of the proposed control method.

The experimental and theoretical efficiency curves of the proposed converter versus output power are shown in Fig. 20. As depicted, the prototype's efficiency in $Vin = 20$ V and $Pout = 210$ W is about 96.3%. Consequently, the proposed converter provides higher efficiency than 95.25% for different output power ranges.

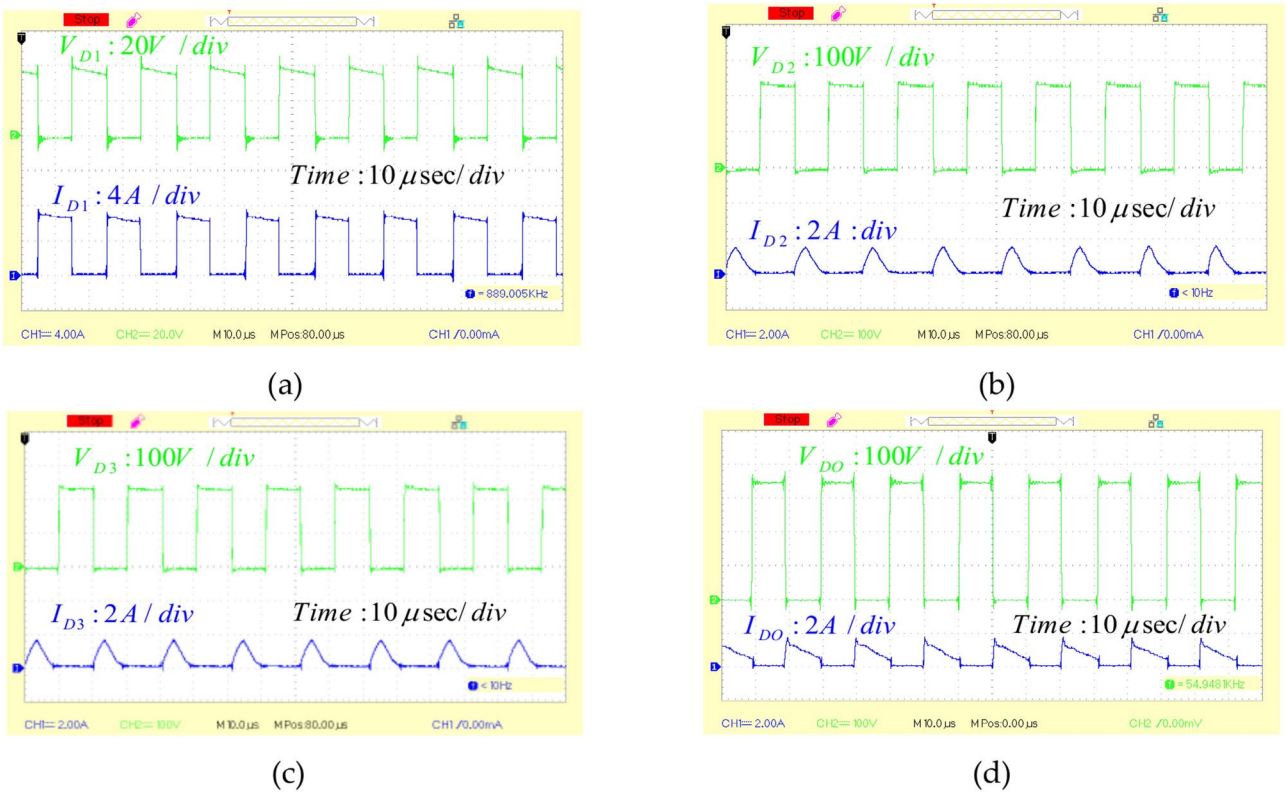

Fig. 17. Voltage and current experimental waveforms of. (**a**) D_1. (**b**) D_2. (**c**) D_3. (**d**) D_O.

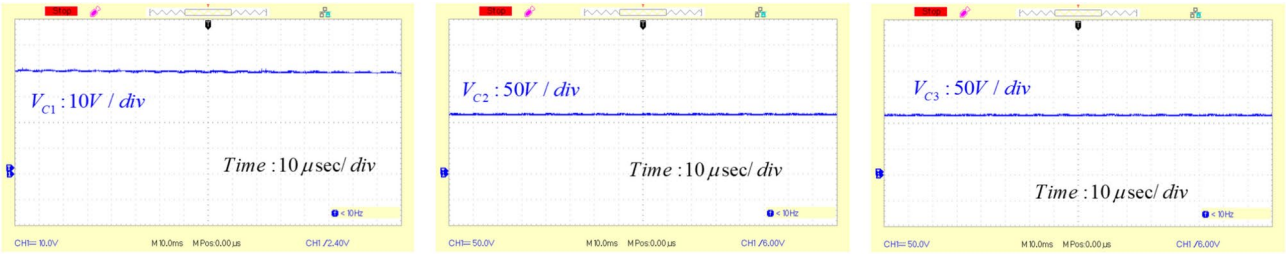

Fig. 18. Experimental results: Voltage waveforms of. (**a**) C_1 (**b**) C_2 (**c**) C_3.

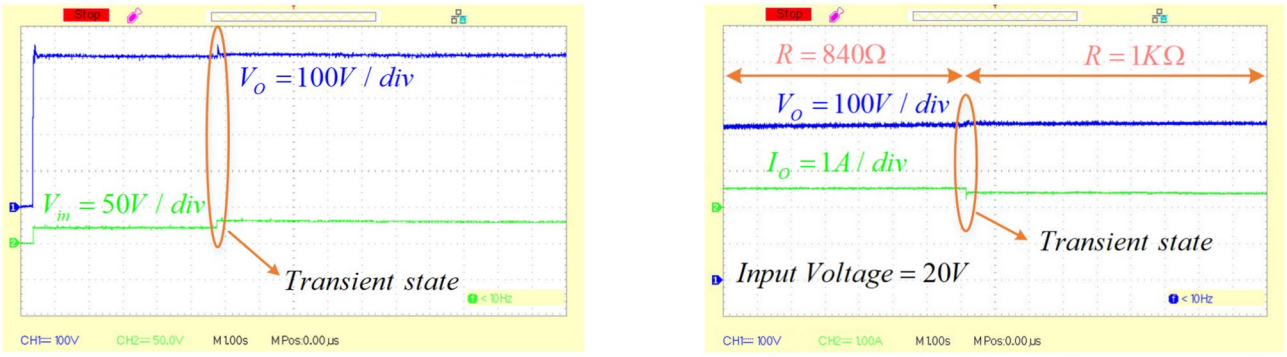

Fig. 19. Experimental validation of the control strategy under. (**a**) input voltage variation. (**b**) load variation.

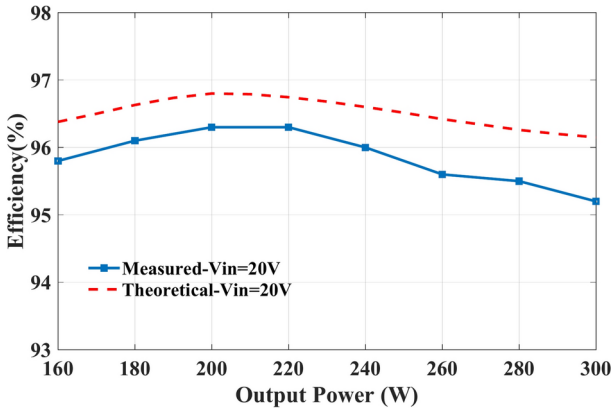

Fig. 20. Experimental and theoretical efficiency of the proposed converter versus output power.

Conclusion

In this paper, a non-isolated quadratic high-step-up DC-DC converter is presented. A coupled inductor and the switched capacitor cell are utilized in this structure to increase the voltage gain. The proposed converter provides high voltage gain with a low number of elements. Low voltage stress across power switches is another advantage of the presented topology, which leads to the selection of MOSFETs with low internal resistance $R_{ds(on)}$. A diode-capacitor clamp circuit is utilized to reduce the negative effects of leakage inductance and recover stored energy, leading to soft switching conditions for half of the diodes. The combination of these features provides a new topology with a high efficiency of 96.3%, which is recorded at 210W. Steady-state analysis, design consideration, and efficiency analysis are presented in detail. The proposed converter is compared with related structures, and it is observed that the proposed topology has higher efficiency and voltage gain compared to other structures. Finally, to verify the converter's performance qualification and mathematical analysis, a 210 W laboratory prototype is built, and its outcomes are thoroughly examined.

Data availability

All data generated or analyzed during this study are included in this published article.

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References

1. Selvam, S., Sannasy, M. & Sridharan, M. Analysis and design of two-switch enhanced gain SEPIC converter. *IEEE Trans. Ind. Appl.* **59**(3), 3552–3561 (2023).
2. Qiu, M., Sun, Z., Liu, X., Meng, H., Marzang, V., Cao, D. A 15x matrix autotransformer switched-capacitor DC-DC converter for datacenter application. 2024 IEEE APEC, Long Beach, CA, USA, 2024, pp. 88-93
3. Fani, R., Akhlaghi, Z. & Adib, E. High step-up DC-DC converter by integration of active switched inductors, built in transformer, and multipliers. *IEEE Trans. Power Electron.* **39**(2), 2468–2477 (2024).
4. Karimi, K., Babaei, E., Karimi, M., Alizadeh, D. & Mousavi, S. M. J. An interleaved high step-up DC–DC converter based on coupled-inductor. *IET Power Electron.* **17**, 473–485 (2024).
5. Nadermohammadi, A. et al. Cost-effective soft-switching ultra-high step-up DC–DC converter with high power density for DC microgrid application. *Sci. Rep.* **14**, 20407 (2024).
6. Marzang, V., Babaei, E., Mehrjerdi, H., Iqbal, A. & Islam, S. A high step-up DC–DC converter based on ASL and VMC for renewable energy applications. *Energy Rep.* **8**, 12699–12711 (2022).
7. Nadermohammadi, A. et al. A non-isolated single-switch ultra-high step-up DC–DC converter with coupled inductor and low-voltage stress on switch. *IET Power Electron.* **17**, 251–265 (2024).
8. Hashemzadeh, S. M., Marzang, V., Pourjafar, S. & Hossein Hosseini, S. An ultra high step-up dual-input single-output DC–DC converter based on coupled inductor. *IEEE Trans. Ind. Electron.* **69**(11), 11023–11034 (2022).
9. Goyal, V. K. & Shukla, A. Two-stage hybrid isolated DC–DC boost converter for high power and wide input voltage range applications. *IEEE Trans. Ind. Electron.* **69**(7), 6751–6763 (2022).
10. Kiran, R. & Kalpana, R. An isolated dual-input half-bridge DC–DC boost converter with reduced circulating power between input ports. *IEEE Canad. J. Electr. Comput. Eng.* **45**(1), 68–76 (2022).
11. Salehi Dobakhshari, S., Milimonfared, J., Taheri, M. & Moradisizkoohi, H. A quasi-resonant current-fed converter with minimum switching losses. *IEEE Trans. Power Electron.* **32**(1), 353–362 (2017).
12. Abbasi Shahabi, M. et al. Symmetric wide-input-voltage range boost Z-source DC–DC converter with reduced current of source and active components. *IEEE Trans. Power Electron.* **38**(8), 9961–9971 (2023).
13. Hassan, W., Lu, D.D.-C. & Xiao, W. Single-switch high step-up DC–DC converter with low and steady switch voltage stress. *IEEE Trans. Ind. Electron.* **66**(12), 9326–9338 (2019).
14. Meier, M. B., da Silva, S. A., Badin, A. A., Romaneli, E. F. R. & Gules, R. Soft-switching high static gain DC–DC converter without auxiliary switches. *IEEE Trans. Ind. Electron.* **65**(3), 2335–2345 (2018).
15. Eskandarpour Azizkandi, M., Sedaghati, F., Shayeghi, H. & Blaabjerg, F. Two-and three-winding coupled-inductor-based high step-up DC–DC converters for sustainable energy applications. *IET Power Electron.* **13**(1), 144–156 (2020).
16. Alavi, P., Mohseni, P., Babaei, E. & Marzang, V. An ultra-high step-up dc–dc converter with extendable voltage gain and soft-switching capability. *IEEE Trans. Ind. Electron.* **67**(11), 9238–9250 (2020).

17. Mohseni, P., Hosseini, S. H. & Maalandish, M. A new soft switching dc–dc converter with high voltage gain capability. *IEEE Trans. Ind. Electron.* **67**(9), 7386–7398 (2020).
18. Sadeghpour, D. & Bauman, J. High-efficiency coupled-inductor switched-capacitor boost converter with improved input current ripple. *IEEE Trans. Ind. Electron.* **69**(8), 7940–7951 (2022).
19. Hasanpour, S., Siwakoti, Y. P., Mostaan, A. & Blaabjerg, F. New semiquadratic high step-up dc/dc converter for renewable energy applications. *IEEE Trans. Power Electron.* **36**(1), 433–446 (2021).
20. Hasanpour, S., Forouzesh, M., Siwakoti, Y. P. & Blaabjerg, F. A new high-gain, high-efficiency SEPIC-based DC–DC converter for renewable energy applications. *IEEE J. Emerg. Sel. Top Ind. Electron.* **2**(4), 567–578 (2021).
21. Marzang, V. et al. A high step-up nonisolated DC–DC converter with flexible voltage gain. *IEEE Trans. Power Electron.* **35**(10), 10489–10500 (2020).
22. Khan, S., Zaid, M., Siddique, M. D. & Iqbal, A. Ultra high gain step up DC/DC converter based on switched inductor and improved voltage lift technique for high-voltage applications. *IET Power Electron.* **15**, 932–952 (2022).
23. Marzang, V. et al. A modified triple-switch triple-mode high step-up DC–DC converter. *IEEE Trans. Ind. Electron.* **69**(8), 8015–8027 (2022).
24. Fani, R., Farshidi, E., Adib, E. & Kosarian, A. Analysis, design, and implementation of a ZVT high step-up DC–DC converter with continuous input current. *IEEE Trans. Ind. Electron.* **67**(12), 10455–10463 (2020).
25. Hu, X., Liang, W., Liu, X. & Yu, Z. A hybrid interleaved DC–DC converter with a wide step-up regulation range and ultralow voltage stress. *IEEE Trans. Ind. Electron.* **67**(7), 5479–5489 (2020).
26. Liang, T.-J., Luo, P. & Chen, K.-H. A high step-up DC–DC converter with three-winding coupled inductor for sustainable energy systems. *IEEE Trans. Ind. Electron.* **69**(10), 10249–10258 (2022).
27. Akhlaghi, B., Molavi, N., Fekri, M. & Farzanehfard, H. High step-up interleaved ZVT converter with low voltage stress and automatic current sharing. *IEEE Trans. Ind. Electron.* **65**(1), 291–299 (2018).
28. He, L. et al. A plug-play active resonant soft switching for current-auto-balance interleaved high step-up DC/DC converter. *IEEE Trans. Power Electron.* **34**(8), 7603–7616 (2019).
29. Salehi, S. M., Dehghan, S. M. & Hasanzadeh, S. Interleaved-input series-output ultra-high voltage gain DC–DC converter. *IEEE Trans. Power Electron.* **34**(4), 3397–3406 (2019).
30. Marzang, V., Islam, S., Iqbal, A., Mehrjerdi, H., Cao, D. A new quadratic high step-up DC-DC converter based on coupled inductors for renewable energy applications. *IEEE J. Emerg. Sel. Topics Power Electron*.
31 Imanlou, A., Babaei, E. and Hosseini, S. A new high voltage gain common-ground step-up DC-DC converter integrating coupled-inductors and switched-capacitors. *Int. J. Circ. Theor. Appl.* (2024).

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Conceptualization, K.K., V.M, M.K., S.H.H., and M.R.F.; methodology, K.K.; software, K.K., V.M., and M.K.; validation, K.K., S.H.H., and M.R.F.; investigation, K.K., V.M, M.K., resources, K.K., V.M., and M.K.; data curation, K.K.; writing—original draft preparation, K.K., V.M., and M.K.; supervision, S.H.H., and M.R.F.; Funding acquisition: K.K.; Visualization: K.K., V.M, and M.K.; writing—review and editing: K.K., V.M, and M.K.; project administration, K.K., S.H.H., and M.R.F.; Formal analysis: K.K. All authors have read and agreed to the published version of the manuscript.

Declarations

Competing interests

The authors declare no competing interests.

Additional information

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