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A wafer-level sealed silicon cavity microacoustic platform for radio frequency integration

Jiashuai Xu[1], Zijun Ren[1], Fangsheng Qian[1], Junyan Zheng[1] and Yansong Yang[1]✉

Abstract

This study presents a wafer-level sealed silicon cavity (SSC) microacoustic integration platform to address the limitations in the cavity Silicon-on-Insulator (C-SOI) wafers for the 5G/6G wireless communication system. The proposed SSC platform features an extremely smooth suspended membrane with adjustable thickness, flexible cavity shapes with high density, self-formed acoustic wave confinement steps, stable temperature coefficient of frequency (TCF), and highly integrated compatibility with complementary metal-oxide semiconductor (CMOS). A surface smoothing method based on wet oxidation for SSC wafers is presented, which achieves a root mean square (RMS) roughness on the cavity surface of 1.5 nm for the first time. Based on the presented SSC platform, an $Al_{0.75}Sc_{0.25}N$ sealed cavity bulk acoustic wave resonator (S-BAR) is designed, fabricated, and characterized. The experimental results show that the asymmetric second-order (A2) Lamb mode of S-BAR is enhanced for higher frequency with a maximum piezoelectric coupling coefficient (k_t^2) of 9.53%, a maximum quality factor (Q) of 439, and a TCF of −11.44 ppm/K. Different designs' piezoelectric coupling coefficient distribution is consistent with the theoretical prediction. The proposed smoothing process increases the S-BARs' quality factor by ~400%. The frequency shift caused by the temperature (absolute value of TCF) is reduced by 62% compared with the traditional $Al_{0.75}Sc_{0.25}N$ thin film bulk acoustic wave resonator (without temperature compensation). The enhanced performances demonstrated the potential of SSC in the next-generation highly integrated RF communication systems.

Introduction

Microacoustic devices are a class of micrometer/nanometer-scale electroacoustic components designed to generate, sense, control, or utilize acoustic waves. With the combination of piezoelectric materials and micro-electro-mechanical systems (MEMS) technology, microacoustic devices have been widely developed, including acousto-optic modulator[1–3], quantum acoustic microsystem[4–6], piezoelectric micromachined ultrasound transducer (PMUT)[7–9], radio frequency (RF) acoustic resonators[10–12], etc. In terms of PMUT[13], monolithic integration can achieve the highest density of transducers and a wider variety of array geometries. Moreover, an integrated solution is ideal for minimizing system size and reducing power consumption for wearable or implantable microacoustic devices, such as intravascular ultrasound imaging systems[14]. Beyond them, RF communication (5G/6G) is the biggest market for microacoustic devices, and next-generation wireless communication systems require higher integration density. Considering the over 80 microacoustic resonators/filters integrated inside the latest mobile phone, integrated electroacoustic modules not only reduce the board footprint but also significantly reduce the parasitic effects introduced by the wiring and components[15]. However, the existing microacoustic platforms present significant challenges to support the subsequent fabrication process for on-chip integration due to the special structure or process for microacoustic devices.

Most microacoustic devices require suspended structures on the substrate (e.g., silicon) to support the free out-of-plane vibration. To date, two wafer-level platforms and one process have been developed to achieve suspended structures in microacoustic systems: the silicon-on-insulator (SOI) wafer platform, the cavity silicon-on-insulator (C-SOI) wafer platform, and the sacrificial layer process. As is shown in Fig. 1a, the SOI wafer features

Correspondence: Yansong Yang (eeyyang@ust.hk)
[1]Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, China

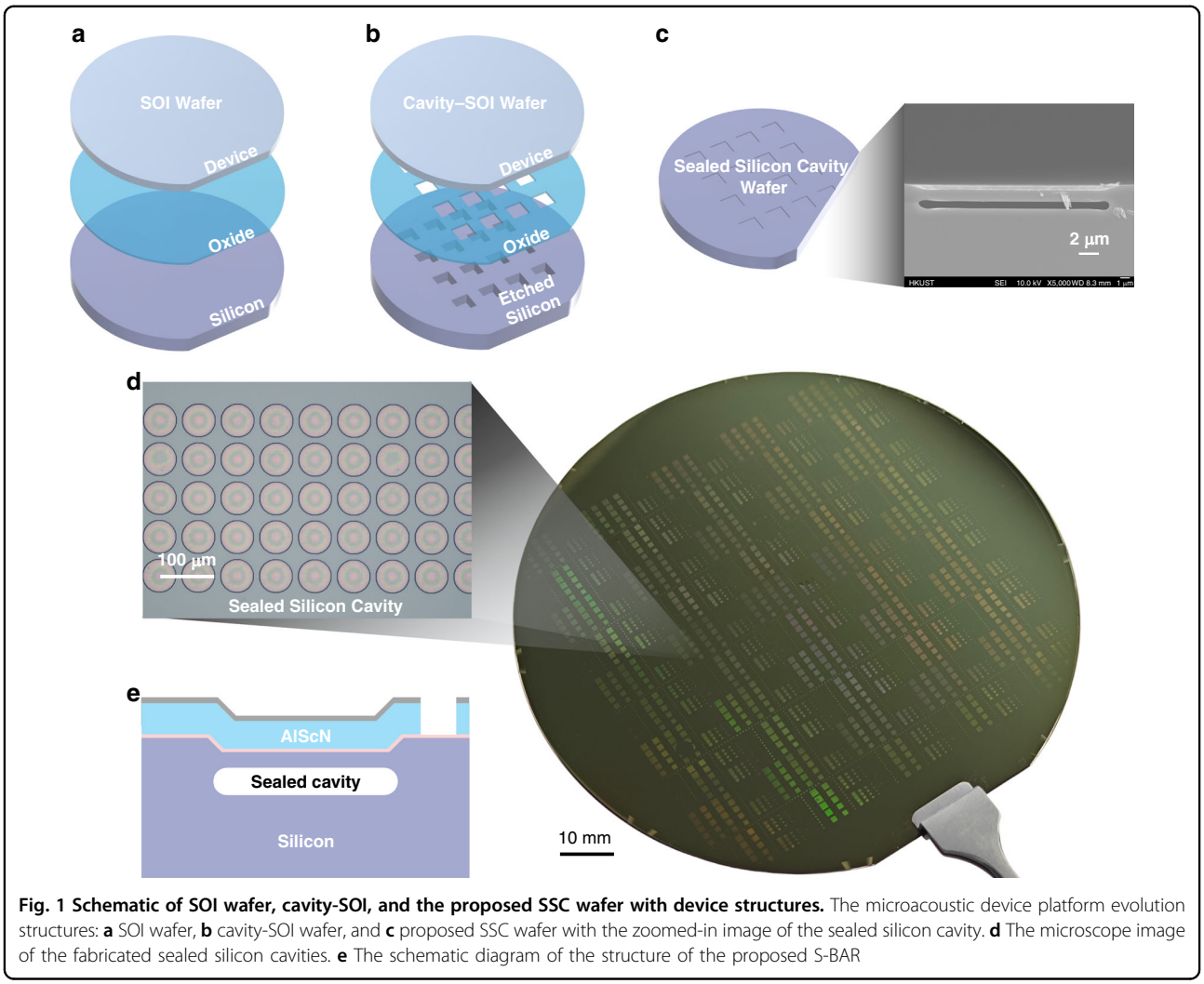

Fig. 1 Schematic of SOI wafer, cavity-SOI, and the proposed SSC wafer with device structures. The microacoustic device platform evolution structures: **a** SOI wafer, **b** cavity-SOI wafer, and **c** proposed SSC wafer with the zoomed-in image of the sealed silicon cavity. **d** The microscope image of the fabricated sealed silicon cavities. **e** The schematic diagram of the structure of the proposed S-BAR

three layers: silicon handle substrate, oxide layer, and silicon device layer. The SOI wafer platform, combined with the back etching process, can be used for the carrier substrate of thin film bulk acoustic resonator (FBAR)[16]. The back etching process selectively removes the silicon substrate to create a hollowed-out region and form the suspended structure. The process has the drawback of weakening the wafer, requiring additional support material[17]. Additionally, the aspect ratio constraints of backside etching necessitate a larger effective area for each device, thereby reducing the number of devices obtainable per wafer. In contrast to backside etching, the releasing process is another approach for suspended mechanical acoustic structures on SOI wafers by front etching. The construction of the suspended structure is achieved by isotropic dry etching of the substrate through release windows[18]. The disadvantage of this approach is that the etching boundaries of the release area cannot be accurately defined. Most importantly, this approach leads to incompatibility issues (between the etchant and device material) and hinders further microfabrication. C-SOI technology was invented to overcome the shortcomings of the SOI platform for microacoustic devices[19]. As illustrated in Fig. 1b, the C-SOI wafer integration platform features pre-etched cavities within the handle silicon. This approach mitigates potential damage to other components from the final etch. The advent of PMUT based on C-SOI wafers has led to a breakthrough in ultrasonic fingerprint recognition technology[8]. Nevertheless, this process requires wafers to have high uniformity for the uniform operating frequency of the microacoustic device, which leads to a high manufacturing cost. If C-SOI is used for high-frequency RF acoustic resonators, a substrate removal process is still required to ensure effective electromechanical coupling. The sacrificial layer process is the third mainstream process for MEMS microacoustic devices. The sacrificial layer is created before device fabrication and is removed after device fabrication to achieve device suspension[20,21]. This method requires a complex multilayer manufacturing process and needs to add a

sealing layer[13] for etching holes to support the subsequent fabrication processes. In summary, there are currently very few wafer-level platforms with low-cost, simple process, high-density suspended structure, and robust mechanical structure for microacoustic device integration.

In this work, we present a wafer-level sealed silicon cavity (SSC) microacoustic platform, as shown in Fig. 1c–e. The SSC wafer features a smooth suspended silicon membrane with controllable thickness, customizable cavity shapes with high density, self-forming acoustic wave confinement steps, and improved temperature coefficient of frequency (TCF) for acoustic resonators. The construction of the SSC is realized by DRIE and a rapid annealing process with low cost and simple steps. Furthermore, the SSC platform is sturdy enough to support both MEMS and CMOS fabrication/bonding/integration. Additionally, the SSC platform can excite higher-order Lamb waves with enhanced electromechanical coupling in the 5G/6G frequency bands. Different from the other annealing smoothing process[22,23], a wet oxidation-based surface smoothing process for the SSC wafer was proposed, achieving a root mean square (RMS) roughness of 1.5 nm on the cavity surface for the first time. The extremely flat cavity surface supports the subsequent high-quality material film deposition. Based on the presented SSC platform, we have designed, fabricated, and characterized C-band AlScN sealed cavity bulk acoustic wave resonators (S-BARs). The structure of S-BAR is shown in Fig. 1c. Compared with the conventional FBAR[24], the proposed S-BAR can improve both electromechanical coupling and TCF. The measured data show that the fabricated S-BARs achieve a maximum quality factor (Q) of 439, a peak piezoelectric coupling coefficient (k_t^2) of 9.53%, and a TCF of −11.44 ppm/K from 113 to 473 K for asymmetric second-order (A2) Lamb mode. The experimental results demonstrate that the proposed SSC platform could be a novel promising integrated microacoustic platform to replace C-SOI for ultrasound and microwave applications.

Results and discussion

Mode analysis and design of S-BAR

Figure 1 shows the structure of the designed S-BAR, which consists of an intrinsic (100) silicon substrate with a sealed cavity, bottom Pt electrode, middle piezoelectric $Al_{0.75}Sc_{0.25}N$ material, and top Al electrode, respectively. The membrane above the sealed cavity is crystalline silicon with a tunable thickness and smooth surface. The sealed cavity has a self-formed boundary with a length and height of ~1 μm and 600 nm, which can help suppress the lateral transmission of acoustic waves to reduce acoustic loss. Pt can provide low resistance as the bottom metal and has good lattice matching with $Al_{0.75}Sc_{0.25}N$. Al is chosen as the top metal due to its high conductivity. Different from the classical FBAR operating on the symmetric first-order (S1) Lamb mode[25], the proposed S-BAR can work on the asymmetric second-order (A2) mode[26] with k_t^2 enhancement. The simulated admittance response of S-BAR in Fig. 2a shows that the thickness ratios (α) of the piezoelectric $Al_{0.75}Sc_{0.25}N$ layer thickness to the total thickness can be used to generate A2 mode. When the α is close to 1, the S1 mode of the resonator has the largest k_t^2 ($k_t^2 = (f_p^2 - f_s^2)/f_p^2$) among all the resonant modes, where the f_s and f_p are the resonance and anti-resonance frequency, respectively. When the α is close to 0.3, the A2 mode of the resonator is fully excited, having the largest k_t^2. The principle behind it is that the silicon membrane participates in tuning the stress distribution of the resonator. The optimized stress distribution can increase the coupling piezoelectric mutual energy U_m for higher-order modes. Then the k_t^2 can be enhanced since the U_m is proportional to the k_t^2 [25]. The coupling piezoelectric mutual energy equation is an integral formula: $U_m = 1/4 \int_V (TdE + EdT)dV$, where the integral domain V is the volume of the piezoelectric $Al_{0.75}Sc_{0.25}N$ layer, T is the stress tensor, d is the piezoelectric (strain) coefficient matrix, and E is the electric field vector[25]. For S-BAR, neither d nor E is a function of the integral domain V and can be seen as constants, only T has a distribution along the z direction. The integral of stress T in $Al_{0.75}Sc_{0.25}N$ layer plays a crucial role of U_m. The simulated stress T distributions based on finite element analysis (FEA) of S-BAR at S1 and A2 modes with different α are illustrated in Fig. 2b. Ignoring the sudden change at the interface of the material stack, the stress distribution of S-BAR satisfies the sinusoidal form, with a period of $0.5n$, where n is the order of the resonant mode. When α is equal to 1, the distribution of half-period stress makes the U_m of the resonator working in the S1 mode reach the maximum value. At the same time, the distribution of one-period stress makes the U_m of the A2 mode almost 0. As α gradually decreases, the U_m of the S1 mode will become smaller due to the smaller integral domain in Fig. 2b, but the U_m of the A2 mode will increase and reach a peak at around $\alpha = 0.31$, and then decrease. When the α decreases, the stress zero point of A2 mode moves from the $Al_{0.75}Sc_{0.25}N$ layer to the interface between the $Al_{0.75}Sc_{0.25}N$ and silicon, which makes the integrated U_m increase and reach the maximum value, thus producing the maximum k_t^2. Figure 2c verifies this conclusion using eigenmode analysis. The A2 mode of $Al_{0.75}Sc_{0.25}N$ S-BAR can be excited and reaches the maximum simulated k_t^2 of 9.69% at $\alpha = 0.31$. Based on Fig. 2c, four S-BAR wafers with different α are fabricated in this work for demonstration.

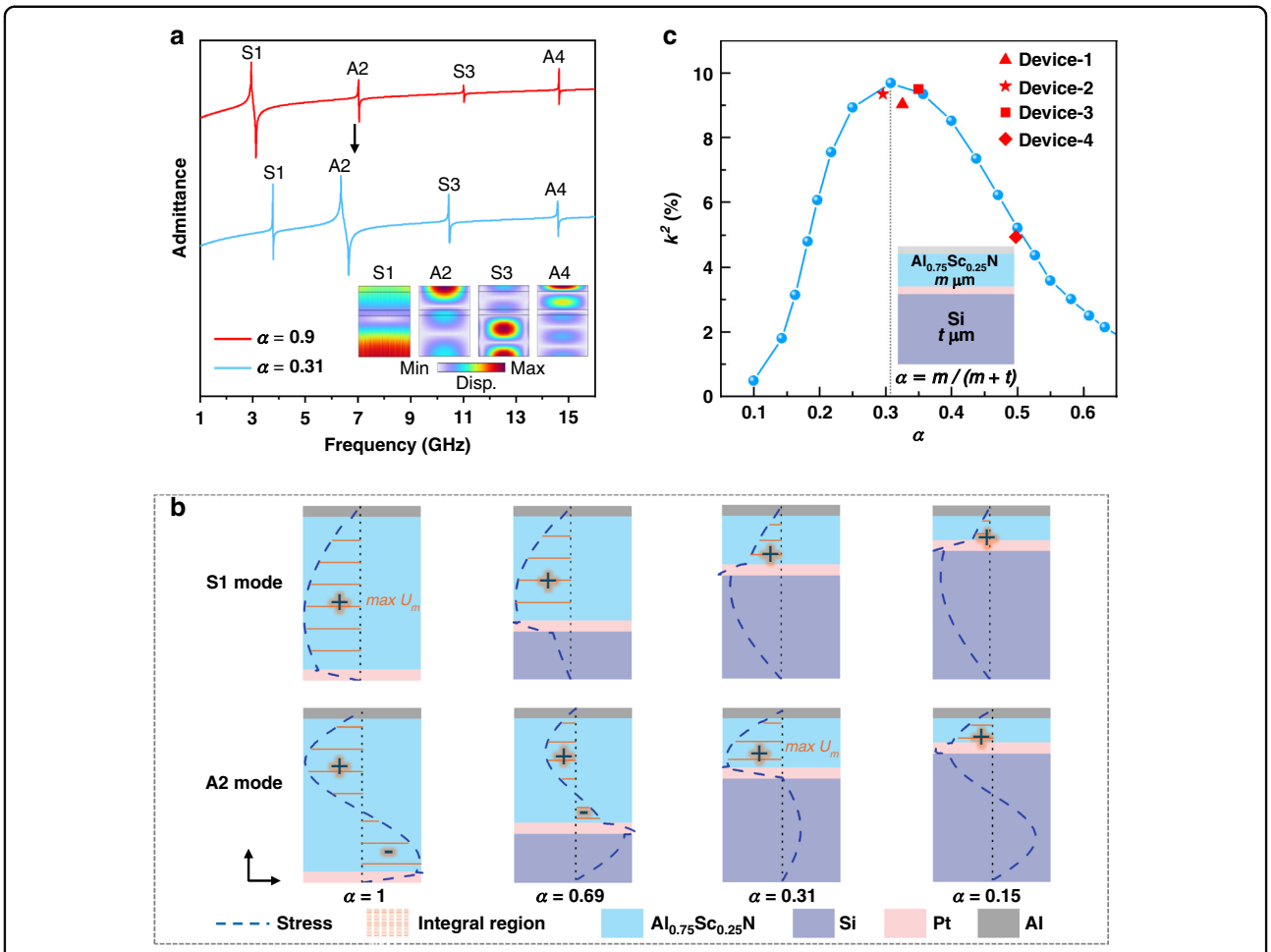

Fig. 2 Simulated resonance characteristics of S-BAR. a Admittance response of S-BAR with second-order mode enhancement. **b** Simulated stress distributions of S-BARs with different thickness ratios. **c** k_t^2 vs. thickness ratio of AlScN to the whole film

Fabrication process

The fabrication process flow chart is shown in Fig. 3. First, a 4-inch intrinsic (100) silicon wafer is photolithographically processed using an ASML PAS5000 Stepper. The photolithography pattern is a defined-boundary rectangular array of circular holes with a diameter of 600 nm and a spacing of 500 nm. Then, the wafer is etched by ICP-DRIE. The etching depth of a 600 nm-diameter hole is around 5 μm. The second step is the rapid annealing at 1150 °C for 100 s in Argon at one atmosphere (1 atm) of pressure. The hole array structure on the surface of the silicon wafer will gradually evolve into a sealed cavity with a suspended crystalline silicon membrane. The principle of sealed cavity formation is the surface diffusion of silicon atoms driven by surface tension. At high temperatures, surface atoms migrate in ways that reduce the local chemical potential[27,28]. Diffusion of silicon atoms occurs at around 1000 °C, without reaching its solid melting point[29]. The cavity's thickness and depth and the silicon membrane's thickness are determined by the diameter, spacing, and depth of the DRIE etched silicon holes. The equation of the membrane's profile is a fourth-order equation without an analytical solution[28]. It is also challenging to obtain numerical simulation solutions[30]. Our experimental results show that by keeping the etching depth of holes constant, the thickness of the silicon membrane is inversely proportional to the diameter of the holes and directly proportional to the spacing of the wells. An array of holes with a 500-nm diameter and 600-nm spacing will produce a 1.2-μm-thick silicon membrane with holes etched to a depth of 5 μm.

The third step is to achieve surface smoothing through wet oxidation and adjust the thickness of the silicon membrane to the designed value. As is shown in Fig. 4a, c, e, AFM measurement results show that the RMS roughness of the suspended membrane manufactured after annealing is 13.1 nm, and the RMS of the un-patterned region also reaches 3 nm. The rough surface is attributed to the diffusion length of adatoms being smaller than the spacing between adjacent discontinuous interfaces before

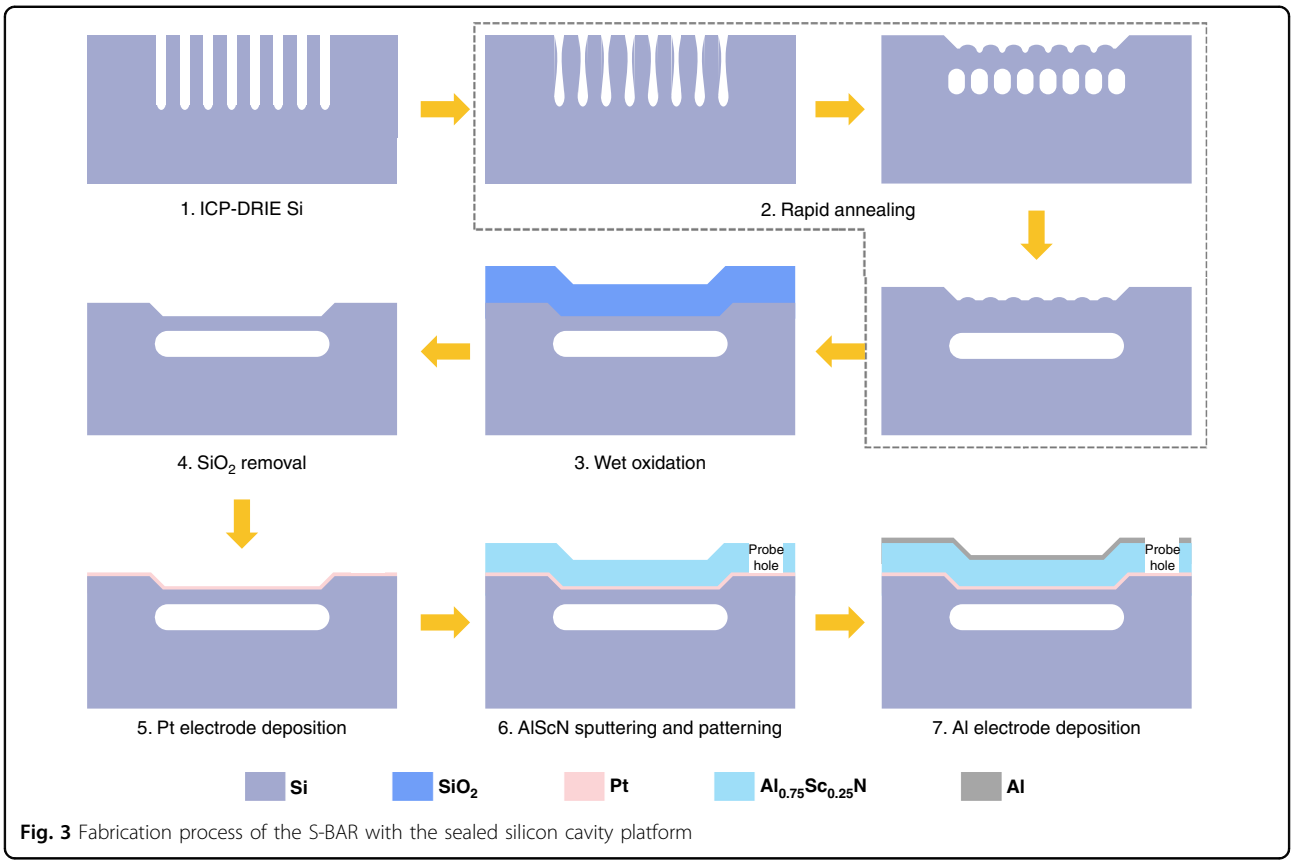

Fig. 3 Fabrication process of the S-BAR with the sealed silicon cavity platform

diffusion occurs, and the nucleation of vacancy islands will occur during the diffusion of silicon atoms[31]. To flatten the membrane on the SSC, additional annealing at 1020 °C in a vacuum chamber for 5630 min is investigated, but this process is very time-consuming[23]. Similarly, annealing at 1000 °C in hydrogen can also achieve a very flat silicon surface, but the smoothing is aimed at the trench structure rather than the SSC[22]. Surface unevenness significantly affects the quality of subsequently deposited metals and piezoelectric materials, thereby degrading device performance. To address this issue, this study proposed a novel wet oxidation method to smooth the surface of migrated Si film to an RMS roughness of 1.5 nm within two cycles (262 min). The oxidation furnace was set at 1050 °C and 1 atm of pressure. Due to the high temperature of the oxidation process, the diffusion rate of silicon atoms is high[29]. The migration of silicon atoms will eventually form a flat surface after a certain time. Moreover, this solution could kill two birds with one stone. As oxidation proceeds, silicon is consumed, and the thickness of the silicon membrane can be reduced for higher-frequency applications. The thickness ratio of consumed silicon and formed silicon dioxide is 0.44 to 1[32], and an oxide layer of 0.5 μm requires 131 min of oxidation time under experiments in our clean room. For example, a silicon membrane with an initial thickness of 1200 nm can be controlled to a thickness of about 1000 nm after a 131-min oxidation cycle (200 nm of silicon is oxidized). Therefore, the oxidation time can control the thickness of the remaining silicon membrane for different requirements. More details of the wet oxidation process of S-BAR can be found in the Supplementary Information. Figure 4b, d, e shows the AFM results of the same SSC wafer after wet oxidation and oxide removal. The RMS inside cavity area decreases from 13.1 to 1.5 nm, and the RMS outside cavity area decreases from 3.6 to 0.2 nm, respectively. This demonstrates the feasibility of the proposed wet oxidation surface smoothing method.

The wet oxidation process can also be used for regional thinning of the suspended silicon membrane. Based on the local oxidation of silicon (LOCOS) process, regional thinning can be realized by the patterned silicon nitride hard mask. Oxygen and water move very slowly in nitride. Therefore, when silicon nitride patterns are formed on silicon, the nitride film serves as an effective oxidation mask, preventing oxidants from reaching the silicon surface covered by the nitride. During the silicon oxidation, the thin layer on top of the nitride film is also converted to silicon dioxide. The thickness of the nitride mask should be greater than the thickness consumed in all oxidation cycles. At moderate pressures (1–8 atmospheres), the consumption rate of the nitride mask is about 4% of the

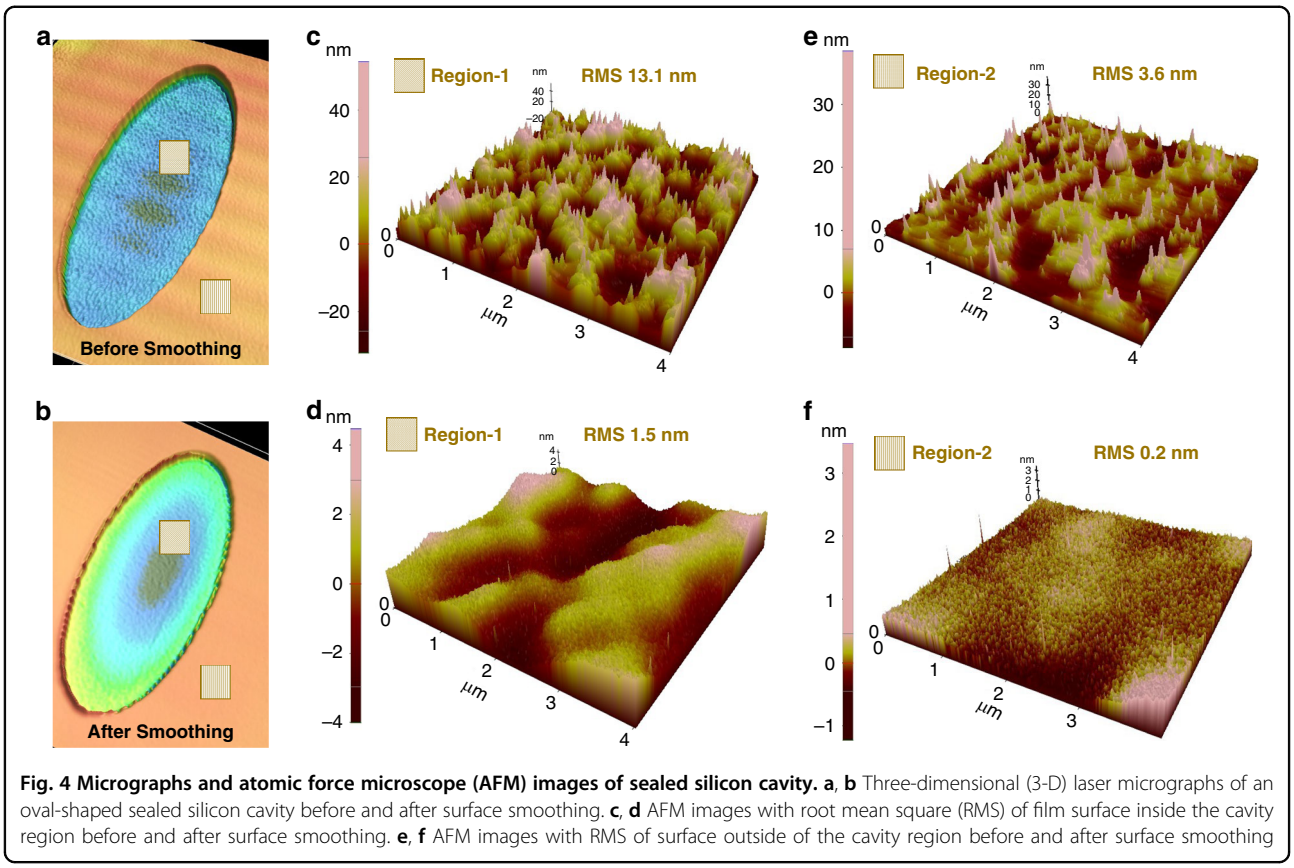

Fig. 4 Micrographs and atomic force microscope (AFM) images of sealed silicon cavity. a, **b** Three-dimensional (3-D) laser micrographs of an oval-shaped sealed silicon cavity before and after surface smoothing. **c**, **d** AFM images with root mean square (RMS) of film surface inside the cavity region before and after surface smoothing. **e**, **f** AFM images with RMS of surface outside of the cavity region before and after surface smoothing

silicon oxidation rate, so a thin nitride layer (<100 nm) is sufficient for masking[33]. Isotropic silicon oxidation causes a "Bird's Beak" phenomenon at the oxidation boundary. A smooth boundary can be formed from the non-oxidized area to the oxidized area, which is conducive to the adequate coverage of the metal electrode at the bottom of the S-BAR. The profile of this boundary can be controlled by the thickness of the nitride mask and the thickness of the generated silicon oxide[34].

Hence, different suspended silicon membrane thicknesses can be achieved on the same wafer. The process flow should be as follows: after forming the cavity and performing the oxidation smoothing treatment on the wafer, a patterned silicon nitride is used as a mask, then an oxidation treatment is performed, and finally, buffered oxide etchant (BOE) can be used to remove the oxide layer and nitride layer.

In step four, the oxide layer is removed by wet etching using BOE. Then, a Pt bottom electrode with a thickness of 77 nm is evaporated on the wafer, followed by the lift-off process. In step six, $Al_{0.75}Sc_{0.25}N$ is sputtered on the wafer. The probe holes are opened by etching $Al_{0.75}Sc_{0.25}N$ with 86% phosphoric acid at 80 °C. In the last step, an Al top electrode with a thickness of 100 nm is deposited on the wafer and patterned. Finally, four 4-inch wafers are fabricated, one of which is not smoothed (Wafer-1), two are smoothed one round (Wafer-2 and Wafer-3), and the remaining one is smoothed two rounds (Wafer-4). The suspended silicon membrane thicknesses of the four wafers are ~1200, 1000, 1000, and 900 nm, respectively. There are three purposes for processing these four wafers. Firstly, experimental data is needed to verify that S-BAR can control the piezoelectric coupling (k_t^2), as shown in Fig. 2c. Notably, the bandwidth of the acoustic filter increases with the increase of the k_t^2.[25] Secondly, it is necessary to experimentally evaluate the impact of the surface smoothing method on the performance of S-BAR, especially the quality factor (Q). The insertion loss of the acoustic filter decreases with the increase of the Q[25]. Finally, the performance of the designed S-BAR working in different frequency ranges needs to be explored. Different thickness designs correspond to different operating frequencies. Therefore, the research on the S-BAR of these four wafers is directly related to the frequency, bandwidth, and insertion loss of the S-BAR filter in practical RF wireless communication scenarios.

Figure 5 shows the scanning electron microscope (SEM) images of the fabricated wafer after different steps. The holes array is formed after ICP-DRIE with a freely defined

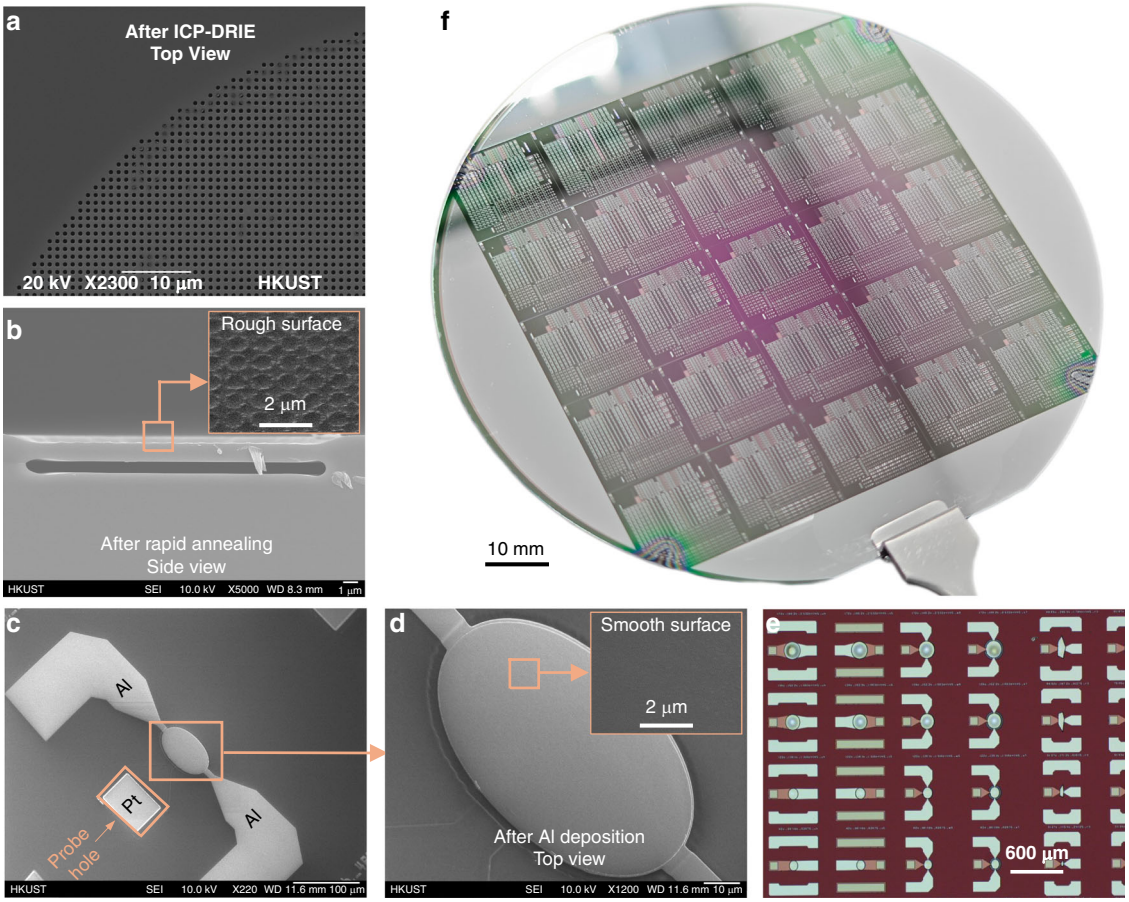

Fig. 5 Fabricated S-BAR device and corresponding four-inch wafer. a SEM image of DRIE holes before rapid annealing. **b** SEM image of cross-section view of sealed cavity after rapid annealing with rough surface. **c** SEM image of 45° top view of fabricated S-BAR. **d** zoomed-in image of the sealed cavity region of S-BAR with a smooth surface. **e** Die micrograph of the fabricated wafer. **f** A fabricated S-BAR wafer

boundary (e.g., ellipse, pentagon) shown in Fig. 5a. After rapid annealing, an around 0.8 µm-high sealed cavity with a 1.2 µm-thick suspended membrane is achieved shown in Fig. 5b. A 600 nm high and 1 µm wide step-like transition boundary is formed at the edge of the holes array. The top surface of the cavity is rough after annealing. The fabricated S-BAR device overview and zoomed-in image are shown in Fig. 5c, d. Benefiting from effective smoothing, a flat surface can be observed on the top of the device region. The die photo in Fig. 5e shows that the devices' cavity area has good uniformity and high yield. The shapes of the cavities can be freely defined and fabricated as any pattern (e.g., ellipse, polygon). Figure 5f shows a fabricated 4-inch wafer with a 5×5 array die distribution. Except for the dies at the four corners, the remaining 21 dies are available, which shows the stability of the fabrication.

Measurement results

The fabricated S-BARs are characterized by a vector network analyzer in dry air at room temperature. The measured admittance responses of Deveice-1 to Deveice-4 of the same layout (Fig. 5c) from four different wafers with their modified Butterworth-Van Dyke (MBVD) modeled fitting curves are shown in Fig. 6a–d. Wafer-1 has not been smoothed, and its silicon membrane thickness is around the initial 1200 nm. The target A2 mode of Device-1 fabricated on it has a k_t^2 of 9.02% at a resonance frequency of 4.23 GHz. Since its rough surface affects the quality of metal and $Al_{0.75}Sc_{0.25}N$, its 3-dB Q_S and Q_P are 81 and 61, respectively. Device-2 and -3 have the same silicon thickness but different $Al_{0.75}Sc_{0.25}N$ thicknesses (420 and 540 nm). Their measured admittance responses show the target A2 mode working at 5.15 and 4.48 GHz with k_t^2 of 9.35% and 9.53% respectively. After smoothing one round, the Q of Device-2 and Device-3 are larger than Device-1, reaching Q_S and Q_P of 106, 116, and 89, 110. Wafer-4 has been smoothed after two rounds. Device-4 on Wafer-4 achieves a Q_S of 363 at 3.81 GHz and a Q_P of 149 at 3.90 GHz. Due to design considerations, the thicker $Al_{0.75}Sc_{0.25}N$ makes its $\alpha = 0.51$, which brings a k_t^2 of

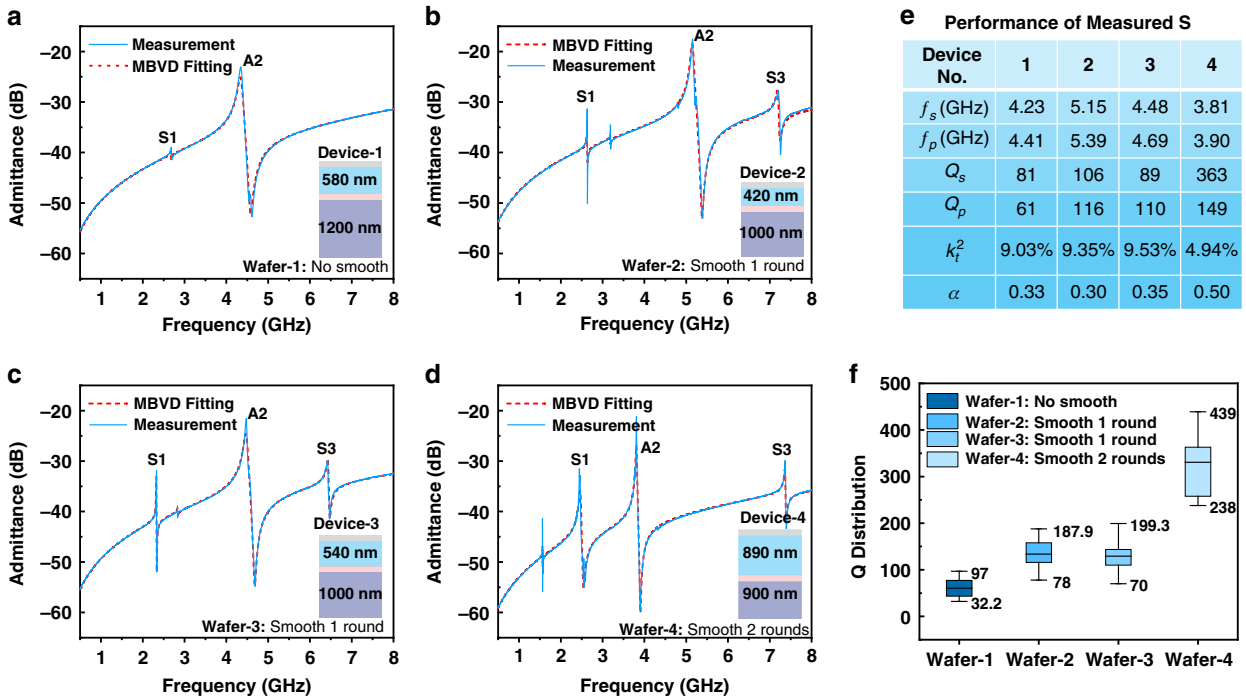

Fig. 6 Measured performance of the fabricated S-BAR devices. a–d Admittance responses from Device-1 to Device-4. **e** Performance summary of measured S-BARs. **f** Quality factor distribution of S-BARs on the four fabricated wafers

4.94%. The k_t^2 of four devices are plotted with a theoretically predicted curve in Fig. 2c. The theoretical design is consistent with the experimental results. The performance summary of measured S-BARs is shown in Fig. 6e. In addition, the measured admittance responses are also verified by simulation (in Figs. S3 and S4). Fig. S5 shows the MBVD fitting circuits of the four measured S-BARs with a table of critical parameters. Compared with the unsmoothed Wafer-1, the R_0 and R_S of Wafer-2 to Wafer-4 are smaller, which indicates that the deposited metal electrode on the smoothed wafers has better quality and sputtered $Al_{0.75}Sc_{0.25}N$ has smaller dielectric loss. This is beneficial to improving the Q of the fabricated S-BARs. In Fig. 6f, the Q distribution box plot of measured S-BARs on four wafers also demonstrates that the Q of the devices are increased by the smoothing process. After two rounds of smoothing, the measured maximum Q of S-BAR increased by around 400% (from 97 to 439). It is believed that the performance of S-BAR can be further improved by optimized thickness design (k_t^2) and smoothing process (Q) in the future.

The TCF of the S-BAR is measured in a vacuum cryogenic probe station shown in Fig. S5. As is shown in Fig. 7, the TCF of $Al_{0.75}Sc_{0.25}N$ S-BAR is −11.44 ppm/K from 113 to 473 K, which is much larger than the measured TCF (−30 ppm/K) of $Al_{0.75}Sc_{0.25}N$ FBAR[24]. The temperature compensation effect is attributed to the migrated

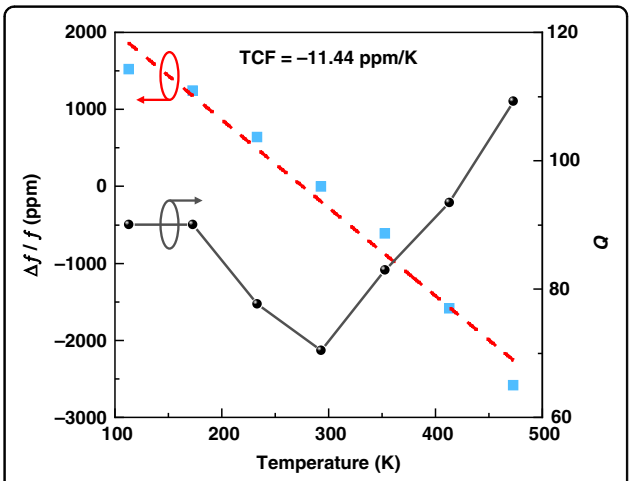

Fig. 7 TCF measurement of the fabricated S-BAR with Q-variation

silicon membrane, and its contribution to composite FBAR has been experimentally validated. $Al_{0.7}Sc_{0.3}N$/Si composite FBAR can achieve temperature compensation of TCF from −38.4 to −16.9 ppm/K[35], and the possible mechanism involves stress-induced temperature compensation. The stress compensation effect has been employed to achieve a TCF of +0.8 ppm/K for multilayer FBAR[36]. In this work, the silicon membrane beneath the $Al_{0.75}Sc_{0.25}N$ exhibits a tensile stress distribution

Table 1 Comparison with other published results

Reference	f_s (GHz)	Q_{max}	k_t^2	TCF (ppm/K)	Piezoelectric material	Process type	Subsequent fabrication compatibility
P3F* FBAR[38]	55.7	60	4.2%	–	AlN/AlScN/AlN	Releasing	No
P3F* FBAR[39]	20.02	166	8.5%	–	3-layer AlScN	Sacrificial Layer	No
P3F* XBAW[40]	10.72	789	10%	–	2-layer AlN	–	–
XBAW[41]	5.2	2136	6.26%	–	Crystalline AlN	Thin Film Transfer	–
FBAR[42]	2.596	1904	6.39%	–	Crystalline AlN	Thin Film Transfer	–
FBAR[24]	–	–	35%	−45	$Al_{0.59}Sc_{0.41}N$	–	–
FBAR[37]	4.3	318	14.5%	−19.2	$Al_{0.8}Sc_{0.2}N$	Sacrificial Layer	No
C-BAR[35]	2.47	536	9.57%	−16.9	$Al_{0.7}Sc_{0.3}N$	Backside Etching	No
FBAR[43]	2.2	600	26%	−45	$LiNbO_3$	Sacrificial Layer	No
This work S-BAR	3.81	363	4.94%	–	$Al_{0.75}Sc_{0.25}N$	Sealed Silicon Cavity	Yes
	4.48	110	9.53%	–			
	5.15	116	9.35%	−11.44			

*P3F** periodically polarized piezoelectric films

(in Fig. S6) prior to $Al_{0.75}Sc_{0.25}N$ sputtering, which contributes to the TCF of −11.44 ppm/K for S-BAR. Further details regarding this mechanism are provided in the Supplementary Information. The measured Q is enhanced by both increasing and decreasing temperature. This may be due to the lower dielectric losses at the low temperatures and lower mechanical losses contributed by high temperatures in the stacked structure.

Conclusion

In this work, we proposed a new microacoustic platform for highly integrated RF microacoustic devices with a smooth suspended sealed membrane, controllable membrane thickness, high-density freely definable cavity, self-formed acoustic wave confinement steps, enhanced coupling, and stable TCF. A S-BAR based on $Al_{0.75}Sc_{0.25}N$ is proposed and fabricated on this platform for demonstration. The k_t^2 of fabricated A2 mode S-BAR can be enhanced from 0 to over 9% by tuning the stress distribution. The presented wet oxidation smoothing method for SSC wafer can effectively help improve the Q of the presented S-BAR (increase by around 400%). The measurement results of S-BAR and other published works are compared in Table 1. With the SSC platform's help, the fabricated S-BAR's TCF is higher than the state-of-the-art FBAR's. However, the low Q value and spurious mode are the issues that need to be addressed. In addition to smoothing the suspended silicon membrane, wet oxidation can also be used to simultaneously thin the thickness of the silicon membrane. Nevertheless, the thickness of the silicon membrane needs to be adjusted to be thinner to cope with higher-frequency applications. Experimental results verify the feasibility, innovation, and advancement of the proposed S-BAR, which has the potential to replace the current FBAR filter for the high Table 1 Comparison with other published results ly integrated front-end module (FEM) of the 5G/6G RF communication system. Higher integration is the development trend of FEMs for wireless communication system. High-integration FEM requires devices to have precisely controllable boundaries. Compared with the existing sacrificial layer process for definable boudaries[37], the SSC platform has the advantage of low cost. The robust mechanical structure of the S-BAR with a sealed cavity can support the subsequent on-chip integration process, and has the advantage of low process complexity compared with the FEM integrated bonding process[15]. The SSC platform supports contact-type processes, which makes it less sensitive to the packaging process than the existing FBAR suspended film structure, which helps to further reduce packaging costs. In addition to S-BAR for FEM, the SSC platform is compatible with CMOS processes and can realize compact, integrated chips, such as wearable or implantable microacoustic sensors or actuators. In conclusion, this paper provides novel insights into the design and fabrication of an SSC microacoustic platform, which has great potential for development in ultrasound and microwave applications.

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Author contributions

J.X. carried out calculations, FEA simulation, fabrication, measurement, data analysis, wrote the paper, and made the modifications to the manuscript. Z.R.,

F.Q., and J.Z. participated in fabrication, characterization, as well as data analysis. Y.Y. conceived the idea, supervised the whole work, wrote the paper, and modified the manuscript. All authors read and approved the final manuscript.

Data availability
All data are fully available without restriction.

Conflict of interest
The authors declare no competing interests.

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