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Polarity control of 2D semiconductor for reconfigurable electronics

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Abstract

The controllable modulation of carrier polarity in semiconductors is essential for enabling dynamic configurations in reconfigurable devices. Ambipolar two-dimensional (2D) semiconductors, characterized by their atomic-scale thickness and excellent gate modulation efficiency, have emerged as highly promising channel materials for such devices. However, existing methods for polarity control encounter challenges in achieving reversible modulation during device operation. Here, we report a novel strategy for reversibly modulating the polarity of ambipolar 2D semiconductors through gate-controlled charge trapping. We demonstrate a double-gate $TaO_x/WSe_2/h$-BN field-effect transistor, which can reversibly switch between n-type and p-type transport characteristics via electric-field-driven bipolar charge trapping at the TaO_x/WSe_2 interface. With this method, an electrically configurable complementary inverter is created with a single WSe_2 flake, exhibiting a power consumption of just 0.7 nW. Additionally, a programmable p-n/n-p diode is realized with a > 100,000-fold change in the rectification ratio. These results demonstrate the great potential of gate-controlled bipolar charge trapping for advancing reconfigurable electronics.

Introduction

Reconfigurable electronic devices offer the technology with run-time reconfigurability at the device level, allowing electronic circuits to be programmed according to specific requirements and diverse functionalities[1,2]. Recent developments in such devices, including field-effect transistors (FETs)[3,4], gate-tunable p-n junctions[5], and photodetectors[6], have exhibited great potential to enhance circuit functions. Semiconductor polarity control serves as a pivotal technology for advancing these devices[7], where reversible polarity modulation enables the dynamic reconfiguration of circuit logic functions and operational modes[2]. Ambipolar two-dimensional (2D) semiconductors, such as molybdenum ditelluride ($MoTe_2$)[8,9], tungsten diselenide (WSe_2)[10,11], and black phosphorus (BP)[12,13], are particularly well-suited for such applications due to their exceptional gate-controlled capability to rapidly and reversibly switch carriers between holes and electrons[14].

To date, polarity control in ambipolar 2D semiconductors has primarily relied on two distinct strategies. The first strategy involves extrinsic doping techniques—including substitutional doping[15,16], chemical intercalation[17], and surface charge transfer[18,19]—which modulate semiconductor polarity through charge transfer between the dopants and the semiconductor material. However, these methods preclude reversible dynamic modulation after fabrication[20]. In contrast, the second strategy utilizes electric field gating[9,21,22] to achieve dopant-free reversible polarity control. This approach, however, requires a continuous power input to maintain field effects during operation, leading to ongoing power consumption that hinders the practical implementation of reconfigurable multifunctional devices[23].

Beyond the aforementioned polarity modulation approaches, recent studies have demonstrated defect engineering strategies for developing reconfigurable electronic devices. Two primary methodologies have emerged: gate-stack-integrated interfacial layers and environmentally responsive approaches. The former

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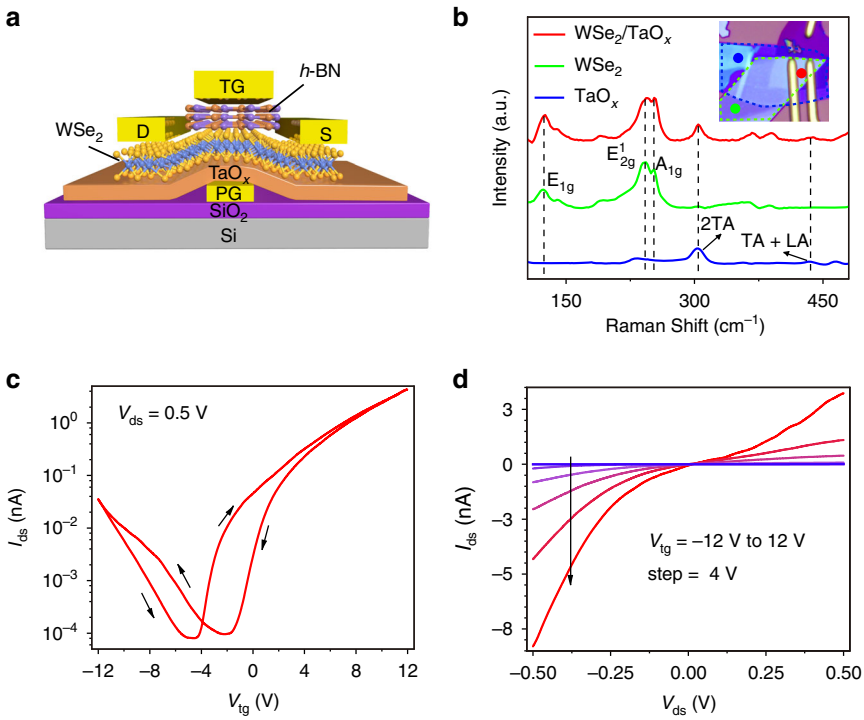

Fig. 1 Structure and electrical properties of the double-gate $TaO_x/WSe_2/h$-BN FET. a 3D schematic of the FET, where D, S, TG, and PG represent the drain, source, top gate, and programming gate electrodes, respectively. **b** Raman spectra of individual WSe_2, TaO_x, and their heterostructure region. The inset shows the Raman measurement regions, with blue, green, and red spots corresponding to the TaO_x, WSe_2, and WSe_2/TaO_x stacking regions, respectively. **c** Transfer characteristic at an applied bias voltage of 0.5 V, with arrows indicating the direction of the top gate voltage sweep. **d** Output characteristics under V_{tg} ranging from -12 V to 12 V with a step of 4 V

utilizes materials such as PbI_2[24], AlO_x[25], and $Bi_4Ti_3O_{12}$[26] in gate stacks, where an electric field-modulated charge trapping/detrapping mechanism at the channel-defect layer interface enables the reconfigurability of the devices. The latter employs either gas-phase exposure, leveraging defect-mediated O_2 adsorption and desorption on channel surfaces for reversible polarity switching, or photon-assisted interfacial charge trapping to achieve non-volatile device operation[27–29]. Crucially, the intrinsic material defects in crystalline structures and the controllable introduction of defects through processing demonstrate that defect engineering is a critical strategy for advancing reconfigurable electronics. The synergistic combination of inevitable crystalline imperfections and tunable defect engineering provides essential guidelines for semiconductor polarity control in reconfigurable electronic devices.

In this work, we demonstrate dynamically controllable polarity modulation of the double-gate $TaO_x/WSe_2/h$-BN FETs through the gate-controlled bipolar charge trapping at the TaO_x/WSe_2 interface. By manipulating the polarity of the gate voltage, electrons or holes in the WSe_2 channel can be selectively captured, resulting in electrostatic doping and polarity modulation of the channel. Using this method, we successfully constructed an electrically configurable complementary inverter within the same WSe_2 flake, representing a power consumption of only 0.7 nW. Additionally, programmable diodes were fabricated based on this strategy, exhibiting reversible transitions between p-n and n-p configurations with a rectification ratio change of over 10^5.

Results and discussion

The schematic structure of a double-gate $TaO_x/WSe_2/h$-BN FET is shown in Fig. 1a, consisting of a few-layer WSe_2 as the channel material, TaO_x as the interface layer, h-BN flake as the gate dielectric and Cr/Au as the gate electrodes and source/drain contacts (the detailed fabrication process is illustrated in Fig. S1). The TaO_x layer was obtained by oxidizing TaS_2 through UV exposure followed by a subsequent heating treatment (see Methods section). The UV treatment enables the rapid formation of oxide layers with nanometer-scale interface uniformity[30]. It can be observed from atomic force microscopy (AFM) characterizations that the surface roughness of the sample increases slightly with increasing duration of UV exposure while remaining at the nanometer level (Fig. S2a, b), demonstrating interface uniformity. At the same time, the

analysis of sample thickness with different oxidation durations indicates that oxidation reached self-limitation after 25–30 min of UV treatment (Fig. S2c). Thus, the subsequent thermal oxidation process effectively circumvents the intrinsic self-limiting oxidation kinetics of TaS_2, facilitating the complete conversion to amorphous TaO_x while preserving its structural integrity[31]. Furthermore, this approach simultaneously induces surface reconstruction to reduce roughness (Fig. S2d) and promotes defect formation through high thermal energy input[32].

The optical differences between TaO_x and TaS_2 are given in Fig. S3a, b. Due to the larger band gap, TaO_x exhibits greater transparency than TaS_2[33,34]. The Raman spectra depicted in Fig. S3c provide additional evidence for the oxidation of TaS_2 into TaO_x, as demonstrated by the observed shifts in the characteristic peaks[35,36]. Given that a volume decrease of approximately 25% would be expected if the TaS_2 was transformed into crystalline TaO_x, the observed thickness reduction of only ~2% (Fig. S3d-f) with unchanged lateral dimensions suggests that the TaO_x is a likely amorphous structure, exhibiting a significantly lower density compared to crystalline TaO_x[37,38]. It is this lower-density non-crystalline structure that enables atmospheric oxygen to penetrate deeply into the material, facilitating uniform and complete thermal oxidation throughout the sample. Raman characterization is also employed to identify the WSe_2, TaO_x, and heterostructure region (Fig. 1b). For TaO_x, the Raman peaks observed at 302 cm^{-1} and 435 cm^{-1} correspond to the 2TA and TA + LA modes, respectively, which arise from two-phonon scattering processes[35]. The Raman spectra of WSe_2 exhibit three distinct peaks at 137 cm^{-1}, 248 cm^{-1}, and 251 cm^{-1}, corresponding to the E_{1g}, E^1_{2g}, and A_{1g} vibrational modes of the WSe_2 flakes[39,40]. Notably, the Raman spectrum of the WSe_2/TaO_x heterostructure region contains all the characteristic peaks of both materials, confirming the successful stacking of the TaO_x and WSe_2 flakes.

Figure 1c, d show the electrical performance of this double-gate FET. The transfer characteristic in Fig. 1c shows a typical ambipolar behavior with an on/off ratio of approximately 10^5 for n-type transport and over 10^2 for p-type transport, indicating that n-type behavior dominates in the WSe_2 FET. The observed hysteresis between the forward and backward sweeps can mainly be attributed to charge trapping effects at the interface of TaO_x/WSe_2 or WSe_2/*h*-BN[41,42]. The output characteristics in Fig. 1d show a significant increase in current as the gate voltage rises, demonstrating the effective modulation of the double-gate FET by the gate electric field.

To investigate the hysteresis mechanism observed in the double-gate FET, we first compared the hysteresis width (ΔV) of FETs with and without the stacked TaO_x layer. The ΔV is extracted by calculating the voltage difference between forward and backward sweeps at a current level of 10^{-3} nA for the electron transport branch. As shown in Fig. S4, the transfer characteristics of the WSe_2 FET with TaO_x stacking exhibit more significant hysteresis, indicating that the hysteresis behavior is related to the TaO_x layer. Then, a comparison of the ΔV in double-gate FETs based on TaO_x prepared by different UV exposure durations (all followed by 300 °C/3 h thermal treatment) reveals a larger hysteresis in the 1.5 h device (7.90 V) versus the 5 min (1.68 V) and 30 min (6.72 V) devices (Fig. S5), once again proving that the hysteresis behavior of the device originates from the TaO_x layer. Therefore, we ascribe the hysteresis in our devices to the presence of TaO_x under the WSe_2 channel.

Additionally, transfer characteristics under varying top-gate voltage (V_{tg}) sweep ranges and rates are obtained to further research this mechanism, as illustrated in Fig. 2a, b. It can be found that the ΔV enlarges with the increase of gate voltage sweeping range or with the decrease of sweeping rate, as shown in Fig. 2c, d, respectively, suggesting that the hysteresis observed in our devices originates from charge trapping under the gate electric stress[42,43]. In particular, as shown in Fig. 2e, when $V_{tg} < 0$, the electric field at the WSe_2/TaO_x interface is oriented downward, which promotes the migration of holes from the WSe_2 channel to the TaO_x surface. These holes are subsequently trapped by defects, creating a positive electrostatic field that shifts the threshold voltage negatively for the forward sweep. Conversely, when $V_{tg} > 0$, electrons are driven and captured, resulting in a negative electrostatic field that causes a positive shift of the threshold voltage for the backward sweep. This bipolar charge trapping behavior, driven by the top-gate electric field, thus generates a clockwise hysteresis for the electron transport branch and a counterclockwise hysteresis for the hole transport branch. As the gate voltage sweeping range increases or the sweeping rate decreases, a greater number of carriers will migrate to and get trapped at the WSe_2/TaO_x interface, thus leading to an enlarged hysteresis.

Leveraging the established thickness dependence of WSe_2 carrier polarity[11], we explore the potential of this bipolar charge trapping in polarity modulation of double-gate FETs fabricated with p-type (~4 nm), ambipolar (~7 nm), and n-type (~10 nm) WSe_2 flakes (Figure S6), respectively. To investigate dynamic modulation effects, voltage pulses with different polarities are applied to the PG electrode. As shown in Fig. 3a, the conductivity type of the WSe_2 FET changes gradually from its initial n-type to a programmed p-type after being programmed by a positive voltage pulse ($V_{PG} > 0$). And a negative voltage pulse ($V_{PG} < 0$) can reverse this change. Conversely, the pristine p-type WSe_2 FET undergoes a transition to a programmed n-type under a negative program voltage

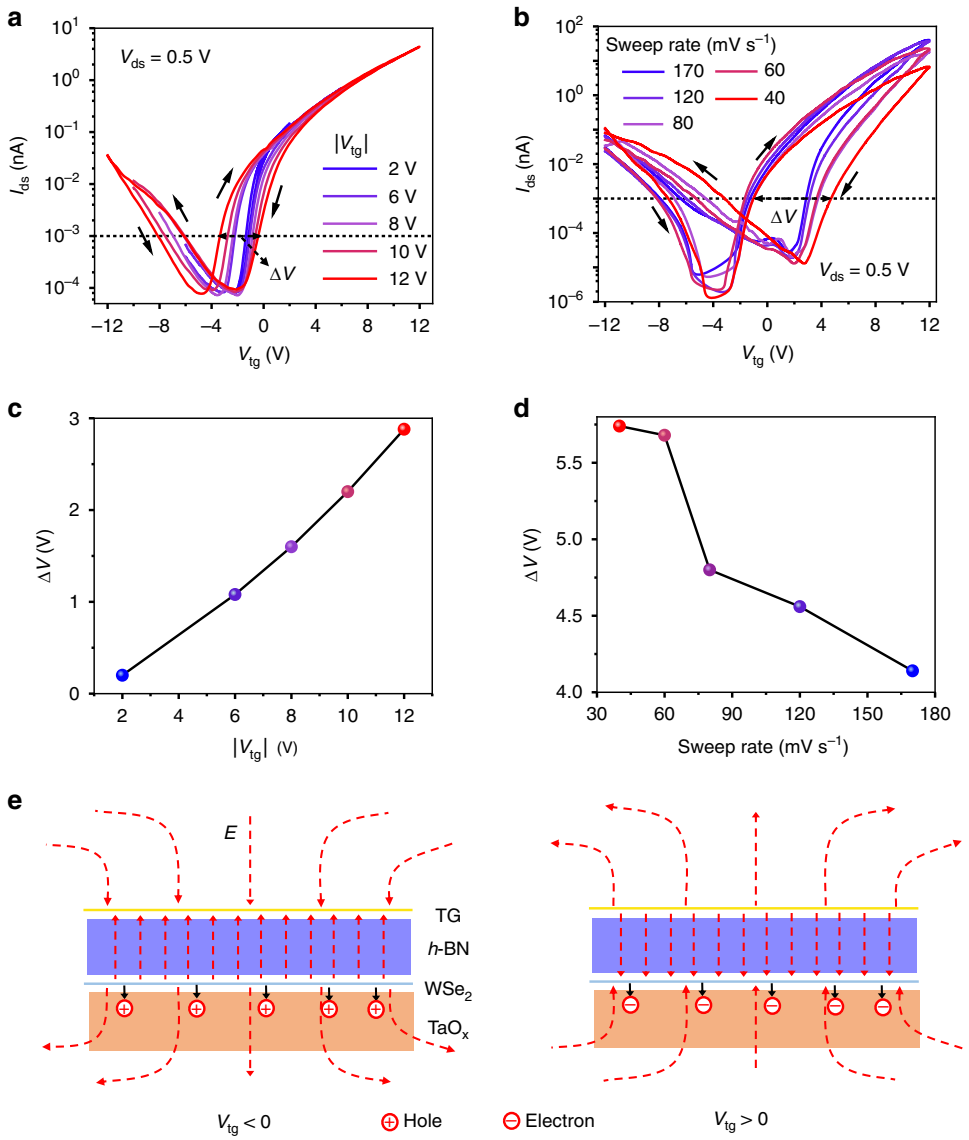

Fig. 2 Characteristics and principal mechanism of the hysteresis in the double-gate TaO_x/WSe_2/*h*-BN FET. Transfer characteristics at different V_{tg} **a** sweeping ranges and **b** sweeping rates. Variation of hysteresis at different V_{tg} **c** sweeping ranges **d** sweeping rates. **e** Principal mechanism underlying the hysteresis behavior. The solid arrows in **a** and **b** indicate the direction of the top-gate voltage sweep. Δ*V* and the dashed line represent the size and the current level of the hysteresis window, respectively. The dashed arrows in **e** show the direction of the top gate electric field

pulse, which can also be reversed by altering the pulse polarity, as shown in Fig. 3b. Furthermore, reversible changes between ambipolar and unipolar transport characteristics are also achieved in the WSe_2 FETs through the gate-controlled bipolar charge trapping (Fig. 3c, d). The detailed processes corresponding to Fig. 3a–d are provided in Fig. S7. This polarity control exhibits a retention time exceeding 10^3 s (Fig. S8). Meanwhile, prolonged pulse durations consistently enhance the efficacy of WSe_2 polarity modulation, indicating an effect similar to that observed when manipulating the amplitude of the pulse voltage (Fig. S9). These findings confirm the great advantage of gate-controlled bipolar charge trapping in realizing reversible polarity control for the ambipolar 2D semiconductor.

The detailed mechanism underlying the reversible polarity modulation of the double-gate TaO_x/WSe_2/*h*-BN FET is schematized in Fig. 3e. As discussed earlier regarding the hysteresis mechanism, when $V_{PG} > 0$, electrons, which are driven and captured at the TaO_x/WSe_2 interface by the gate electric field, induce electrostatic doping to accumulate holes in the WSe_2 channel, resulting in a programmed p-type polarity. Conversely, when $V_{PG} < 0$, holes are trapped to induce electron

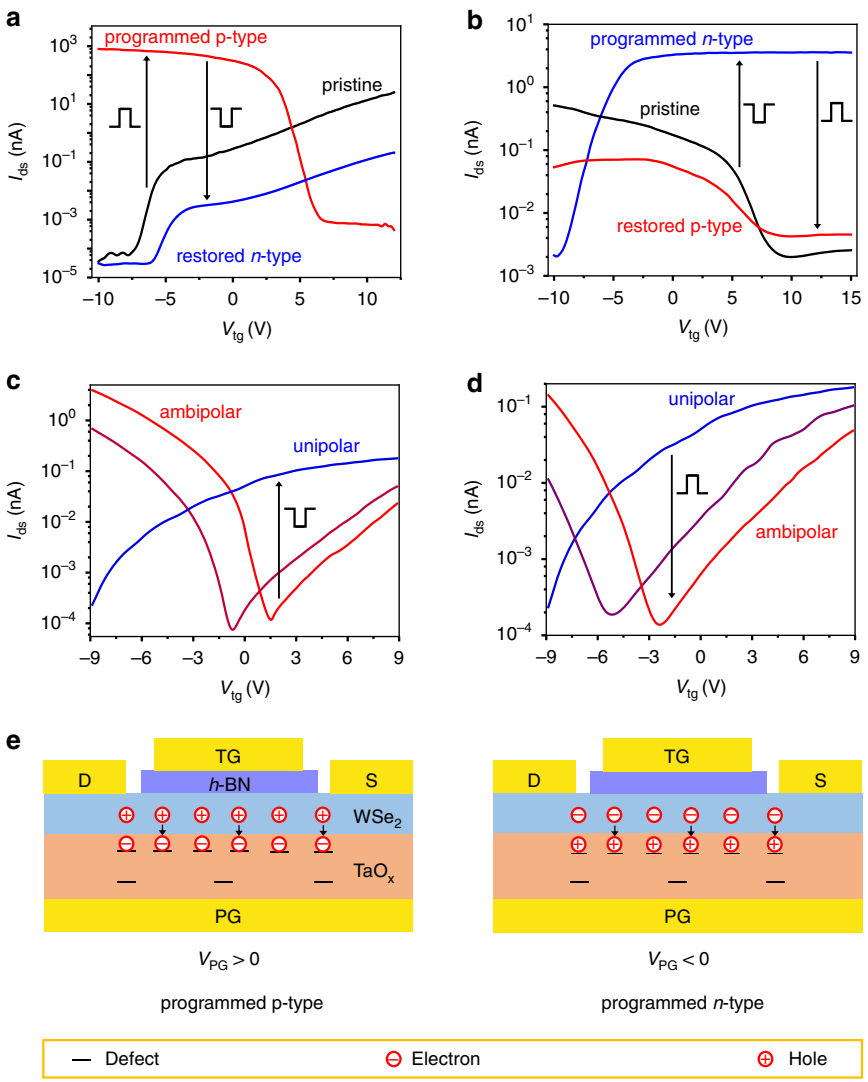

Fig. 3 Characteristics and schematic mechanism of reversible polarity control in the double-gate TaO_x/WSe_2/*h*-BN FET. a Reversible polarity modulation between the pristine n-type and the programmed p-type. **b** Reversible polarity modulation between the pristine p-type and the programmed n-type. **c-d** Reversible polarity modulation between ambipolar and unbipolar. **e** Formation mechanism of the programmed p-/n-type under different voltage pulses. All measurements in **a** and **b** were conducted at $V_{ds} = 0.5$ V. The positive and negative voltage pulses in **a** and **b** are (+2 V, -6 V) and (+7 V, -5 V), respectively. The voltage pulses in **c** and **d** are -7 V and +5 V, respectively. All voltage pulses are applied with a duration of 4 s

accumulation and thus form a programmed n-type polarity. Therefore, the polarity of such a double-gate WSe_2 FET can be reversibly modulated by gate-controlled bipolar charge trapping through altering the polarity of the PG voltage.

A complementary inverter was fabricated based on a single WSe_2 flake to investigate the feasibility of this polarity regulation method for reconfigurable devices. As illustrated in Fig. 4a, the complementary inverter consists of two WSe_2 transistors connected in series, with each transistor controlled by an independent PG (PG1 and PG2). Positive and negative voltage pulses are applied to PG1 and PG2, respectively, to establish a p-type and an n-type FET, as evidenced by their distinct transfer characteristics shown in Fig. 4b, c. Subsequently, the voltage transfer curves, plot of input (V_{in}) versus output voltage (V_{out}), of the complementary inverter under different supply voltages (V_{dd}) were measured, as shown in Fig. 4d. Signal inversions are observed with high V_{out} at negative V_{in} and low V_{out} at positive V_{in}, which further demonstrates that both p- and n-type FETs are successfully achieved through polarity modulation. Figure 4e presents the voltage gain of the programmable inverter, defined as $|dV_{out}/dV_{in}|$, with a maximum gain of 0.7. Notably, the complementary inverter exhibits a peak power consumption of 0.7 nW at $V_{dd} = 2.0$ V (Fig. 4f), indicating

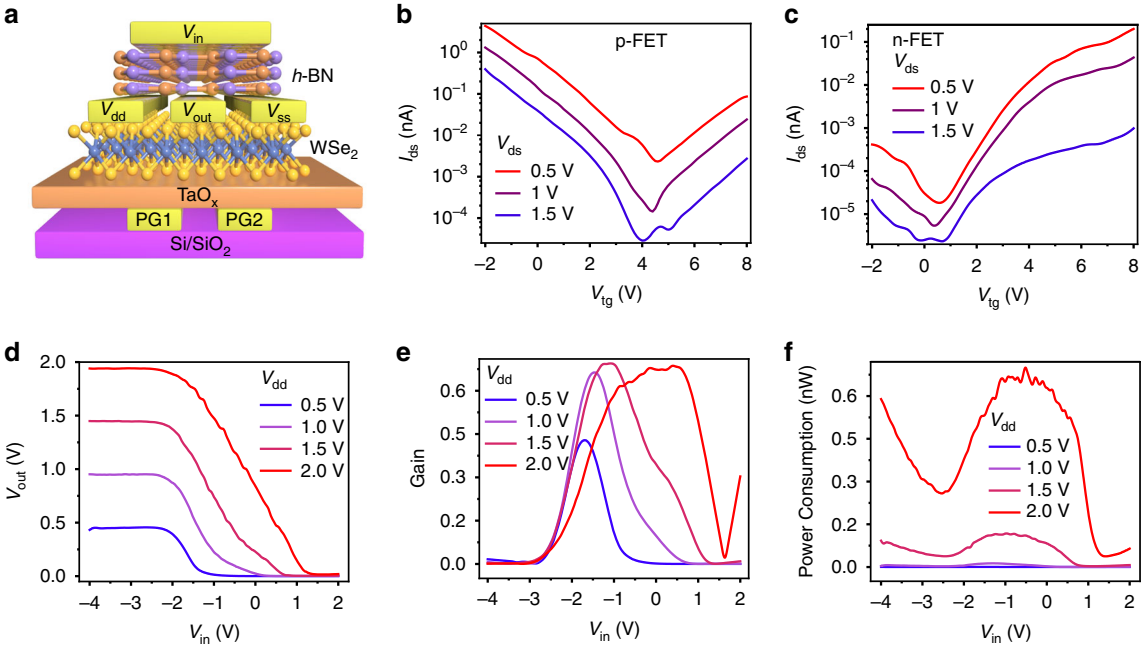

Fig. 4 Structure and electrical performance of the complementary inverter. a Schematic diagram of the complementary inverter. Transfer characteristics of **b** p-FET and **c** n-FET within the inverter. **d** Voltage transfer characteristics of the inverter at various V_{dd}. **e** Voltage gain of the inverter at various V_{dd}. **f** Power consumption of the inverter at various V_{dd}

that gate-controlled charge trapping is an effective strategy for constructing low-power logic devices.

To further explore the potential of this strategy in reconfigurable electronic devices, we created a programmable diode using a single WSe_2 flake. Figure 5a, b shows that the programmable diode has two PGs, PG1, and PG2, which are designed to simultaneously modulate the transport type of the WSe_2 channel by programming with opposite voltage pulses. Figure 5c shows that the transfer behavior gradually changes from p-n type to n-p type after being programmed by negative and positive voltage pulses applied to the PG1 and PG2 electrodes, respectively. This transition can be accurately quantified by the change of the current rectification ratio $|I_+/I_-|$, where I_+ and I_- represent the current values at bias voltages of +2 V and -2 V, respectively. As shown in Fig. 5d, the rectification ratio of the diode changes from 6672 to 0.06, indicating a transition from a p-n diode to an n-p diode after programming. Notably, the formed n-p diode can be reversed into the p-n mode with an over 10^5-fold change in rectification ratio by exchanging the polarity of the voltage pulses applied to PG1 and PG2 electrodes, as shown in Fig. 5e. These results demonstrate reversible conversions between p-n and n-p configurations of the WSe_2 channel and highlight the great potential of the gate-controlled charge trapping strategy in reconfigurable electronics.

Conclusion

A strategy for reversible polarity modulation in ambipolar 2D FETs via the gate-controlled bipolar charge trapping mechanism is proposed. By inserting a TaO_x layer into the gate stack of WSe_2 FET, the conductive characteristics can be reversibly switched between n-type and p-type behavior by controlling the polarity of the PG voltage pulses. Based on this strategy, an electrically configurable complementary inverter with a power consumption of 0.7 nW and a programmable diode with a 100,000-fold change in rectification ratio were successfully fabricated using a single WSe_2 flake, respectively. Our work demonstrates that gate-controlled bipolar charge trapping is a promising method for reconfigurable electronics.

Materials and methods

Fabrication of the double-gate TaO_x/WSe_2/h-BN FET

The WSe_2, TaS_2, and *h*-BN flakes were obtained by mechanical exfoliation from their bulk crystals. The thickness of p-type, ambipolar, and n-type WSe_2 flakes are ~4 nm, ~7 nm, and ~10 nm, respectively. The TaS_2 thickness was controlled in the range of 20–50 nm. The stacked TaS_2 flake and WSe_2/*h*-BN heterostructure were produced with a dry transfer technique, as reported. TaO_x was obtained from TaS_2 through 1.5 h of UV exposure and 3 hours of heating at 300 °C. All electrodes, including the PG (5 nm Cr/15 nm Au), the S/D (5 nm Cr/50 nm

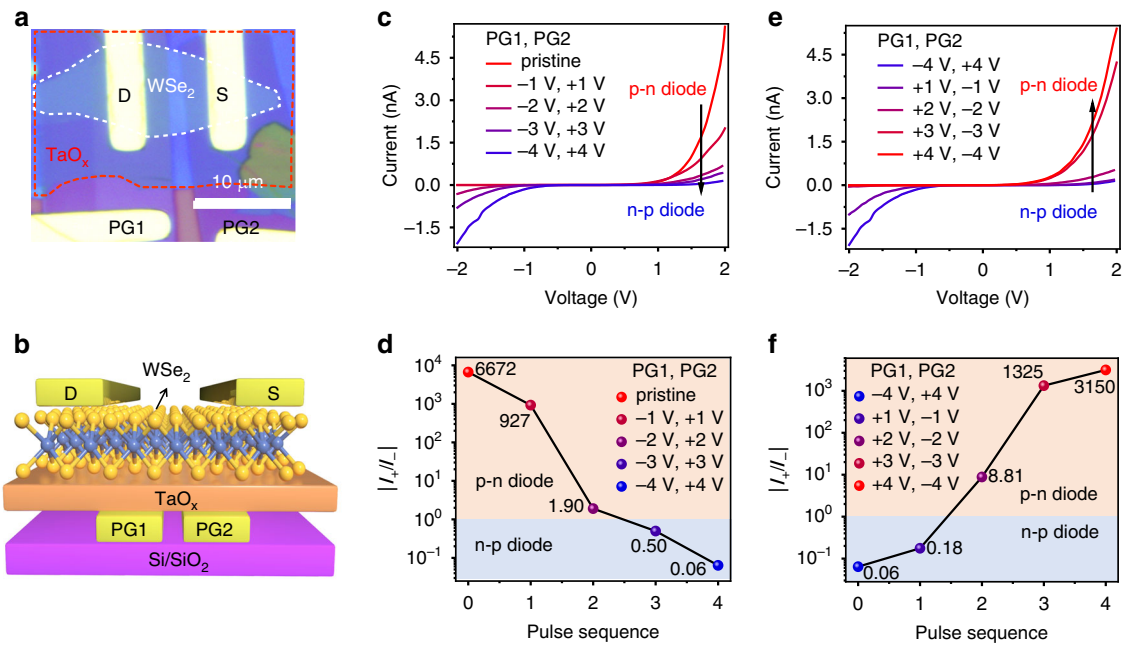

Fig. 5 Structure and electrical performance of the programmable diode. a Optical image and **b** schematic diagram of the programmable diode. **c** *I–V* characteristics of the diode changing from a p-n to an n-p junction after applying negative and positive pulses to PG1 and PG2, respectively. **d** Current rectification ratio $|I_+/I_-|$ for the diode shown in **c**. **e** *I–V* characteristics of the diode reversing from an n-p to a p-n junction after applying opposite pulses. **f** Current rectification ratio $|I_+/I_-|$ for the diode shown in **e**. All voltage pulses are applied with a duration of 8 s

Au), and the TG (5 nm Cr/70 nm Au), were defined using the MicroWriter ML 3 Pro system (Durham Magneto Optics) followed by metal thermal evaporation and lift-off process. A detailed schematic of the fabrication process for the double-gate TaO_x//WSe_2/*h*-BN FET is provided in Fig. S1.

Characterization and measurement of the double-gate TaO_x/WSe_2/h-BN FET

Raman spectra were acquired using an Invia Qontor instrument (Renishaw) with a 532 nm laser of 5 W power under ambient conditions. The measure setting parameters of samples are shown as follows: 1. accumulations: 50; 2. acquire time: 5 s; 3. grating: 1800 (532 nm); 4. ND filter: 10%; 5. Objective: 50x_LWD. The sample thicknesses were measured by atomic force microscopy (AFM, Oxford Instruments MFP-3D AFM) using an Otespa-R3 probe in tapping mode, with optimized parameters: 1. scan rate: 1.0 Hz; 2. samples/line: 256; 3. integral gain: 0.5; 4. proportional gain: 5.0; 5. drive frequency: 300 kHz; 6. amplitude setpoint: 120 mV; 7. drive amplitude: 120 mV. All electrical measurements were conducted in a vacuum probe station using a Keithley 4200A-SCS system.

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Conflict of interest

Ting Zhang is an Editor for the journal, no other author has reported any competing interest.

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