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Single-crystalline High-κ GdOCl dielectric for two-dimensional field-effect transistors

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Two-dimensional (2D) dielectrics, integrated with high-mobility semiconductors, show great promise to overcome the scaling limits in miniaturized integrated circuits. However, the 2D dielectrics explored to date still face the challenges of low crystallinity, diminished dielectric constant, and the lack of effective synthesis methods. Here, we report the controllable synthesis of ultra-thin gadolinium oxychloride (GdOCl) nanosheets via a chloride hydrate-assisted chemical vapor deposition (CVD) method. The resultant GdOCl nanosheets display good dielectric properties, including a high dielectric constant (high-κ) of 15.3, robust breakdown field strengths (E_{bd}) exceeding 9.9 MV/cm, and minimal gate leakage currents of approximately 10^{-6} A/cm^2. The top-gated GdOCl/MoS_2 field-effect transistors (FETs) exhibit commendable switch characteristics, a negligible hysteresis of ~5 mV and a subthreshold swing down to 67.9 mV dec^{-1}. The GdOCl/MoS_2 FETs can also be employed to construct functional logic gates. Our study underscores the significant potential of the 2D GdOCl dielectric for innovative high-speed operated nanoelectronic devices.

The miniaturization law of silicon-based electronics has motivated the development of modern logic electronics[1]. However, physical constraints have hindered advancements in sub-five-nanometer technology nodes due to challenges such as severe gate current leakage, high defect density at interfaces, and mobility degradation[2]. In next-generation nanoelectronics, dielectrics with an atomic thickness offer potential solutions to these issues. Current methods for atomic two-dimensional (2D) dielectric integration generally depend on atomic layer deposition (ALD), capable of depositing high-κ dielectrics with a thickness of sub-10 nm. But due to the inevitable pre-treatment process of ALD, the resulting 2D dielectrics are typically amorphous films with inferior interfacial properties, which reduces gate control and damages the surfaces of the channel material, thereby negatively impacting the intrinsic device performance[3–5]. The surface oxidation of semiconductor channel material into a dielectric layer can avoid the necessity for this pre-treatment. While the lack of native oxides compatible with semiconductors restricts the universality of this method. An emerging strategy involves integrating various crystalline 2D dielectrics through van der Waals forces. Crystalline 2D dielectrics, such as hexagonal boron nitride (*h*-BN)[6] and other van der Waals (vdW) dielectrics[7–9], are characterized by their atomically flat surfaces, facilitating the construction of high-quality semiconductor/dielectric interfaces. This significantly suppresses undesired charge scattering, thereby improving channel carrier mobility and diminishing device hysteresis[10,11]. Although *h*-BN can serve as a gate dielectric due to its optimal vdW interfaces, its broader application is still limited by low dielectric constant, unfavorable band offsets to most 2D semiconductors, and harsh synthesis conditions. Consequently, innovative crystalline 2D dielectrics with high-κ, large bandgap, ultra-clean vdW interfaces and easy synthesis method are highly desirable[6].

A series of 2D MOCl dielectrics, encompassing transition metal oxyhalides and rare-earth oxychlorides with either layered or non-layered structures, have garnered significant interest due to their superior dielectric properties. Notably, both CrOCl and VOCl exhibit high dielectric constants (>10)[9,12]. LaOCl, on the other hand, demonstrates wide band gaps (4.26 eV) and a high breakdown field strength

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(10 MV cm^{-1})[8]. Previous studies have underscored the pivotal role of MOCl dielectrics in enhancing the performance of 2D field-effect transistors (FETs), such as reconfiguring the carrier polarity in MoS_2[12], suppressing leakage currents[9], and reducing the subthreshold swing[8]. Despite the recent development of various general growth methods for MOCl[13,14], the unique dielectric properties of MOCl remain inadequately explored.

To date, the majority of crystalline 2D dielectrics have been synthesized using chemical vapor deposition (CVD) process. But traditional CVD process usually requires two or more types of precursors for growth[15–17]. The multi-source evaporation growth process demands strict control over several parameters, including deposition rates, temperatures, and duration of different gas phases[18]. As a result, the synthesis of these products often yields poor lateral compositional homogeneity and poor morphology, significantly reducing the interfacial properties of nanosheets and limiting their potential applications. Therefore, the synthesis methods of crystalline 2D dielectrics need to be improved and extended to grow high-quality products with uniform surfaces, which is crucial for enhancing the performance of 2D transistors and advancing the practical application of 2D-based integrated circuits.

Here, we report the successful synthesis of crystalline high-κ GdOCl dielectric using a chloride hydrate-assisted CVD method. The resultant GdOCl nanosheets display a variable thickness down to 5 nm and a large lateral size of 80 μm. These nanosheets possess a wide bandgap, a high out-of-plane dielectric constant of 15.3, and a minimal leakage current of 10^{-6} A/cm^2. Notably, these GdOCl nanosheets exhibit good air stability and remain unoxidized on the nanosheet surface over a period of 45 days. This indicates that GdOCl nanosheets could serve as effective dielectric materials, providing superior interfacial quality and device performance stability. Additionally, it is demonstrated that GdOCl nanosheets can function as gate dielectrics for MoS_2 field-effect transistors (FETs). Taking advantage of the high crystallinity, low surface defect density, and high-κ value of GdOCl nanosheets, the GdOCl dielectric offers robust gate coupling over charge carriers. This effectively mitigates Coulomb scattering in the MoS_2 FETs, significantly reducing the subthreshold swing down to 67.9 mV dec^{-1} and the hysteresis down to 5 mV, while also exhibiting a large on/off current ratio (10^6) and low gate leakage currents of 10^{-6}A/cm^2. It is important that ultra-clean van der Waals interfaces and band offsets exceeding 1 eV between GdOCl and MoS_2 play a crucial role in achieving superior performance in MoS_2 FETs. Remarkably, the highly effective gate control of GdOCl facilitates the construction of short-channel MoS_2 transistors. Furthermore, logic functions based on multiple GdOCl/MoS_2 FETs are implemented, including NOT, OR, and AND gates.

Results

Controlled growth and structural characterization of GdOCl

GdOCl is an insulating material with a matlockite-type structure, crystallizing in the tetragonal crystal system. From the side view of the GdOCl structure, the crystal structure consists of repeating hexatomic layers of Cl-Gd-O-Gd-Cl, wherein each Gd atom bonds with four O atoms and five Cl atoms, respectively, and each hexatomic layer has a thickness of 6.72 Å (Fig. 1a). From the top view, the structure appears as consisting of multiple [Gd_4O] tetrahedral units, with the Gd atoms

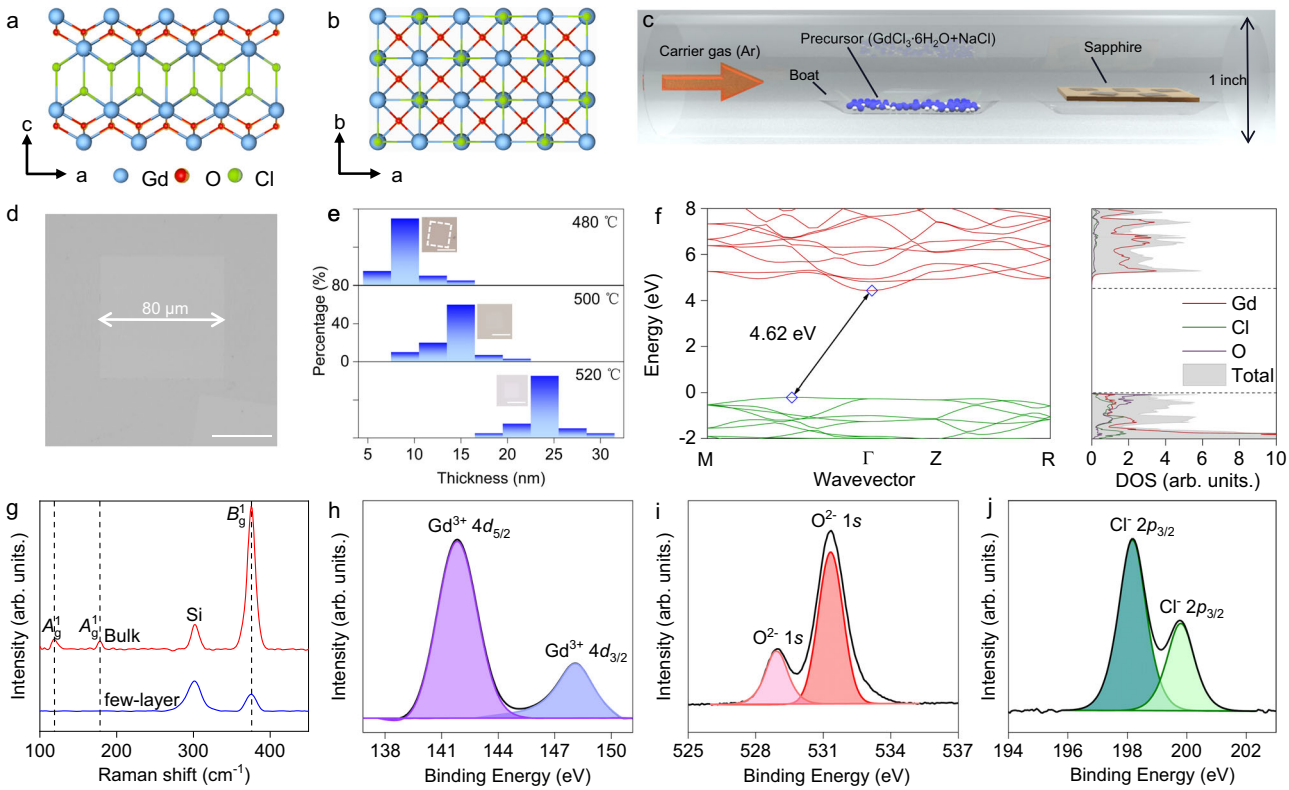

Fig. 1 | Synthesis and characterization of GdOCl nanosheets. a,**b** Side and Top views of GdOCl atomic structure, respectively. Blue, red and green spheres represent Gd, O and Cl atoms, respectively. **c** Schematic illustration of the synthesis process of GdOCl nanosheets. **d** Typical optical microscopy (OM) images of GdOCl nanosheets. Scale bars: 40 μm. **e** Corresponding thickness histogram distributions of GdOCl nanosheets obtained at different substrate temperatures of 480, 500, and 520 °C, respectively. Insets show the corresponding OM images. Scale bars: 10 μm. **f** Calculated electronic band structure and density of states (DOS) of GdOCl. The valence band maximum (VBM) and conduction band minimum (CBM) have been pointed out by the arrows and dashed lines, respectively. **g** Raman spectra of multilayer and bulk GaOCl nanosheets on SiO_2/Si substrate. The dashed lines represent the three Raman peaks at 118.7 cm^{-1}, 177.9 cm^{-1} and 375.3 cm^{-1}, respectively. **h**–**j**, Typical XPS patterns of Gd 4*d* (**h**), O 1*s* (**i**) and Cl 2*p* (**j**) orbitals.

forming the framework and the O atoms occupying the center (Fig. 1b). GdOCl nanosheets were synthesized using a custom CVD system, employing *c*-plane sapphire as the substrate, $GdCl_3{\cdot}6H_2O$ powders as the growth precursor, and NaCl as the catalyst (Fig. 1c). The reaction process is represented as: $GdCl_3{\cdot}6H_2O \rightarrow GdOCl + 2HCl + 5H_2O$[19]. Optical microscopy (OM) images confirm that the GdOCl nanosheets exhibit a rectangular shape, with maximum lateral sizes of 80 μm (Fig. 1d). Atomic force microscopy (AFM) corroborates the successful synthesis of a series of GdOCl nanosheets, varying in thickness from 5.2 nm to 35.2 nm (Supplementary Fig. 1). Additionally, AFM studies also show the remarkable air stability of GdOCl nanosheets, revealing no significant change in their morphology after 45 days of exposure to air (Supplementary Fig. 2).

The selection of $GdCl_3{\cdot}6H_2O$ powders as the precursor is crucial, which transform into homogeneous GdOCl powders through thermal dehydration at an optimal temperature. Upon reaching the evaporation temperature, the GdOCl powders are converted into a gaseous phase of GdOCl and subsequently transported to the downstream substrate for the growth of ultra-thin GdOCl nanosheets. The growth mechanism has been elucidated through X-ray diffraction (XRD) and Raman spectra of precursors at different growth temperatures (Supplementary Fig. 3). Different from the dual-source evaporation in conventional CVD method, which requires precise control of the mass ratio between the two precursors, the formation of a single-source GdOCl vapor during the pre-growth stage ensures a stable vapor supply. This approach is more conducive to achieving highly uniform nucleation and thickness-controlled growth. Furthermore, NaCl plays a pivotal role in the growth process: it (i) lowers the melting point and increases the vapor pressure of GdOCl[20], and (ii) acts as a passivation agent to inhibit growth along the [001] direction of GdOCl nanosheets, resulting in thin nanosheets[21,22]. The thermogravimetry and differential thermal analysis (TG-DTA) measurements have been conducted to verify the transformation of the precursor and the role of NaCl during the the synthesis process of GdOCl (More details in Supplementary Fig. 4).

Systematic growth studies have demonstrated the ability to grow GdOCl nanosheets of specific thickness and patterns. By varying the substrate temperature from 480 °C to 500 °C and 520 °C, it is observed that the average thickness of the resultant GdOCl nanosheets ranges from 5 nm to 15 nm and 30 nm, respectively (Fig. 1e and Supplementary Fig. 5). In general, the growth process is governed by the competition between thermodynamic and kinetic effects. At elevated temperatures, the thermodynamic effect becomes predominant, resulting in thicker nanosheets with reduced surface energy. In contrast, at lower temperatures, the kinetic effect takes precedence, causing precursor atoms to continuously diffuse towards the swiftest growth front at the nanosheet edge. This diffusion accelerates lateral growth and promotes thin nanosheet formation. Such low-temperature growth conditions are favorable for the formation of vdW heterojunctions. As demonstrated in Supplementary Fig. 6, vertically stacked GdOCl/WSe_2 heterostructures were successfully synthesized at a substrate temperature 520 °C. In addition, by adjusting the flow rates from 60 sccm to 100 sccm, the growth mode of GdOCl transitions from in-plane to out-of-plane growth, and the corresponding scanning electron microscope (SEM) images are shown in Supplementary Fig. 7. This shift in growth mode correlates with changes in precursor vapor pressure. At higher flow rate, more precursors are delivered to the substrate and reach supersaturation, thus favoring out-of-plane GdOCl nanosheet growth due to its lower nucleation barrier compared to in-plane growth[7,23,24].

The band structure of GdOCl was examined using density functional theory (DFT) calculations. As depicted in Fig. 1f, GdOCl possesses a wide indirect band gap of ~4.62 eV, with a valence band maximum (VBM) located between the M and Γ points, and a conduction band minimum (CBM) located at the Γ point. The CBM and VBM are mainly dominated by the Gd atoms and the O atoms, respectively. The absorption spectra (from 225 to 500 nm) were characterized to inspect the optical feature of the GdOCl nanosheet, and the value of the GdOCl bandgap extracted using the absorption spectrum and Tauc formula is 4.58 eV, which is consistent with the theoretical value of 4.62 eV (Supplementary Fig. 8). To study the chemical structure and crystallinity of GdOCl, Raman spectroscopy and XRD measurements were conducted. Raman spectroscopy of bulk GdOCl identifies three peaks at 118.7 cm^{-1}, 177.9 cm^{-1} and 375.3 cm^{-1}, which correspond to phonon with A_g^1, A_g^1 and B_g^1 modes, respectively, consistent with previous experimental Raman results (Fig. 1g)[25]. Notably, the peaks at 118.7 cm^{-1} and 177.9 cm^{-1} are associated with Gd-Cl bond vibrations, whereas the peak at 375.3 cm^{-1} is related to Gd-O bond vibrations[26]. However, as the thickness decreases, the two peaks at 118.7 cm^{-1} and 177.9 cm^{-1} become less pronounced, which can be attributed to the weaker intensities of A_g^1 modes in few-layer GdOCl nanosheets[27]. XRD analysis was performed directly on *c*-plane sapphire, revealing an XRD pattern indexed to the space group P4/nmm with lattice parameters of a = b = 3.9495 Å, c = 6.6708 Å (PDF no. 97-005-9232) (Supplementary Fig. 9). The three diffraction peaks align well with the (001), (002), and (003) planes, suggesting that the grown nanosheets exhibit high alignment with the [001] orientation parallel to the *c*-plane sapphire direction. Additionally, the chemical states within the GdOCl nanosheets were analyzed using X-ray photoelectron spectroscopy (XPS) (Fig. 1h–j). The binding energies of 141.83 and 148.17 eV confirm the presence of Gd^{3+} $4d_{5/2}$ and Gd^{3+} $4d_{3/2}$, respectively. The O 1*s* binding energies of 528.93 and 531.32 eV are assigned to O^{2-}, while the Cl $2p_{3/2}$ binding energies of 198.17 and 199.80 eV are attributed to Cl^-.

To further investigate the microstructure and chemical composition of the synthesized GdOCl nanosheets, scanning transmission electron microscopy (STEM) was performed on the transferred nanosheets. Figure 2a displays the high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of a rectangular GdOCl nanosheet taken from the [001] direction at a large field, confirming a perfect atomic arrangement. The intensity of atom imaging in the HAADF image exhibits a positive correlation with the atomic number (Z). Therefore, the bright spots in this context represent Gd atoms, while the O and Cl atoms are not identifiable due to the significant difference in Z values between the Gd atom and these other atoms. To identify three distinct types of atoms within GdOCl nanosheets, the integrated differential phase contrast scanning transmission electron microscopy (iDPC-STEM) imaging technology is utilized. The intensity of the iDPC-STEM image is approximately linear related to the projected electrostatic potential of the nanosheet, allowing for the simultaneous imaging of both light and heavy atoms at an elevated resolution[28]. The iDPC image is shown in Fig. 2b, Gd and O atoms can be clearly distinguished, but the distinction between Cl atoms is not possible due to their overlapping with Gd atoms along the [001] orientation. The atomic arrangement in GdOCl nanosheets was further proved by matching the top view crystal model with the iDPC-STEM image. Meanwhile, the selected area electron diffraction (SAED) image shows a singular set of diffraction spots with fourfold symmetry, which underscores the high crystalline quality of the GdOCl nanosheets (Fig. 2c). Furthermore, the calculated lattice spacing of 2.8 Å and 4.0 Å aligns well with the (110) and (100) lattice planes, respectively, which is supported by the intensity line profile analysis (Fig. 2d, e). In addition, energy dispersive X-ray spectroscopy (EDS) elemental mapping confirms a uniform distribution of the Gd, O and Cl elements across the rectangular nanosheets (Fig. 2f–h). The EDS data reveals that the stoichiometric ratios of the elements Gd, O, and Cl in the nanosheets are approximately 1:1:1 (Fig. 2i).

Dielectric properties of GdOCl

To verify the feasibility of GdOCl nanosheets as gate dielectrics, metal-insulator-metal (MIM) devices were fabricated to characterize their

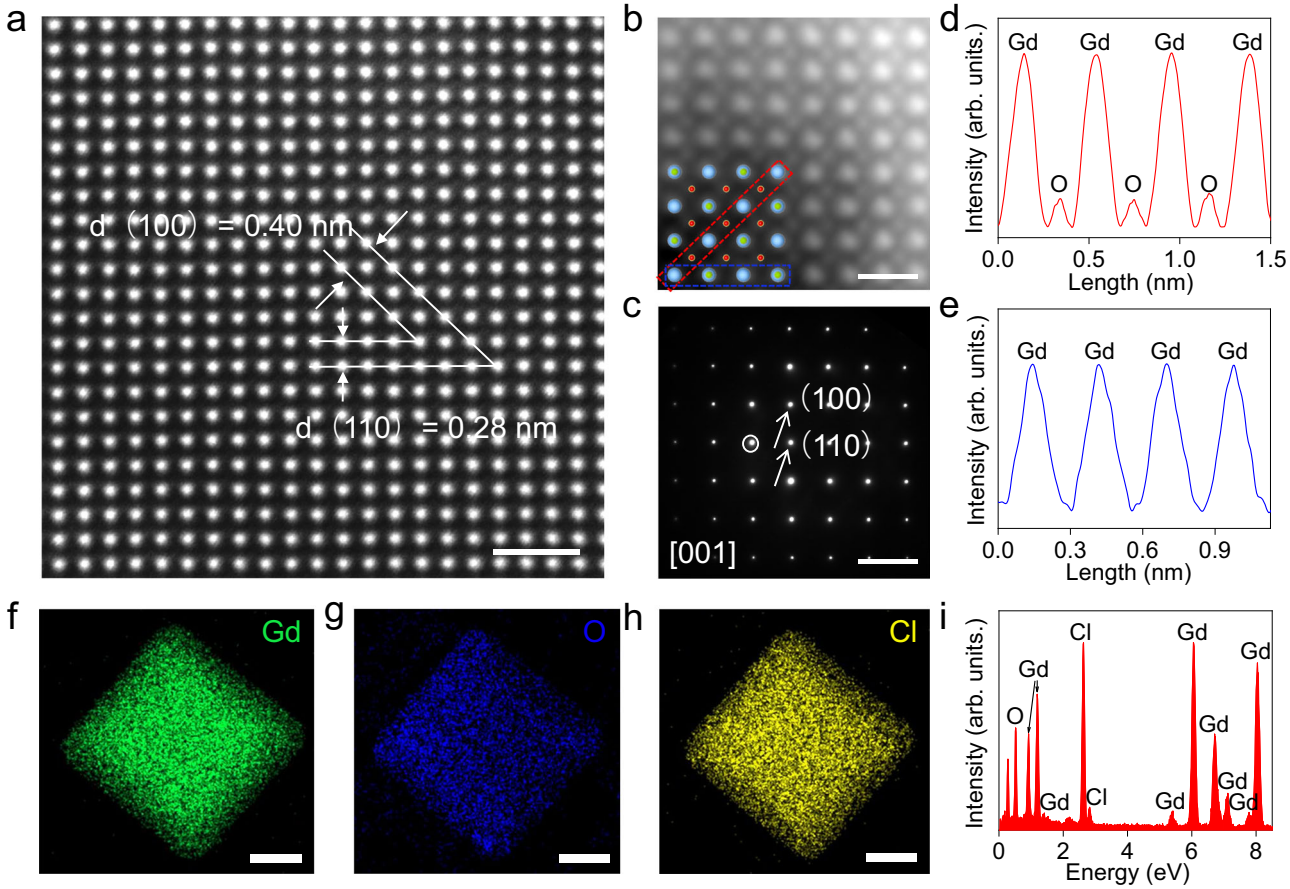

Fig. 2 | Atomic structure and chemical composition of GdOCl nanosheets. **a** High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of GdOCl nanosheet. d(100) and d(110) represent the lattice spacing of (100) and (110) planes, respectively. Scale bars: 1 nm. **b** Integrated differential phase contrast scanning transmission electron microscopy (iDPC-STEM) image of GdOCl nanosheet. Blue, red and green spheres represent Gd, O and Cl atoms, respectively. Scale bars: 0.5 nm. **c** Selected area electron diffraction (SAED) pattern of GdOCl nanosheet. Scale bars: 5 1/nm. **d**,**e** Intensity line profiles along the red (**d**) and blue (**e**) rectangles in panel (**c**). **f**–**h** The corresponding energy dispersive X-ray spectroscopy (EDS) mapping images of Gd (**f**), O (**g**) and Cl (**h**) elements. Scale bars: 3 μm. **i** The EDS elemental analysis of GdOCl nanosheet.

dielectric properties. As shown in Fig. 3a, these MIM devices were prepared on a glass substrate and the corresponding OM and AFM images of the MIM devices with different dielectric thicknesses are shown in Supplementary Fig. 10. Capacitance at varying thicknesses was assessed using capacitance-voltage (C–V) measurements at a frequency of 100 kHz (Fig. 3b). It is noteworthy that the capacitance is strongly dependent on the thickness of the nanosheets. Specifically, the GdOCl nanosheet with a thickness of 5.2 nm exhibits a high capacitance of 2.3 μF/cm^2, which diminishes when the thickness increases to 42.8 nm. Moreover, the capacitance of the GdOCl nanosheets shows negligible change across different frequencies (Supplementary Fig. 11). The effective dielectric constant can be calculated by the following equation: $\varepsilon_{eff} = \frac{Cd}{A\varepsilon_0}$, where C is the measured capacitance, d is the thickness of the GdOCl nanosheets, A is the effective capacitor area, and $\varepsilon_0 = 8.987551 \times 10^9$ N m^2 C^{-2} represents vacuum permittivity. Figure 3c illustrates the calculated ε_{eff} values for various thicknesses. Notably, ε_{eff} consistently exceeds 15.3 over a wide range of thicknesses, and remains largely invariant with respect to thickness, indicating that GdOCl serves as a high-κ dielectric. It is worth noting that the ε_{eff} of polycrystalline GdOCl powders was 28.7 which is higher than the out-of-plane ε_{eff} of GdOCl nanosheet (Supplementary Fig. 12). This may originate from the averaged crystal orientation of a polycrystalline powder in all crystal orientations[29].

Furthermore, the breakdown characteristic is also critical for a gate dielectric, particularly in terms of low leakage current and high breakdown strength, where the leakage current is a determining factor of the static power consumption of the FETs. Figure 3d displays the leakage current characteristics of GdOCl nanosheets with thicknesses of 5.2 nm, 9.6 nm, 13.9 nm, 27.1 nm, and 45.3 nm, respectively. All MIM devices show the leakage currents below 10^{-6}A/cm^2 before breakdown, a value four orders of magnitude lower than the low-power limit (10^{-2} A/cm^2) required by the International Technology Roadmap for Semiconductors (ITRS). In detail, Fig. 3e presents the breakdown field strength ($E_{bd} = \frac{V_{bd}}{t_{GdOCl}}$) and breakdown voltage (V_{bd}) as a function of thickness. These results for a specific thickness were obtained from measurements conducted on at least 10 individual MIM devices. It is found that V_{bd} increases linearly with thickness. The V_{bd} for GdOCl nanosheets with thicknesses of 5.2 nm, 10 nm, 15 nm, 20 nm, 25 nm, 30 nm, and 45 nm are 9.0 V, 16.0 V, 17.3 V, 22.5 V, 25.9 V, 29.5 V, and 44.6 V, respectively. The E_{bd} are consistently higher than 9.9 MV/cm across a broad range of thicknesses, peaking at an E_{bd} value of 17.1 MV cm^{-1} at a thickness of 5.2 nm. Furthermore, the E_{bd} exhibits an opposite decreasing trend as thickness increases, in agreement with the $E_{bd} \sim EOT^{-0.3}$ for high-κ materials (the theoretical fitting seen from the red dashed line in Fig. 3e). It is worth nothing that the E_{bd} of GdOCl significantly surpasses that of most previously reported 2D insulators at the same thickness[7–10,30–36]. To further validate the potential of GdOCl as a dielectric, the relationship between the breakdown field strength and corresponding dielectric constant of currently reported dielectrics was plotted in Fig. 3f[7–10,29,33,37–40]. Achieving both a high

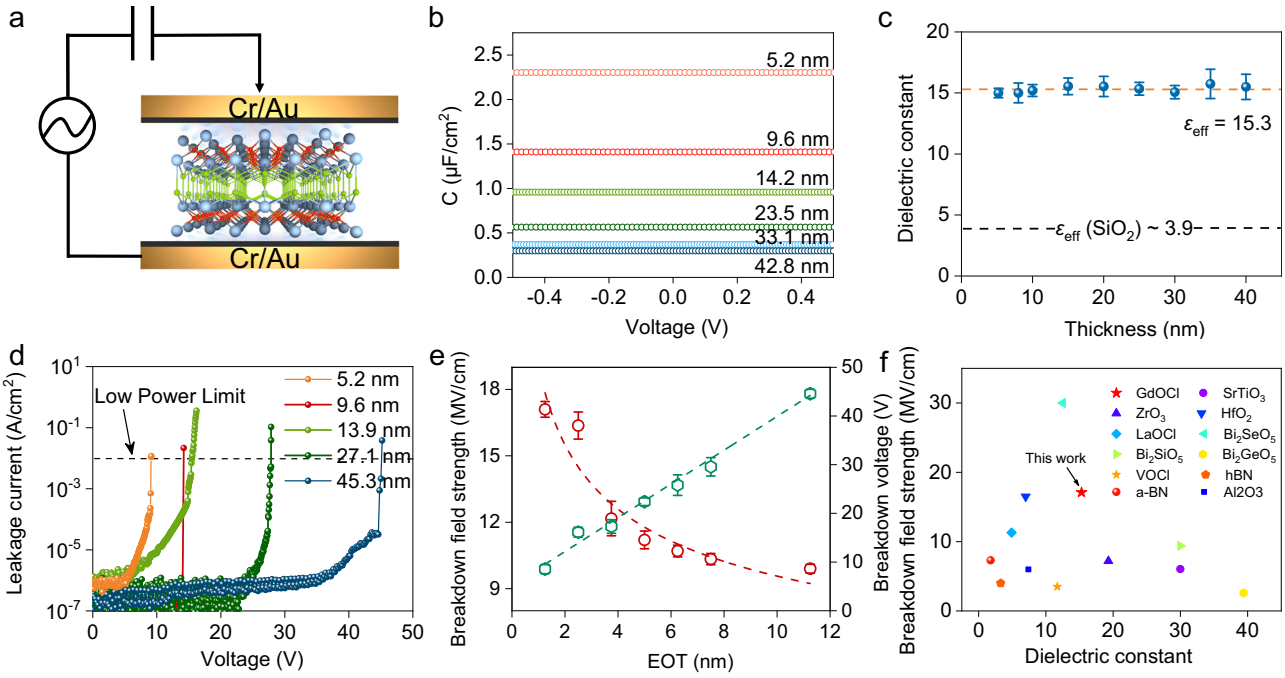

Fig. 3 | Dielectric properties of synthesized GdOCl nanosheets. a Schematic of a typical metal-insulator-metal (MIM) device. **b** Thickness-dependent C–V measurements of GdOCl nanosheets at measurement frequency of 100 kHz. **c** Thickness-dependent dielectric constant of GdOCl nanosheets. The horizontal dashed line represented the average value of the dielectric constant for different thicknesses. **d** Thickness-dependent leakage current *versus* applied voltage curves of GdOCl nanosheets measured by MIM devices. **e** The breakdown field strengths (E_{bd}) and breakdown voltage (V_{bd}) as a function of the various equivalent oxide thickness (EOT). **f** Comparison of E_{bd} and corresponding dielectric constant of the existing dielectric materials[7–10,29,33,37–40].

dielectric constant and robust breakdown field strength simultaneously remains a key challenge. However, GdOCl demonstrates E_{bd} values that are comparable to the widely used Al_2O_3 and HfO_2, and exceed most existing two-dimensional dielectrics. Besides, it possesses a relatively higher dielectric constant (as evidenced by ε_{eff} = 3.3 for *h*-BN, ε_{eff} = 7.3 for a-BN, ε_{eff} = 10.8 for LaOCl and ε_{eff} = 11.7 for VOCl). Notably, the EOT value of GdOCl is significantly smaller, approximately 1.3 nm, which corresponds to a thickness of 5.2 nm (Supplementary Table 1). Given these promising dielectric properties of GdOCl, it is expected to attract considerable interest in subsequent studies.

MoS_2 transistors with GdOCl top-gate dielectrics

To examine the potential of GdOCl as a dielectric in practical applications, a MoS_2 FET with GdOCl as the top-gate dielectric was fabricated. The device structure is shown schematically in Fig. 4a. The GdOCl/MoS_2 top-gate FET was fabricated on a SiO_2/Si substrate, utilizing Cr/Au as the source and drain electrodes to match the work function between Cr and MoS_2. The top-gate electrode covered the entire channel, thereby enabling effective modulation of the GdOCl top gate. The output characteristics of the GdOCl/MoS_2 FET (channel width/channel length, W_{CH}/L_{CH} = 2 μm/3 μm) are shown in Fig. 4b. The output curves show linear characteristics at low V_{ds}, indicating a good ohmic contact between the electrodes and MoS_2, and exhibit current saturation at high V_{ds}. Figure 4c illustrates the double-sweep transfer curves under varying V_{ds} from 0.1 to 2 V, where the MoS_2 FET exhibits a typical n-type behavior and low gate leakage currents (I_g) as low as 10^{-13} A (Supplementary Fig. 13). The GdOCl top gate effectively controls the FET, enabling it to be switched on and off within a narrow gate voltage (V_g) range of -1.5 ~ 1 V. Meanwhile, the high-quality GdOCl top gate significantly suppresses leakage current, resulting in a high I_{on}/I_{off} of 10^6, which is two orders of magnitude higher than the standards of practical logic circuits (10^4). Significantly, due to the ultra-thin thickness of the GdOCl top gate, the drain current (I_{ds}) already saturates at V_g = 1 V. It is also observed that all the double-sweep transfer curves at different V_{ds} exhibit negligible hysteresis (<5 mV), ensuring the operational stability of devices (The inset of Fig. 4c and Supplementary Fig. 14). Upon comparing the normalized hysteresis widths (Norm.$\Delta V_H = \frac{\Delta V_H}{E_g}$), it is found that the Norm. ΔV_H of GdOCl/MoS_2 FETs is 2.99, surpassing most of the previously reported 2D top-gate FETs (Fig. 4d)[7,30,32,40–43]. Within the steep rise region of transfer curve, the subthreshold swing (SS) can be extracted by the equation $SS = \frac{dV_g}{dlgI_{ds}}$, yielding an approximate SS value of 67.9 mV dec^{-1}. Such a small SS indicates that the MoS_2 FET can quickly switch between on and off states. This value is further confirmed by plotting the SS as a function of I_{ds} (Supplementary Fig. 15). Notably, the ideal SS and negligible hysteresis are attributed not only to the ultra-thin thickness of the GdOCl top gate, but also to the high-quality interface between the GdOCl and MoS_2. The interface trap density (D_{it}) can be calculated by equation: $SS = \ln(10)\frac{k_BT}{q}(1+\frac{qD_{it}}{C_{ox}})$, where SS represents the subthreshold swing, *T* represents the absolute temperature, k_B is the Boltzmann constant, C_{ox} is the dielectric capacitance, and *q* denotes the elementary charge. The obtained D_{it} displays a small value of 7.81×10^{11} cm^{-2} eV^{-1}. This high-quality interface is realized through dry transfer, greatly reducing the strain and effectively eliminating residual impurities typically found in traditional wet transfer processes (see Methods and Supplementary Fig. 16 for more details). To illustrate the scalability potential of GdOCl as a gate dielectric, GdOCl/MoS_2 top-gate FETs with varying dielectric thicknesses were fabricated. The corresponding OM and AFM images of the GdOCl/MoS_2 top-gate FETs with different dielectric thicknesses are shown in Supplementary Fig. 17. As shown in supplementary Fig. 18, a decrease in the thickness of GdOCl results in a gradual shift of V_{th} towards the positive gate voltage direction, and a slight increase in Ion due to the higher capacitance in thinner GdOCl. Notably, the MoS_2 FET with a 5.2 nm GdOCl (EOT ~ 1.3 nm) still maintains a high I_{on}/I_{off} ratio and an elevated on-state current. This suggests that GdOCl holds significant potential for development in the

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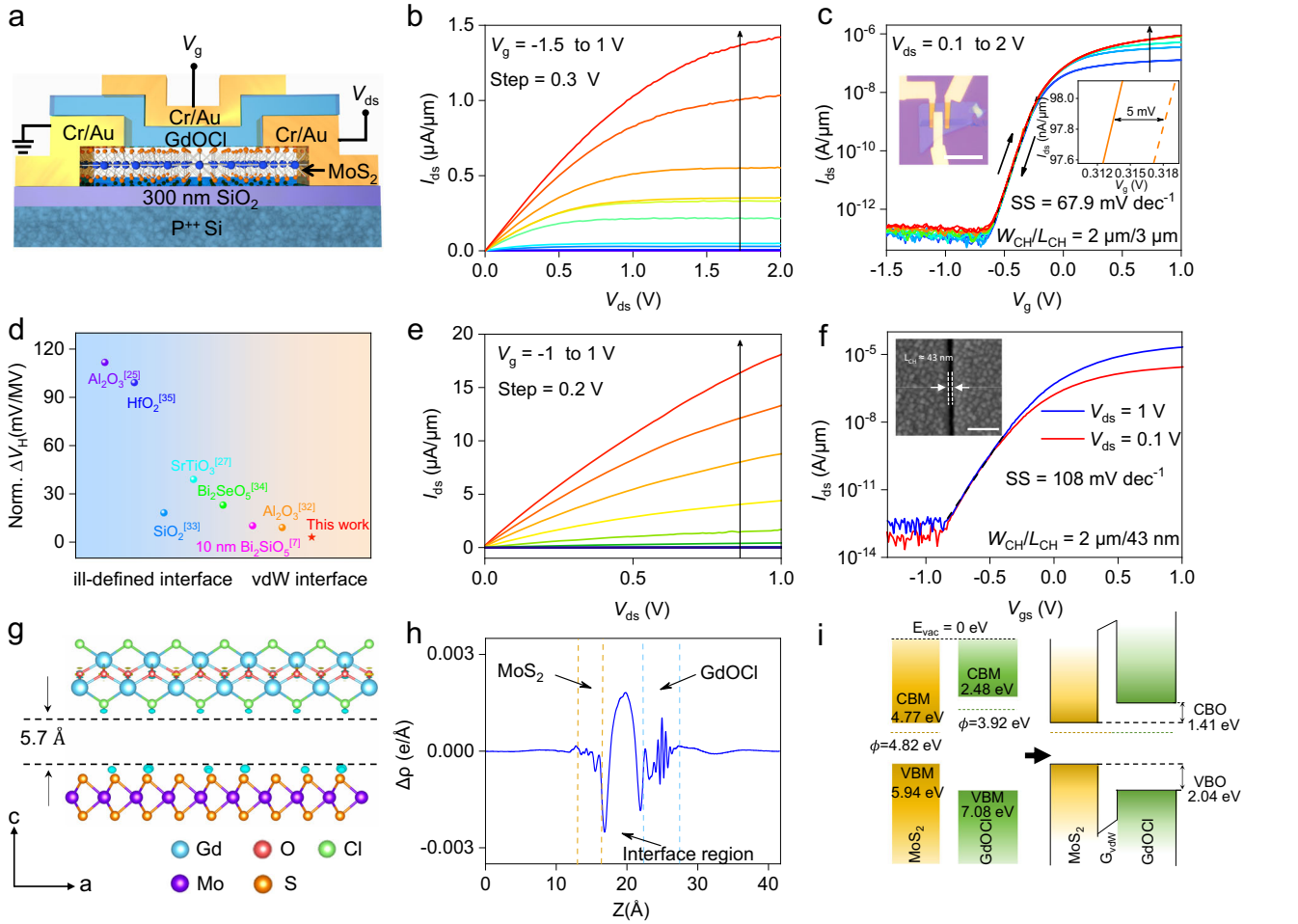

Fig. 4 | Electrical measurement of GdOCl/MoS_2 field-effect transistors (FETs). **a** Schematic of a top-gated MoS_2 FET with high-κ GdOCl dielectric. **b**,**c** The output curves (**b**) and double-sweep transfer curves (**c**) of a typical MoS_2 FET with 14.5 nm GdOCl top gate. Inset: OM image of GdOCl/MoS_2 FET; the negligible hysteresis at V_{ds} = 1.5 V. Scale bars: 10 μm. **d** Normalized hysteresis widths (Norm. ΔV_H) of the GdOCl/MoS_2 FET is plotted against other dielectric materials[7,25,27,32–35]. **e**,**f** The output curves (**e**) and transfer curves (**f**) of a 43 nm-channel GdOCl/MoS_2 FET. Inset: SEM image of the 43 nm-channel in GdOCl/MoS_2 FET. Scale bars: 300 nm. **g** Side views of the differential charge density of the GdOCl/MoS_2 vdW heterostructure. The blue and yellow isosurface contours represents electron depletion and electron accumulation, respectively. The isosurface value of charge difference is 0.00001 e/Bohr^3. **h** Plane-averaged differential charge density of the GdOCl/MoS_2 vdW heterostructure as a function of position along z direction. **i** Band diagrams and alignment of MoS_2 and GdOCl, estimated based on the results in Supplementary Fig. 20.

continuous scaling process of devices. Furthermore, with the shrink of the size of FETs, the reduction in channel size leads to a noticeable decrease in the drain-induced barrier. This inevitably results in the loss of electrostatic control over the gate, leading to a smaller the subthreshold current, a decrease in the I_{on}/I_{off}, and poorer SS values. To assess the effective gate control of GdOCl dielectric, short-channel MoS_2 FETs (L_{CH} ≈ 43 nm to L_{CH} ≈ 81 nm; Supplementary Fig. 19a) were fabricated. The output curves of 43 nm-channel MoS_2 FET show satisfactory current control (Fig. 4e). The transfer characteristics of the 43-nm GdOCl/MoS_2 back-gate FET (Fig. 4f) exhibit an I_{on}/I_{off} of >10^7, an SS value of 108 mV dec^{-1} and a low drain-induced barrier lowering (DIBL) value of ~196 mV/V. These performance metrics also evident in the 63 nm-channel and 81 nm-channel GdOCl/MoS_2 FETs (Supplementary Fig. 19b, d). All the results confirm the promising potential of GdOCl as a gate dielectric for 2D electronic applications.

Commercial amorphous metal oxide dielectrics previously reported have typically been integrated using ALD, a process that frequently results in involuntary chemical bonding at the dielectric/semiconductor interface. This interaction adversely affects the bandgap of semiconductors due to the ill-defined interface, thereby compromising the properties of semiconductors. Consequently, this leads to a substantial gate leakage current and a low I_{on}/I_{off} ratio[44]. Therefore, the utilization of crystalline dielectrics to create an atomically flat dielectric/semiconductor interface via vdW contact is critical for preserving the independent electronic properties of the semiconductor in the FETs. To ascertain the vdW interface between the GdOCl dielectric and the MoS_2 channel, a differential charge density calculation was performed on the GdOCl/MoS_2 heterostructure, utilizing density functional theory (DFT) calculations. As shown in Fig. 4g,a GdOCl/MoS_2 parallelogram supercell was introduced to establish the GdOCl/MoS_2 contact system. The atomic structure of both two subsystems shows no deformation after the contact, suggesting that there is no bonding between GdOCl and MoS_2. Moreover, Fig. 4h illustrates the planar averaged charge density difference in a direction perpendicular to the contact surface. The orange dashed line signifies the boundary of S atoms in MoS_2, while the blue dashed line denotes the boundary of Cl atoms in GdOCl. The average vdW gap between these two subsystems is 5.7 Å. This value is significantly larger than the combined covalent radius of both Cl and S atoms, thereby providing further evidence for the existence of a vdW contact. Additionally, to determine the band offset in the GdOCl/MoS_2 FET, an ultraviolet photoelectron spectroscopy (UPS) measurement is conducted. The work functions of

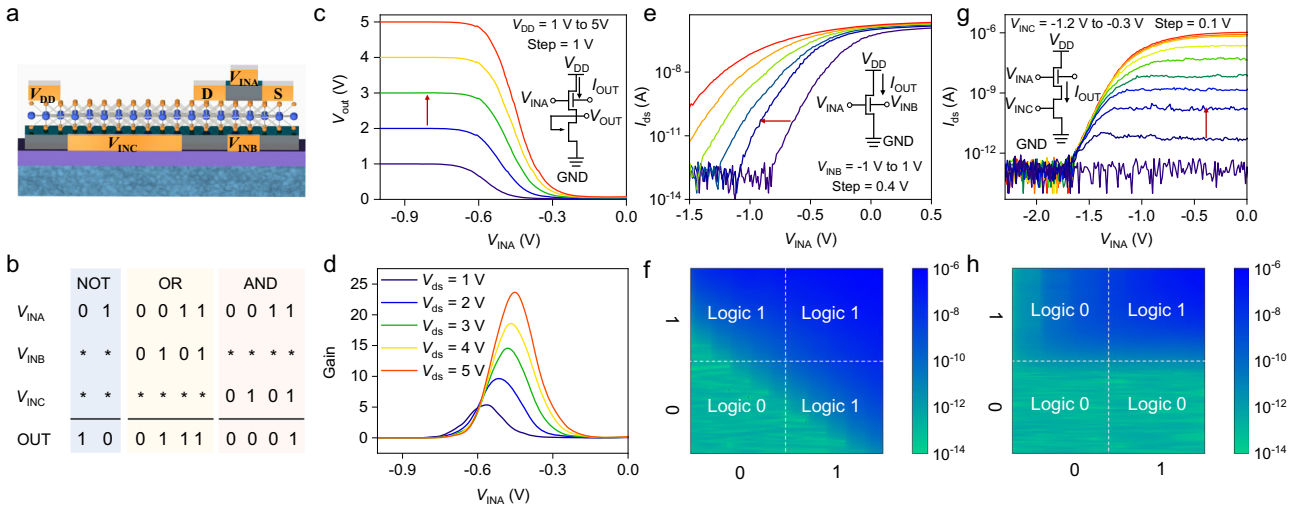

Fig. 5 | Logic gates constructed using GdOCl/MoS_2 transistors. a Structure schematic of the fabricated logic device. **b** The truth tables for the logical functions of "NOT", "OR", and "AND" realized by different gate inputs. **c** Voltage transfer characteristics of an NMOS inverter constituted by two GdOCl/MoS_2 FETs with the bias voltage (V_{dd}) ranging from 1 V to 5 V. **d** The corresponding voltage gains of the resulting inverter in Figure (**c**). **e** Transfer curves of top-gate (V_{INA}) transistors at different V_{INB}. **f** Logic OR gate implemented with varying V_{INA} and V_{INB} values. **g** Channel current as a function of V_{INA} for varying V_{INC} values. **h** Logic AND gate implemented with varying V_{INA} and V_{INC} values.

MoS_2 and GdOCl were calculated by the following formula: $\Phi = h\nu - (E_{cutoff} - E_f)$, where $h\nu$ is the energy of the excitation light He I (21.22 eV), E_{cutoff} is the secondary electron cut-off, and E_f is the Fermi edge, which can be extracted from the UPS spectra (Supplementary Fig. 20)[34]. The band alignment between MoS_2 and GdOCl is determined based on the aforementioned parameters. Figure 4i illustrates that the VBM offset and CBM offset are approximately 2.04 eV and 1.41 eV, respectively. Both meet the band offset criterion (>1 eV), effectively mitigating the leakage current produced by Schottky emission.

Logic gates based on GdOCl/MoS_2 transistors

Leveraging the benefits of GdOCl nanosheet as a gate dielectric, multigate operation logic circuit can be fabricated. Figure 5a presents the schematic diagram of the device structure, which comprises a double-gate transistor and a buried-gate transistor in series, with channel widths of 4 μm and 7 μm, respectively. The corresponding OM image is provided in Supplementary Fig. 21. Using this device structure, transistor-to-transistor logic functions such as NOT, OR, and AND gates are implemented. The corresponding operational diagrams are shown in Fig. 5b. Figure 5c, d illustrate the switching function of the NMOS inverter, demonstrating highly sharp voltage conversion with the input V_{INA} and a voltage gain up to 23.7 at V_{dd} = 5 V. This high voltage gain is crucial for signal regeneration. As shown in Fig. 5e, the transfer curves of the 4 μm-channel MoS_2 transistor change with increasing the buried gate voltages (V_{INB}), which can be attributed to the dual-gate coupling effect. When the V_{INB} increases from −1 to 1 V, there is an increase in the on-current, a shift of threshold voltage (V_{TH}) towards negative direction and an increase of the off-state current from 1.6×10^{-13} A to 2×10^{-10} A. Consequently, when both V_{INA} and V_{INB} are inputted, the low- and high-output currents are designated as logic 0 and logic 1, respectively, achieving the OR gate. The circuit diagram is displayed in the inset of Fig. 5e and the corresponding truth table is shown in Fig. 5b. The graphical demonstration clearly illustrates the desired logic function of the OR logic operation, where blue and green regions denote the on and off states, respectively (Fig. 5f). Furthermore, by taking V_{INA} and V_{INC} as inputs, the AND logic can be achieved. The corresponding circuit and truth table are shown in the inset of Fig. 5g, b, respectively. Figure 5g shows the transfer curves of two transistors connected in series. The graphical demonstration of AND gate logic shown in Fig. 5h indicates effective operation. The successful construction of NOT, OR, and AND gates demonstrates that the capability of the GdOCl for logic circuit integration.

In summary, we have successfully synthesized air-stable 2D GdOCl nanosheets with tunable thickness through the chloride hydrate-assisted CVD method. By manipulating the flow rate during the growth process, vertical growth of these GdOCl nanosheets is achieved, facilitating their transfer to form a high-quality gate dielectric-channel material interface. Importantly, our research demonstrates that GdOCl is the most promising insulator among those currently available, meeting all the essential criteria for advanced gate dielectrics such as a wide bandgap, high dielectric constant, low leakage currents, and high breakdown field strength. We have fabricated the high-performance GdOCl/MoS_2 top-gate FETs, characterized by negligible hysteresis, low subthreshold swing, and high I_{on}/I_{off} ratio. Furthermore, GdOCl/MoS_2 FETs demonstrate robust functionality in short-channel transistors and logic devices. These dielectric properties of GdOCl offer promising opportunities for the development of novel high-speed operated nanoelectronic devices and low-power electronic applications.

Methods

Growth of ultrathin GdOCl nanosheets on *c*-sapphire substrate

2D GdOCl nanosheets were successfully synthesized inside a custom CVD system, which equipped with 1 inch diameter quartz tube. $GdCl_3 \cdot 6H_2O$ powders (purity 99.9%, Aladdin) and NaCl powders (purity 99.99%, Aladdin) were mixed in a ceramic boat and placed in the center of the furnace as precursors. A piece of 1 cm × 2 cm clean *c*-sapphire was used as the growth substrate, placed above another ceramic boat downstream. Prior to the growth process, the system was purged with ultra-high purity argon (Ar) at a flow rate of 900 sccm for a duration of 5 minutes to eliminate residual oxygen and moisture. Then, the furnace was heated to a temperature of 950 °C over a period of 30 minutes, maintaining a constant Ar flow rate of 90 sccm. The temperature was then held at 950 °C throughout the growth process without altering the Ar flow rate. After 15 minutes, the growth process was stopped and the furnace was allowed to naturally cool down to room temperature. We adjusted different source temperature from 950 °C, 980 °C, to 1010 °C, which corresponding to the substrate temperature

of 480 °C, 500 °C, and 520 °C, respectively, and Ar flow rate of 60 sccm and 100 sccm to get nanosheets of various thicknesses and growth mode, ensuring the stable deposition of nanosheets and the generation of appropriate thicknesses.

Crystal structure characterizations of GdOCl nanosheets

The morphology of the GdOCl nanosheets was analyzed using optical microscopy (DP27, Olympus), The thickness was verified with an atomic force microscope (Dimension Icon, Bruker). The Raman spectra were performed using a High-resolution Raman spectrometer (LabRAM HR Evolution, HORIBA Scientific) equipped with a 532 nm laser excitation source. The crystal microstructure and component proportions investigated through XRD (D8 DISCOVER, Bruker), XPS (ESCALABXi + , Thermo Scientific), TEM (JEM-ARM200F, JEOL), STEM (FEI Titan cubed Themis G2 300). The band offset was characterized using a UPS (ESCALAB 250XI, Thermo).

Calculations of band structure

All calculations were performed in the framework of the DFT with the projector augmented plane-wave method, as implemented in the Vienna ab initio simulation package. The exchange-correlation potential was selected based on the generalized gradient approximation proposed by Perdew, Burke, and Ernzerhof [45]. The long range van der Waals interaction was described by the DFT-D3 approach[46]. A cut-off energy for the plane wave was set to 400 eV, with an energy criterion set to 10^{-5} eV during iterative solution of the Kohn-Sham equation. All structures were relaxed until residual forces on atoms fell below 0.03 eV/Å. Brillouin zone integration employed a $6 \times 6 \times 3$ k-mesh for GdOCl. The bands were calculated along a high-symmetry path in the irreducible Brillouin zone obtained using the automatic flow program (AFLOW)[47], while the electronic density of states (DOS) was derived from the dense $8 \times 8 \times 4$ k-mesh GdOCl.

Calculations of the differential charge density

All calculations were conducted within the framework of the DFT, utilizing the projector augmented plane-wave method as implemented in the Vienna ab initio simulation package[48]. The generalized gradient approximation proposed by Perdew-Burke-Ernzerhof (PBE) was selected for the exchange-correlation potential[45].

Here, we defined $\Delta\rho = \rho_{A+B} - \rho_A - \rho_B$ as the charge density difference of an A/B heterostructure, where ρ_{A+B}, ρ_A and ρ_B were the charge densities of the A/B heterostructure, isolated A and B slabs, respectively.

Device fabrication and electrical measurements

To accurately determine the capacitance of GdOCl with thickness >5.2 nm, metal-insulator-metal (MIM) capacitors were fabricated on quartz substrates. The bottom electrode was written using electron beam lithography (EBL), followed by deposition of 5 nm Cr and 20 nm Au via thermal evaporation process. Later, the GdOCl nanosheets on the sapphire were transferred to polydimethylsiloxane (PDMS) through direct pressure, and then transferred onto the bottom electrode with the help of multi-axis translation stages (translation precision roughly 1 μm). Finally, a top electrode composed of Cr/Au (5/50 nm) was defined in a secondary standard EBL and thermal evaporation process. The fabrication of the top electrode in 5.2 nm GdOCl MIM capacitors was adopted the metal films transfer method previously reported[49].

For the MoS_2 FETs, the mechanically exfoliated MoS_2 flake was transferred onto a SiO_2/Si substrate and Cr/Au (10/50 nm) source-drain electrodes were fabricated on it by EBL and thermal evaporation process, respectively. This was followed by the transfer of GdOCl nanosheets onto the MoS_2 using PDMS as a top-gate dielectric. After that, Cr/Au (10/70 nm) top-gate electrodes were deposited on the GdOCl nanosheet via standard EBL and thermal evaporation processes. The fabrication process for the NMOS logic inverter, aside from employing graphene as a bottom-gate electrode, closely mirrored that of the MoS_2 FETs. Two back gate electrodes are prepared on SiO_2/Si substrate firstly. Following this, GdOCl and MoS_2 are sequentially transferred onto the back gate electrodes via dry transfer method. This process prepares dual-gate and buried-gate transistors with channel lengths of 3 and 10 μm, respectively.

For the logic gate devices, two buried gate electrodes are firstly prepared on a SiO_2 substrate by EBL and thermal evaporation techniques. Subsequently, the GdOCl and MoS_2 are sequentially transferred onto two buried gate electrodes. Then, two MoS_2 channel transistors with varying lengths were defined by the same way with two buried gate electrodes. Finally, the GdOCl was transferred above the shorter channel MoS_2 transistor to create a top-gate structure.

The C–V measurement of polycrystalline GdOCl powders were conducted using an impedance analyzer (E4990A, Keysight). The remaining electrical measurements were performed by a semiconductor analyzer (B1500, Keithley) equipped with a probe station (TTPX, Lake shore), and carried out at room temperature and in a vacuum environment (10^{-4}Torr).

Data availability

Relevant data supporting the key findings of this study are available within the article and its Supplementary Information file. All raw data generated during the current study are available from the corresponding author upon request.

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Author contributions

S.Y. conceived the idea and designed the study. W.X. synthesized the samples and performed material characterizations. W.X., J.J. and N.T. fabricated and measured the devices. Y.C. conducted theoretical calculations. W.X., S.Y. and C.J. co-wrote and revised the manuscript. All authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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