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Step-necking growth of silicon nanowire channels for high performance field effect transistors

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Ultrathin silicon nanowires (diameter <30 nm) with strong electrostatic control are ideal quasi-1D channel materials for high-performance field effect transistors, while a short channel is desirable to enhance driving current. Typically, the patterning of such delicate channels relies on high-precision lithography, which is not applicable for large area electronics. In this work, we demonstrate that ultrathin and short silicon nanowires channels can be created through a local-curvature-modulated catalytic growth, where a planar silicon nanowires is directed to jump over a crossing step. During the jumping dynamic, the leading droplet undergoes significant stretching, producing a short necking segment of <100 nm in length, with a reduced diameter from approximately 45 nm to <25 nm. Compared to the FETs with uniform silicon nanowire channels, our step-necked silicon nanowire FETs exhibit substantially enhanced on/off current ratio $I_{on/off} > 8 \times 10^7$ and a sharper subthreshold swing of 70 mV/dec, thanks to a stronger gating effect in the middle channel and markedly improved electric contacts at the thicker source/drain ends. These findings mark the pioneering experimental demonstration of catalytic growth acting as a deterministic fabrication method for precisely crafting engineered FET channels, ideally fitting the requirements of high-performance large-area displays and sensors.

Metal-droplet-mediated catalytic growth offers a rather cost-effective, versatile, and high-yield approach to manufacturing ultrathin silicon nanowires (SiNWs) that are optimal quasi-one-dimensional (1D) channels for building high-performance field effect transistors (FETs)[1–13]. Typically, to attain enhanced electrostatic control and increased drive current, it is imperative to scale down the diameter of the SiNW channels to <30 nm and shorten the channel length to <100 nm, as evidenced in the latest fin or gate-all-around FETs[14–19]. However, the fabrication of such ultrathin and short c-Si channels necessitates the use of advanced deep/extreme ultraviolet or electron beam lithography techniques, which are incompatible with large area electronics, such as the thin film transistor (TFT) logics utilized in flat panel display, which are fabricated on glass/polymer substrates with a limited thermal budget <500 °C and a coarser lithography resolution usually >1.5 μm[11]. This limitation makes it impossible to define and pattern any delicate channel or source/drain (S/D) electrodes with feature dimensions <100 nm.

Indeed, ultrathin catalytic SiNWs with diameters <30 nm have previously been fabricated using tiny metallic droplets as catalyst[20] in what is known as the vapor-liquid-solid (VLS) mechanism[21–25]. However, one of the challenges associated with the VLS-grown SiNWs is their formation as typically standing arrays, which complicates their post-

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growth transfer and integration onto flat substrates for scalable electronic applications[25–32]. Moreover, the creation of FET prototypes with very short channel L_{SD} < 200 nm[33,34] continues to rely solely on the use of the high-precision EBL technique, which remains a bottleneck for mass production and scalable application of the catalytic SiNW FET devices.

Inspired by the channel configuration in fin-gate FETs, as depicted schematically in Fig. 1a, where a short ultrathin c-Si channel is sandwiched between a pair of bulky S/D contacts, one is drawn to ponder the possibility of replicating such thick/thin/thick short-channel geometry through a single-run catalytic growth process. In theory, this will require precise manipulation of the soft leading droplet during catalytic growth, enabling its substantial deformation to effectively modulate the diameter of the resulting SiNWs. Despite of several reports in the literature on the diameter variation during VLS growth[35–37], deterministic control over the SiNW diameter at designated locations, and the shaping thereof into a specific channel geometry, has not yet been achieved, particularly on planar substrate surfaces.

Built upon our previous works on an in-plane solid-liquid-solid (IPSLS) growth mechanism[38–40], we explore here a geometry control strategy, based on a local-curvature-modified growth necking dynamic, as showcased in Fig. 1b. This can help to achieve a designable diameter necking at predetermined locations, creating such a highly modulated thick/thin/thick short channel configuration. Specifically, the IPSLS process employs indium (In) droplets as catalysts and produces SiNWs confined onto the substrate surface pre-coated with amorphous Si (a-Si) precursor thin film[41–46]. Thanks to a step-guiding-growth technology of IPSLS mechanism, the catalyst droplet, and thus the SiNW, can be directed by a guiding step to grow/jump over another crossing step, providing a high-curvature edge surface akin to the diameter of the droplet. As a result, a SiNW with an initial diameter of around 45 nm can be continuously narrowed down to <25 nm during the step-jumping dynamic, forming a middle channel of <100 nm long, connected by two thicker segments at both ends as de facto S/D electrodes. Compared to the uniform channel SiNW FETs, these step-necked FETs achieve a much higher I_{on}/I_{off} ratio >8×10^7 and a steeper subthreshold swing (SS) of 70 mV/dec, thanks to a stronger electrostatic gating in the middle thinner channel and improved S/D contacts at the thicker ends, as revealed in a TCAD model analysis.

Results

Guiding step formations and IPSLS growth procedure

In order to direct the catalyst droplet to grow/jump over a step edge at the desired location, a guiding growth technology established in our previous works[37] has been adopted here. As schematically illustrated in Fig. 1g, a parallel array of guiding steps was first patterned on a planar c-Si wafer substrate coated with a 2 μm SiO_2 layer, by using conventional lithography to define the terrace position. A total of 3 layers of high-density mini-steps (~100 nm wide) were formed at the terrace edge, via an alternating etching-oxidation procedure as detailed in the

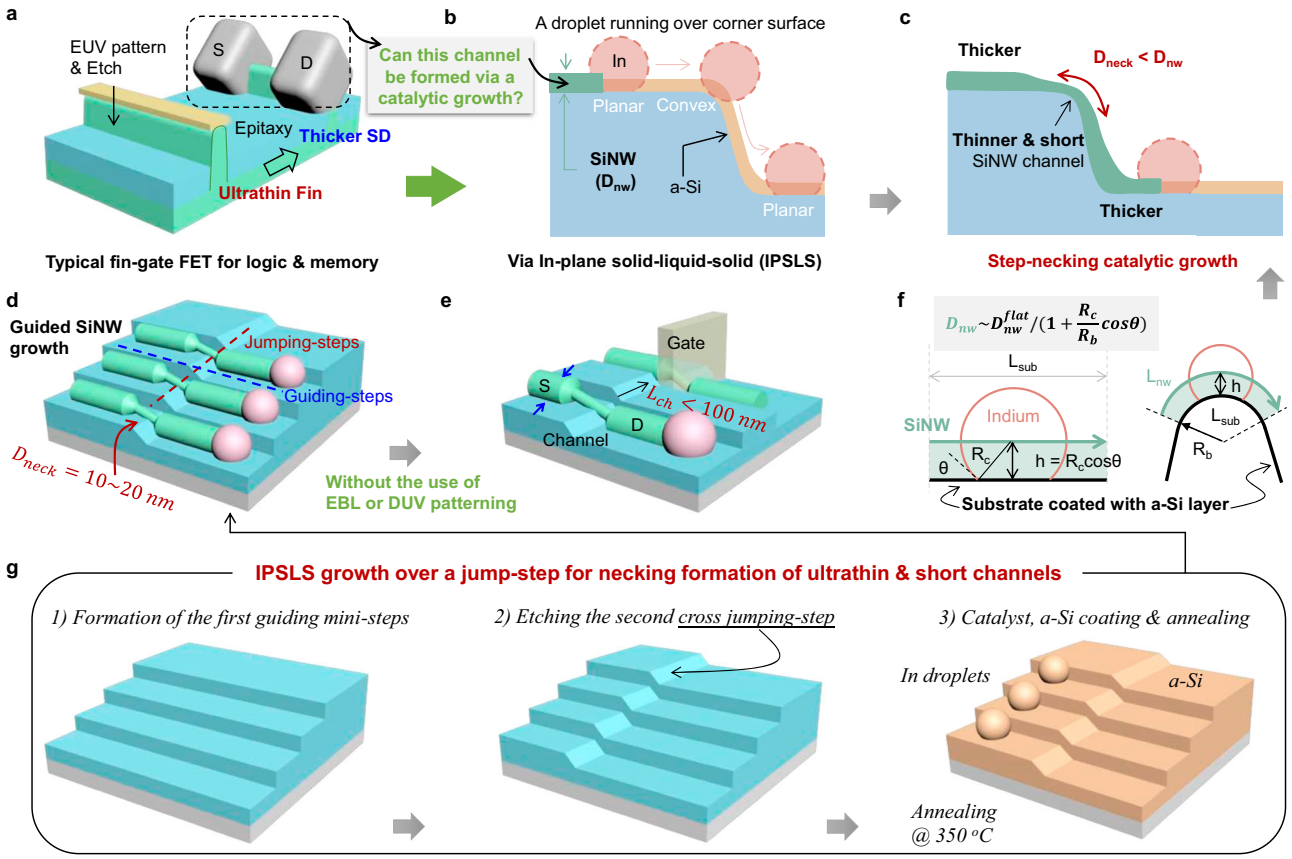

Fig. 1 | Step-necking growth of ultrathin and short SiNW channels. a Illustration of a conventional fin-type field-effect transistor (finFET) architecture for logic circuits, featuring a narrow channel and wider source/drain (S/D) contacts. Fabrication involves extreme ultraviolet lithography (EUV) for patterning and epitaxial growth for the S/D regions. **b**,**c** Demonstration of the step-necking catalytic growth technique, which results in a distinctive thick/thin/thick channel profile. As depicted in **f** SiNWs grown over a convex edge exhibit a narrowed (necked) diameter (D_{neck}) compared to those on a flat substrate (D_{nw}^{flat}) when the curvature radius of the bending track (R_b) is comparable to the size of indium catalyst droplet (R_c). **d** Schematics of a guided growth of a parallel array of IPSLS SiNWs to grow over a jumping step to form an array of necked SiNWs with middle diameters <20 nm and a short channel length (L_{ch}) of <100 nm. **e** Short-channel FET built upon necked SiNWs, where the thin middle serves as the channel and two thick ends as de facto source/drain electrodes. **g** Detailed fabrication steps for the step-necking SiNWs, including guiding step formation, jumping step etching, catalyst deposition/a-Si precursor coating, and annealing growth.

the Methods section. Note that this alternating mini-step etching doesn't require high-resolution lithography, but can help to achieve a high-density growth integration of SiNWs to boost the driving current.

Then, the jumping steps, perpendicular to the guiding steps, are patterned and etched to the desired heights, as showcased in Supplementary Fig. 1. For the IPSLS growth of SiNWs, In strips were first evaporated and defined at the starting ends of the guiding steps, as depicted in the 3rd panel in Fig. 1g and Supplementary Fig. 2. After loading the sample into a PECVD system for H_2 plasma treatment at 250 °C, the In strips were transformed into discrete droplets, followed by coating with an a-Si layer at 100 °C, and annealing in vacuum at 350 °C to kick off the IPSLS growth of SiNWs. During the annealing growth, the In droplets became molten and started to absorb the a-Si nearby to move along the guiding steps to produce crystalline SiNWs.

Jumping step design for step-necking dynamic

The role of the jumping step, formed by a cross-etching as depicted in the middle panel of Fig. 1g, is to introduce a short segment of sharply turning edge surface, with local curvature radius reduced to that comparable to the In droplet size, as illustrated in Fig. 1b,c. Generally, a curved surface will alter the supply of a-Si for the IPSLS growth, thereby causing a change in the local SiNW diameter. Although our previous study has showcased a guided growth of IPSLS SiNW over large bending tracks, with curvature radius significantly larger than catalyst droplet size, $R_b >> R_c$[47], the impact of curvature on diameter variation was found to be negligible. In this work, when the bending radius is aggressively reduced to approximately the droplet size, $R_b \sim R_c$, the growth balance condition could be significantly modified. To formularize this effect, we consider the scenario illustrated in Fig. 1f, where a catalyst droplet traverses a distance L_{sub} on a flat substrate surface coated with a thin a-Si layer. During movement, the droplet absorbs the a-Si layer from the surface, producing a SiNW segment of length $L_{nw}=L_{sub}$ with a diameter of D_{nw}^{flat}. However, when the catalyst droplet encounters a curved surface with a local bending radius of R_b, the relationship between the length of the SiNW produced and the distance traveled by the droplet along the substrate changes. Specifically, the SiNW length becomes longer relative to the substrate distance, with a ratio of $L_{nw}/L_{sub} = 1+ h/R_b$, where $h=R_c\cos\theta$ is the average height of the catalyst droplet above the substrate surface, and θ is the contact angle of the catalyst liquid to the surface. As the amount of absorbed a-Si supply is always proportional to the travel distance of L_{sub}, a longer SiNW segment produced at the convex edge surface will lead to a thinner diameter:

$$D_{nw} \sim D_{nw}^{flat} / \left(1 + \frac{R_c}{R_b}\cos\theta\right) \quad (1)$$

Note that, according to Eq. (1), this diameter-necking will become more significant when the curvature radius decreases and approaches to the droplet size. This also highlights the sensitivity of the SiNW diameter to the surface topology during the growth process.

While it is challenging to pattern a highly curved surface with $R_b < 100$ nm using conventional lithography, such geometries naturally emerge at the convex upper corners of the jumping steps, as exemplified in Fig. 1d. More importantly, the step-necking effect is localized specifically at the jumping step, leading to the formation of a narrowed short channel at the predetermined location. The length of the narrowed channel is proportional to the periphery of the convex step-edge, that's $L_{ch} \sim R_b < 100$ nm. Away from the jumping step, the SiNW growth returns to a balanced state, resulting in thicker segments that are well-suited to function as favorable thicker electrodes to improve the electrical S/D contacts.

Step-necking dynamics at jumping steps

As a reference for comparison, Fig. 2a,b present the typical SEM images of the normal (without jumping step) guided growth of SiNWs upon three terrace mini-steps. The SiNWs highlighted in green feature a uniform diameter of $D_{nw} = 39 \pm 8$nm, as evidenced by the statistics in Fig. 2c. Note that the surface roughness of SiNWs, resulting from fluctuations in the guiding steps, can be mitigated by refining the

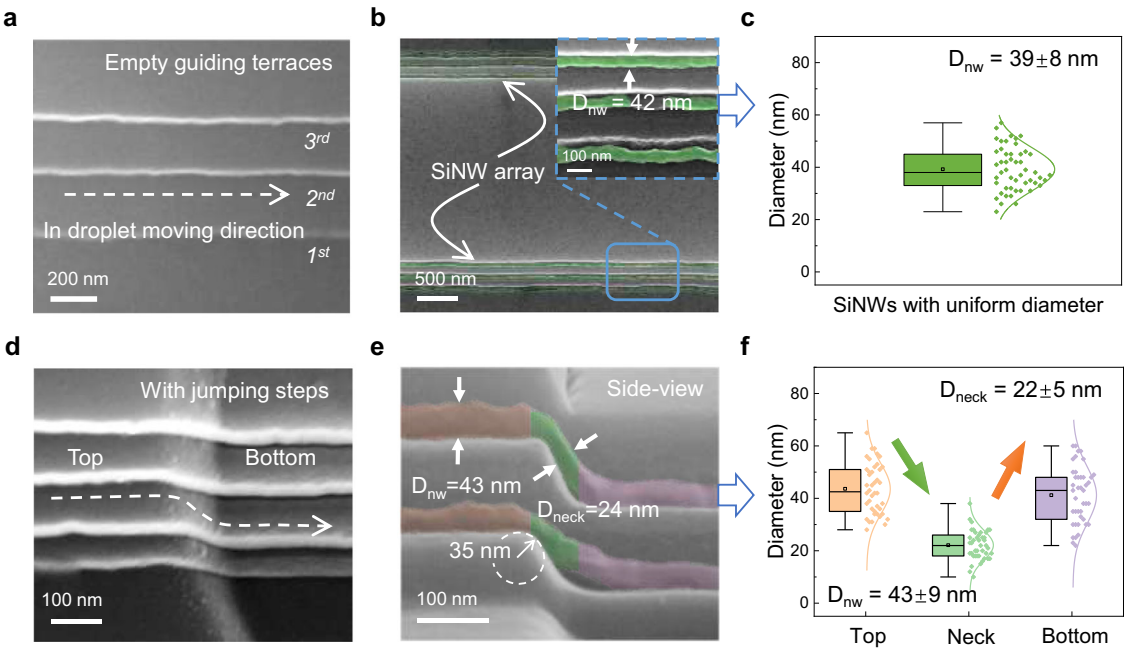

Fig. 2 | Morphology and statistics of SiNWs guided by terraces without and with jumping steps. a SEM image of the multi-level guiding steps with the growth direction of SiNWs marked by a white arrow. **b** Typical SEM images of the SiNWs grown upon the flat guiding steps. **c** Statistics on the diameter of SiNWs. **d** Empty terraces with jumping steps, where the catalyst In droplets will be led to grow from the left (top) to the right (bottom) over the crossing step. **e** SEM image of the step-necked SiNWs, where the diameter of the necked segment is only half of that in the thicker ends. **f** Statistics on the diameters of SiNWs at different step-necking stages.

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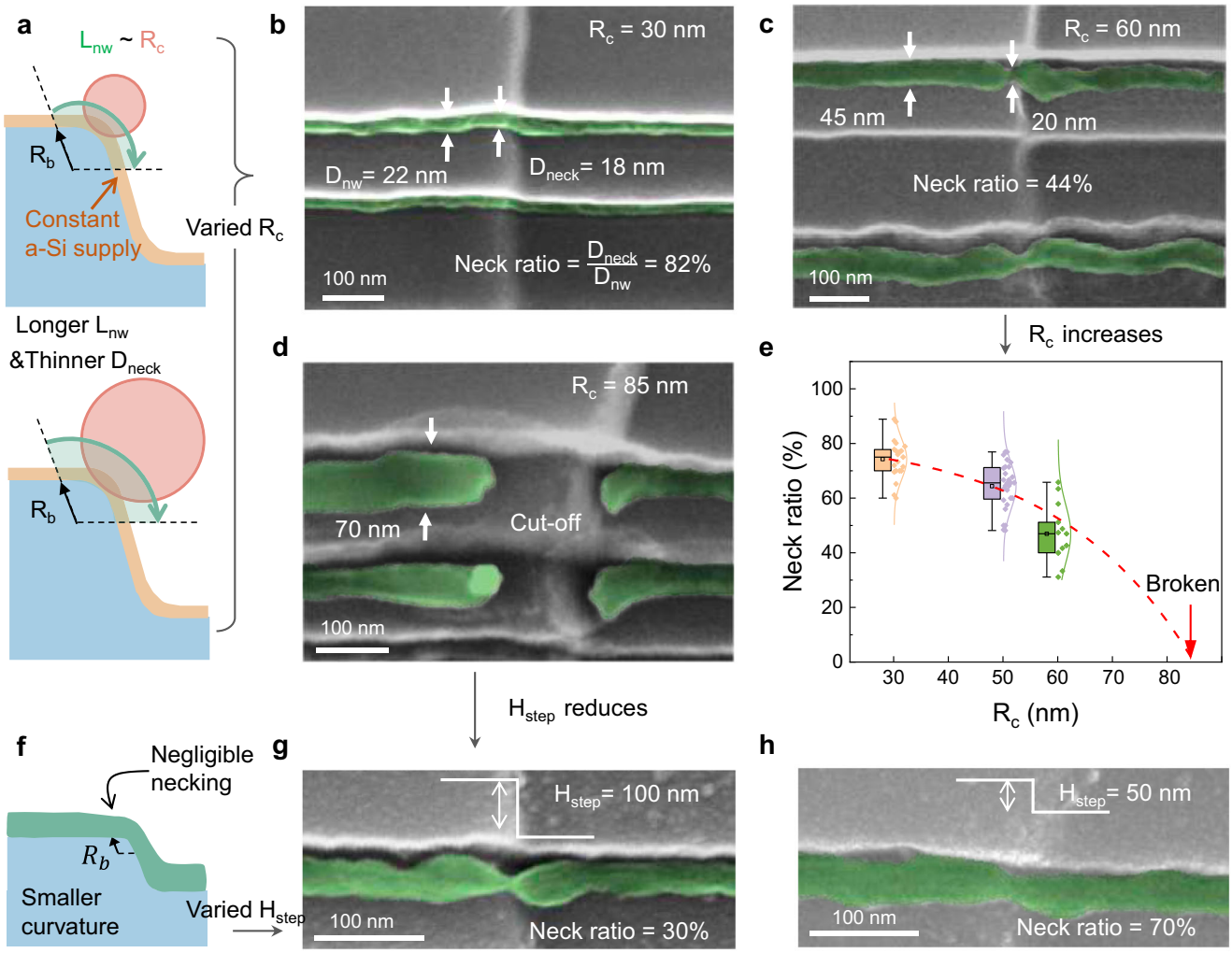

Fig. 3 | Necking structure tailoring by the size of In droplets and the height of the jumping step. a Schematic illustration of the evolution of D_{neck} grown via different droplet sizes, with the corresponding SEM images of the as-grown SiNWs provided in **b**–**d**. **e** Statistics on neck ratio. **f** Schematic diagram of SiNWs growing over a lower jumping step. **g**,**h** SEM images of SiNWs grown with different jumping step heights.

lithography and etching processes, as demonstrated in Supplementary Fig. 3. Upon introducing a jumping step with a height of H_{step} ~ 100 nm and a local curvature radius of R_b ~ 35nm, as observed in the SEM images shown in Fig. 2d,e, the SiNWs growing from left to right remarkably thin out gradually at the jumping step. As indicated in Fig. 2e and corroborated by the statistics in Fig. 2f, the SiNWs that initially pose a diameter of $D_{nw}^{top} = 43 \pm 9$ nm on the top platform, shrink to a reduced diameter of $D_{nw}^{neck} = 22 \pm 5$ nm over the step corner section, followed by returning to thicker segments at the flat bottom edges, forming thus a thick/thin/thick channel with an effective narrow channel length of L_{ch} ~ 95 nm. This finding highlights the potential of a simple catalytic growth to shape delicate and precise nanoscale geometries – a capability that has remained uncharted until now. It is also noteworthy that this step-necking dynamic has been consistently observed across hundreds of independent growth experiments, provided the catalyst size, a-Si thickness, and jumping step are appropriately designed.

Parametric control of step-necking dynamics

To serve as advantageous channels in FETs, it is preferable that the middle segment becomes thinner (D_{neck}) to facilitate complete gate depletion, while the two ends remain thicker (D_{nw}) to ensure a larger contact area for improved S/D contact. To this end, a continuous SiNW with a lower necking ratio (NR) of $NR = D_{neck}/D_{nw}$ is desirable for achieving excellent field effect device performance. As one of the key tuning parameters, the impact of the In droplet size (R_c) on NR was first investigated. The R_c can be effectively adjusted by varying the thickness of the indium film and the H_2 plasma treatment conditions, including duration, power, and temperature. As depicted in Fig. 3a, for the same jumping step profile and a-Si coating, a larger R_c leads to the formation of a longer SiNW (represented by the green segment) over the convex corner, coated with a constant a-Si supply. So, according to Eq. 1, the local SiNW will be reduced to a much thinner diameter, thus lowering the NR, as the size of the catalyst droplets increases. Interestingly, this is indeed observed in the experiment, as shown in Fig. 3b–d, where the smaller droplets with R_c = 30nm, as inferred from the diameter of the as-grown SiNW, produce continuous SiNW with only a slight diameter shrinkage at the jumping step. In contrast, the step-necking phenomenon becomes far more significant for the double-sized droplets with R_c = 60nm, and even breaks up at the jumping step for even larger ones, as witnessed in Fig. 2c,d, respectively. This evolution trend can be better seen in the extracted statistics in Fig. 3e, which indicate that the NR factor can be steadily reduced to around 47%, with R_c up to 60 nm, while preserving a continuous growth of SiNW, a criterion for the FET channel. The breakage of SiNW for larger droplets with R_c > 85 nm can be attributed to the insufficient a-Si supply, which causes the soft In droplet to experience a stretching force exerted by the front In/a-Si absorption and the rear SiNW/In

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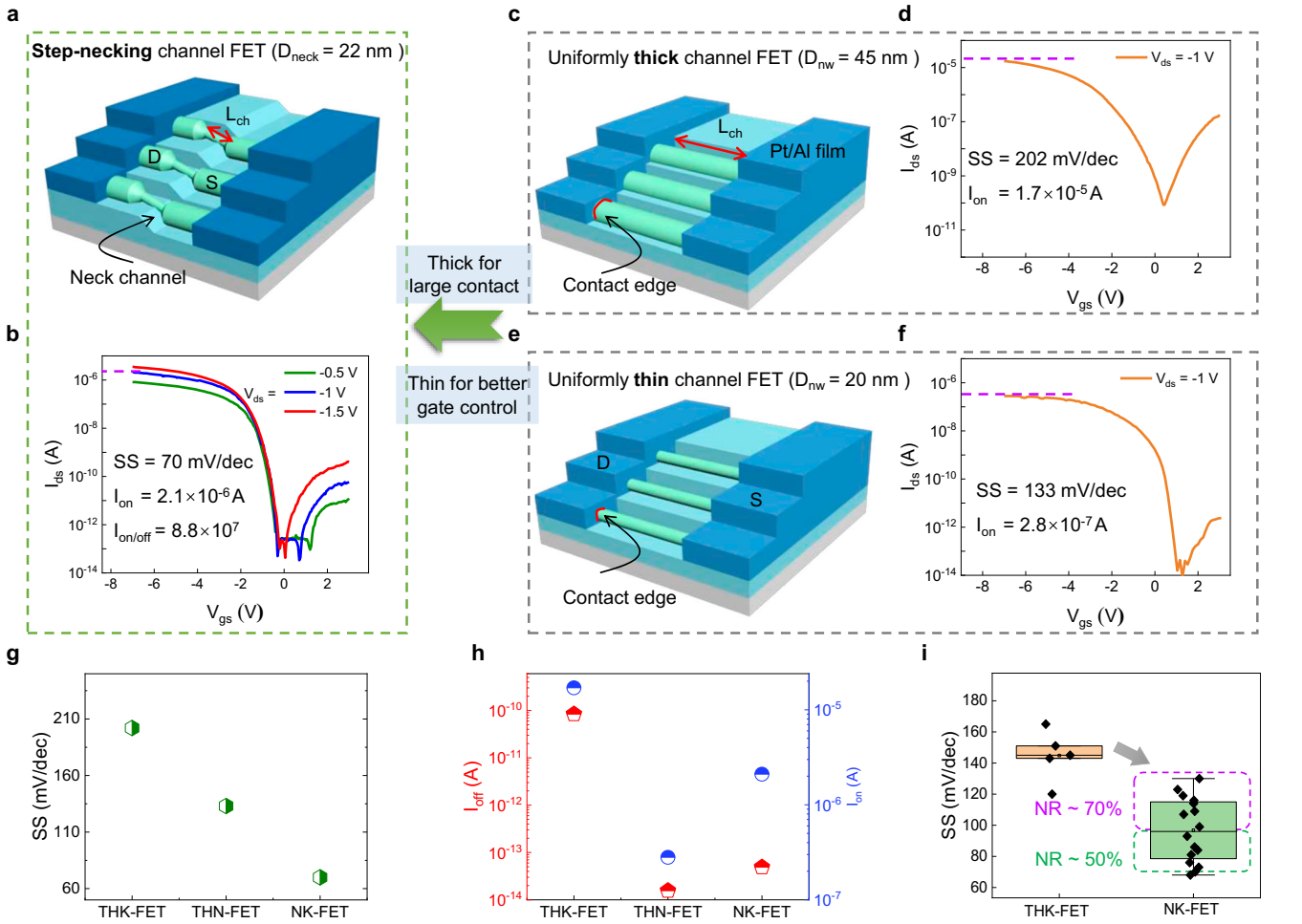

Fig. 4 | Comparison of SiNW FETs with step-necked and uniform channels. **a** Short-channel transistor built upon step-necking SiNWs with L_{ch} controlled by the height of jumping steps, where the thinner middles serve as the channel and the thicker ends act as the S/D contacts. **b** Improvement of device performance with step-necking SiNWs. **c** Illustration of the transistor based on uniform thick channels, where the source/drain contact area is proportional to the diameter of SiNWs. **d** Transfer characteristic of the long-channel transistor with L_{ch} defined by lithography. **e** Device structure with uniform thin channels, while the I_{ds}–V_{gs} curve is demonstrated in **f**. **g**,**h** Comparison of key performance indicators for devices with uniform thick (THK-FET), uniform thin (THN-FET), and necked SiNWs (NK-FET), respectively. **i**, Statistics on SS of THK-FETs and NK-FETs.

deposition interfaces, as explained with more details in our previous works[48]. This thus forces the liquid droplet to deform or elongate, against the surface tension, up to a limit where the pulling force will suddenly break the contact between the In droplet and the SiNW end. After that, a new segment of SiNW will nucleate and grow starting from the bottom edge of the jumping step, leaving a gap proportional to the diameter of the leading droplets ($\sim 2R_c$).

In parallel, the height of the jumping step emerges as a critical factor in regulating the step-necking geometry, thereby influencing the NR factor (Fig. 3f). Ideally, the step height should be higher than the local bending radius, a condition met in the aforementioned examples where $H_{step} \sim 120$ nm > R_b. Although the a-Si layer thickness coated on the step sidewall depends on the step height, we focus here solely on the shallow step scenarios for the sake of simplicity, where $H_{step}<3R_b$ and assuming that variations in a-Si thickness are negligible for the PECVD deposition conditions employed herein. Therefore, as the step height is gradually reduced from H_{step} = 120 nm to 100 nm and 50 nm, even the large droplets, which previously resulted in broken SiNWs, as seen in Fig. 3d, begin to yield continuous channels. This transition is accompanied by a notable rise in the NR factor, from 30% to 70%, as evidenced in Fig. 3g,h, respectively. Additionally, the step-necking growth is performed for deep jumping steps with heights up to 1 µm. Given that the influence of gravity is negligible compared to the surface or interfacial tensions due to the small size of the In droplets and the vacuum growth environment, the droplets can maintain stable contact with the sidewall of the jumping step, enabling the growth of a long vertical SiNW segment, as shown in Supplementary Fig. 4. While more comprehensive studies are still needed to fully elucidate the intricacies of this step-necking dynamics, these preliminary experimental findings underscore the efficacy of both the step profile and droplet size as highly effective and adjustable control parameters for fabricating short-necked channels through a single-run catalytic growth.

Device performances of short-necked channel FETs

To testify the influence of channel engineering on the device performance, a group of prototype junctionless FETs were built upon SiNWs with or without the step-necked channel geometries. For all the FET devices, the channel is composed of 3 parallel SiNWs, connected by a pair of Pt/Al metal pads as S/D electrodes, separated 3 µm apart and defined by using conventional lithography, as shown in Supplementary Fig. 5. Then, the samples were coated with a dielectric layer of 25 nm Al_2O_3 by using atomic layer deposition (ALD), followed by patterning and deposition of a 60 nm thick Al film as top-gate electrodes. As illustrated schematically in Fig. 4a,c,e, the devices with necked SiNW channels are referred to as NK-FET, while the devices with

uniform-diameter thick or thin SiNWs are designated as THK-FET and THN-FET, respectively. Notably, all three types of devices use the same gate stack. The transfer characteristics of these three types of FETs are shown in Fig. 4b,d,f, while the corresponding output curves are provided in Supplementary Fig. 6. All these SiNW FETs exhibit p-type channel FET behavior, which can be assigned to the incorporation of In atoms, a p-type dopant in c-Si, into the SiNW channels during the IPSLS growth[40,49].

Specifically, the I_{ds}-V_{gs} curve shown in Fig. 4d reveals that the THK-FET, with a uniform channel diameter of $D_{nw} \sim 45$nm, achieves a high current I_{on} up to 1.7×10^{-5} A, accompanied by a high leakage/off current I_{off} of 8.4×10^{-11} A, and a SS of 202 mV/dec, indicating an insufficient gate depletion of these relatively thick SiNW channels. In comparison, the use of a thinner SiNW channel, with a reduced diameter down to 20 nm, can help to suppress the off current to 1.5×10^{-14} A and obtain a steeper SS of 133 mV/dec, as witnessed in Fig. 4f. However, this comes with a significant drop in the on-current I_{on} of 2.8×10^{-7} A, which results from a reduced S/D contact area, and thus larger contact resistances. A consistent conclusion is drawn from the on-state resistance (R_{on}), where R_{on} increases by over an order of magnitude when D_{nw} is reduced from 45 nm (THK-FET) to 20 nm (THN-FET). This represents a dilemma for the junctionless SiNW FETs with Schottky barrier (SB) contacts at the S/D electrode, which demands a trade-off between seeking a higher drive current and better electrostatic control for lower leakage and sharper SS.

Fortunately, this dilemma can be better addressed using the step-necking channel design. As shown in Fig. 4b, a rather steep SS down to 70 mV/dec, a higher I_{on} and an excellent on/off current ratio of 8.8×10^7 have been accomplished simultaneously in the NK-FET, outperforming all FETs fabricated based on the catalytically grown SiNW channels. These overall device performance improvements can be clearly seen in Figs. 4g-h, where the SS, on/off ratio, and leakage current are extracted and summarized for stagging more straightforward comparisons. Notably, an oxidation process, conducted at 850 °C for 1 minute, is used to introduce a thin, high-quality SiO_2 layer between the high-k dielectric and the SiNWs surface to reduce the interface states. This rapid thermal oxidation process can be replaced by a low-temperature annealing step at 500 °C for 2 h. Decent device performance, with an SS of 78 mV/dec, an on/off current ratio > 10^7, and an on-current of 3.2×10^{-7} A, has been achieved as demonstrated in Supplementary Fig. 7, although a lower I_{on} is observed compared to those with high-temperature oxidation. This may result from a higher defect density in the SiNWs without the high-temperature process, which reduces the probability of hole tunneling from Pt/Al metal film into the thick SiNW source segment. Nevertheless, these results represent the demonstration of catalytic SiNW FETs with an SS < 100 mV/dec, achieved with the entire device fabrication procedure carried out below 500 °C, highlighting the advancement of combining ultrathin channels with naturally connected thick source/drain ends.

The benefit of forming the necking channel can also be learned by comparing the NK-FETs with different NR factors. As shown in Fig. 4i, with a gradual decrease of NR from 100% (THK-FET), to 70% and 50%, the SS has steadily improved from >140 mV/dec to 100 mV/dec, and then to 70 mV/dec, respectively. These findings highlight the benefits of combining a short (<100 nm) and ultrathin (~20 nm) middle channel and a pair of thicker SiNW segments for improved S/D contacts. Note that all these devices are fabricated by exclusively employing the lithography with a resolution of 3 µm.

Compared to the p-type and short channel FETs reported in the literature, especially those with channel materials prepared within a thermal budget of 500 °C as summarized in Supplementary Tables 1 and 2, the necked channel FETs achieve a high on-current of 32 µA/µm and a sharp SS of 70 mV/dec. While even higher device performance can be achieved for the FETs fabricated with higher thermal budget of 800–1000 °C, this high-temperature processes or the reliance on the use of silicon wafers are incompatible with large-area electronics. Moreover, the step-necking growth method offers several additional advantages: First, it eases the lithography resolution demand for fabricating short-channel FETs, facilitating their use in large-area electronics; Second, the thick/thin/thick structure enables an efficient gate control capability owing to the ultrathin necked segment, while also providing favorable source/drain contact conditions through the thick ends; Third, the natural connection between the necked channel and thick source/drain segments eliminates the need for high-temperature epitaxial process to form source/drain, simplifying device fabrication procedure.

Compared to the conventional SiNW FETs, targeting at large area electronics, the fabrication of necked channel FETs requires just one more step, that is the patterning and etching of a jumping edge, by using conventional lithography and a dry etching process. This extra cost will be justified by a significant device performance improvement of the necked-channel SiNW FET, which can outperform basically all the other TFT technologies, in terms of on/off ratio and SS (now arriving at <70 mV/dec, while the others typically at >100 mV/dec, as seen in Table S1). So, this step-necking channel technology, based on a scalable guided growth of SiNWs, has an important potential to boost the TFT performances for large-area display logics, with just one more step and minimal additional complexity and cost.

Device model and analysis

To gain deeper insights into the enhanced performance of the NK-FET, a numerical model has been built by using the TCAD simulation suite. Despite the actual channel length of the fabricated FETs being 3 µm, to reduce simulation resources and time, this model employs a simplified geometry. Specifically, the length of the thinner channel has been set to 100 nm, while the thicker segments to 200 nm at each end. Note that this simplification in the simulation model, with the shorter thick ends, leads to an overestimation of I_{on} due to the increased V_{ds} applied to the thin channel. Additionally, the I_{off} is lower than that of the experimental device since the simulation allows the demonstration of currents far below 10^{-14} A, the lowest detectable value of our measurement system. Furthermore, to facilitate comparative analysis, a model of a traditional, thick-channel FET (THK-FET) with an extended length of 500 nm has also been constructed (Supplementary Fig. 8). The simulated electrical characteristics reproduce very well the key features of the experimentally measured I_{ds}–V_{gs} curves, as evidenced in Fig. 5a,d, where the off-state current (I_{off}) is notably higher for the THK-FET, but accompanied by a greater SS.

This can be understood from the band alignment profile extracted from the model in Fig. 5b, which shows a large number of hole carriers (~10^{16} cm^{-3}) in the thick channel even in the off-state, resulting in the high leakage current. Indeed, in the case of the THK-FET, it is more difficult to achieve a full depletion of the heavily doped channel, caused by dissolved In atoms in SiNWs, about 1×10^{19} cm^{-3} as revealed by atom probe tomography (APT) mapping[10,50], when its diameter exceeds 40 nm.

With regard to the NK-FET, the ultrathin middle, with a diameter down to ~20 nm, enables a full depletion of this short segment, thus blocking thoroughly the majority hole transportation, and resulting in a low off current, as revealed in Fig. 5e. As for the two thicker ends, the larger NW/metal contact area ensures a lower resistance at the S/D electrode (Fig. 5g). A better view of this point is provided by examining the potential profile within the NK-FET channel. As showcased in Fig. 5f, the V_{ds} is mainly applied on the thin and short middle NW segment, while there is minimal voltage drop on the two thicker ends, different from that of the THK-FET (Fig. 5c). Therefore, it is based on this observation that the effective channel length (L_{ch}) should be defined as the length of the short necked middle segment in NK-FET, rather than the edge distance between two S/D electrodes. In other words, the step-necking growth dynamic offers a strategy to construct

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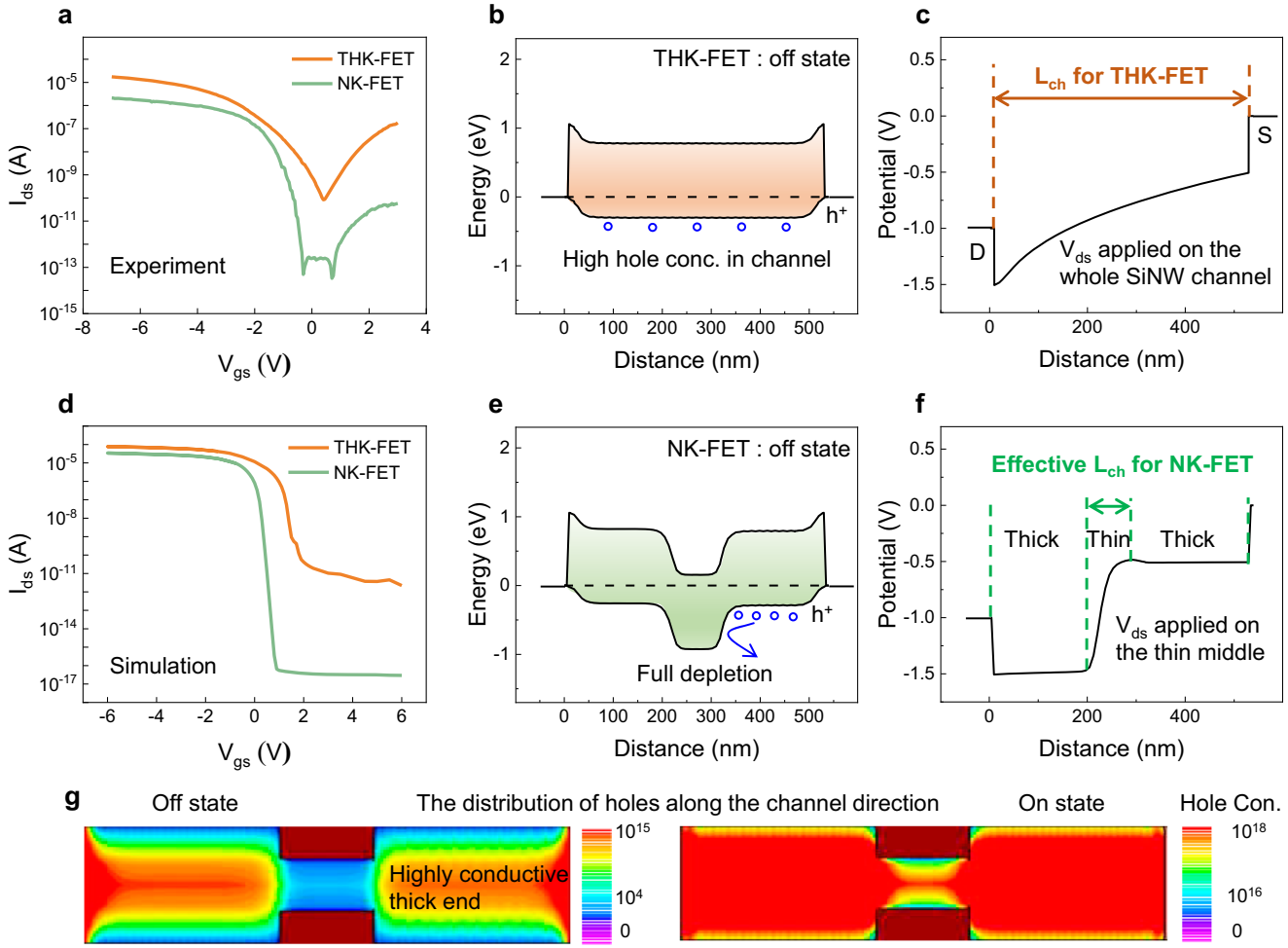

Fig. 5 | Device simulation and model analysis. a Comparison of the measured I_{ds}-V_{gs} curve for THK-FET and NK-FET. **b** Band alignments in the off state for the THK-FET extracted from the TCAD simulated model. **c** Potential on the uniform thick channel. **d** Simulated transfer curve for THK-FET and NK-FET. **e** Band alignments in the off-state for the NK-FET. **f** Partial pressure on the thin channel. **g** The distribution of hole carrier along the channel direction.

ultrathin short-channel FETs on designated locations, without the need for high-precision EBL or D/EUV lithography.

In summary, we report a step-necking growth strategy to fabricate ultrathin and short-necked SiNW channels for building high-performance FETs. It has been shown that these thick/thin/thick SiNW channels, with a necked diameter down to <25 nm, a short effective channel length <100 nm, and a pair of thicker ends of 45 nm, can be steadily obtained by adjusting the size of In droplets and the height of the jumping steps. This intricate channel engineering has indeed contributed to demonstrating high-performance SiNW-FETs, featuring a steep SS < 70 mV/dec and a high I_{on}/I_{off} current ratio > 10^7. This significantly outperforms their counterparts with uniformly sized SiNW channels. These results highlight the potential of a relatively simple yet highly efficient, but so far unexplored, catalytic growth shaping strategy, which is widely applicable for high-performance large-area electronics and sensor applications.

Methods

Notably, lithography with a resolution of 3 μm was used exclusively in all fabrication procedures.

Jumping steps formation

First, a photolithography process was conducted to define the locations of the guiding steps on a silicon substrate coated with a 2-μm-thick SiO_2 layer. Then, the sample was alternately etched by C_4F_8 and O_2 plasma in an inductively coupled plasma (ICP) system, to form multiple layers of mini-steps. The RF power, ICP power, gas flow rate, and chamber pressure for C_4F_8 plasma etching were 30 W, 400 W, 12.5 sccm, and 2 mtorr, respectively. As for the O_2 plasma etching, the parameters were set to an RF power of 50 W, gas flow of 30 sccm, and a chamber pressure of 30 mtorr. Next, the jumping steps were patterned orthogonally to the guiding steps, and etched by SF_6 with RF power of 30 W, bias power of 400 W, gas flow of 10 sccm, chamber pressure of 1.5 mtorr.

Step-necking SiNW channels growth

In stripes were patterned at one end of the guiding steps, i.e. the top surface near the jumping step, by lithography. Subsequently, In film with designated thickness was deposited using a thermal evaporation system at a rate of 0.1 Å/s, followed by a lift-off process via N-Methyl-2-Pyrrolidone (NMP). Then, the sample was loaded into the PECVD system for H_2 plasma treatment at 250 °C with a chamber pressure of 140 Pa, and an RF power of 10 W, to transfer the In film into discrete In droplets and remove the outer oxide layer. After that, a-Si thin film as precursor was deposited at 100 °C by pure silane plasma with an RF power of 2 W and a chamber pressure of 20 Pa. Next, the growth was activated in a vacuum at 350 °C where the In catalyst droplets started to absorb the nearby precursor and move along the guiding steps to form SiNWs. Finally, the remnant a-Si was etched by H_2 plasma at 150 °C with an RF power of 20 W, and a chamber pressure of 140 Pa.

FET device fabrication

First, SiNWs were oxidized in a tube furnace at 850 °C for 1 minute or at 500 °C for 2 h. Subsequently, source and drain electrode regions with a separation of 3 μm were defined at the two sides of the jumping steps via lithography. Before depositing Pt/Al (5 nm/55 nm) electrodes by an electron beam evaporation (EBE) system, the oxide layer of SiNWs was removed by soaking in BOE solution for 4 s. Then, the Al_2O_3 layer with a thickness of 25 nm was deposited as a dielectric layer using an atomic layer deposition (ALD) system at 200 °C. After that, the gate region, which overlapping the Pt/Al electrodes, was defined by lithography, followed by the evaporation of a 60-nm thick aluminum (Al) gate electrode using a magnetron sputtering system. Finally, the devices were annealed in the vacuum at 300 °C for 100 s by a rapid thermal processing (RTP) system.

Electrical measurement

The electrical measurements were conducted using a dual-channel source meter unit (Keithley 2636B instrument) at room temperature in ambient air.

Simulation setup

The electrical behavior of FETs was simulated by using the Silvaco-TCAD simulator. All devices were configured with Ohmic contacts between the SiNWs and metal electrodes, and a gate-all-around (GAA) structure. For the NK-FET model, the SiNW channel consisted of a necked region with a diameter of 20 nm and a length of 100 nm, connected to two thick segments, each with a diameter of 45 nm and length of 200 nm. For the THK-FET and THN-FET models, SiNW channels with a diameter of 45 nm and 20 nm were used, respectively, with a consistent channel length of 500 nm. The simulation incorporated several physical models, including SRH, Fermi, and CVT.

Data availability

All data are available in the main text or the Supplementary Information.

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Author contributions

J.W. and L.Y. proposed and supervised the project. R.H. and L.Y. designed the experiments. L.W. performed the sample fabrication and device measurement. Z.H. and L.L. contributed to the data analysis. R.H., J.W. and L.Y. co-wrote the paper. All authors discussed the results and commented on the paper.

Competing interests

The authors declare no competing interests.

Additional information

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