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Controllable synthesis of nonlayered high-κ Mn_3O_4 single-crystal thin films for 2D electronics

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Two-dimensional (2D) materials have been identified as promising candidates for future electronic devices. However, high dielectric constant (κ) materials, which can be integrated with 2D semiconductors, are still rare. Here, we report a hydrate-assisted thinning chemical vapor deposition (CVD) technique to grow manganese oxide (Mn_3O_4) single crystal nanosheets, enabled by a strategy to minimize the substrate lattice mismatch and control the growth kinetics. The material demonstrated a dielectric constant up to 135, an equivalent oxide thickness (EOT) as low as 0.8 nm, and a breakdown field strength (E_{bd}) exceeding 10 MV/cm. MoS_2 field-effect transistors (FETs) integrated with Mn_3O_4 thin films through mechanical stacking method operate under low voltages (<1 V), achieving a near 10^8 I_{on}/I_{off} ratio and a subthreshold swing (SS) as low as 84 mV/dec. The MoS_2 FET exhibit nearly zero hysteresis (<2 mV/MV cm^{-1}) and a low drain-induced barrier lowering (~20 mV/V). This work further expands the family of 2D high-κ dielectric materials and provides a feasible exploration for the epitaxial growth of single-crystal thin films of non-layered materials.

Two-dimensional (2D) materials, with their atomic-level thin layers and unique electronic properties, have shown tremendous potential in surpassing the performance limitations of traditional silicon materials[1–3]. However, significant challenges remain in selecting and integrating high-κ materials to optimize the performance of 2D material-based field-effect transistors (FETs) and to further scale down device sizes[4]. Traditional high-κ insulating materials such as Al_2O_3, and HfO_2, despite being widely used in modern semiconductor processes, often introduce charge scattering and trap states due to their amorphous structures, negatively impacting the electronic transport characteristics of 2D FETs[5–7]. Therefore, the research community has started exploring high-κ single crystal materials with atomically smooth surfaces as gate dielectrics, aiming to improve the interface quality and enhance device performance[8]. Materials such as LaOCl ($\varepsilon_r \approx 10.8$)[9], $SrTiO_3$ ($\varepsilon_{max} \approx 105$)[10], Bi_2SiO_5 ($\varepsilon_r \approx 30$)[11], Bi_2GeO_5 ($\varepsilon_r \approx 40$)[12] and CaF_2 ($\varepsilon_r \approx 8.4$)[13] show significant potential by forming smoother dielectric/semiconductor interfaces compared to traditional amorphous dielectrics[9–11]. Transferring mechanically exfoliated ultrathin high-κ dielectrics, such as h-BN ($\varepsilon_r \approx 3.8$)[14], 2D perovskite oxide $Sr_2Nb_3O_{10}$ ($\varepsilon_r \approx 24.6$)[15], Bi_2SeO_5 ($\varepsilon_r \approx 15.6$)[16] and onto 2D materials has demonstrated its potential for damage-free integration to optimize the performance of 2D devices[10,17,18]. High-κ materials, due to their high dielectric constants, enable the use of thicker dielectric layers while preserving high capacitance. This effectively addresses the leakage current and reliability challenges posed by thinner dielectric layers.

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Recently, chemical vapor deposition (CVD) has emerged as a promising technology capable of directly growing high-quality 2D nanosheets on various substrates[19–21]. However, the challenge of further extending the growth of high-quality ultrathin dielectric single-crystal films remains[11]. This underscores the urgent need for high-κ, high-quality single-crystal films that can be controllably synthesized via CVD, which is crucial for the continuation of Moore's Law. Bulk Mn_3O_4, with its high static permittivity ($\varepsilon_{bulk} \approx 1703$ at room temperature), presents itself as a potential gate dielectric for electrostatic modulation of silicon, graphene, or 2D electron gases at complex oxide heterointerfaces[22]. Despite its potential, the controlled synthesis of ultrathin Mn_3O_4 films remains a significant challenge. Overcoming this obstacle is essential to leverage the advantages of high-κ materials in next-generation electronic devices.

In this work, by employing strategies of hydrate-assisted thinning and reducing substrate lattice mismatch, the single-oriented growth of non-layered ultrathin Mn_3O_4 on mica was successfully customized. The Mn_3O_4 single crystal nanosheets exhibit dielectric constants ε_r up to 135 and EOT as low as 0.8 nm, which are among the best obtained for 2D gate insulating materials. Compared to the more challenging thinning strategies required for existing high-κ ($\varepsilon_r < 100$) 2D gate dielectrics, the selection of higher-κ Mn_3O_4 offers a solution for integrating and optimizing FET performance and further miniaturizing device dimensions. Electrical performance tests further demonstrated the favorable properties of higher-κ Mn_3O_4 as a gate dielectric in MoS_2 FETs. These performance advantages stem from the atomically smooth surface of Mn_3O_4 single crystals, ensuring high compatibility with MoS_2 and clean vdW interface formation.

Results

Synthesis of high-quality ultrathin Mn_3O_4 arrays

Mn_3O_4 is a magnetic oxide known for its non-layered tetragonal spinel structure[23]. At room temperature, it adopts the stable tetragonal hausmannite structure with the I41/amd (141) space group. In this structure, Mn^{3+} and Mn^{2+} ions occupy octahedral and tetrahedral sites, respectively. As illustrated in Fig. 1a, ultrathin Mn_3O_4 exhibits a standard non-layered tetragonal crystal system structure (a = 5.762 Å, b = 5.762 Å, c = 9.439 Å, $\alpha = \beta = \gamma = 90°$) and presents a top view of the atomic hexagonal arrangement along the [111] zone axis.

Supplementary Fig. 1 depicts the experimental setup used to synthesize ultrathin Mn_3O_4 array single crystals on a mica ($KMg_3(AlSi_3O_{10})F_2$) substrate through CVD technique. In brief, NaCl and $MnCl_2{\cdot}4H_2O$ were utilized as precursors, and the growth process took place in an Ar gas atmosphere to facilitate the formation of the Mn_3O_4 array structure. Figure 1b displays the OM image of the resulting Mn_3O_4 arrays, showcasing uniform geometric morphologies. The consistent size and unidirectional arrangement of Mn_3O_4 domains highlight the precise control achieved in the synthesis process. To confirm the uniformity and phase purity of the ultrathin Mn_3O_4 arrays across different thicknesses, the Raman spectra presented in Fig. 1c validate the structural integrity of ultrathin Mn_3O_4. By using the characteristic peak of mica at 263 cm^{-1} for calibration, three significant Raman peaks corresponding to the hexagonal phase of Mn_3O_4 are observed, indicating the characteristic lattice vibration modes, which align with previous findings[24,25]. Specifically, the A_{1g} mode peak at 658 cm^{-1} signifies the Mn-O breathing vibrations of Mn^{2+} in tetrahedral coordination, while the two weak peaks at 317 cm^{-1} and 371 cm^{-1} are attributed to the T_{2g} mode of oxygen atom vibrations.

The high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image revealed the precise hexagonal geometry of the ultrathin Mn_3O_4 nanosheets, which exhibited exceptional crystal quality with uniformity at the atomic level (Fig. 1d). The lattice spacing measurement of 0.312 nm confirmed the presence of the (112) crystal plane (Fig. 1e). The selected area electron diffraction (SAED) pattern demonstrated favorable in-plane sixfold symmetry, confirming the high-quality single-crystal structure of the hexagonal

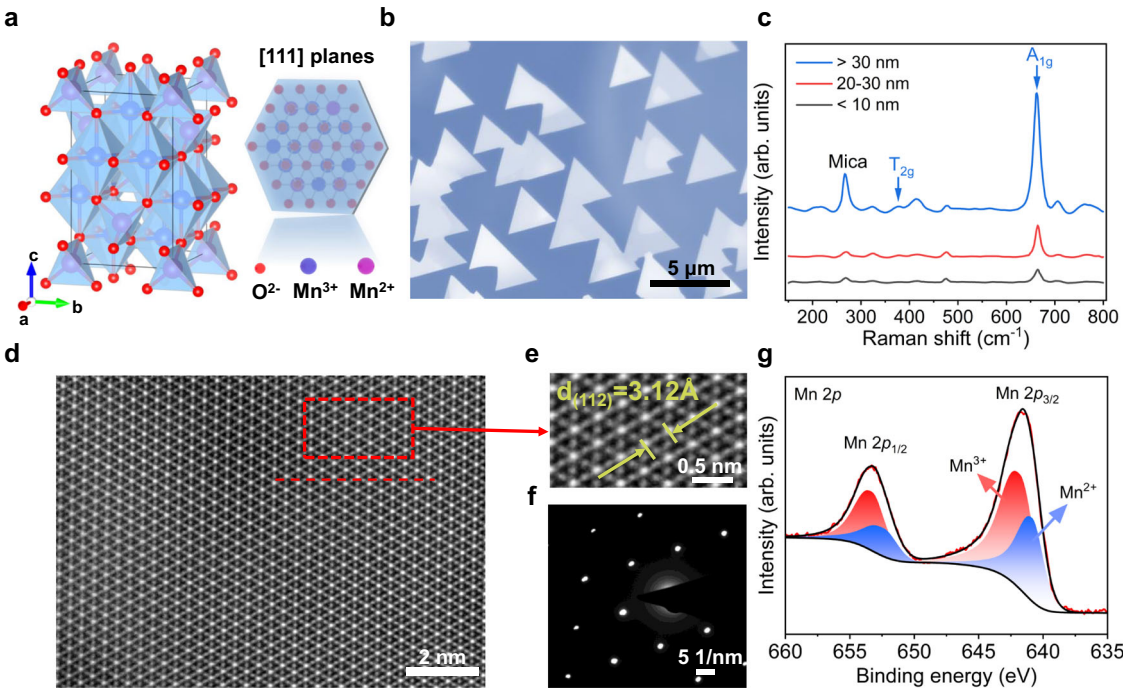

Fig. 1 | Structure and characterization of array-grown ultrathin Mn_3O_4 single crystals. a The crystal structure diagram of ultrathin Mn_3O_4 nanosheets. Blue sites represent Mn^{3+} atoms, purple sites represent Mn^{2+} atoms, and red sites represent O^{2-} atoms. Special attention is given to the blue hexagons representing the atomic arrangement corresponding to the projection plane along the [111] zone axis. **b** Optical micrograph (OM) image of array-grown ultrathin Mn_3O_4 nanosheets. **c** Typical Raman spectra of hexagonal ultrathin Mn_3O_4 nanosheets at various thicknesses. **d** High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of a hexagonal ultrathin Mn_3O_4 nanosheet. **e** The enlarged HAADF-STEM image along the red square in **d**. **f** Selected area electron diffraction (SAED) pattern of ultrathin Mn_3O_4. **g** X-ray photoelectron spectroscopy (XPS) characterization of the Mn 2*p* states in hexagonal ultrathin Mn_3O_4 nanosheets.

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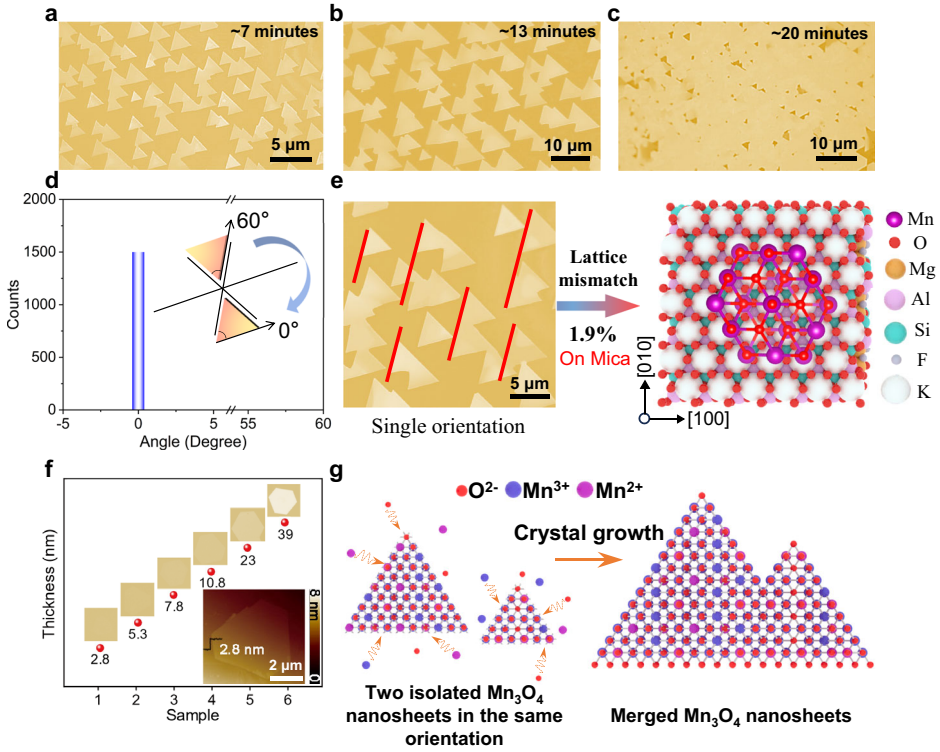

Fig. 2 | Array-grown and characterization of ultrathin Mn_3O_4 nanosheets. a-c OM images of ultrathin Mn_3O_4 nanosheets on mica for growth durations of ~7, ~13, and ~20 minutes, respectively. **d** Statistical analysis of the growth direction of ultrathin Mn_3O_4 nanosheets on mica along 0 degrees triangles. The illustration represents the growth orientation diagram of Mn_3O_4 nanosheets along 0° and 60°. **e** The growth mechanism of Mn_3O_4 nanosheets on mica, optical images of Mn_3O_4 grown on mica, and the lattice mismatch model demonstrate that the low lattice mismatch rate of 1.9% between the Mn_3O_4 nanostructure and mica leads to arrays growing in a single direction. The red line indicates the growth orientation of the Mn_3O_4 nanosheets. **f** OM image of ultrathin Mn_3O_4 nanosheets on mica showing thickness-dependent color contrast. The inset displays a typical AFM image of an ultrathin Mn_3O_4 nanosheet with a thickness of 2.8 nm (4 layers) and a smooth surface. **g** Schematic illustration of the coalescence mechanism of unidirectionally oriented ultrathin Mn_3O_4 nanosheets.

phase Mn_3O_4 (Fig. 1f). As shown in Supplementary Fig. 2, the energy dispersive X-ray spectroscopy (EDS) analysis exhibited a uniform distribution of Mn and O elements, highlighting the consistency of the chemical composition. Furthermore, EELS analysis provided detailed information on the electronic structure of the nanosheets, particularly the Mn L-edge and O K-edge spectra, which revealed distinct "white lines" corresponding to transitions of Mn ions and pre-edge structures consistent with previous data (Supplementary Fig. 3)[26–28]. The Mn X-ray photoelectron spectroscopy (XPS) analysis confirmed the presence of Mn $2p_{1/2}$ and Mn $2p_{3/2}$ spin-orbit states at 652.9 and 641.3 eV, respectively, corresponding to Mn^{2+} and Mn^{3+} valence states (Fig. 1g)[24,25,29]. The full spectrum analysis further supported the presence of these valence states (Supplementary Fig. 4).

Ultrathin Mn_3O_4 nanosheets show ferromagnetic behavior at low temperatures, transitioning from paramagnetic to ferrimagnetic states near 48 K, influenced by size and surface effects (Supplementary Fig. 5)[30]. These properties suggest potential applications in electronic and spintronic devices, advancing data storage, sensing, and spin manipulation technologies.

High-quality ultrathin Mn_3O_4 arrays

The oriented growth of 2D nanosheet arrays is of significant importance for the synthesis of single-crystal thin films[8,31,32]. On the single crystal substrate such as sapphire, wafer-scale growth of 2D transition metal dichalcogenides (such as MoS_2 and WS_2), has been achieved. This method relies on designing specific c/a ratios and sapphire planes to confine monolayer nucleation at the substrate step edges, thereby achieving unidirectional orientation and single-crystal growth[33,34]. Nonetheless, maintaining the orientation and height of sapphire step edges with high precision across a wafer scale remains a challenge[33].

We have developed a hydrate-assisted thinning CVD method. By pre-calculating the lattice mismatch between Mn_3O_4 and various substrates, including mica and sapphire, we found that Mn_3O_4 has the smallest lattice mismatch with mica (1.9%). This enabled the precise prediction of the synthesis of controllable ultrathin Mn_3O_4 nanosheet arrays on mica without any pretreatment of the mica substrate. The change in free energy for vertical growth (ΔE_{ver}) primarily arises from the binding forces at the upper interface subunits, while the loss in edge energy dominates lateral growth (ΔE_{lat}). Therefore, their difference (ΔE) can serve as a criterion for evaluating growth modes (Supplementary Fig. 6)[35]. In fact, besides the material itself, the surrounding microscale atomic environment may also influence these energies during real growth processes. When ΔE is negative, it favors lateral growth of the material. Additionally, interface adsorption or passivation can suppress vertical growth of the material. Choosing hydrates as precursors, water molecules adsorb on the material surface, lowering ΔE to promote the material's lateral growth. The transition of ultrathin Mn_3O_4 nanosheets from isolated islands to continuous films on a mica substrate has been demonstrated through a CVD growth strategy, revealing the microscopic mechanisms behind macroscopic orientation control of 2D materials (Fig. 2a-c, Supplementary Fig. 7). Notably, nearly 100% uniformly oriented ultrathin Mn_3O_4 triangular nanosheets were observed on the mica substrate, a stark contrast to the antiparallel orientations of previously reported 2D TMDCs grown on the same substrate[36,37]. This unique unidirectional alignment not only demonstrates the orientation selectivity of ultrathin Mn_3O_4 nanosheets during the crystal growth process but also highlights the strong interaction with the mica substrate. Further statistical analysis, as illustrated in Fig. 2d, validates the consistency of nanosheet orientation, attributed to the growth of ultrathin Mn_3O_4 nanosheets being

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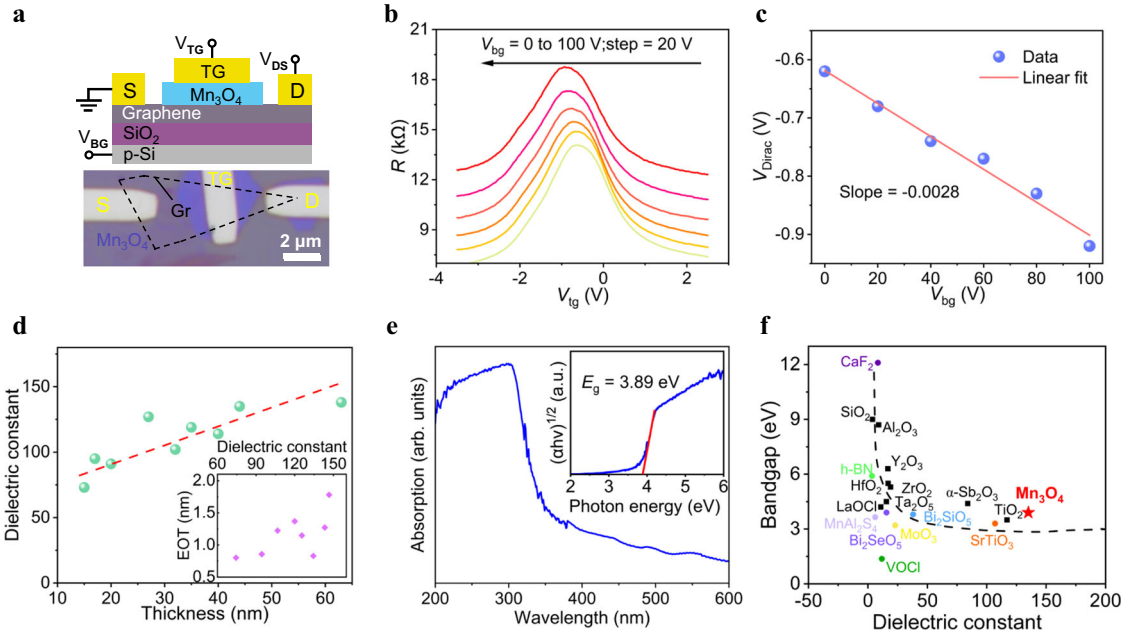

Fig. 3 | Dielectric performance of ultrathin Mn_3O_4 nanosheets. a Schematic and OM image of a dual-gate graphene (Gr) field-effect transistor (FET) with ultrathin Mn_3O_4 as the top gate dielectric on a SiO_2/p-type (Si/p-Si) substrate. S, D, and TG represent the source, drain, and top gate, respectively. **b** Total resistance of a typical dual-gate graphene FET as a function of back-gate voltage (V_{bg}) at different V_{tg} values. Source-drain voltage (V_{ds}) = 10 mV. **c** Relationship between the back gate Dirac point voltage of the Gr FET and V_{bg}. The slope of the linear fit represented by the red solid line is -0.0028. **d** Thickness dependence of Mn_3O_4 dielectric constant measured by dual-gate Gr FET and metal-insulator-metal (MIM) devices at 1 kHz. The inset shows the dielectric constant dependence on equivalent oxide thickness (EOT). The red dashed line indicates the fitting curve of dielectric constants at different thicknesses. **e** Ultraviolet-visible (UV) absorption spectrum of ultrathin Mn_3O_4. Inset: Corresponding Tauc plot, indicating the optical bandgap (E_g) of ultrathin Mn_3O_4. α, h, and ν respectively represent the absorption coefficient, Planck's constant, and photon frequency. **f** Comparison of the bandgap and dielectric constant of ultrathin Mn_3O_4 with devices employing other gate dielectrics[6,8–10,13,16,45,50–55].

influenced by a dual-coupling guided mechanism[38]. Initially, the interaction between Mn_3O_4 and the substrate induces epitaxial growth. Subsequently, the interaction between nanosheets determines the preferential growth in a single direction. As shown in Fig. 2e and Supplementary Fig. 8, the lattice constant of mica ($a_1 \approx 5.3$ Å) equals $\sqrt{3}a_2$ of Mn_3O_4 ($a_2 \approx 3.12$ Å), with a mismatch rate of 1.9%. The lattice constant of sapphire ($a_3 \approx 4.81$ Å) equals 1.5 a_2 of Mn_3O_4 ($a_2 \approx 3.12$ Å), with a mismatch rate of 3.3%. This low lattice matching achieves strong interaction between mica and Mn_3O_4, inducing the epitaxial growth of ultrathin Mn_3O_4.

The surface roughness of ultrathin Mn_3O_4 nanosheets of different thicknesses grown on the same mica piece has been measured, and their flatness is confirmed by the root mean square roughness (R_q) of 0.13 nm and the height profile shown in Supplementary Fig. 9 Mn_3O_4 synthesized via CVD exhibits outstanding air stability. Even after being exposed to air for over a year, its surface morphology remains nearly unchanged, which is critical for the fabrication of devices using high-κ gate dielectrics (Supplementary Fig. 10). The reduction of surface defects in dielectric materials significantly improves the performance of 2D semiconductor electronic devices. By precisely controlling the growth conditions of CVD, ultrathin Mn_3O_4 single crystals of various thicknesses can be obtained, as shown in Fig. 2f. At a relatively suitable growth temperature (923 K), ultrathin Mn_3O_4 nanosheets demonstrating controllable atomic thinness down to 2.8 nm are presented. Figure 2g shows a schematic illustration of the fusion of two isolated single crystals. Supplementary Fig. 11 shows the atomic resolution TEM image collected from the merged region of two adjacent Mn_3O_4 nanosheets, and an ideal atomic stitching is clearly observed. As shown in Supplementary Fig. 12 presents AFM images of ultrathin Mn_3O_4 nanosheet arrays grown at different times, and the height profile further demonstrates the thickness consistency among different islands on the same mica (all around 11.2 nm), providing a feasible solution for synthesizing reliable and uniform non-layered ultrathin single-crystal films.

Dielectric properties of ultrathin Mn_3O_4 single crystals

To further explore the potential of ultrathin Mn_3O_4 as a dielectric material in sophisticated electronic devices, a graphene dual-gate FET is utilized to measure the dielectric properties. This evaluation method has been validated in previous studies, effectively measuring the dielectric capabilities of materials[15,39]. For the convenience of transferring and fabricating individual devices, we have selected only sparsely distributed independent monocrystalline nanosheets for transfer. In the experiment, the graphene channel was strictly limited to a single layer to ensure effective coupling between the top and back gates. The thickness of the graphene was characterized using Raman spectroscopy, as shown in Supplementary Fig. 13b. In Fig. 3a, a dual-gate graphene FET is fabricated by integrating monolayer graphene with ultrathin Mn_3O_4 nanosheets (~15 nm), employing advanced transfer techniques. In this article, ultrathin Mn_3O_4 and 285 nm SiO_2 function as the dielectric layers for the top and back gates, respectively, with the device channel spanning 2.5 μm in width. This configuration facilitates independent modulation of channel carriers via separate adjustments of top and back gate voltages (V_{tg} and V_{bg}). The R-V_{tg} characteristics exhibits the graphene channel's bipolar conductivity under back gate voltage modulation in Fig. 3b. The alteration in the Dirac point voltage signifies shifts in the charge neutrality point, illustrating the capability of back gate voltage adjustments to effectively modulate the channel charge[40]. The observation of a minor shift in the top gate voltage corresponding to the graphene Dirac point is attributed to the competing capacitance effects arising from simultaneous voltage applications to both the ultrathin Mn_3O_4 top gate and SiO_2 back gate dielectrics. The back-gate V_{Dirac} shows a linear dependence on the V_{tg} (Fig. 3c). This relationship hinges on the

capacitance ratio of the top gate to the back gate (C_{TG}/C_{BG}), encapsulated in the following formula:

$$-\frac{\Delta V_{TG}}{\Delta V_{Dirac,\,BG}} = \frac{C_{BG}}{C_{TG}} = \frac{\varepsilon_{SiO_2} t_{Mn_3O_4}}{\varepsilon_{Mn_3O_4} t_{SiO_2}} \quad (1)$$

where C, ε, and t stand for capacitance, effective dielectric constant, and thickness of Mn_3O_4, respectively. Given the characteristics of the back gate dielectric SiO_2—C_{BG} at 11.6 nF cm^{-2}, ε_{SiO_2} at 3.9, and thickness at 285 nm—the dielectric constant for 15 nm Mn_3O_4 calculates to 73. To precisely determine the effective dielectric constant of Mn_3O_4, we systematically analyzed ultra-thin Mn_3O_4 nanosheets with thicknesses ranging from 15 to 40 nm, as shown in Supplementary Fig. S13. The peak dielectric constant for the 35 nm Mn_3O_4 sample was measured to be 119. To further enhance measurement accuracy, we fabricated MIM capacitors (Supplementary Fig. S14a) and extracted dielectric constants for Mn_3O_4 (17-63 nm) via C-V measurements. The 44 nm Mn_3O_4 showed a dielectric constant of ~135 at 1 kHz. This result aligns with dual-gate FET measurements, confirming the reliability of the data.

As shown in Fig. 3d, the effective dielectric constants for Mn_3O_4 with different thicknesses were extracted from both dual-gate FET and MIM devices. A decline in the dielectric constant with reduced Mn_3O_4 nanosheet thickness aligns with trends observed in other 2D dielectrics. Such behavior is convincingly explained by the interface effects in nanoscale dielectric layers, particularly where the interface capacitance (C_i) at the electrode/dielectric interfaces manifests a dielectric constant lower than the material's intrinsic bulk value, a phenomenon known as the "dead layer" effect[41,42]. These "dead layers" act as additional series capacitors, reducing the overall dielectric constant relative to bulk material values. In alignment with the International Roadmap for Devices and Systems (IRDS)[43], which stipulates that the most cutting-edge MOSFETs (5 nm node FinFET) necessitate an EOT below 1 nm, the findings illustrated in the inset of Fig. 3d reveal that Mn_3O_4 thicknesses below 30 nm meet this EOT criterion, with the EOT for 15 nm thick nanosheets dropping to as low as 0.8 nm. As shown in Supplementary Fig. 15, a dual-gate MoS_2 FET was fabricated to further confirm the high dielectric constant of 149 for the 48 nm Mn_3O_4.

Beyond the dielectric constant, parameters such as optical band gap, leakage current density, and breakdown field strength are critical in high-κ dielectric materials research[44]. The optical band gap of ultrathin Mn_3O_4 nanosheets was accurately determined through UV absorption spectroscopy, which revealed a pronounced absorption edge at a wavelength of approximately 300 nm (Fig. 3e). Analysis utilizing the Tauc plot method yielded an optical band gap of 3.89 eV (inset of Fig. 3e). This is close to the theoretically calculated band gap of 4.21 eV (Supplementary Fig. 16).Additionally, the band gap was corroborated by examining the low-loss region in the electron energy loss spectrum (EELS) of ultrathin Mn_3O_4 crystals, affirming a value of approximately 3.9 eV as shown in Supplementary Fig. 17. The leakage current characteristics of a metal/Mn_3O_4/graphene dual-gate structure under operational voltages, revealing an exceptionally low leakage current of 10^{-14} A, equating to a current density of approximately 10^{-7} A/cm^2 (Supplementary Fig. 18). These findings emphasize the high insulating performance of ultrathin Mn_3O_4, attributed to its wide band gap.

Comparative optical imaging conducted before and after the breakdown of devices with disparate thicknesses substantiated the electrical stability of the ultrathin Mn_3O_4 nanosheets, which demonstrated E_{bd} exceeding 13.2 MV/cm (Supplementary Fig. 19, Supplementary Fig. 20). This performance aligns with the benchmarks set by the IRDS for breakdown field strength (>10 MV/cm)[45]. Remarkably, for 66 nm Mn_3O_4 nanosheets, an increase in voltage leads to a significant escalation in leakage current to the μA range. Despite this, no breakdown-induced short circuiting or current disorder was observed, with the E_{bd} consistently maintained at 9.5 MV/cm. (Supplementary Fig. 19d). This resilience is ascribed to the high dielectric constant of ultrathin Mn_3O_4. As shown in Supplementary Fig. 21, the large E_{bd} (13.2 MV/cm) and low EOT (0.8 nm). It is one of the best-performing advanced dielectric materials available. As shown in Fig. 3f, ultrathin Mn_3O_4 is a material with a suitable wide bandgap and a high dielectric constant. The dielectric constant of ultrathin Mn_3O_4 is 135, which is comparable to that of favorable high-κ non-layered oxides and complex oxides (exemplified by $SrTiO_3$ with $\varepsilon_r \approx 105$ and TiO_2 with $\varepsilon_r \approx 117$). It provides an important physical foundation for further scaling of micro and nanoscale devices and for providing a stable dielectric environment.

High performance of MoS_2 FET with Mn_3O_4 dielectric

The high dielectric constant and atomically flat surface of ultrathin Mn_3O_4 nanosheets suggest their significant potential for integration with 2D semiconductor devices. Few-layer MoS_2 was prepared on the SiO_2/Si substrate through mechanical exfoliation to construct Mn_3O_4/MoS_2 top gate FETs. Reportedly, vdW gaps effectively prevent carrier tunneling, significantly reducing gate leakage current[10,15,18]. This feature stems from the chemical inertness and lack of dangling bonds on vdW material surfaces, allowing stable and definitive vdW interfaces with two-dimensional materials[46]. As shown in Fig. 4a, observation of the cross-section with TEM confirmed the existence of an accurate vdW gap of approximately 5.6 Å between Mn_3O_4 and MoS_2. This clear interface ensures no interface disorder above the MoS_2 channel, with the ultrathin Mn_3O_4 gate dielectric forming an ideal coupling. Furthermore, EDS analysis revealed a high degree of uniformity in the elemental distribution at the interface, proving the formation of a high-quality vdW interface between Mn_3O_4 and MoS_2. This discovery not only highlights the potential of using Mn_3O_4 as a top gate dielectric in optimizing the performance of 2D FETs but also provides an essential physical basis for designing 2D electronic devices with low leakage current and high stability. Mn_3O_4/MoS_2 top-gate FET was fabricated on a SiO_2/Si substrate, as shown in Fig. 4b, where the SiO_2/Si also served as the back gate dielectric and electrode roles when necessary. Through I_{ds}-V_{tg} characteristic curve measurements conducted at various V_{ds}, as shown in Fig. 4c, the favorable gate control capability of 22.9 nm Mn_3O_4 as a gate dielectric for MoS_2 FETs was demonstrated, achieving an I_{on}/I_{off} ratio of nearly 10^8 at operational voltages from −0.8 V to −0.2 V. Supplementary Table 1 provides a detailed comparison of various key performance parameters of FETs using Mn_3O_4 and other materials as gate dielectrics. To demonstrate the reliability and scalable potential of the electrical performance, the Mn_3O_4 top-gate FET array consists of 15 independent devices, fabricated based on monolayer MoS_2 films that were grown on a glass substrate by CVD. Raman spectroscopy was used to characterize the typical monolayer MoS_2 features (Supplementary Fig. 22). Supplementary Fig. 24a and b show the optical images of the array FET devices. Further electrical statistics indicate that all devices achieve steep subthreshold slopes (Supplementary Fig. 24c). The on/off ratios and field-effect mobilities follow a Gaussian distribution, with average values of 5×10^6 and 24.6 cm^2 V^{-1} s^{-1}.

Further electrical performance analysis showed a linear I_{ds}-V_{ds} relationship in the low V_{ds} region and gradual saturation in the high V_{ds} region for the MoS_2 transistor, indicating good ohmic contact performance and sufficient gate modulation effect (Fig. 4d). During both forward and reverse top-gate scans, for different orders of magnitude of I_{ds}, the SS remained below 100 mV/dec (Fig. 4e), highlighting the efficient dielectric modulation capability of ultrathin Mn_3O_4. Furthermore, the extremely low gate leakage current (10^{-14} A) (Fig. 4f), equivalent to a current density of 10^{-7} A/cm^2, corresponds to near the detection limit of the measurement system, significantly below the low-power limit value (10^{-2} A/cm^2), demonstrating tremendous application potential in MOSFETs[47]. The low normalized hysteresis of <2 mV/MV cm^{-1} at a sweep rate of 5 mV/s and the low DIBL of approximately 20 mV/V further confirm the formation of a high-quality

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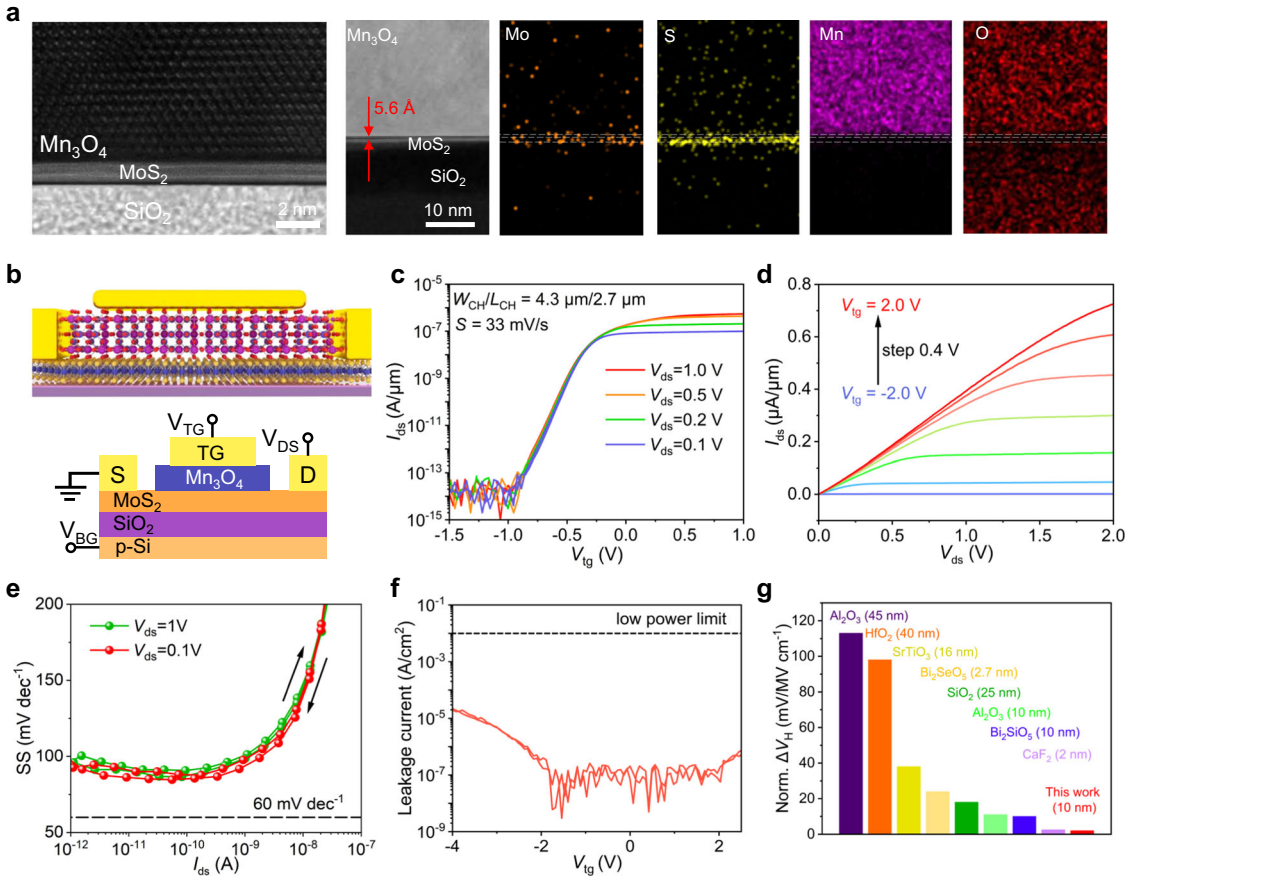

Fig. 4 | Local top-gated MoS_2 FET with high-κ Mn_3O_4 dielectric. a Cross-sectional TEM image and elemental distribution of the Mn_3O_4/MoS_2. **b** Schematic of the top-gated MoS_2 FET on a SiO_2/Si substrate, with ultrathin Mn_3O_4 serving as the top gate dielectric. **c** Transfer characteristics curves of few-layer MoS_2 field-effect transistors at different V_{tg}, exhibiting a steep subthreshold slope. The channel width (W_{ch}) to channel length (L_{ch}) ratio is 4.3 μm / 2.7 μm. The step size (S) is 33 mV/s. **d** Output characteristics (I_{ds}-V_{ds}) of the same device. **e** Relationship between the subthreshold swing extracted from (**c**) and the I_{ds}. **f** Leakage current versus applied voltage relationship at V_{ds} = 1 V for the same device. **g** Comparison of normalized hysteresis in our devices with other reports in the literature[6,10,11,13,16].

vdW interface between Mn_3O_4 and MoS_2 (Fig. 4g, Supplementary Figs. 25-27)[48]. These measurement results not only highlight the high efficiency and low power consumption characteristics of the device but also confirm the effectiveness of Mn_3O_4 as a top gate dielectric in improving interface quality and overall device performance.

A high-κ dielectric environment is commonly believed to enhance MoS_2 mobility by reducing charged impurity scattering and providing effective encapsulation[49]. In our experiments, we employed a rigorous design where the bottom SiO_2 was consistently used as the back-gate dielectric to ensure channel control uniformity. As shown in Fig. 5a, the only variable was the presence of the Mn_3O_4 encapsulation, thus increasing the reliability and comparability of our data. At 300 K, we measured the V_{bg}-dependent two-probe I_{ds}-V_{ds} curves (Fig. 5b). The output characteristics showed linear behavior over a wide voltage window, confirming ohmic contact formed by Cr/Au electrodes. Notably, the Mn_3O_4-encapsulated MoS_2 device demonstrated an on-current approximately three times that of the unencapsulated device, preliminarily indicating that the encapsulation significantly enhanced electronic transport. To further understand the influence of encapsulation on mobility, we conducted temperature-dependent I_{ds}-V_{bg} measurements from 80 to 300 K, as shown in Fig. 5c. These measurements enabled us to extract the mobility versus temperature for the encapsulated and unencapsulated FETs (Fig. 5d). The results demonstrated that across all temperature ranges, the mobility of Mn_3O_4-encapsulated devices was consistently higher than that of unencapsulated devices. This enhancement can be attributed to the effective shielding provided by the Mn_3O_4 top layer, particularly in mitigating Coulomb impurity scattering, thereby improving the carrier mobility. Supplementary Fig. 28 and Supplementary Table 2 further confirmed the generality of this trend through multiple sample testing. The results showed that Mn_3O_4-encapsulated devices consistently outperformed their unencapsulated counterparts at 300 K, demonstrating a consistent mobility advantage. Overall, we validated that the top encapsulation of Mn_3O_4, a high-κ material, significantly enhanced device mobility without directly controlling the channel dielectric. This allowed the encapsulation layer to act purely as an environmental shield, providing a clearer demonstration of the effect of encapsulation on improving electrical performance. Correctly utilizing high-quality monocrystals and 2D materials to construct vdW interfaces is crucial for optimizing device performance.

Discussion

In summary, this study achieved the growth of ultrathin Mn_3O_4 nanosheet arrays through CVD. Through a hydrate-assisted thinning strategy and the calculation of low lattice mismatch between single-crystal Mn_3O_4 and various substrates, Mn_3O_4 achieved tunable growth from single orientation to thin films on mica. Mn_3O_4 nanosheets exhibit a high dielectric constant of 135 (at 44 nm), making them one of the outstanding gate dielectric materials discovered to date, while maintaining favorable gate modulation and *h*-BN-like encapsulation capabilities. This work opens promising avenues for the fabrication of next-generation highly integrated, high-performance 2D transistors.

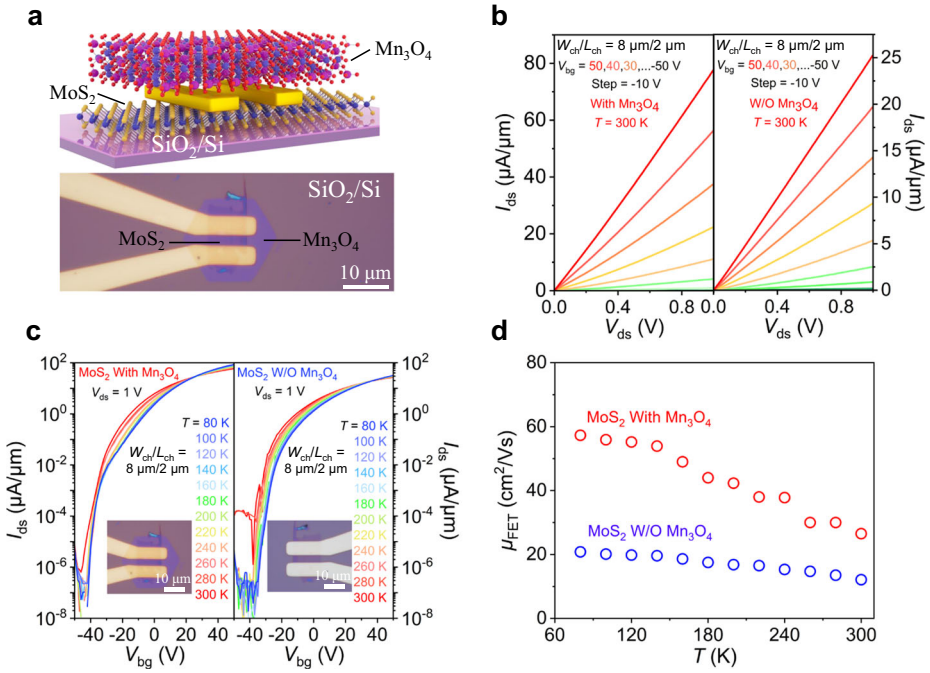

Fig. 5 | Encapsulation and mobility enhancement studies of MoS_2 double-probe FETs using high-κ Mn_3O_4 as top encapsulation layer. a Schematic illustration and optical microscopy image of the MoS_2/Mn_3O_4 double-probe FET device. **b** Comparison of linear output characteristics (I_{ds}–V_{ds}) of the MoS_2 double-probe FET encapsulated with Mn_3O_4 (left) and without Mn_3O_4 encapsulation (right) at 300 K. **c** Transfer characteristics (I_{ds}–V_{bg}) of the MoS_2 double-probe FET measured at different temperatures (80-300 K), comparing the device with Mn_3O_4 encapsulation (left) and without (right). The illustrations are OM images before encapsulation (right) and after encapsulation (left). **d** Extracted temperature-dependent mobility (μ_{FET}), comparing the device performance with and without Mn_3O_4 encapsulation.

Methods

Synthesis and transfer of Mn_3O_4 nanosheet arrays

Within a 2-inch diameter quartz tube, ultrathin Mn_3O_4 nanosheet films were successfully prepared on mica substrates using in situ atmospheric pressure chemical vapor deposition (APCVD) technology. Pure KCl (Aladdin, 99.9%) and $MnCl_2{\cdot}4H_2O$ (Aladdin, 99.9%) were used as the solvent and reactant, placed at the core of the heating zone. The substrate material, freshly cleaved fluorphlogopite mica [$KMg_3(AlSi_3O_{10})F_2$], was positioned above the mixture. Prior to the reaction, the furnace was purged with argon gas at a flow rate of 200 sccm for 15 minutes to remove residual gases. During the growth process, argon gas was used as the carrier gas at a flow rate of 50 sccm. The temperature was ramped up to 660 °C and maintained for 10 minutes to allow for the growth of the nanosheet arrays. After growth, the system was naturally cooled to room temperature, resulting in high-quality Mn_3O_4 nanosheet arrays on the mica substrate. To transfer the grown nanosheets onto the target substrate, a polystyrene (PS) assisted transfer method was employed, as shown in Supplementary Fig. 29. Firstly, 10 grams of PS pellets were dissolved in 200 mL of toluene, and then this solution was evenly spin-coated on the Mn_3O_4 nanosheets/mica and cured on a hot plate at 80 °C for 5 minutes. Subsequently, the PS film deposited with Mn_3O_4 was carefully lifted in deionized water and transferred to a clean SiO_2/Si wafer. Finally, after air drying at room temperature for 10 minutes, the PS layer was removed by treating with toluene for 5 minutes, completing the transfer of the nanosheets.

Material characterization

The morphology and thickness characteristics of the two-dimensional nanosheets were finely observed using an optical microscope (Nikon instrument ECLIPSE LV150N) and an atomic force microscope (Bruker Dimension Icon). Furthermore, Raman spectroscopy of the Mn_3O_4 nanosheets was conducted at room temperature using a micro-Raman spectrometer (LabRAM HORIBA) equipped with a 532 nm laser source. Chemical composition and elemental analysis were performed using X-ray photoelectron spectroscopy and ultraviolet photoelectron spectroscopy (250Xi ESCALAB). The bandgap of Mn_3O_4 was characterized using a micro-ultraviolet-visible absorption spectrometer (Mstarter ABS). The atomic structure and elemental composition were characterized using a field-emission transmission electron microscope (JEM-F200, EELS). Magnetic measurements were conducted using a physical property measurement system and a vibrating sample magnetometer (PPMS-9T and VSM, Quantum Design).

First-principles calculations

All calculations were based on DFT, executed by Vienna Ab-initio Simulation Package (VASP). The whole three-dimensional (3D) periodic models were constructed by Materials Studio (MS). The Perdew-Burke-Ernzerhof (PBE) of generalized gradient approximation (GGA) was used to describe the exchange-correlation effect. The core interactions were treated using the pseudo-potential of projector-augmented-wave (PAW) method. In the study, the cutoff of 500 eV, 3 x 3 x 1 (Mn_3O_4) k-points for entire geometry calculation. All the geometry structures and atomic positions were fully relaxed by a conjugate gradient (CG) method with convergence criteria of −0.01 eV/Å, and 10^{-5} eV/atom for force and energy, respectively.

Array device fabrication

First, large-area monolayer MoS_2 is grown on glass using chemical vapor deposition (CVD) and transferred onto a SiO_2/Si substrate using a wet transfer method. Then, ion beam etching (IBE) is used to pattern the MoS_2, and Cr/Au contact electrodes are deposited using electron beam lithography (Raith) and electron beam evaporation. Next, the grown Mn_3O_4 monolayer nanosheets are transferred onto the MoS_2 using a wet transfer method with PDMS alignment. Finally, the gate

electrodes are patterned and metal electrodes are deposited (see Supplementary Fig. 23).

Device fabrication and testing

Bulk MoS_2 crystals were dispersed on blue tape, and then the dispersed MoS_2 crystals on blue tape were pressed gently against PDMS. After slowly separating PDMS and blue tape, the thin layers of two-dimensional MoS_2 were peeled off onto PDMS. The MoS_2 was then transferred to a SiO_2/Si substrate using a dry transfer platform for two-dimensional materials, and the grown Mn_3O_4 nanosheets were wet transferred onto MoS_2. All devices were defined using electron beam lithography (Raith) for electrode patterning, and Cr/Au (10/50 nm) contact electrodes were deposited on the SiO_2/Si substrate using electron beam evaporation. Electrical measurements were performed at room temperature in a vacuum probe station coupled with a semiconductor parameter analyzer (Agilent 4155B). The MIM devices were tested using the Keithley 4200-SCS Semiconductor Characterization System, known for its high measurement speed and accuracy. This system integrates four SMU channels, with two channels equipped with preamplifiers that enable measurements of current as low as 10 pA and voltage down to 1 μV. Additionally, it features a CV measurement module that supports AC impedance testing across frequencies from 1 kHz to 10 MHz, covering a capacitance range from aF to μF. The system's graphical interface allows comprehensive testing without programming.

Data availability

All raw data generated during the current study are available from the corresponding authors upon request. Source data are provided with this paper.

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Author contributions

W.L. conceived the original idea and supervised the entire project. J.Y., with the assistance of C.J., Y.Y., B.W., Y.L., Z.F., M.L., and X.H., carried out CVD growth, characterization, device fabrication, and electrical measurements. J.Y., assisted by C.J., performed part of the TEM characterization and contributed to the preparation of some figures. Z.S., under the supervision of R.W. and W.H., conducted the theoretical calculations. J.Y., with input from other authors, drafted the manuscript. Q.C. co-supervised the entire project and provided constructive suggestions. All authors participated in scientific discussions.

Competing interests

The authors declare no competing interest.

Additional information

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