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Sacrifice-layer-free transfer of wafer-scale atomic-layer-deposited dielectrics and full-device stacks for two-dimensional electronics

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Transfer printing techniques have enabled the fabrication of devices on soft or delicate substrates that are incompatible with conventional manufacturing processes. However, the involved sacrifice-layer removal process typically causes damage to the quality of device interfaces. Here, we develop a sacrifice-layer-free transfer printing strategy by pre-depositing the device constituents onto commercially available mica substrates. The intrinsic weak interfacial interaction enables the transfer of various pre-deposited device constituents at the wafer scale, including well-known strongly adhesive dielectrics grown by atomic layer deposition (ALD). Moreover, entire top-gated device stacks can be simultaneously transferred onto few-layer MoS_2 to form fully gated two-dimensional (2D) transistors, showing an atomically sharp interface, negligible gate hysteresis (~5 mV) and subthreshold swings near the thermionic limit. Importantly, the conformal growth of ALD dielectrics enables the one-step fabrication of complex top-gated Hall devices with a fully encapsulated structure, allowing multi-terminal gate-tunable transport measurements on fragile 2D materials, such as black phosphorus. Our work not only enriches the transfer printing methodologies for difficult-to-transfer materials, but also provides a method to investigate the properties of fragile 2D materials.

Transfer printing is a widely used assembly technique for device fabrication and heterostructure construction in soft electronics[1–5] and low-dimensional physics[6–12]. Comparatively, transfer printing technique can loosen the constraints of processing compatibility in terms of thermal stability, chemical tolerance, and deposition damage, thus allowing the fabrication of devices on flexible or delicate substrates that are incompatible with conventional manufacturing processes[13–15]. Typically, the transfer printing process includes three steps: (1) pre-pattern the device constituents on a rigid substrate; (2) pick up the pre-patterned objects from the mother substrate; (3) release these objects to a receiver substrate. Generally, the pick-up process is the key step determining the fabrication yields of transfer printing[16–18]. However, owing to strong interfacial adhesion, it usually requires an additional sacrificial layer on top of the mother substrate to make all the device constituents transferrable[19,20]. Besides, the sacrificial layer is typically removed by another destructive step, such as O_2 plasma and chemical etching, which will inevitably increase the processing complexity and cause damage to the quality of device interfaces. Therefore, it is highly appealing to develop a sacrifice-layer-free approach for damage-free

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transfer printing of electronic materials, especially for those with strong adhesions with rigid substrates.

As we know, the metal electrode and atomic-layer-deposited (ALD) dielectric are two of the most important device constituents to fabricate top-gated transistors[21–23]. Thus, the prerequisite for successful transfer printing is to simultaneously transfer and delaminate the metal electrodes and ALD dielectrics from the mother substrate. With great efforts by scientists, sacrifice-layer-free transfer printing of metal contacts can be achieved by surface engineering such as hexamethyldisilazane treatments[24,25], graphene passivation[26,27], precise stress control[1,28], and using specific substrates[29,30]. On the other hand, ALD dielectrics, such as Al_2O_3 and HfO_2, play an indispensably important role in modern electronic industry, for their conformal growth characteristic, precise film thickness control, and remarkable deposition reproducibility[31]. In general, the ALD process involves a long-time H_2O and heat treatment, thus making the ALD process incompatible with fragile two-dimensional (2D) materials. Besides, the as-deposited Al_2O_3 and HfO_2 bond tightly with the ordinary epi-substrates, such as SiO_2/Si substrate, which typically requires precise substrate engineering to make the ALD dielectrics detachable from the mother substrate[31–34]. However, the widely used approaches for substrate modifications, such as graphene and self-assembled molecular layer[35,36], cannot support direct ALD deposition and thus require pre-deposition of seed layers (e.g., thermally evaporated AlO_x or SiO_2) to enable subsequent ALD processes and dielectric transfer. Up to now, the wafer-scale damage-free transfer of pristine ALD dielectrics on a commercial-available substrate without a sacrificial layer or seed layer has not been achieved yet.

Here, we report a damage-free approach to transfer wafer-scale ALD dielectrics, contact electrodes, and the entire top-gated stack on commercial-available mica substrates. Owing to mica's specific layered structure, the ALD dielectrics can uniformly nucleate and form a well-defined van der Waals (vdW) gap on mica substrate. This feature greatly reduces the interfacial interactions and thus makes the ALD dielectrics transferrable on mica without any sacrificial layer. Consequently, fully encapsulated top-gated MoS_2 transistor with perfect interfaces can be faithfully fabricated by one-step vdW integration, which can simultaneously avoid the well-known deposition-damage issues and ALD-incompatible problems with 2D semiconductors. The as-transferred MoS_2 transistor exhibited an atomically sharp interface, ignorable gate hysteresis (~5 mV) and large on-state current. More importantly, taking advantage of the conformal growth of ALD dielectrics, fully encapsulated top-gated Hall devices with a complex device configuration were successfully fabricated to investigate the intrinsic properties of air-sensitive 2D materials. With this method, gate-tunable electrical transport measurements were successfully performed on a few-layer delicate black phosphorus (BP), showing a merely unchanged high room-temperature Hall mobility of 703 cm^2V^{-1} s^{-1} after exposure to air for a week.

Results

Weak interfacial interaction between ALD-oxides and mica substrate

To make the ALD dielectrics transferrable, the key is to reduce the interfacial adhesion between ALD dielectrics and substrates. Here, we chose the mica substrate as the supporting layer for ALD-dielectric deposition and subsequent transfer due to the following reasons. First, mica is a kind of commercial-available substrate with a graphite-like atomically flat surface[29,37]. As we know, surface roughness is a key factor for the template-stripping transfer[36,38], since the peeled-off structure and subsequent stacked heterojunction will take on the substrate's roughness. Second, mica has a unique ALD-compatible non-neutral layered structure, which is totally different from ALD-incompatible inert surfaces of traditional vdW layered materials (such as graphene and MoS_2)[39]. As illustrated in Fig. 1a, the ALD precursors can uniformly nucleate on the mica substrate and form a continuous Al_2O_3 or HfO_2 film on top. More importantly, we found an unexpectedly large vdW gap of ~0.5 nm in the interface between the ALD-oxide and mica substrate, as evidenced by the cross-sectional TEM imaging on the Al_2O_3/mica (Fig. 1b and Supplementary Fig. 1) and HfO_2/mica (Fig. 1c) stacks. Compared to traditional interfaces with strong chemical bonds, the vdW gap in the ALD-oxide/mica interface will undoubtedly weaken its interfacial adhesion, thus facilitating the detachment and peel-off from the mica substrate. Thereafter, we designed a simple

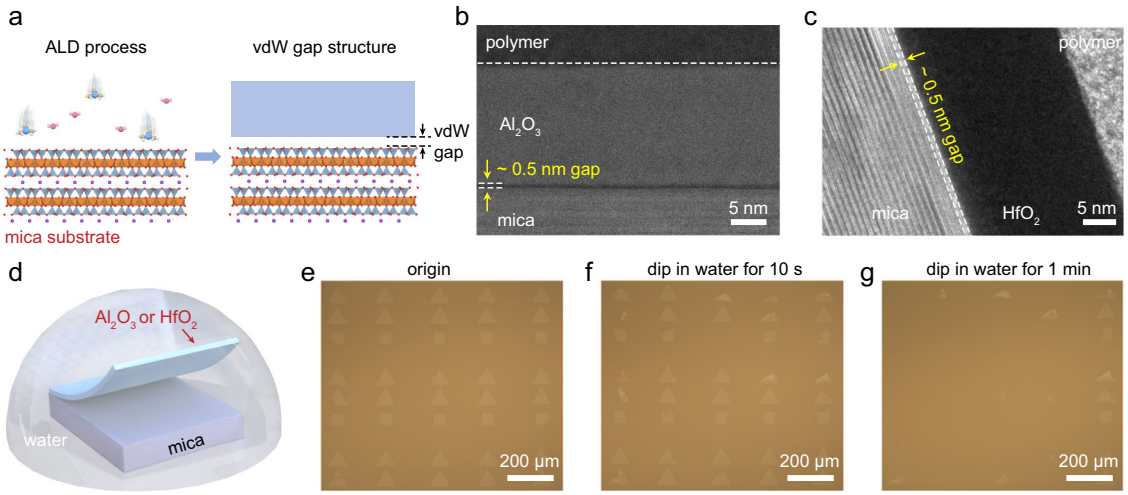

Fig. 1 | Weak interfacial interaction between atomic-layer-deposited (ALD) oxides and mica substrate. a Schematic diagram of the ALD process and the formation of a well-defined van der Waals (vdW) gap between ALD-oxides and mica substrate. **b** Cross-sectional high angle annular dark field (HAADF) image of the ALD-grown Al_2O_3 film and mica substrate, showing an atomically sharp interface and clear vdW gap of ~0.5 nm. **c** Cross-sectional bright-field transmission electron microscope (TEM) image of ALD-grown HfO_2 film and mica substrate, showing a clear vdW gap of ~0.5 nm. **d** Schematic illustration of natural peel-off of ALD-grown Al_2O_3 or HfO_2 from mica substrate in water due to the water intercalation into the vdW gap. **e**–**g** Typical optical microscope (OM) images of lithography-patterned Al_2O_3/HfO_2 (5 nm/15 nm) on mica (**e**), and corresponding OM images of the one immersed in water for 10 s (**f**), and 1 min (**g**). The apparent peel-off after a short-time water immersion confirms the weak adhesion between ALD-oxides and mica substrate. The growth of HfO_2 film on Al_2O_3 film was performed to increase the visibility of the films on transparent mica substrates.

experiment to check whether the ALD-oxide on mica can be easily peeled off (Fig. 1d). It's well-known that mica has a super-hydrophilic surface, which is beneficial for the water to intercalate into the vdW gap. As depicted in Fig. 1e–g, the ALD-grown Al_2O_3/HfO_2 patterns (5 nm/15 nm) kept their morphologies unchanged on the mica surface after lift-off in acetone. However, apparent detachment appeared after a short-time water immersion for 10 s and 1 min. Similar results were also observed for the ALD-grown HfO_2 (20 nm) patterns on mica (Supplementary Fig. 2). In contrast, the ALD-oxide patterns grown on the commercial SiO_2/Si substrate strongly attach to the surface, as confirmed by the unchanged morphologies even after long-time water immersion (Supplementary Figs. 3 and 4). With these experimental facts, it's evident that the ALD-grown dielectrics will form weak interfacial interactions with mica. To investigate the possible origin of the observed ~0.5 nm van der Waals (vdW) gap, we have monitored the thickness evolution of ALD dielectrics during vacuum heating at 250 °C (Supplementary Fig. 5), substrate-to-substrate transfer (Supplementary Fig. 6) and ALD water-pulse treatment (Supplementary Fig. 7) by atomic force microscopy (AFM) measurements. Based on experimental evidence and prior literature[40–42], we propose that this enlarged vdW gap likely arises from the ALD process-induced water vapor intercalation into the superhydrophilic mica/oxide interface during cyclic H_2O dosing (for details, see Supplementary Fig. 8).

Sacrifice-layer-free transfer of wafer-scale ALD-oxide films on mica

The easily detachable feature for ALD-grown oxide makes it possible to achieve wafer-scale intact transfer from the mica to a target substrate when a proper supporting media is used. Figure 2a and Supplementary Fig. 9 illustrate the detailed flow-process diagram of the wafer-scale transfer. Typically, the transfer process involves the ALD growth of Al_2O_3 or HfO_2 on mica substrate, spin-coating of poly (methyl methacrylate) (PMMA) polymer, peeling off in water assisted by a polydimethylsiloxane (PDMS) stamp, and pressing onto the SiO_2/Si substrate. Here, we choose PMMA as the adhesive layer because the work of adhesion[43] in $PMMA/Al_2O_3$ is much higher than that in Al_2O_3/mica (Supplementary Figs. 10–12 and Supplementary Tables 1 and 2). Figure 2b, c shows the typical photograph of an ALD-grown Al_2O_3 wafer (2.2-cm-long, 20-nm-thick) transferred on a PDMS supporter (Fig. 2b) and then laminated onto a two-inch SiO_2/Si wafer (Fig. 2c). It's worth noting the PDMS plays an important role on the winkle-free transfer of the Al_2O_3 film. Besides, the PDMS stamp can be used as a rigid supporter during AFM measurements. As shown in Fig. 2d, the backside of peeled-off Al_2O_3 film takes on the mica's roughness, showing an atomically flat and clean surface (R_a = 0.12 nm), and no signal of mica residues was detected by X-ray diffraction (XRD, Supplementary Fig. 13). Moreover, after thermal release from PDMS stamp and PMMA removal in acetone under mild ultrasonication, the Al_2O_3

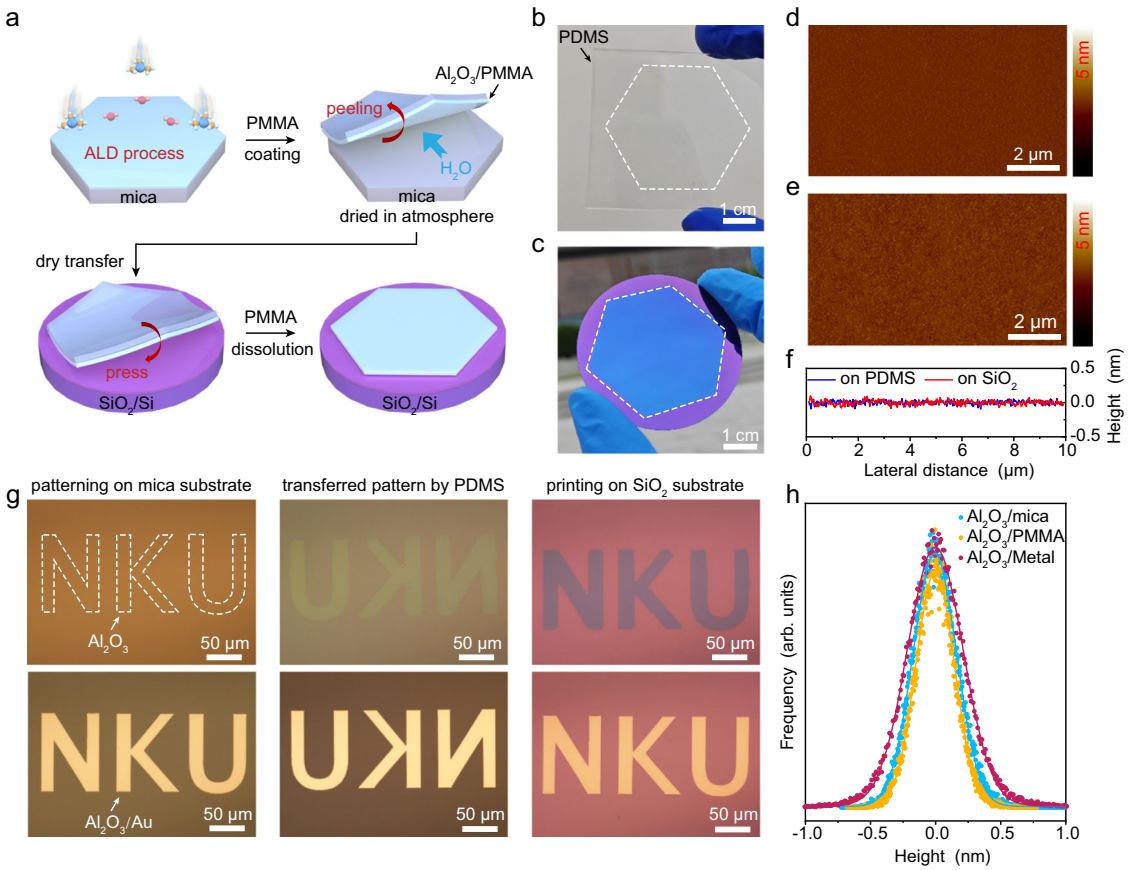

Fig. 2 | Sacrifice-layer-free transfer of wafer-scale ALD-oxide films on mica. **a** Schematic illustration of completely transferring the wafer-scale ALD-oxides from a mica substrate to a target SiO_2/Si substrate. **b** Typical photograph of a hexagonal Al_2O_3/poly (methyl methacrylate) (PMMA) wafer (2.2-cm-long, 20-nm-thick) on a polydimethylsiloxane (PDMS) supporter after peeled off from mica substrate in water. **c** Corresponding photograph of the transferred Al_2O_3 wafer that laminated onto a two-inch SiO_2/Si wafer, after removing PMMA by dissolution in acetone. **d** Typical atomic force microscope (AFM) image of as-transferred Al_2O_3 film on the PDMS in (**b**), showing an atomically flat surface and ultralow surface roughness (R_a ~ 0.12 nm). **e** Typical AFM image of ALD-grown Al_2O_3 film after transferred on the SiO_2/Si substrate, showing an ultra-flat and clean surface. **f** Corresponding height profile of (**d**) and (**e**), showing atomic-level height fluctuations. **g** OM images of ALD-grown Al_2O_3 film (20 nm) and Al_2O_3/Au high-κ metal gate (HKMG) (10 nm/30 nm) patterns with an NKU logo, showing the complete transfer from mica (left) to PDMS (middle) and SiO_2 (right) substrates. **h** Height histograms of ALD-grown Al_2O_3 film on mica substrate (blue), as-transferred Al_2O_3/PMMA (yellow) and Al_2O_3/Au/PMMA (red) film on PDMS stamp, showing a surface roughness of 0.12 , 0.12 , and 0.15 nm, respectively.

film transferred on the target substrate also has a uniform, continuous surface with little PMMA residuals, no observable cracks and wrinkles (Fig. 2e, f and Supplementary Figs. 14 and 15), indicating the successful transfer of large-scale ALD-grown oxide film from mica to SiO_2/Si wafer.

Next, we checked the lithographic compatibility of our mica-assisted transfer method, since it determines whether on-demand dielectric and high-κ metal gate (HKMG) patterns can be obtained or not for subsequent device fabrication. As shown in Fig. 2g and Supplementary Fig. 16, an NKU logo composed of ALD-Al_2O_3 (20 nm) and Al_2O_3/Au (10 nm/30 nm) was pre-patterned on the mica substrate by a traditional photolithographic method, serving as the examples of the patterned dielectric layer and HKMG, respectively. Notably, the NKU patterns can be entirely transferred onto the PDMS stamp and SiO_2/Si substrate, showing no apparent physical damage during the transfer regardless of Au capped or not. More importantly, both the patterned Al_2O_3 and Al_2O_3/Au stacks preserved the atomic-scale flatness after peeling off from the mica substrate (Fig. 2h and Supplementary Fig. 17), suggesting the possibility of forming atomically sharp dielectric/semiconductor interfaces by subsequent vdW integration.

To assess the quality of the transferred Al_2O_3 films, we examined their dielectric properties (e.g., dielectric constants and breakdown behavior) across a wide thickness range (2.8 nm to 20 nm, Supplementary Figs. 18 and 19). Specifically, the 2.8-nm-thick Al_2O_3 film achieves a low equivalent oxide thickness (EOT) of 1.86 nm, demonstrating the applicability of our method for ultrathin dielectrics. In theory, the EOT value can be further scaled when the Al_2O_3 dielectric was replaced by HfO_2 with a higher dielectric constant. To validate the scalability and uniformity of our technique, we fabricated 400 capacitor arrays by stacking the as-transferred HKMG stacks to the pre-patterned bottom electrode arrays on sapphire substrate (2 × 2 cm, Supplementary Fig. 20). Notably, the transfer yield for the HKMG on mica can be as high as 100% (Supplementary Fig. 21). Based on the capacitance density measurements of 100 randomly selected capacitors, we found that most of the devices' (> 60%) permittivity was concentrated between 6.5 ~ 7.5 at 1 MHz, which was comparable to the permittivity obtained by traditional direct ALD process. These device-level electrical results illustrate the high quality and uniformity of the transferred HKMG stacks.

One-step transfer and vdW integration of full-device stacks

Based on the successful transfer of ALD dielectrics and HKMG on mica, we further investigated the possibility of simultaneously transfer the full-device stacks (including contact electrodes and HKMG) for one-step integration of multi-terminal fully encapsulated top-gated transistors with 2D materials, which is a remaining unresolved issue among the 2D community. It's well-known that conventional device fabrication processes, including complex lithography, vacuum deposition, and ALD processes, will inevitably induce physical and chemical damages to the delicate 2D materials, thus making the investigation of their intrinsic electrical properties challenging[44]. Comparatively, one-step transfer of full-device stacks offers a totally lithography-free approach to fabricate fully encapsulated top-gated devices, which can simultaneously avoid the well-known evaporation-damage issue[45,46] and ALD-incompatible problems[39,47] in 2D electronics. Here, two types of device configurations, namely top-gated field-effect transistor (FET) and Hall devices, were fabricated as an example, both of which are widely used in the field of electromagnetic transport measurements to investigate the gate-tunable electrical properties of 2D materials.

Prior to the full-device stack transfer, we conducted a preliminary experiment to investigate whether the metal electrodes on mica are transferrable or not. As shown in Supplementary Figs. 22 and 23, the pre-patterned Au electrodes and even the wafer-scale continuous Au film can also be entirely transferred onto the targeted substrate in the same way mentioned above (Fig. 2a). Moreover, no detectable mica residue was peeled off from mica substrate (Supplementary Fig. 24). Figure 3a shows the detailed flow-process diagram of one-step transfer process to fabricate fully encapsulated top-gated 2D transistors. Typically, it includes 4 elementary steps: (1) define the source and drain electrodes on mica by photolithography and thermal evaporation; (2) deposit the ALD dielectrics and top-gated electrodes with another step of photolithography; (3) peel off the full-device stack from mica in water with the assistance of PMMA polymer and PMDS stamp; (4) laminate the dried full-device stack onto the target 2D material in a glove box filled with argon. As shown in Fig. 3b, c, the full-device stacks, shaped into the top-gated two-terminal FET and six-terminal Hall bar, can be readily pre-fabricated on mica substrate, and completely transferred onto the PDMS substrate for subsequent thermal release and vdW integration. On the contrary, the full-device stack transfer is merely impossible on traditional SiO_2/Si substrate due to the strong interaction between ALD-oxides and SiO_2/Si substrate (Supplementary Fig. 25). Importantly, the peeled-off device stack showed a clean and atomically flat surface with a surface roughness of ~0.15 nm (Fig. 3d, e), which guarantees the subsequent close integration with 2D materials to form heterojunction devices with neat interfaces. To investigate the interfacial microstructures, a stacked MoS_2 transistor was cut along a specific direction by focused ion beam for cross-sectional TEM imaging. As clearly demonstrated in Fig. 3f, g and Supplementary Fig. 26, the device showed an atomically sharp and damage-free interface in Al_2O_3/MoS_2 heterojunction with no observable disorders and defects, which is fundamentally important for the hysteresis-free gate control.

One-step integrated hysteresis-free top-gated MoS_2 transistors

In this part, we evaluated the electrical properties of one-step vdW integrated top-gated MoS_2 transistors, exhibiting two distinct advantages (namely higher on-state current and ignorable gate hysteresis). As shown in Fig. 4a, two types of top-gated FETs were schematically illustrated, whose top-gated stack partially encapsulates or fully encapsulates the underlying MoS_2 channel (namely partially gated or fully gated FET). Theoretically speaking, the fully gated FET is a favorable device configuration, since it allows better electrostatic control over the channel and results in a higher on-state current. However, fabricating the fully gated transistor usually requires a precise deposition of conformal ALD dielectrics to prevent the current leakage between the overlapped top and bottom electrodes. Given the well-known ALD-incompatible issue, almost all the previous works regarding top-gated 2D MoS_2 transistors with vdW stacked dielectrics adopted a partially gated device configuration[27,44,47,48], which will limit the on-state current in theory. In our study, the partially gated and fully gated MoS_2 FETs were fabricated by using one-step transfer approach with the same channel thickness (1.5 nm, 2 layers) and channel length (10 μm). The HKMG were 10-nm-thick Al_2O_3 with Pd/Au (5/30 nm) metals. Indium (In), a well-known low-work-function metal[49], was adopted as the adhesive layer of contact electrodes to get a higher on-state current. It should be emphasized that the sacrifice-layer-free transfer of strong-adhesion metals[26], such as In, is still a big challenge among 2D community, thus resulting in limited regulations to the contact interfaces. Nevertheless, this remaining issue can be well resolved by using the commercial-available mica as substrate, which can be regarded as a general intermediate substrate, similar to the well-known water-soluble $Sr_3Al_2O_6$[50,51], to get the free-standing and difficult-to-transfer functional layers.

The typical dual-sweep transfer curves and corresponding output curves were plotted in Fig. 4b, c, respectively. Thanks to the excellent quality of dielectric and channel interface, both of the devices can be effectively turned on and off ($I_{on}/I_{off} > 10^6$) in the gate voltage (V_g) range of 1.5 to −1.7 V, demonstrating the highly efficient tunability of HKMG by using the damage-free vdW integration. It was noteworthy that the fully gated FET exhibited a larger on-state current (> 42 times)

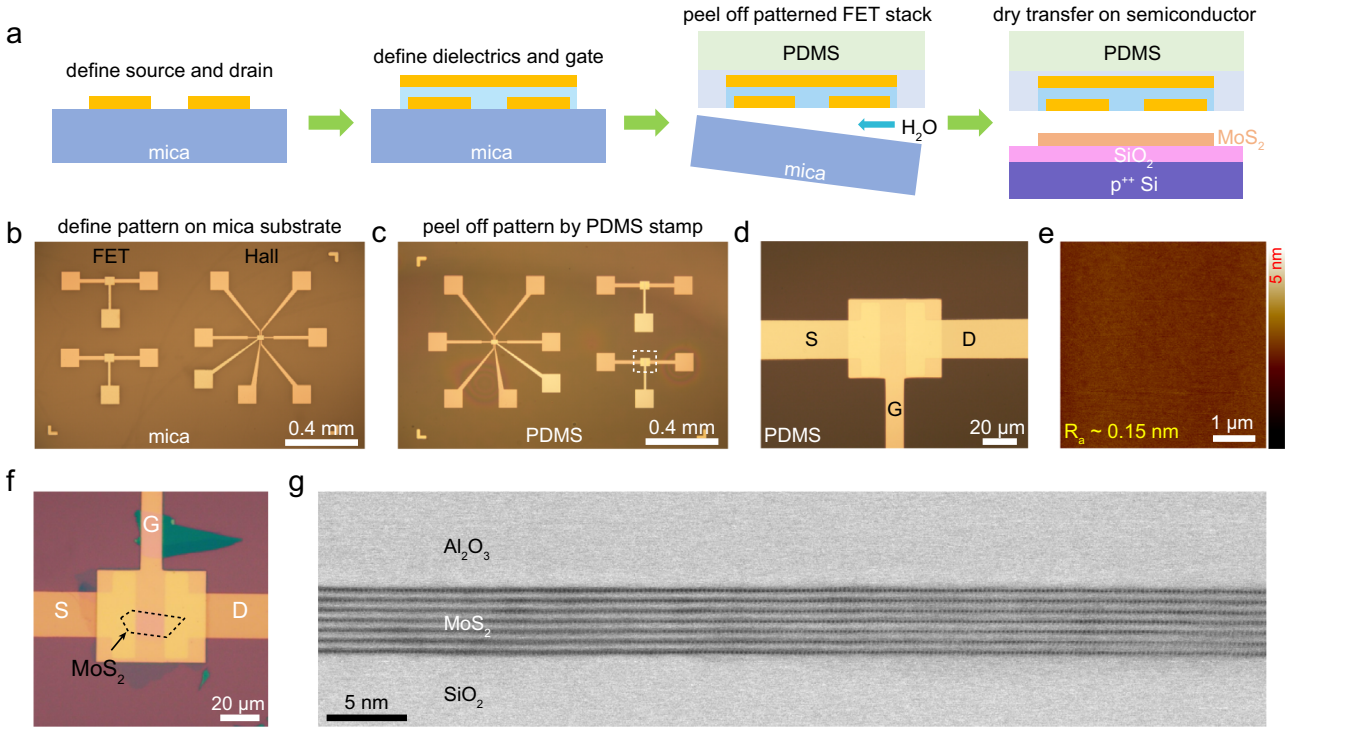

Fig. 3 | One-step simultaneous transfer and integration of contact electrodes and the entire gate stack. a Schematic diagram of one-step transfer process to fabricate fully encapsulated top-gated transistors, which involves pre-fabricating the entire top-gated device stack on mica and laminating it onto the surface of target channel materials. **b** Typical OM image of pre-fabricated entire device stack on mica, including top-gated two-terminal field-effect transistors (FETs) and six-terminal Hall-bar device. **c** Corresponding OM image of the entire top-gated device stack after delaminating and picking up from mica substrate. Here, the PMDS acts as the rigid support substrate to reduce the wrinkles during the transfer process. **d** Enlarged OM image in the white dotted box area in (**c**). **e** Typical AFM image of as-transferred gate stack (Al_2O_3/Pd/Au) on PDMS substrate, showing an atomically flat surface (R_a ~0.15 nm) when peeled off from the mica substrate. **f** Typical OM image of a top-gated MoS_2 FET fabricated on SiO_2/Si substrate by one-step vdW transfer. The underlying MoS_2 sheet was marked out by the dash line. **g** Corresponding cross-sectional bright-field scanning transmission electron microscope (STEM) image of as-transferred MoS_2 FET, showing a perfect interface and as-expected stacking sequence of $Al_2O_3/MoS_2/SiO_2$.

than that of partially gated FET under the $V_{ds} = 1$ V, since the fully depleted channel by the encapsulating gate can lead to a smaller channel resistance between source and drain electrodes. Particularly, based on the following equation:

$$\mu_{FET} = \frac{L}{W} \times \frac{1}{C_g} \times \frac{dI_{ds}}{V_{ds} dV_g} \quad (1)$$

where C_g is the top gate oxide capacitance, L and W are the channel length and width, two-terminal field-effect mobility (μ_{FET}) of fully gated MoS_2 can be estimated as high as ~61.5 $cm^2 V^{-1} s^{-1}$, which was about 13 times higher than the value of partially gated MoS_2 (~4.6 $cm^2 V^{-1} s^{-1}$). This feature greatly highlights the advantage of higher on-state current in the one-step integrated fully gated FET compared to the partially gated one. Furthermore, we investigated the gate hysteresis of the fully gated FET under different gate bias sweeping ranges (Fig. 4d) and sweeping rates (Fig. 4e), both of which exhibited an ignorable value of ~5 mV. This value is comparable to the minimum one among 2D transistors with precise interfacial optimization[47,48,52]. Additionally, it showed an ultra-low drain induced barrier lowering (DIBL) of ~3.5 mV/V (Supplementary Fig. 27). The ignorable gate hysteresis and DIBL value indicated that a clean and high-quality vdW interface was formed between the transferred ALD-grown Al_2O_3 dielectric and MoS_2 channel, which is in accordance with the TEM data (Fig. 3g) and gate-dependent capacitance measurements (Supplementary Fig. 28). Similar results were observed in another one-step integrated MoS_2 transistor with 5-nm-thick Al_2O_3 as gate dielectrics (Supplementary Figs. 29 and 30). In addition, to further demonstrate the interface properties, the trap density (D_{it}) at the Al_2O_3/MoS_2 interface was estimated using the following expression:

$$SS = \ln 10 \frac{k_B T}{q} \left(1 + \frac{q D_{it}}{C_g}\right) \quad (2)$$

where k_B is Boltzmann constant, T is absolute temperature, q is the elementary charge, and C_g is the gate capacitance obtained from MIM capacitance measurements. The subthreshold swings of the fully gated and partially gated MoS_2 FETs can be as low as 73.3 mV/dec and 62.8 mV/dec, thus extracting an ultralow D_{it} of 1.02×10^{12} cm^{-2} eV^{-1} and 2.26×10^{11} cm^{-2} eV^{-1}, respectively.

One-step integrated top-gated Hall device for fragile 2D materials

Top-gated Hall measurement is a widely used powerful tool to investigate the gate-tunable electrical properties in low-dimensional physics[53–55]. However, the top-gated Hall measurements on delicate 2D materials have been a big challenge, since they usually decay quickly during the lithography, thermal evaporation, and ALD process. The full-device stack transfer printing approach not only offers a non-invasive process with minimum interfacial damage, but also provides a fully encapsulated structure to isolate H_2O/O_2 during electrical measurements, thus enabling the highly desirable gate-tunable transport measurements on sensitive 2D materials (Fig. 5a, b). Here, a few-layer black phosphorus (BP) was chosen as the model-sensitive 2D material[56,57]. As shown in Fig. 5c, the BP nanosheet (~11.5 nm) was mechanically exfoliated in the glove box on the SiO_2/Si substrate, followed by one-step integrated into a six-terminal top-gated Hall device, whose contact metal, dielectric layer and top-gated electrode

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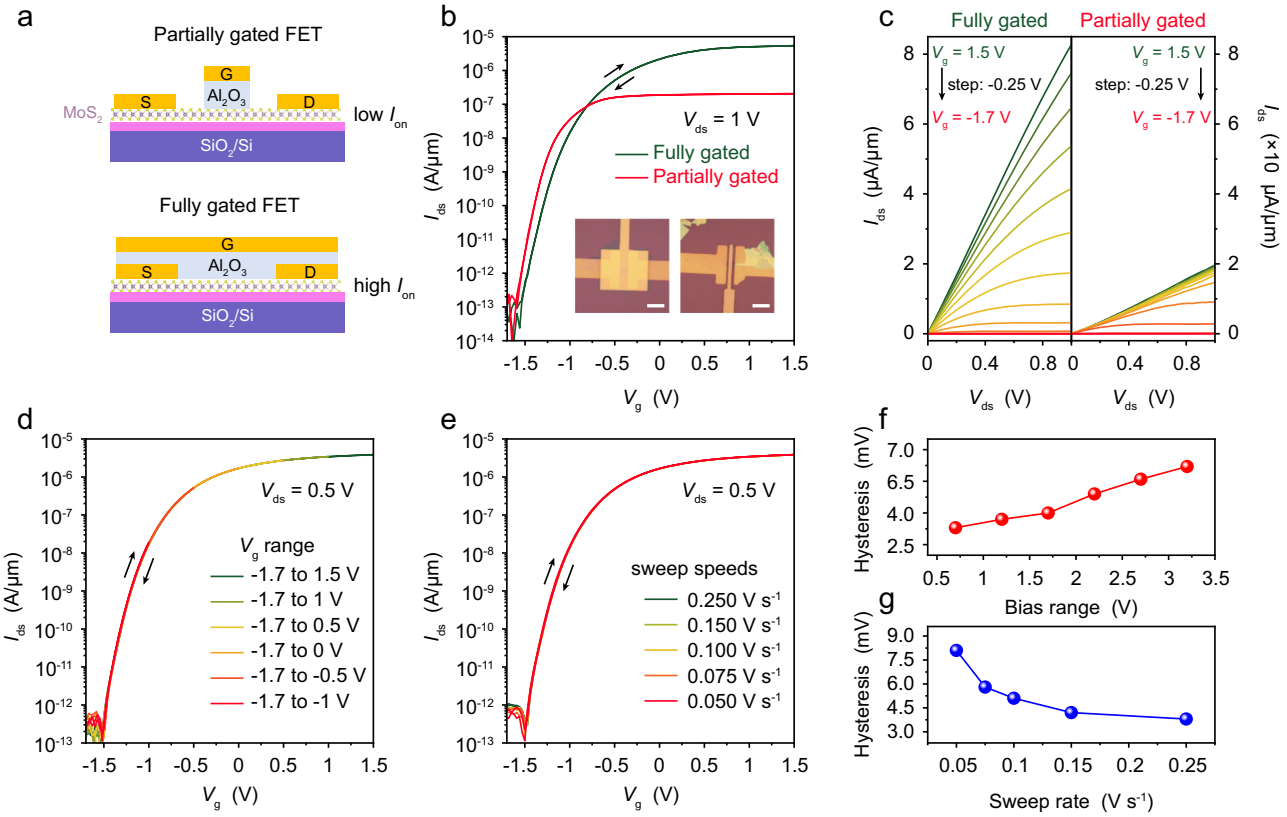

Fig. 4 | As-transferred fully gated MoS_2 transistors with improved on-state current and ignorable gate hysteresis. a Cartoons of two different device configurations adopted in top-gate FETs, whose top-gate stack partially encapsulate or fully encapsulate the underlying MoS_2 channel (namely partially gated or fully gated FETs). **b** Typical dual-sweep transfer curves of the as-transferred MoS_2 transistors with a fully gated and a partially gated device configuration. Apparently, the fully gated FET exhibited a much larger on-state current and switching ratio than the partially gated one. The thickness of MoS_2 was kept the same as ~1.5 nm. The insets are the OM images of fabricated fully (left) and partially (right) gated FETs (scale bar, 20 μm). **c** The corresponding output curves of the devices in (**b**), in which the gate voltages V_g varied from 1.5 V to −1.7 V with a step of −0.25 V. The on-state current of fully gated FET is higher (> 42 times) than that of partially gated FET with the source-drain voltage V_{ds} = 1 V. **d** The transfer curves of the fully gated MoS_2 FET under different V_g sweep ranges. **e** Corresponding transfer curves with different gate-voltage sweeping speeds ranging from 0.05 to 0.25 V s^{-1}. **f**, **g** Extracted bias-range (**f**) and sweep-rate (**g**) dependent gate hysteresis from the dual-sweep transfer curves in (**d**) and (**e**).

were Au (30 nm), ALD-Al_2O_3 (10 nm) and Pd/Au (10/50 nm), respectively. As shown in Supplementary Fig. 31, cross-sectional TEM reveals an atomically sharp and flat Al_2O_3/BP interface with no detectable oxidation layer or structural defects, confirming the effectiveness of our encapsulation strategy.

Two-terminal current-voltage (*I-V*) measurement is a direct and simple way to check whether the fabricated devices still work or not. As shown in Fig. 5d, the top-gated Hall device showed linear and merely unchanged *I-V* curves even exposed to air for 1 month, confirming the excellent encapsulation function. In contrast, the BP device fabricated by the conventional manufacturing processes became highly insulating because of the surface degradation (Supplementary Fig. 32). Subsequently, to investigate its gate tunability, we conducted temperature-dependent resistance (R_{xx}-T, Fig. 5e) and room-temperature Hall measurements (Fig. 5f) under different V_g. Notably, the encapsulated BP always exhibited a typically semiconducting behavior when the V_g varied from 0 to −1.5 V. Besides, by linearly fitting the Hall resistance (R_{xy}) versus magnetic field (B) curves, the gate-dependent Hall mobilities were extracted in Fig. 5g, showing a gradual decrease from 703 to 557 $cm^2 V^{-1} s^{-1}$ on hole mobility when the V_g was varied from 0 to −1.4 V. Furthermore, to confirm the excellent air stability, twice Hall measurements were performed on the same stacked BP device to extract the temperature-dependent Hall mobility and carrier density before and after exposure to air for 1 week. As shown in Fig. 5h, i, both the carrier mobility and density of the BP device underwent very slight change among the whole temperature range from 300 to 50 K, demonstrating the advantages of one-step fully gated integration to protect the air-sensitive materials.

In summary, we developed a mica-assisted strategy to achieve the damage-free transfer of pristine wafer-scale ALD gate dielectrics without requiring additional seed and sacrifice layer. Moreover, owing to its atomic-scale flatness and comparability to direct ALD growth, our approach achieves significant improvements in transfer yield and interface cleanliness, compared to other reported techniques (for details, see Supplementary Table 3). In addition, the entire top-gate stack, composed of the ALD dielectrics and metal contacts, can be one-step transferred onto few-layer MoS_2 to form high-performance 2D transistors with a fully gated device structure, showing an enhanced on-state current and ignorable gate hysteresis. Besides, the one-step full-device stack transfer approach can be extended to fabricate the complex fully encapsulated top-gated Hall devices, enabling the rapid investigation of the intrinsic gate-tunable properties of fragile 2D materials. Our work provides an alternative scalable way to avoid the well-known issues of ALD incompatibility and deposition damages among 2D community.

Methods

Damage-free transfer of wafer-scale ALD-oxide films

In this paper, the sacrifice-layer-free transfer printing strategy was performed by using mica as mother substrate. Because of the weak

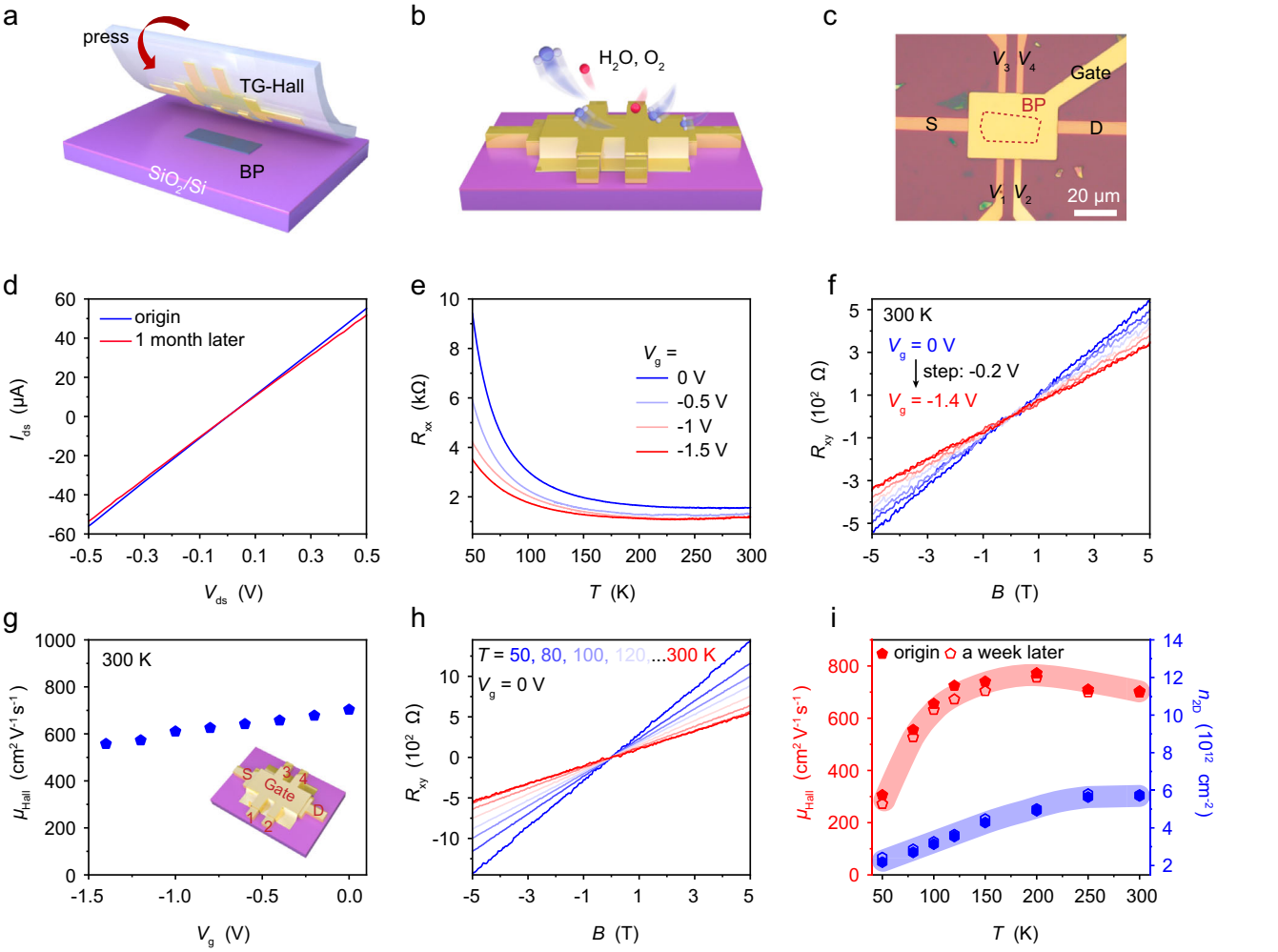

Fig. 5 | As-transferred top-gated Hall device used to perform multi-terminal electrical measurements on air-sensitive black phosphorus (BP). a Schematic diagram of one-step transfer process to fabricate the top-gated Hall bar of black phosphorus in the glove box. **b** Diagram of a fully encapsulated Hall-bar device that can effectively isolate water and oxygen in the air, thus allowing for the measurements of the intrinsic properties of the air-sensitive black phosphorus. **c** Typical OM image of the fabricated top-gated BP hall-bar device. The underlying BP sheet with the thickness of ~11.5 nm was marked out by the dash line. **d** The *I*-*V* curves of the device in (**c**), preserving linear ohmic contact even after exposed to air for one month. **e** Longitudinal resistance (R_{xx}) as a function of temperature (T) under different V_g from 0 to −1.5 V. **f** Hall resistance (R_{xy}) as a function of magnetic field (B) under various V_g from 0 to −1.4 V at 300 K. **g** Corresponding V_g-dependent Hall mobility extracted from (**f**). The inset is the schematic of the top-gated BP hall-bar device. **h** Temperature-dependent R_{xy}-B curves varied from 300 to 50 K under V_g = 0 V. **i** The extracted temperature-dependent Hall mobility and hole carrier density of black phosphorus before (filled points) and after (open points) exposure to air for 1 week. The red and blue shaded lines are the visual guide for the temperature-dependent mobility and carrier density, respectively.

interfacial interaction between ALD-oxides and mica, the ALD-oxides can be peeled off smoothly and printed onto the receiver substrate. The specific steps were as follows. First, a fresh and atomically flat mica surfaces were obtained by mechanical cleavage using a needle tip, and then the fresh mica substrate was immediately loaded in the ALD chamber (TALD-100A) for ALD growth at 150 °C and a base pressure of 0.15 Torr. We used trimethyl aluminum and water as the precursors for ALD growth of Al_2O_3 film, while tetrakis (dimethylamido) hafnium and water for the growth of HfO_2 film. The film thickness can be controlled precisely by altering the deposition cycles. Specifically, the pulse time of Al, Hf, and water was 20, 40, and 15 ms, respectively, while the purge time was 90 s. During the ALD growth, high-purity N_2 of 14 sccm was used as the carrier gas.

After ALD growth, a layer of PMMA polymer (950 PMMA A4, Kayaku Advanced Materials) was spin-coated at 2000 rpm for 1 min, and baked at 120 °C for 2 min to form a flat supporting layer on top of ALD-oxides. After that, a PDMS stamp with a suitable size was laminated on the surface of PMMA polymer. Specifically, the edge of the ALD-oxides/mica substrate was intentionally scratched off to allow water to intercalate into the vdW gap between ALD-oxides and mica substrate smoothly. Afterward, the composite film of Al_2O_3/PMMA/PDMS was peeled off naturally from mica substrate in water (immersion ~ 5 h) and fully dried in atmosphere, and then was dry-transferred onto the target SiO_2/Si substrate. Finally, the PDMS was thermally released from the PMMA surface and PMMA polymer was removed by dissolution in hot acetone solution (70 °C) under mild ultrasonication (30 W) for 5 min, leaving a desired wafer-scale ALD-oxide film on the target substrate.

Fabrication and transfer of full-device stacks on mica

The full-device stacks in Fig. 3c were fabricated via the following procedures. First, the 2-terminal and 6-terminal contact electrodes were patterned on the mica substrates by photolithography by using a maskless laser direct writing system (LDW, Microlab III), followed by thermal evaporation of desired metals such as In/Au (5/30 nm). Subsequently, we defined the fully encapsulated gate patterns by another step of LDW, and then 10-nm-thick Al_2O_3 dielectrics and top-gate electrodes of Pd/Au (5/30 nm) were deposited by ALD and thermal

evaporation, respectively. After lift-off in acetone, the designed full-device stacks of top-gated transistors and Hall bars were obtained on mica substrates.

The full-device stack transfer procedures were listed as follows. First, a layer of PMMA polymer was spin-coated at 2000 rpm for 1 min, and baked at 120 °C for 2 min. Second, the fabricated full-device stacks were successfully peeled off from mica in water with the assistance of PMMA layer and PMDS stamp, which was pre-attached to a glass slide as the handling substrate for subsequent transfer. The dried full-device stacks were kept in the glove box for later use. Notably, for individual top-gated FETs or Hall devices, complete peeling typically occurs within <10 s of water immersion; for 2 cm × 2 cm HKMG (high-κ/metal gate) arrays, immersion for ~ 30 s ensures reliable release.

For the one-step vdW integration of fully encapsulated top-gated devices, few-layer MoS_2 and BP flakes were mechanically exfoliated on the highly doped silicon substrate covered with 285-nm-thick SiO_2 in the glove box, which was precleaned by O_2 plasma (50 W, 5 min). Then, the peeled-off full-device stacks were aligned under a microscope and physically laminated on the target material surface, resulting in an atomically shape and clean interface. Finally, the designed fully encapsulated top-gated device was obtained by thermally releasing the PDMS stamp at 120 °C in 3 min and dissolving the PMMA polymer in hot acetone solution (70 °C) under mild ultrasonication (30 W) for 5 min.

Characterizations and electrical measurements

The as-grown ALD-oxides and full-device stacks were characterized by optical microscopy (OM, Olympus BX53), atomic force microscope (AFM, Bruker Dimension Icon), and XRD (Rigaku Smart Lab 30 KW). The cross-sectional TEM samples were prepared by a focus ion/electron dual beam system (FEI, Helios 5 CX). A layer of conductive polymer and Pt were deposited to protect the samples from Ga ion implantation. The high-resolution cross-sectional TEM was performed by transmission electron microscopy (TEM, JEM-2800), and aberration-corrected scanning transmission electron microscopy (STEM, FEI Titan cubed Themis G2 300 operating at 300 kV). The contact angles of the surfaces were tested and recorded by a geometer (SFMIT, SDC-200).

The electrical properties of top-gated MoS_2 transistors were performed on a semiconductor parameter analyzer (PDA, FS-Pro) and a probe station with a shielded vacuum chamber (<0.1 Pa) at room temperature. The temperature-dependent top-gated Hall measurements were performed on a Physical Property Measurement System (PPMS-9 T, Quantum Design) equipped with a home-made electrical measurement system.

Data availability

Relevant data supporting the key findings of this study are available within the article and the Supplementary Information file. All raw data generated during the current study are available from the corresponding authors upon request.

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Author contributions

J.W. convinced the original ideas and supervised the whole project. Y. H. performed the transfer of ALD films, characterization, device fabrication, and electrical measurements under the assistance of Z.Lv., M.Y., W.A., J.C., W.C., and B.W. The cartoon diagrams were designed and plotted by Z.L. and Y.H. The contact angles were measured by Z.Lv. The paper was written by J.W. and Y.H. with input from other authors. F.L. and X.F. co-supervised the whole project and gave constructive suggestions. All authors contributed to the scientific discussions.

Competing interests

The authors declare no competing interests.

Additional information

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