nature communications

Article

https://doi.org/10.1038/s41467-025-65750-8

Improving interfacial thermal conductivity by constructing covalent bond between Ga_2O_3 and SiC

Received: 26 February 2025

Accepted: 23 October 2025

Published online: 28 November 2025

Check for updates

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Gallium oxide (Ga_2O_3) is emerging as a promising semiconductor for next-generation power and radio-frequency electronics due to its ultra-wide bandgap and high breakdown field. Yet, its intrinsic thermal conductivity is extremely low, which causes severe self-heating and limits reliable device operation. A common approach to overcome this challenge is to integrate Ga_2O_3 with substrates of high thermal conductivity such as silicon carbide (SiC). However, weak bonding across the heterojunction interface creates large thermal resistance, preventing efficient heat removal. Here we show that constructing strong covalent bonds between Ga_2O_3 and SiC through an engineered interlayer enables both structural compatibility and efficient phonon transport. This bonding strategy increases the interface thermal conductivity to 162 MW/m²·K, the highest value reported for Ga_2O_3 heterostructures. Infrared thermography confirms that the bonded devices exhibit a temperature reduction of up to 29 °C under high power densities, demonstrating significant mitigation of self-heating. These findings establish a practical route for enhancing thermal management in Ga_2O_3 electronics and highlight the importance of interfacial bonding design. Beyond Ga_2O_3, this approach may be extended to other wide-bandgap semiconductors where thermal bottlenecks constrain device performance.

Since modern electronic devices have evolved toward the higher power, frequency and temperature capabilities, wide-bandgap semiconductor materials have garnered significant research interest due to their exceptional physical properties[1–3]. Silicon carbide (SiC) is widely utilized in high-power applications because of its wide bandgap of 3.2 eV and low conduction loss. However, the low saturated electron mobility still limits the effectiveness of SiC in high-frequency domains. In contrast, gallium nitride (GaN) offers notable advantages under high-frequency conditions but lacks the ability to produce self-supporting substrates, which restricts its use in high-power scenarios. Gallium oxide (Ga_2O_3), a semiconductor with an ultra-wide bandgap (approximately 4.8 eV), has attracted considerable attention for its potential in high-voltage power and high-frequency electronic devices[4]. Ga_2O_3 exhibits exceptionally high critical breakdown field

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(projected to be up to 8 MV/cm) and low on-resistance, which can significantly reduce losses in power devices. Furthermore, it has a high saturation electron velocity (~2×10^7 cm/s) and an impressive Johnson's figure of merit (JFOM), thus being an ideal candidate for high-frequency applications[5–7]. Beyond its outstanding electronic properties, Ga_2O_3 possesses a combination of unique material advantages that make it a highly promising candidate for next-generation semiconductor applications[8]. It demonstrates excellent thermal and chemical stability, maintaining performance under extreme conditions such as ultra-low temperatures and strong radiation environments[9]. Additionally, Ga_2O_3 exhibits strong absorption in the deep-ultraviolet (DUV) spectral region (~250–280 nm), making it highly suitable for solar-blind UV photodetectors and space-based optoelectronic applications[10]. From a materials perspective, Ga_2O_3 is advantageous in both bulk and epitaxial growth. It supports melt-based bulk crystal growth techniques such as edge-defined film-fed growth (EFG) and Czochralski (CZ), enabling the production of large-area, low-cost single crystals—unlike SiC, which requires expensive high-temperature vapor-phase growth[11]. At the same time, Ga_2O_3 shows excellent compatibility with various heteroepitaxial growth methods, including MOCVD (Metal-Organic Chemical Vapor Deposition), MBE (Molecular Beam Epitaxy), and PLD (Pulsed Laser Deposition), on substrates such as sapphire, Si, and SiC[12]. In addition, Ga_2O_3 has relatively low hardness compared to SiC, reducing wafer slicing and processing costs. Given the breakthrough in manufacturing, including the production of 6-inch substrates, Ga_2O_3 shows great promise for the development of next-generation high-power and high-frequency devices[13,14].

However, one significant disadvantage of Ga_2O_3 is the low thermal conductivity (approximately 10–27 W/m·K)[15,16], which is inferior to that of other semiconductors, such as Si (150 W/m·K), AlN (180 W/m·K), GaN (230 W/m·K), SiC (490 W/m·K), and diamond (2000 W/m·K)[5]. Such a low thermal conductivity value can lead to serious thermal management issues when operating at high temperatures and powers. Energy losses during conduction and switching generate heat, raising the temperature of the device's active junction and package. In turn, excessive junction temperatures (T_j) negatively affect the performance and reliability of the device[17]. To ensure the long-term reliability, T_j in commercial power devices is typically kept[18]. The "10 K rule" indicates that the failure rate of electronic components can double for every 10 K increase[19]. Chatterjee et al. have found that T_j in Ga_2O_3 devices can reach up to 1500 °C at a power density of 10 W/mm[20]. Therefore, this thermal management is a major bottleneck in the use of Ga_2O_3 in high-power and high-frequency applications.

In recent years, various strategies have been proposed to enhance the heat dissipation performance of Ga_2O_3-based devices[9]. As illustrated in Supplementary Fig. 1, heat generated during operation is typically transferred through a thermal interface material (TIM) to the substrate and then dissipated via an external heat sink[21,22]. While adding heat sink modules can improve thermal efficiency, this strategy often leads to bulkier device structures and limited heat removal from localized hotspots, which hampers device miniaturization and reliability. A possible strategy to circumvent the low thermal conductivity of β-Ga_2O_3 is to thin the Ga_2O_3 substrate[23]. However, while improving heat dissipation, this route may compromise the mechanical strength under harsh operating conditions and reduce reliability of the appliance. A more effective approach is near-junction thermal management (NJTM), using a highly conductive substrate in direct contact with the heat source so as to ensure the direct heat dissipation, e.g., Si[24], SiC[25–27], Ge[28] and diamond[29–31] substrates. NJTM is a highly effective heat dissipation method, enabling to position the heat-conducting materials or heat-sinking structures directly near the heat source of a chip to rapidly transfer heat outward, thereby enhancing the overall thermal efficiency[32]. The effective NJTM is essential to ensure the optimal heat dissipation, which has been demonstrated in GaN high-electron-mobility transistors through the use of substrates with high thermal conductivity[33,34]. Among high-thermal conductivity substrates, SiC is considered one of the most suitable substrates for heat dissipation. Yuan et al. demonstrated that although SiC, with a thermal conductivity of 490 W/m·K, has a lower value than diamond, a substrate thermal conductivity exceeding 400 W/m·K is sufficient to achieve comparable heat dissipation performance to that of diamond[35]. Besides that, SiC possesses excellent thermal stability and lattice matching with β-Ga_2O_3. At the same time, compared with diamond, SiC is more suitable for the preparation of large-size substrates at low cost, which is conducive to the large-scale industry of relevant devices. Numerous studies have been reported using composite substrates bonded with SiC and Ga_2O_3 so as to prepare high-frequency devices[36] and high-power devices[37–39].

Although SiC possesses noticeable thermal management advantages, there still exists the problem of low interface thermal conductivity (ITC), resulting in the ineffective heat conduction to the high-thermal conductivity substrate, limiting its applicability in high-power systems[40]. Song et al. introduced SiN_x into the interface to enhance the ITC of Ga_2O_3 and SiC bonding, but the value was still only 22 MW/m²·K[25]. Chen et al. bonded a Ga_2O_3 single crystal to a SiC substrate via the ion-cutting technique[27]. As a result, the ITC was increased from 72 to 100 MW/m²·K once the thickness of the Al_2O_3 interlayer was decreased from 30 to 9 nm. Xu et al. found that the introduction of Al_2O_3 between SiC and Ga_2O_3 lowered the ITC to 70 MW/m²·K[24]. Moreover, the interfacial microstructure has a pronounced impact on the thermal conduction efficiency[41]. Good lattice matching and low interfacial roughness enable to reduce phonon scattering and thus increase the ITC[42]. On the contrary, defects and impurities within the interface increase the thermal resistance and decrease the heat transfer efficiency. Research indicates that for diamond-based Ga_2O_3 devices, the reduction in junction temperature can be optimized by increasing the ITC to 200 MW/m²·K[35]. The researchers found that covalent binding can increase ITC by 1–2 orders of magnitude compared to Van der Waals force (VdW) binding[43,44]. In addition, the local molecular environment between heterogeneous materials can regulate the ITC[45]. In particular, the enhancement of phonon transport occurs when the chemical bond changes from a weak VdW interaction to a strong covalent bond. M-D. Losego et al. also found through research that as the number of covalent bonding sites increases, the coupling of phonons at the interface will be stronger, resulting in a significant increase in interfacial thermal conductivity[46]. Therefore, properly adjusting the interface microstructure and constructing covalent bonds are among the key strategies to furtherly improve the ITC of SiC-based Ga_2O_3.

In view of the above, this work achieved high ITC by constructing a covalent bond between Ga_2O_3 and SiC. Through precise interfacial engineering, a stable and flat SiO_2 interlayer was successfully formed, facilitating the formation of strong covalent bonds between the SiO_2 layer and both adjacent layers—Ga_2O_3 and SiC. As a result, the ITC increased ninefold, reaching 162 MW/m²·K, which is the highest value ever reported so far. The NJTM approach effectively enhanced the dissipation of heat generated under light source irradiation, thereby reducing the operating temperature of 29 °C. Therefore, these results highlight the potential of interfacial covalent bonding as a cutting-edge method for improving thermal management in wide-bandgap semiconductor materials, with substantial academic and practical significance.

Results and discussion

Sample preparation and interfacial characterization

In this work, an approximately 70-nm-thick Ga_2O_3 film was deposited on a SiC substrate using atomic layer deposition (ALD), as depicted in Fig. 1a. The microstructural evolution of the interface was monitored using transmission electron microscopy (TEM) in coupling with energy-dispersive X-ray spectroscopy (EDS) (see Fig. 1b–g). Figure 1b

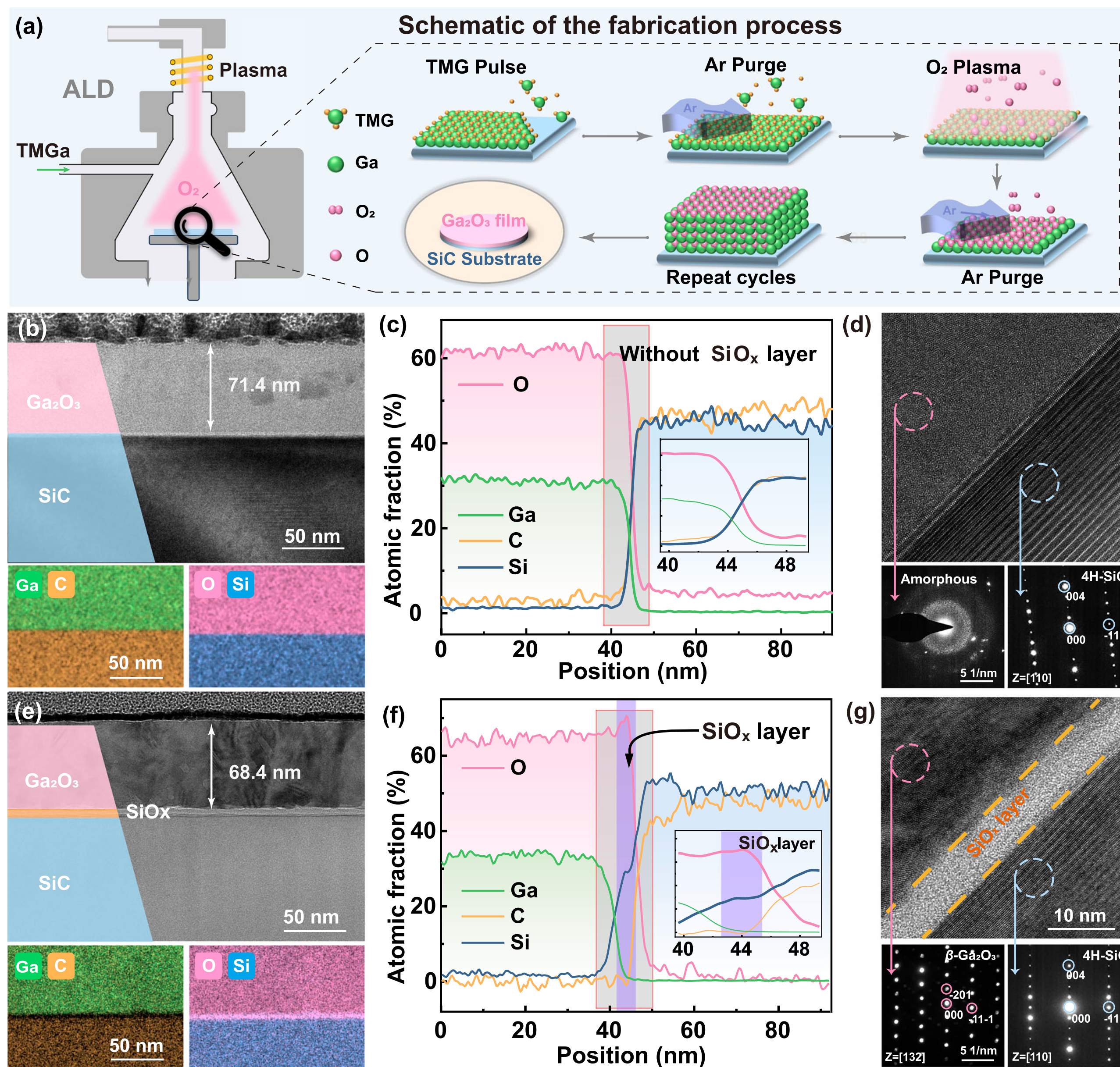

Fig. 1 | TEM images of Ga_2O_3/SiC and Ga_2O_3/SiO_2/SiC heterojunctions before and after annealing. a Schematic of the fabrication process. **b** Cross-sectional TEM image and corresponding EDS maps of the untreated sample. **c** EDS line scans of the cross-section. **d** HRTEM micrograph of Ga_2O_3/SiC heterojunction interface and SAED pattern (**e**) Cross-sectional TEM image and corresponding EDS maps of the sample annealed for 120 min at 1173 K. **f** EDS line scans of the cross-section. **g** HRTEM micrograph of Ga_2O_3/SiO_2/SiC heterojunction interface and SAED pattern.

displayed a representative region of the Ga_2O_3/SiC interface for the deposited sample, which appeared very flat and exhibited the Ga_2O_3 thickness of about 71.4 nm. The corresponding EDS elemental maps and vertical line-scan data indicated that the Ga_2O_3 film was homogeneous and had a single layer structure. The high-resolution TEM (HRTEM) image and selected area electron diffraction (SAED) results, as shown in Fig. 1d, indicate that the as-deposited Ga_2O_3 layer is amorphous, while the underlying SiC substrate exhibits high-quality single-crystal characteristics. A cross-sectional TEM image of the sample after 120 min of annealing at 1173 K is depicted in Fig. 1e. Compared to the untreated samples, the annealed ones clearly demonstrated the formation of a reaction layer between Ga_2O_3 and SiC. Simultaneously, the Ga_2O_3 film became thinner, and the interface became rougher. According to the EDS elemental maps, the intermediate reaction layer was rich in Si and O, while being poor in Ga and C. Figure 1f depicts the elemental content variation in the vertical direction, confirming that the Ga_2O_3 film and SiC substrate maintained their typical elemental percentages. A zoomed-in view of the interface is shown in the inset image of Fig. 1f. The results suggested that the intermediate reaction layer had an oxygen-to-silicon ratio of approximately 2:1, which corresponded to a SiO_2 structure. A HRTEM image of the Ga_2O_3/SiC interface is displayed in Fig. 1g, in which the crystalline regions were ascribed to Ga_2O_3 and SiC, while the SiO_2 layer had a structurally amorphous state. The SAED patterns in Fig. 1g, taken from Ga_2O_3 and SiC regions, confirmed their β-Ga_2O_3 and 4H-SiC structures, corresponding to the [132] and [110] zone axes, respectively. The evolution of microstructure under different annealing conditions was further investigated by TEM, as shown in Supplementary Figs. 2–4. The data show that the thickness of the reactive layer and the interface roughness gradually increase with increasing annealing time and annealing temperature. When annealed at the lower temperature of 1073 K, the thickness of the SiO_2 was slightly thinner, but the overall

https://doi.org/10.1038/s41467-025-65750-8

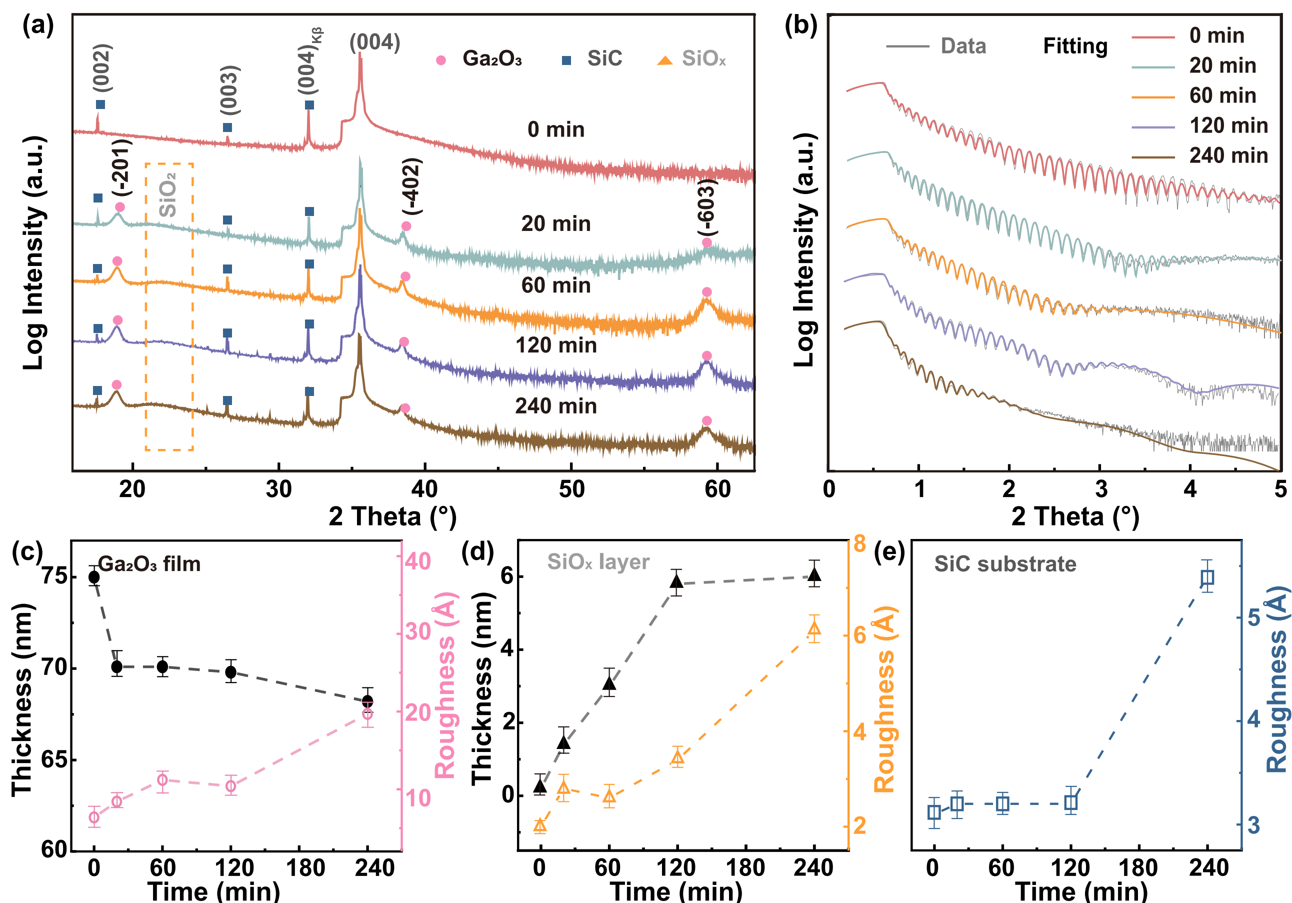

Fig. 2 | Structural characterization of as-deposited and annealed samples by XRD and XRR analyses. a XRD patterns and (**b**) Measured and fitted XRR curves of the as-deposited and annealed samples. **c–e** The extracted XRR data for the corresponding layers and the error bars represent standard deviation.

interface was flatter. When annealed at 1273 K, the growth rate of SiO_2 was significantly higher than that at 1073 K and 1173 K. However, deterioration of the interface and the Ga_2O_3 film, as well as an increase in roughness, was also clearly observed.

To gain deeper insight into the structural composition of each film layer, X-ray diffraction (XRD) and X-ray reflectivity (XRR) measurements were performed on the samples annealed at 1173 K. In addition to the prominent SiC-related peak around 35.6° (Fig. 2a), the annealed Ga_2O_3 exhibited a distinct crystalline peak, while a broad hump appeared near 22°. This was due to the diffuse scattering from the amorphous material, confirming the formation of a SiO_2 layer in the middle of the structure. Figure 2b shows measured and fitted XRR curves of the as-deposited and annealed samples and corresponding information of different layers was plotted in Fig. 2c–e. For the untreated samples, the 5-degree oscillatory cycles were observed, indicating that the interface and film surface were flat and possessed the low roughness. Once the annealing time increased, there was the decay in the oscillations, accompanied by another periodic oscillation in the curve, which corresponded to a thinner SiO_2 film layer. As soon as Ga_2O_3 reacted with SiC during the annealing process, the thickness of the Ga_2O_3 film decreased, while there was little change in the roughness of the SiC substrate. With the further annealing, the crystallinity of the sample increased, enhancing the roughness of the Ga_2O_3 surface. More details regarding the atomic force microscopy (AFM) analysis of the Ga_2O_3 surface morphology are described in Supplementary Fig. 5 of the Supporting Information. However, after 240 min of annealing, a sharp increase in the roughness of both the substrate and the SiO_2 interface was observed, indicating the deterioration of the interfacial structure. A representative region of the $Ga_2O_3/SiO_2/SiC$ interface after annealing for 240 min is displayed in Supplementary Fig. 6. The TEM maps revealed humps of approximately 3–8 nm in height, which were distributed across the entire interface, and the EDS maps suggest that these were SiO_2. Moreover, the TEM characterization confirmed that the prolonged heat treatment led to the formation of an undulating and uneven interface, which coincided with the larger roughness observed in the XRR results.

To further elucidate the bonding conditions at the interface and the changes in chemical composition, the X-ray photoelectron spectroscopy (XPS) experiments were conducted across the Ga_2O_3/SiC heterojunction at various etching depths. The depth-profiled XPS spectral maps for the Ga *3s*, Si *2s*, and O *1s* core levels of the Ga_2O_3/SiC heterojunction are displayed in Fig. 3 along with the fitted XPS spectra. Figure 3a depicts a pronounced interface between the Ga_2O_3 film and SiC substrate. As seen from Stage I of Fig. 3a, the representative O *1s* XPS spectrum within the Ga_2O_3 film consisted solely of the O-Ga peak[47]. At the interface, the Ga *3s* core-level spectrum exhibited a modest downward band bending, whereas the Si *2s* component shifted toward the higher binding energies. Additionally, the Si *2s* core-level spectrum revealed the presence of a Si-O bond at 153.93 eV alongside the Si-C bond at 151.92 eV, which were interpreted based on reports[48,49], indicating the weak Si-O bonding at the interface. In Stage VI, a low-intensity O-Ga peak remained still detectable despite etching up to the SiC substrate. This was likely due to a small amount of the product sputtering onto the fresh surface during the etching process. From the spectral maps of annealed samples, it was concluded that the surface layer had a pure Ga_2O_3 structure similar to the untreated specimen (Fig. 3c). As soon as the etching depth increased to 65 nm, the emergence of signals related to the Si-O and O-Si bonds was observed in Si

Fig. 3 | Depth-resolved XPS analysis and structural evolution of Ga_2O_3/SiC heterojunctions before and after annealing. **a** Depth-profiled XPS spectral maps corresponding to Si *2s* and O *1s* core-level features across the Ga_2O_3/SiC heterojunction in the untreated sample. **b** The corresponding Si *2s* and O *1s* XPS peaks at different etching depths. **c** Depth-profiled XPS spectral maps corresponding to Si *2s* and O *1s* core-level features across the Ga_2O_3/SiC heterojunction in the sample annealed for 120 min. **d** The corresponding Si *2s* and O *1s* XPS peaks at different etching depths. **e** Schematic crystal structures of β-Ga_2O_3 and amorphous Ga_2O_3 after high-temperature thermalization. **f** Radial distribution function of amorphous Ga_2O_3. **g** Heterogeneous interface of Ga_2O_3 and 4H-SiC before and after the reaction. **h** Si-O bond ratios vary with reaction time.

2s and O *1s* spectra, respectively. This indicated that the reaction between Ga_2O_3 and SiC at high temperatures facilitated the formation of SiO_2. To analyze the chemical bonding in detail, a split-peak fit of the core-energy levels was performed at specific locations, as shown in Fig. 3d. The signal associated with the Si-O bond was located at a binding energy of approximately 154.55 eV, while that ascribed to the Si-C bond was centered at 151.05 eV. Taking the binding energy of the Si-C bond as a reference, the difference was about 3.50 eV. For the untreated sample, the binding energy of the Si-O bond was only 2.01 eV higher than that of the Si-C bond, providing evidence that the heat-treated samples possessed a higher binding energy at the interface. This suggests that strong covalent bonding between Ga_2O_3 and SiC was enabled by the SiO_2 layer, as opposed to the VdW force connections formed directly in the untreated samples. Similarly, from the O *1s* core-level mapping, it can be found that the covalent bond between Ga_2O_3 and SiO_2 is constructed by O atoms. With a further increase in etching depth, the Si-O bonds were transformed to the Si-C ones.

To describe the reaction between Ga_2O_3 and SiC, the interaction between both components was simulated by combining density functional theory (DFT) and molecular dynamics (MD) methods. Calculating the reaction energy enables to predict whether the reaction will proceed spontaneously or not. The heat released during the reaction between Ga_2O_3 and SiC was calculated to be −460 kJ/mol at 0 K, indicating its exothermic nature under standard conditions. The corresponding reaction can be expressed as follows:

$$Ga_2O_3 + SiC \rightarrow SiO_2 + CO(g) + 2Ga \tag{1}$$

where Ga_2O_3 reacted with SiC to produce Ga, SiO_2, and CO gas. At 0 K, the negative heat value indicated that the reaction occurred spontaneously and was accompanied by the heat release[50]. At 1173 K a continuous heat input from the environment promoted the ongoing reactions. The thermodynamic analysis confirmed that Ga_2O_3 reacted with SiC to form SiO_2. To gain a deeper understanding of the reaction mechanism and kinetic behavior at the molecular level, an MD simulation was conducted at 2000 K. The results are depicted in Fig. 3e–h. First, the β-Ga_2O_3 is annealed at a high temperature of 2600 K to obtain a disordered amorphous Ga_2O_3 structure, as shown in Fig. 3e. From

Fig. 3f, the radial distribution function has multiple peaks within 4 Å, and gradually approaches 1 after it is greater than 4 Å, indicating that the system exhibits a short-range ordered and long-range disordered structure, corresponding to the amorphous state. The obtained amorphous Ga_2O_3 and 4H-SiC are used to construct a heterostructure as shown in Fig. 3g. After a thermal reaction at 2000 K for 1 ns, it can be found from the interface that some of these Si atoms will completely detach from SiC and form the structure of SiO_2 tetrahedra inside Ga_2O_3 after a reaction of 1 ns. In the local magnified image, SiO_2 crystal structure can be clearly found, proving that Ga_2O_3 and 4H-SiC can form SiO_2 at the interface at high temperature. At the same time, the change curve of the number of Si-O bonds over time is also statistically analyzed as shown in Fig. 3h. It can be observed that in the early stage, with the contact between amorphous Ga_2O_3 and 4H-SiC, the number of Si-O bonds increases rapidly. Afterwards, the bonding rate slows down, indicating that the reaction of Ga_2O_3 and SiC to form SiO_2 is not a slow process. At the same time, the number of Si-O bonds increases steadily over time with no saturation trend, indicating that SiC will continue to be oxidized.

To validate the accuracy of ReaxFF in describing the energy variations during MD simulations, the formation energy of SiO_2 obtained from DFT was compared with that from ReaxFF. As shown in Supplementary Fig. 10a, the two values are in close agreement, with only a-1.3% difference, confirming that the ReaxFF potential can reliably capture the energy change during the SiO_2 formation process. In addition, to further verify the reliability of the employed potential, we calculated the binding energies of the O–SiC, O–Ga_2O_3, C–SiC, and Si–Ga_2O_3 systems using DFT, and ReaxFF-based MD, as shown in Supplementary Fig. 10b. Both methods exhibit consistent trends. The Si–Ga_2O_3 binding energy is positive, suggesting that Si atoms released from SiC do not tend to bond directly with Ga_2O_3 but are more likely to undergo alternative reactions such as SiO_2 formation. This observation is consistent with the reaction pathway identified in our MD simulations of Ga_2O_3 and SiC.

Characterization of interfacial heat transfer properties

To investigate the covalent bond formation within the Ga_2O_3/SiC interface based on the heat transfer characteristics, the ITC values were measured via the time-domain thermoreflectance (TDTR) experiment, as depicted in Fig. 4a. The experimental details of the TDTR measurements are provided in Supplementary Section 2. The thickness of SiO_2 layer as a function of time at different temperatures is shown in Fig. 4b and corresponding ITC values as a function of thickness of SiO_2 layer are presented in Fig. 4c. The amplitudes of TDTR signals versus the delay time and their best fits are shown in Supplementary Figs. 7–9. The corresponding results are summarized in Supplementary Table 4. The ITC value of the untreated sample was found to be 17.5 MW/m²·K. After covalently bonded treatment in 1173 K, the emergence of covalent bonds led to an exponential increase in ITC to 100.9 MW/m²·K. Once the thickness of SiO_2 layer increased to 5.8 nm, the ITC achieved a value of 162.1 MW/m²·K, which was nine times higher than that of the sample undergoing the VdW interactions. At 1073 K, SiO_2 can be formed after 60 minutes, but at a much slower rate compared to the 1173 K conditions. For similar thickness, its ITC is also slightly lower than that of the 1173 K annealing conditions. When the temperature is raised to 1273 K, the rate of SiO_2 formation increases, but the quality significantly decreases, resulting in a final ITC much lower than that of the 1173 K annealing conditions. This result demonstrated that the low interface thermal resistance (ITR) can be achieved through the formation of covalent bonds, enhancing heat transport compared to the VdW interactions, which was consistent with the previous research[51,52]. SiO_2 itself has a low thermal conductivity, and an excessively thick layer of SiO_2 significantly increases the interfacial thermal resistance. However, since the phonon mean free path of SiO_2 is about 6 nm, the thermal conductivity decreases further when its thickness is less than 5 nm. In addition, the interfacial mass also has an important effect on the thermal conductivity. Therefore, under the premise of maintaining covalent bonding, it is experimentally measured that when the thickness of the SiO_2 layer is 5.8 nm, an optimal balance between thickness and interfacial mass can be achieved, resulting in the highest interfacial thermal conductivity. Meanwhile, the thermal conductivity of the Ga_2O_3 film before treatment was 5.7 W/m·K. The heat treatment eliminated defects within the Ga_2O_3 film, causing thermal conductivity to achieve to 6.2 W/m·K. Nevertheless, the thermal conductivity value of the defect-optimized film remained lower than the levels of 10–27 W/m·K reported for bulk materials[15,16]. This discrepancy is due to the fact that the phonon mean free path of Ga_2O_3 is on the order of hundred nanometers (up to 700 nm) in the [010] direction[53]. Thus, in the layers thinner than the phonon mean free path, the phonon-boundary scattering significantly affects thermal conductivity values, especially for films thinner than 100 nm[27]. The room-temperature ITC values of Ga_2O_3 with different high-thermal conductivity substrates (GaN, Sapphire, SiC, and Diamond) are summarized in Table 1, indicating that the ITC values obtained in this work exceeded those from other reports. However, when the thickness of SiO_2 layer increased to 6 nm, the ITC exhibited a slight decrease to 148.4 MW/m²·K, primarily due to the deterioration of the interfacial structure caused by the prolonged heat treatment. This led to a significant increase in interface defects, such as atomic mixing, disorder, dislocations and roughness, which altered the phonon transmission path and reduced thermal transfer efficiency[54,55]. For instance, multiple reflections at the interface impaired phonon transmission, while increasing the interface roughness and enhancing diffuse reflection of phonons.

An in-depth analysis was conducted to elucidate the interfacial heat transfer mechanisms of covalent bonding and VdW force contacts using molecular dynamics (MD) simulations, with the computational details provided in Supplementary Section 1. Three distinct interface structure models for the Ga_2O_3/SiC and Ga_2O_3/SiO_2/SiC trilayer composite structure were constructed, as depicted in Fig. 4d, g, j. Additionally, to validate the accuracy of the constructed model, binding energies were calculated in non-reactive molecular dynamics simulations. The results are shown in Supplementary Fig. 10b. It can be observed that these results are consistent with those obtained from ab initio and MD calculations with the ReaxFF potential. The relevant heat flux results are displayed in Fig. 4e, h, k. The heat flow value of 400 eV/ns associated with covalent bonding was found to be higher by an order of magnitude than that relying on VdW forces. In the covalently bonded interface, the thermal resistance was drastically reduced from the hot source to the cold end. The corresponding temperature profiles are illustrated in Fig. 4f, i, l. Compared to the direct Van der Waals contact between Ga_2O_3 and SiC, the insertion of a SiO_2 layer introduces an additional van der Waals-bonded interface, resulting in a higher ITR due to the presence of this extra interface and the low thermal conductivity of SiO_2. Figure 4i also indicated that the ITR between SiC and SiO_2 was smaller than the respective value between Ga_2O_3 and SiC. This discrepancy is attributed to stronger VdW forces between SiC and SiO_2, resulting in a tighter bond at the interface, which promoted heat transfer and consequently decreased the ITR. It was evident that the temperature difference between the Ga_2O_3 and SiC interfaces decreased dramatically, following the formation of covalent bonds. Furthermore, the temperature distribution suggested that the ITC of SiO_2 with Ga_2O_3 was greater than that with SiC, which was due to the better thermal property matching between Ga_2O_3 and SiO_2. Some researchers have also found through simulations of different intermediate layer materials that SiO_2 can act as a phonon bridge, transmitting phonon vibrations on both sides of Ga_2O_3 and SiC to improve the ITC[56]. This work further constructed a covalent bond connection through SiO_2, which greatly improved the thermal conductivity of the interface. Using the heat flow and temperature

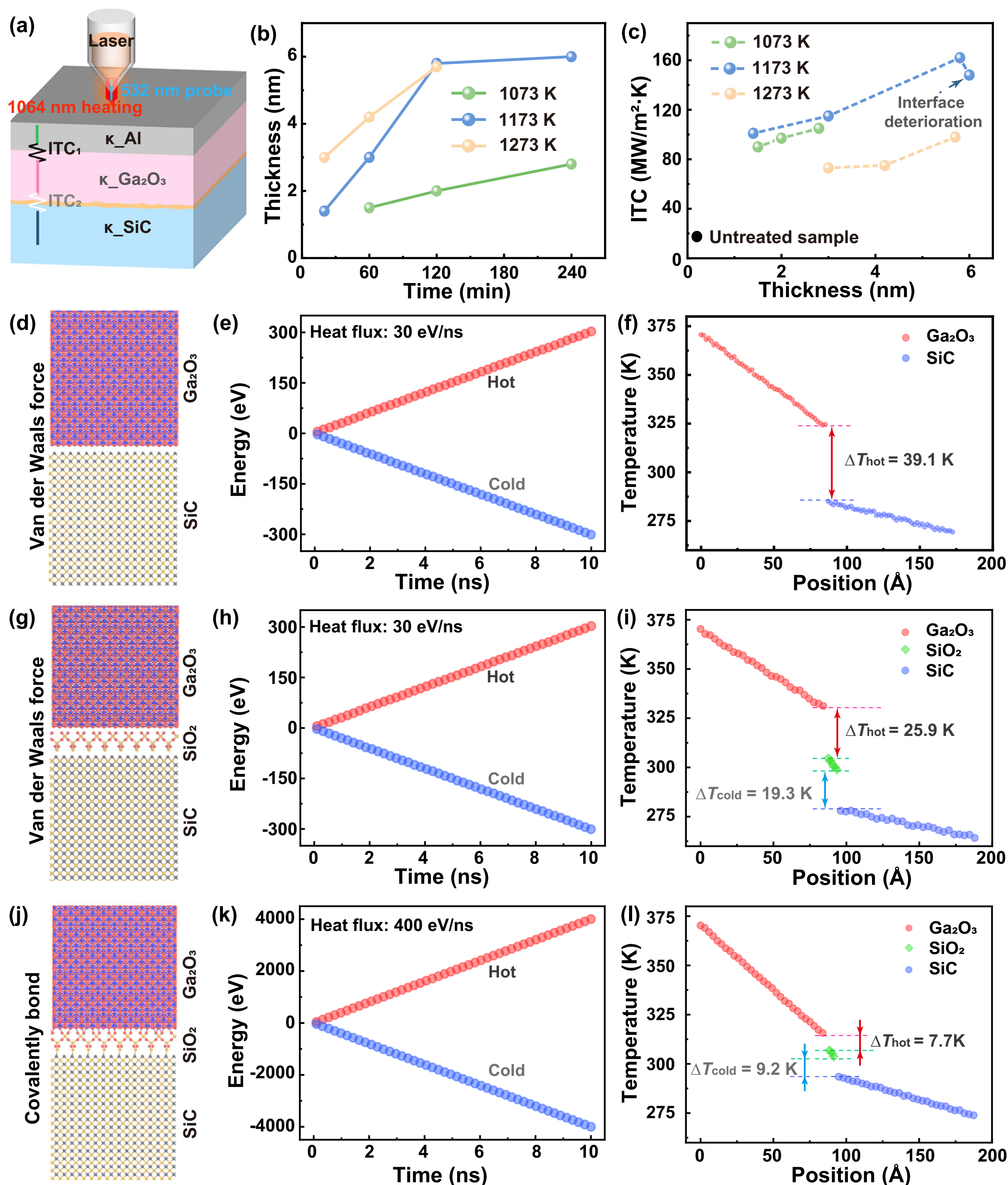

Fig. 4 | The TDTR experimental and MD simulation analysis of interfacial thermal transport across Ga_2O_3/SiC and Ga_2O_3/SiO_2/SiC heterojunctions with different bonding configurations. a Schematic diagram of the sample structure and the TDTR experiment. **b** The thickness of SiO_2 layer as a function of time at different temperatures. **c** The ITC values established via the TDTR measurements at different thickness of SiO_2 layer. **d**, **g**, **j** Structural modeling for molecular dynamics calculations at the Ga_2O_3/SiC interface bonded by (**d**) VdW and Ga_2O_3/SiO_2/SiC interface bonded by (**g**) VdW and (**j**) covalent interactions. The accumulative energy of the heat source and heat sink of the Ga_2O_3/SiC interface bonded by (**e**) VdW and Ga_2O_3/SiO_2/SiC interface bonded by (**h**) VdW and (**k**) covalent interactions. Typical temperature profiles of the Ga_2O_3/SiC interface bonded by (**f**) VdW and Ga_2O_3/SiO_2/SiC interface bonded by (**i**) VdW and (**l**) covalent interactions.

difference at the interface, the ITC can be calculated as[40]:

$$G = \frac{J}{A\Delta T} \quad (2)$$

where J represents the heat flux continuity at the interface, A is the cross-sectional area for energy transfer (900 Å^2 in this model), and ΔT is the temperature jump at the interface. For the Ga_2O_3, SiO_2, and SiC layers connected through VdW interactions, the ITC values were

Table 1 | The ITC values for different high-thermal conductivity substrates

Substrate	Preparation Method	Characterization	TBC (MW/m²·K)	Ref.
SiC	Covalent bond	TDTR	162.1	This work
SiC	Ion-Cut, 30 nm Al_2O_3 buffer	TDTR	72	Ref. 27
SiC	Ion-Cut, 30 nm Al_2O_3 buffer, annealed	TDTR	65	Ref. 27
SiC	Ion-Cut, 9 nm Al_2O_3 buffer	TDTR	100	Ref. 27
SiC	Ion-Cut, 9 nm Al_2O_3 buffer, annealed	TDTR	88	Ref. 27
SiC	Fusion bonding	TDTR	21.2	Ref. 25
SiC	Ion-Cut	TDTR	21.2	Ref. 72
SiC	MBE	TDTR	142	Ref. 73
SiC	Bonding	TDTR	10	Ref. 74
SiC	MBE	TDTR	141	Ref. 42
SiC	Ion-Cut, 20 nm Al_2O_3 buffer	TDTR	60	Ref. 24
SiC	Ion-Cut, 20 nm Al_2O_3 buffer, annealed	TDTR	133	Ref. 24
SiC	Ion-Cut	TDTR	91	Ref. 24
SiC	Ion-Cut, annealed	TDTR	105	Ref. 24
Diamond	Mechanically exfoliated	TDTR	17	Ref. 29
Diamond	Mechanically exfoliated	Raman thermometry	7.58	Ref. 75
Diamond	ALD	TDTR	136	Ref. 30
Diamond	CVD	TDTR	110	Ref. 76
Diamond	ALD	TDTR	19.2	Ref. 31
Diamond	PLD + AlN buffer	TDTR	61	Ref. 77
GaN	Thermal oxidation of GaN	TDTR	31.2	Ref. 78
Sapphire	MBE	TDTR	156	Ref. 72
Sapphire	MBE	TDTR	155	Ref. 42

20.6 MW/m²·K between Ga_2O_3 and SiO_2 and 27.7 MW/m²·K between SiO_2 and SiC. Once the covalent bonding formed within the Ga_2O_3/SiO_2/SiC structure, there was an order of magnitude enhancement in thermal conductivity. The ITC value between Ga_2O_3 and SiO_2 reached 919.9 MW/m²·K, while that between SiO_2 and SiC was measured to be 773.9 MW/m²·K.

Characterization of thermal management capabilities

The effects of covalent bonding and interfacial thermal conductivity enhancement were demonstrated at the atomic scale using MD. In order to further elaborate the intrinsic mechanism, finite element simulation was carried out on the micrometer scale, and the corresponding simulation structure was shown in Fig. 5a, and more detailed simulation details are shown in Supplementary Fig. 11 and Supplementary Tables 5–6 of the Supporting Information. In the computational results of Fig. 5b–d, it can be seen that when 5.8 nm of SiO_2 forms covalent contacts with Ga_2O_3 and SiC, respectively, the corresponding interfacial temperature changes are consistent with that of Fig. 4, and the interfacial temperature difference (temperature difference = 72.5 K) is significantly lower than that in the case of VdW contact (temperature difference = 90.4 K). In addition, we calculated the heat flux of the covalent contact based on this steady-state temperature distribution, and it is 2.23×10^9 pW/μm², which is 187% higher than that of the VdW contact (7.77×10^9 pW/μm²), and the excellent heat transfer performance of the covalent contact is directly proved at the micrometer scale.

To evaluate the heat dissipation ability of the Ga_2O_3/SiC heterojunction, the VdW and covalently bonded samples were further compared conforming to the experimental design in Fig. 5e. First, samples of the same size were placed on a cold stage and maintained at room temperature. The temperatures of both samples were then increased rapidly upon illumination at 390 mW/cm², reaching thermal equilibrium. Eighty-five seconds after the light was turned off, the temperature dropped rapidly and gradually returned to room temperature, as shown in Fig. 5f. Corresponding temperature distributions of the samples surface captured in situ at different time were shown in Fig. 5g. Moreover, the surface temperature of the as-deposited specimen increased more rapidly than that of the covalent bond sample. Notably, the peak temperature of the as-deposited sample reached a value of approximately 76 °C, which was about 29 °C higher than that of the thermally treated sample. This confirmed that the covalent bonded sample possessed a superior ITC. Supplementary Fig. 12 of Supporting Information presents a histogram illustrating the measured heating and cooling rates for the samples. During the heating process, sample bonded via VdW forces exhibits a rapid rise in surface temperature, primarily due to the inefficient thermal conduction through the SiC substrate. In contrast, covalently bonded sample demonstrates a significantly lower surface heating rate, attributed to its higher ITC. Moreover, the surface temperature of the covalently bonded sample reaches equilibrium more quickly compared to their VdW bonded counterparts. The results highlight significantly improved thermal transport efficiency during both the heating and cooling processes in the covalently bonded sample.

In order to quantitatively evaluate the impact of heat dissipation on the electrical properties of the device, the on-state characteristics of Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) with homogeneous and heterogeneous SiC substrates were further investigated via a technology computer-aided design (TCAD) approach[20], as shown in Fig. 5h. In the heterogeneous MOSFET structure, different ITC values between Ga_2O_3 and SiC were set. To observe the effect of ITC on heat dissipation, the lattice temperature maps and zoomed-in views of localized hotspots were acquired, as shown in Fig. 5i. Because of the low thermal conductivity value of Ga_2O_3, the homogeneous substrate exhibited a large high-temperature area within the MOSFET. At the low ITC (17.5 MW/m²·K), heat remained trapped within the Ga_2O_3 layer and was not efficiently conducted to the SiC substrate. In contrast, once the ITC increased to 162.1 MW/m²·K, the SiC substrate effectively conducted heat away

https://doi.org/10.1038/s41467-025-65750-8

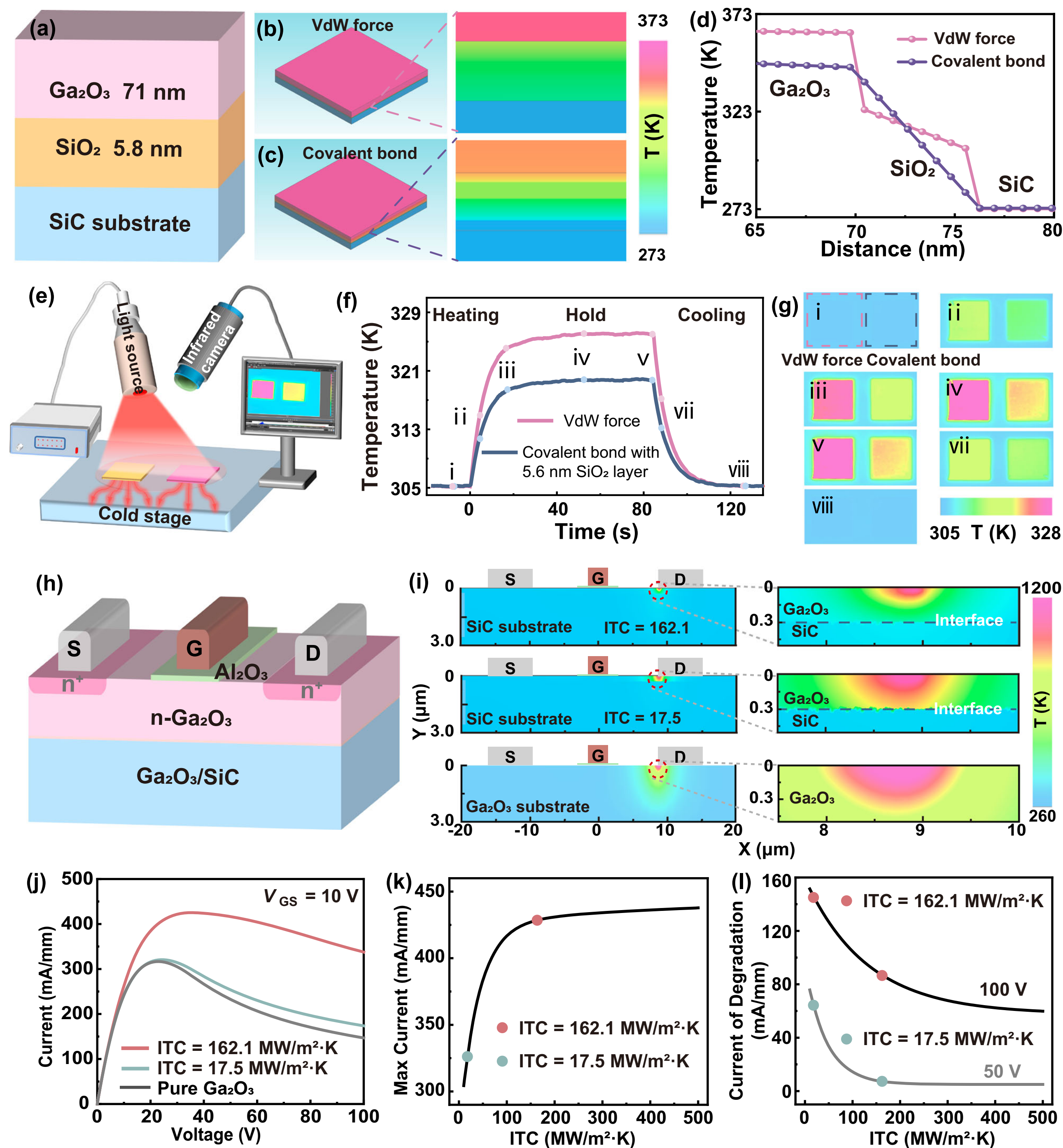

Fig. 5 | Multiscale simulation and experimental characterization of interfacial thermal transport across Ga_2O_3/SiC heterojunctions. a Schematic diagram of Finite Element Method simulations. **b**, **c** The comparison of heat dissipation capability based on simulated profiles. **d** The temperature profiles of the different interface. **e** Schematic diagram of the infrared thermography measurements. **f** The surface temperature evolution of VdW force and covalent bond samples as a function of time, captured with an infrared camera. **g** Corresponding temperature distributions of the samples surface captured in situ at different time. **h** Schematic illustrations of the MOSFET device. **i** Simulated 2D heat maps of the cross-section of the MOSFET device. **j** I_D as a function of V_D at different ITC values. **k** Maximum I_D as a function of ITC values. **l** I_D of degradation as a function of ITC values.

from the device, reducing the internal temperatures. The output characteristics of various MOSFET structures are displayed in Fig. 5j at a gate voltage (V_{GS}) of 10 V. Then, the maximum I_D as a function of ITC values was summarized in Fig. 5k. The SiC substrate enhanced the peak current of the Ga_2O_3 MOSFET, and the output current degradation of the Ga_2O_3 device on the SiC substrate with 17.5 MW/m²·K of ITC was less pronounced than that of the homogeneous Ga_2O_3 device with the increase in drain voltage. Once the ITC rose from 17.5 to 162.1 MW/m²·K, the output current of the MOSFET increased from 321 to 425 mA/mm, representing a roughly 104 mA/mm enhancement. The maximum output current rises significantly, eventually approaching its limit at around 200 MW/m²·K. Additionally, the I_D of degradation as a function of ITC values was summarized in Fig. 5l. When the drain voltage reaches 100 V, the current degradation decreases from 147 to 87 mA/mm as the ITC increases from 17.5 to 162.1 MW/m²·K, indicating that enhancing the ITC significantly alleviates the self-heating effect.

When the ITC exceeds 300 MW/m²·K, the performance begins to stabilize near its maximum value. Furthermore, the device exhibits low heat generation during low-voltage operation at 50 V. For devices with an ITC of 162.1 MW/m²·K, the current only decreased by 9 mA/mm from the maximum value, while samples with an ITC of 17.5 MW/m²·K decreased by 67 mA/mm. It is well known that the carrier mobility decreases exponentially with the increasing temperature[35,57]. Therefore, increasing the ITC of the SiC/Ga_2O_3 heterojunction can effectively improve performance, stability, and reliability of the device. Additionally, the large bandgap of SiO_2 (approximately 8 eV) effectively prevents the leakage current conduction to the substrate, enhancing energy efficiency and thus reducing power consumption, extending device lifetime, and improving electrical performance, particularly in high-power applications[58,59].

In summary, the heat dissipation of a Ga_2O_3 film on the SiC substrate was successfully enhanced through a simple route consisting of the formation of covalent bonds, which is compatible with existing production lines. Furthermore, we conducted TCAD simulations by treating the ITC derived from the experimental tests on both covalent and VdW contacts as a variable. The results showed that the increase of ITC from 17.5 to 162.1 MW/m²·K significantly reduced the impact of the self-heating effect, leading to an 83 mA/mm improvement in the maximum output current of the MOSFET along with a notable drop in the local junction temperature. By optimizing the heat treatment process, the microstructure at the interface was adjusted so as to facilitate the formation of robust covalent bonds and the creation of effective phonon transport channels. Time-domain thermoreflectance (TDTR) measurements revealed that the ITC between Ga_2O_3 and SiC after the covalent bond formation achieved a remarkable value of 162 MW/m²·K, representing a nine-fold increase compared to the van der Waals (VdW) force connection (17.5 MW/m²·K). Furthermore, the NJTM approach was applied to enhance the ITC whereby the bonding temperature of samples exposed to intense illumination was reduced by approximately 29 °C relative to those with VdW connections. This significantly enhanced performance and reliability of the appliance. Moreover, in-situ XPS studies during the deep etching confirmed the formation of SiO_2 upon heat treatment. The Si-O and Si-C covalent bonds at the interface ensured the effective phonon transport, in which the SiO_2 layer acted as a phonon bridge between Ga_2O_3 and SiC. MD simulations further confirmed that the formation of covalent bonds considerably increased the heat flow at the interface, thereby reducing its thermal resistance. The ITC value between Ga_2O_3 and SiO_2 was enhanced by approximately 40 times compared to that in the case of VdW forces, reaching an impressive value of 919.9 MW/m²·K. Through the comprehensive experimental and theoretical analyses, it was concluded that introducing a SiO_2 layer between Ga_2O_3 and SiC was conducive to the formation of covalent bonding, significantly enhancing heat diffusion and providing a promising strategy to address the low thermal conductivity of Ga_2O_3.

Methods

Sample preparation

The Ga_2O_3 films were deposited onto 4H-SiC substrates by means of a BENEQ TFS200 ALD system (BENEQ Inc., Espoo, Finland). The growth temperature was maintained at 473 K using Trimethylgallium (TMGa) and high-purity O_2 (99.995%) as Ga and O precursors and N_2 as the carrier gas. The precursor for the oxygen was O_2 plasma, which was activated at a power of 200 W. For every cycle, TMGa and O_2 plasma were applied for 50 ms and 8 s, respectively. After that, the chamber was purged for 2 s with Ar gas at the end of each step. The thickness of Ga_2O_3 films was kept at around 75 nm. The fabricated Ga_2O_3 films were annealed in a tube furnace under an O_2 atmosphere. To investigate the effect of annealing conditions, post-annealing was conducted at 1073 K for 60, 120, and 240 minutes; at 1173 K for 20, 60, 120, and 240 minutes; and at 1273 K for 20, 60, and 120 minutes.

Characterization

The XRD measurements (Bruker D8 ADVANCE) were carried out using Cu Kα radiation (λ = 1.54 Å) at a scanning speed of 2.5°/min to obtain the information about the crystal structure, surface morphology, and microstructure of Ga_2O_3 thin films. The X-ray reflection (XRR) was tested by D8 Discover from Bruker. The cross-sectional microstructures and elements distributions were observed via the transmission electron microscopy (TEM, Talos F200x) coupled with energy-dispersive X-ray spectroscopy (EDS). The cross-sectional TEM lamellar samples were fabricated by means of a dual-beam focused ion beam (FIB) system (Thermo Scientific, Helios 5 CX). X-ray photoelectron spectroscopy (XPS, Shimadzu AXIS SUPRA +) was employed to characterize the chemical state and the interior of samples after exposure to Ar^+ ion etching. The XPS spectra were calibrated with reference to the C 1 s peak (284.8 eV) from adventitious carbon. This work employs the Autinst Pioneer ONE TDTR system for measurement for the thermal characteristics, as described in detail in Supplementary Section 2. All characterizations were conducted at room temperature. Infrared thermography (FLIR A325sc) was utilized to in situ monitor the temperature evolution of the samples.

Simulation and calculation

Density functional theory (DFT) calculations were carried out to evaluate the reaction energies between Ga_2O_3 and SiC. The DFT simulations were done using the projector augmented plane-wave basis embedded in Vienna ab-initio simulation package[60]. During simulations, the plane waves were cut-off at 400 eV. The exchange-correlation functionals of electrons were described in terms of generalized gradient approximations proposed by Perdew, Burke, and Ernzerhof[61]. A DFT-D3 approach was utilized to capture the long-range VdW interactions[62]. The Brillouin zone was sampled by employing resolutions better than 0.05 $Å^{-1}$, using the Monkhorst-Pack scheme[63]. For the heterostructure model, a vacuum of 15 Å was applied along the thickness direction so as to eliminate the interactions between periodic images. The energy converge criterion for solving the self-consistent Kohn-Sham equations was kept at 10^{-5} eV. All the structures were fully optimized until the residual Hellman-Feynman forces and stresses were below 0.05 eV/Å. The reaction energy was calculated as follows:

$$E_{reax} = E[CO(g)] + E\left[SiO_2\right] + 2E[Ga] - E\left[Ga_2O_3\right] - E[SiC]$$

where $E[CO(g)]$ is the energy of CO gas, and $E[Ga]$ is the energy of Cmce-Ga. The Langevin dynamic algorithm was utilized to simulate the NpT ensemble[64,65] at the time interval of 2.0 fs.

Molecular dynamics (MD) simulations with LAMMPS package[66] were performed to examine the reaction process between Ga_2O_3 and SiC that leads to the formation of SiO_2. The reactive force fields (ReaxFF) are utilized to describe the interaction potentials between atoms[67,68]:

$$E_{system} = E_{bond} + E_{over} + E_{under} + E_{lp} + E_{val} + E_{tor} + E_{vdW} + E_{Coulomb} + E_{qeq}$$

in which E_{bond} denotes the bonding energy, E_{over} and E_{under} are energy penalty to prevent over- and undercoordination, E_{lp} is the energy of long-pairs of atoms, E_{val} and E_{tor} are three-body energy from valence angle and four-body torsions, E_{vdW} is van der Waals dispersion energy, $E_{Coulomb}$ is electrostatic energy and E_{qeq} is the charge equilibrium energy[67,69,70]. The force field parameters are in line with former study, which is suitable to describe the interations between SiC, Ga and oxygen[71]. The time step for integration of equation of motion is 0.1 fs. For the simulation of annealing to obtain amorphous Ga_2O_3 film structure, the NpT ensemble with temperature of 2600 K is utilized and 50 ps is to conducted to drive the system into liquid phase. Then, another 100 ps simulations is utilized to quench the temperature to

300 K to obtain amorphous. For the simulation of SiC/amorphous Ga_2O_3, 1 ns simulation is conducted in total, under NpT ensemble. To accelerate the chemical processes, temperature is set to 2000 K.

The MD simulation also was analyzed the heat transfer behavior in Ga_2O_3/SiC and Ga_2O_3/SiO_2/SiC heterostructures. The whole process was done using LAMMPS molecular dynamics software. The cvff parameter was chosen to describe the force field, and periodic boundary conditions were applied. The equilibrium molecular dynamics simulations were carried out within a certain system, and the NVT equilibrium system was employed. The kinetic time was set to 10 ns and 1 fs as the time step. The NPT simulations were then performed under a standard atmospheric pressure of 1 kPa and a temperature T of 300 K. The running kinetic time was 10 ns. The thermal conductivity along the x-direction was assessed by means of the non-equilibrium molecular dynamics. The right-end region of the model was set as a cold source (200 K), while the left-end of the module was set as a hot source (370 K). After 1 ns of structural relaxation, the temperature distribution tended to achieve dynamic equilibrium over the space along the x-direction. The cross-sectional area of the model was 30 × 30 Å. The formulas and parameters for non-bonded interactions and covalent bond interactions were shown in Supplementary Section 1.

The formation energy of SiO_2 and the binding energies with different systems were calculated. The calculations of density functional theory are done with the projector augmented plane-wave basis, which is implemented in Vienna ab-initio simulation package[60]. And the plane-waves are cut-off at 400 eV. The exchange-correlations of electrons are described by the generalized gradient approximations with the form proposed by Perdew, Burke, and Ernzerhof[61]. DFT-D3 approach is utilized to capture the long-range van der Waals interactions[62]. The Brillouin zone is sampled with resolutions better than 0.05 $Å^{-1}$, using the scheme of Monkhorst-Pack[63]. A vacuum of 15 Å is placed at thickness direction to eliminate the interactions between periodic images. The energy converge criterion for solving self-consistent Kohn-Sham equations is 10^{-5} eV. All the structures all fully optimized until the residual Hellman-Feynman Forces and stresses below 0.05 eV/Å. The forcefield calculations are done with LAMMPS package[66]. The reactive force fields (ReaxFF) are utilized to describe the interaction potentials between atoms[67,68]:

$$E_{system} = E_{bond} + E_{over} + E_{under} + E_{lp} + E_{val} + E_{tor} + E_{vdW} + E_{Coulomb} + E_{qeq}$$

in which E_{bond} denotes the bonding energy, E_{over} and E_{under} are energy penalty to prevent over- and undercoordination, E_{lp} is the energy of long-pairs of atoms, E_{val} and E_{tor} are three-body energy from valence angle and four-body torsions, E_{vdW} is van der Waals dispersion energy, $E_{Coulomb}$ is electrostatic energy and E_{qeq} is the charge equilibrium energy[67,69,70]. The force field parameters are in line with former study, which is suitable to describe the interations between SiC, Ga and oxygen[71]. The binding energy is calculated via

$$E_b = E[AB] - E[A] - E[B]$$

where $E[AB]$ is the energy of linked system, and $E\left[A/B\right]$ is the energy of individual system. The formation energy of SiO2 is defined by:

$$E_{form} = E\left[SiO_2\right] - E[Si] - E\left[O_2(g)\right]$$

where $E\left[SiO_2\right]$ is the energy of α-SiO_2, $E[Si]$ is the energy of Si, $E\left[O_2(g)\right]$ is the energy of oxygen molecule.

In addition, TCAD simulations were used to model two types of Ga_2O_3-based MOSFETs, namely Ga_2O_3 and Ga_2O_3/SiC devices, in order to investigate their electrical characteristics. Both kinds of devices had the same structure which consisted of a 20-nm-thick Al_2O_3 dielectric, a~ 300-nm-thick Ga_2O_3 drift layer with the low dopant content of $5 \times 10^{17}\,cm^{-3}$, and a semi-insulating Ga_2O_3 or SiC substrate with the lower dopant of $1 \times 10^{13}\,cm^{-3}$. The total device length, source-to-gate spacing (L_{GS}), gate length (L_G), and gate-to-drain spacing (L_{GD}) were set to 40, 11, 2, and 11 μm, respectively. The source and drain had highly dopant content of $1 \times 10^{19}\,cm^{-3}$.

Data availability

All data supporting the results of this study are available in the manuscript or the supplementary information. Additional data are available from the corresponding author upon request. Source data are provided with this paper.

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Acknowledgements

W.D. acknowledges support from the National Key R&D Program of China (2022YFA1203100) and the National Natural Science Foundation of China (62574209); H.P.M. acknowledges support from the Science and Technology Innovation Plan of Shanghai Science and Technology Commission (No. 21DZ1100800, 23ZR1405300); Q.J.Z. acknowledges support from the Science and Technology Innovation Plan of Shanghai Science and Technology Commission (20501110700, and 20501110702); Q.L.Y. acknowledges support from the National Natural Science Foundation of China (52302202); N.J. acknowledges support from the Yongjiang Talent Introduction Program of Ningbo (2021A-037-C and 2021A-108-G).

Author contributions

Y.S. carried out the experiment and test, including growing the material and performing physicochemical characterization results and wrote the original draft. X.Q., Y.D.G., Q.M.H. and C.X.D. simulated the TCAD. Y.S., X.Q., Y.L., Q.M.H., Q.L.Y., L.G., W.J.C. and F.Y.S. organized the data. W.D., N.J., Q.J.Z.and H.P.M. supervised the complete work. M.Y.Y., Z.L.J. did first-principle calculation. W.D., C.T.L. and H.P.M. reviewed and edited the original draft. All authors discussed the results and remarked on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41467-025-65750-8.

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Peer review information *Nature Communications* thanks Mykola Isaiev, Riccardo Rurali and the other anonymous reviewer(s) for their contribution to the peer review of this work. A peer review file is available.

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