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High-density three-dimensional integration of dynamic random-access memory using vertical dual-gate IGZO TFTs

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An architecture for three-dimensional integration of dynamic random-access memory that enables higher memory density is presented as a new solution to the bottleneck currently faced in artificial intelligence deployment. The basis of this architecture is a vertical dual-gate two-transistors-zero-capacitor memory cell which yields a small feature size and reliable read operation, and naturally scalable to large-scale arrays. However, three-dimensional integration of the dynamic random-access memory faces highly-limiting challenges related to lateral misalignment and thermal cycling as a result of separate stacking processes. To solve the issues of cell misalignment and thermal cycling, a single step process is used to stack the dual-gate In-Ga-Zn-O transistors simultaneously. By optimizing the contact metallization and its interface through an in-situ ozone oxidation method, the vertical dual-gate transistor exhibits a high on-state current and small subthreshold slope as well as high thermal stability and device variation. Furthermore, a four-bit multi-bit operation is demonstrated with an ultra-scaled 4F^2 two-transistors-zero-capacitor dynamic random-access memory to further increase the storage density. The approach presented here provides a promising alternative to high-density three-dimensional dynamic random-access memory integration as a means for more efficient near memory computing for artificial intelligence systems.

With the rapid expansion of computational technologies, we are witnessing an increasing demand for storage solutions that are higher in capacity, faster, and more efficient. This is particularly true for artificial intelligence (AI) systems such as deep learning, machine learning and big data processing, which require large volumes of training data and model parameters[1–3]. These applications present significant challenges for the development of future memory systems.

Large-scale dynamic random-access memory (DRAM) arrays, when juxtaposed with the central processing unit (CPU), enabled by back-end-of-line (BEOL) integration, can provide higher speed and

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lower latency for data transfer between the CPU and memory, potentially offering a solution to these challenges[4–6]. The conventional DRAM based on the one-transistor-one-capacitor (1T1C) architecture has faced the inherent limitation: the necessity to scale down capacitors in high aspect ratio geometries in accordance with advanced process nodes[7–9]. Therefore, the ubiquitous 1T1C DRAM does not lend itself to BEOL integration.

Most amorphous oxide semiconductors with their wide bandgap and relatively low defect density, hence low off-state current, are amenable to BEOL-processing as they can be manufactured at low temperatures. This is particularly true for indium gallium zinc oxide (IGZO) thin film transistors (TFTs)[10–16]. By replacing the capacitor in the 1T1C DRAM with a gate oxide capacitance, a two-transistor-zero-capacitor (2T0C) DRAM can be realized[17–33]. This architecture first proposed by IMEC implemented using IGZO transistors yields a long data retention time, with no constraints in stacking for high density, showing great promise for BEOL DRAM applications[20–26]. IGZO-based 2T0C DRAM can also be used as on-chip memory with high bandwidth, concurrent access, and low latency for AI systems by BEOL integration. Here on-chip memory directly integrated onto the processor chip (such as CPU, GPU, NPU, etc.) can provide higher bandwidth, lower access speed and lower latency compared to off-chip memory. Furthermore, multi-bit storage operation in 2T0C is also demonstrated for further increasing storage density with more data in single cell[18,24,25,32]. Despite the many advantages, the two SG transistor structure is costs bit-cell area and faces unreliable read issue and IR drop issue at the array level. In this vein, the vertical DG 2T0C cell in the work reported here shows the following advantages: (1) achieves $4F^2$ bit-cell area by the self-aligned single-step (SASS) process. (2) Dual-gate structures eliminate the typical unreliable read issue and IR drop issues. The layout design of the array is presented in Supplementary Fig. 1, where two WLs and BLs form a crossbar structure, with the etching holes besides the sidewalls. The deposition process for the gate stack and channel layer is also exhibited in Supplementary Fig. 1. In detail, the gate stack and channel layer (IGZO/HfO_2/IZO) are deposited in single ALD process and pattering under one mask which is shown in the yellow region in Supplementary Fig. 1c.

However, creating a 3D integration DG 2T0C cell remains a challenge. Any lateral misalignment resulting from vertical stacking of the write/read transistor in the bit cell would introduce coupling issues and increased area[17]. Additionally, V_{TH} shift and channel current variation in the TFT, following a relatively complex fabrication flow, can pose reliability issues. To circumvent these limitations, we present a novel SASS process wherein both T_R and T_W were simultaneously integrated within a single channel deposited process. As a result, the process not only mitigates photolithographic misalignment between the upper and lower layers, but also lends to a reduction in processing steps(Supplementary Fig. 2). We have successfully fabricated vertical DG IGZO TFTs with channel length (L_{CH}) defined by the gate length (L_G), yielding an exceptionally low subthreshold slope (SS) of 63 mV/dec and ultrahigh on-state current of 50.3μA/μm at $V_{GS} = V_{TH} + 1$ V and $V_{DS} = 1$ V. Low positive bias stress temperature stability (PBTS) of 87.7 mV and negative bias stress temperature stability (NBTS) of −22.6 mV at 85 °C are achieved, demonstrating high thermal stability. The high-density $4F^2$ DRAM bit-cell achieved reliable read/write operations with an extended retention time of 350 s (>500 s) of data '1' (data '0') with large storage current ratio over 300 and multi-bit operation (4bits) is further demonstrated for high-density DRAM.

Result

Design and fabrication of $4F^2$ DG 2T0C cell

Fig. 1a–b illustrates a schematic of the multi-layers $4F^2$ DG 2T0C DRAM array and the corresponding bit-cell, which incorporates two vertical DG IGZO TFTs as write/read transistors (T_W/T_R) enabled by the SASS process. The fabrication flow of this bit-cell, as shown in Supplementary Fig. 2, is as follows: (i) deposition of T_W/T_R stack sequentially, (ii) one-step etching of T_W/T_R stacks including five electrode layers (30 nm ITO for GND/BL/SN layers, 40 nm Ta for RWL/WWL layers) and four isolation layers (40 nm SiO_2) to simultaneously form the self-aligned circular channel region in the bit-cell, (iii) Ta self-oxidized under ozone atmosphere at 250 °C for 45 mins to form high-k Ta_2O_5 gate dielectric, (iv) in-situ atomic layer deposition (ALD) of IGZO/HfO_2/IZO stack in one ALD chamber at 250 °C and patterning the triple-layers for isolation. In this process, the upper and bottom vertically-stacking DG transistors are simultaneously fabricated under single process flow, sharing the same ITO metal layer as common bit-line (BL) for interconnecting. This differs from conventional integration scheme where T_W/T_R in the bit cell are fabricated layers-by-layers and isolation with inter-layer-dielectric (ILD). This simple one-step process can efficiently reduce area overhead, fabricating cost and minimizing thermal cycling and contamination issues. Additionally, the DG 2T0C architecture in this bit-cell can provide a more reliable read scheme, immune to issues such as current sharing and IR drop in large-scale array and the dual-gate architecture can also provide additional channel protection against electrical crosstalk[15,34]. Based on the vertical channel transistors (VCT) and 3D-integration technique, the 2T0C cell can achieves ultra-high density with a smaller footprint of $4F^2$ compared to planar 2T0C of $20F^2$[35]. We believe that upward stacking of this vertical structure is feasible. Stacking upwards can be realized through the integration of layer-by-layer stacking as shown in the Fig. 1a. In detail, one inter-layer dielectric is integrated between upper/lower-layer arrays to facility stacking up. In this way, this two-layer arrays, although integrated monolithically, their BLs and WLs are controlled separately by external circuitry and do not need any interconnects between storage cells in different layers. Thus, no additional metal lines or vias are needed for interconnects. It is worth noting that, due to the source-gate interconnection, the 2T0C fabricated in this way can simultaneously couple the parasitic capacitance of T_W/T_R as a storage node (SN) to achieve a larger charge storage capacity as shown in the circuit schematic (Fig. 1e). It should also be noted that the method for creating the gate oxide by oxidizing the Ta metal gate can fundamentally meet the requirements of metal gate (resistivity)/gate dielectric (high-k) as shown in the Supplementary Fig. 3.

The cross-section transmission electron microscope (TEM) image of the $4F^2$ DG 2T0C cell and the corresponding EDX element mapping are shown in Fig. 1c, d and Supplementary Fig. 4, respectively. Consistent with the schematic diagram in Fig. 1b, five layers of electrodes are isolated by four layers of SiO_2 ILD, in which all the ILD and Ta electrodes layers have thickness of 40 nm while the ITO layer has thickness of 30 nm. No misalignment between top/bottom devices is observed, which highlights the main advantage of SASS process compared to conventional sequential integration $4F^2$ single-gate (SG) 2T0C. The channel (~6 nm IGZO) and two individual gate stacks (G_1:Ta/9 nm Ta_2O_5, G_2:15 nm HfO_2/25 nm IZO) can be clearly distinguished. The positional differences between T_R/T_W in our previous work[36] possibly originate from the sidewall dry etching process as shown in the Supplementary Fig. 5. This can be further improved by optimizing the dry etch process using a large etch selectivity process in the up/bottom layer.

To further investigate the advantage of the vertical DG IGZO TFTs, we categorize the vertical SG structures into sidewall gate, horizontal gate, GAA, and CAA based on their geometries as shown in the Supplementary Fig. 6 and Tabel S1. For comparisons between gate-all-around geometries and SG, DG structure, there exist a trade-off between control ability and fabrication complexity. Although vertical GAA structure can achieve the best performance with its gate-all-around topology, the fabrication cost of vertical devices makes it hard to scale to large arrays. Our vertical DG 2T0C cell enabled by the SASS process proposed in this work can be fabricated with less cost and achieves more reliable read operation by the DG control which GAA cannot offer.

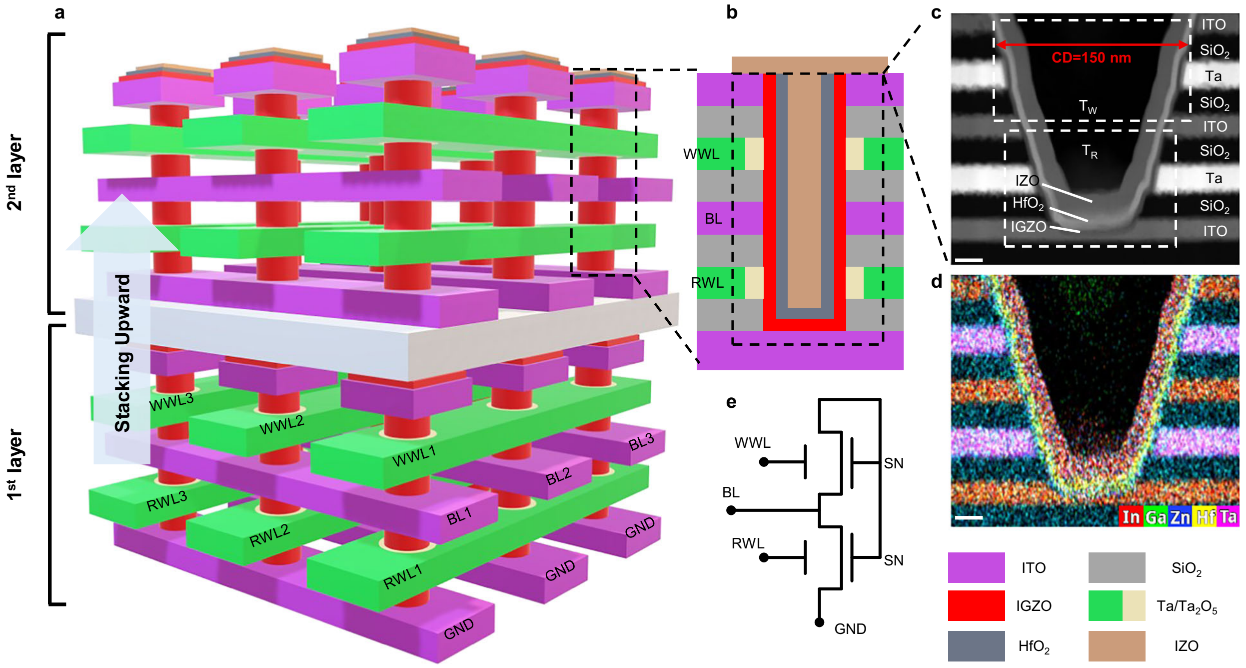

Fig. 1 | High-density dual-gate IGZO 2T0C DRAM. a Schematic illustration of $4F^2$ 2T0C DRAM array based on DG vertical channel IGZO TFTs by a self-align and single-step integration process. Stacking upwards is feasible through sequential integration. **b** Zoom-in schematic DG $4F^2$ 2T0C bit-cell including two DG IGZO TFTs as write/read transistors (T_W/T_R) fabricated by the self-aligned process. **c** Cross-section TEM image of the $4F^2$ DG 2T0C cell with CD = 150 nm. No misalignment between top/bottom devices is observed. Scale bar: 20 nm. **d** Corresponding EDX element mapping of the TEM image in (**c**), which show that the elements In, Ga, Zn, Sn, Hf, Ta are evenly distributed as expected. Scale bar: 20 nm. **e** The corresponding circuit schematic of $4F^2$ DG 2T0C cell. The additional gate of T_W increases the capacitance of the storage node.

Vertical DG IGZO TFT performance

In order to boost the driving current and achieve high-density integration in the aforementioned 3D integration DG 2T0C, a high-performance and scaled-down vertical DG IGZO TFT is necessary. To precisely optimize the device performance, we fabricate vertical DG IGZO TFTs following self-oxidation process as illustrated in Supplementary Fig. 7. The process start with multi-layer depositing including ITO S/D layers and Ta metal gate layers, and hole etching, followed by the Ta self-oxidation to form High-k Ta_2O_5 insulator, and finish by ALD IGZO and second gate stack.

Since the contact and channel regions of the vertical transistor are formed by dry etching, these regions contain numerous etching-induced defects. As a result, the performance of the VCT is severely limited by the contact and interface. To optimized the interface, we developed an in-situ O_3 self-oxidation process by performing O_3 oxidation of metal gate and depositing IGZO channel in one ALD chamber. The key step of the in-situ process is as followed: deposited multi-layer stacks (Fig. 2b), channel region etching (Fig. 2c), Ta self-oxidation to form High-k Ta_2O_5 insulator by ozone at 250 °C (Fig. 2d) and finished by ALD channel & second gate stack. The so-called in-situ process refers to the self-oxidation and ALD process being completed within the same chamber, which can improve interface between Ta_2O_5 and IGZO by reducing the impurity (Fig. 2e). Furthermore, the stronger oxidative activity of O_3 can also optimized the self-oxidation Ta_2O_5 film quality as shown in the Fig. 2f. We first evaluate leakage, breakdown and C-V characterization of self-oxidation Ta_2O_5 film as shown in the Supplementary Fig. 3. The 7 nm Ta_2O_5 grown by in-situ self-oxidation maintains low leakage current over a wide operating range, with a breakdown voltage of 5 MV/cm. Additionally, a high dielectric constant up to 21 can be extracted from the C-V characteristic curve.

Fig. 2g compare the performance of 24 randomly chosen vertical DG IGZO TFTs fabricated by the in-situ O_3 oxidation process and ex-situ O_2 oxidation process which exhibits high performance and small device-to-device variation. The corresponding fabrication flow of ex-situ O_2 process is shown in the Supplementary Fig. 8. Due to the in-situ process, both the device performance and variations have been significantly improved. Low SS of 68 ± 5 mV/dec, I_{ON} of 45 ± 5 μA/μm and V_{TH} near to zero are achieved as shown in the Fig. 2h–j. We next investigate how the deposition method, PEALD or sputtering, impact on the quality of IGZO films and device performance for vertical channel devices. As the TEM images shown in Supplementary Fig. 9, the sputtering-deposited IGZO film shows much larger thickness variation exceeding 1.5 nm and thickness attenuation compared to the target. The PEALD-deposited IGZO film shows less thickness variation of 0.3 nm and almost no thickness attenuation. The large thickness variation can lead to the increased carrier scattering, resulting in current reduction. Based on these advantages mentioned above, ALD deposition is a promising solution for vertical IGZO TFTs structure even with elevated aspect ratios[37,38].

We further carried out a contact metal optimization by investigating the influence of Mo, TiN and ITO in vertical DG TFTs. As shown in the Supplementary Fig. 10, the device with ITO contact metal exhibits remarked improvement in both I_{ON} and SS compared to the other two. Specifically, the I_{ON} increases from 0.18μA/μm at $V_{DG} = 1$ V to 7.67 μA/μm, while the SS improves from 113 mV/dec to 78.7 mV/dec. The main reason for this improvement is that ITO can effectively prevent contact metals from further oxidation during SASS heat treatment and the following ALD process. In this way, the ITO contact metal would not form an oxidized interfacial layer in contact/IGZO stack, similar like TiO_xN in TiN or MoO_x in Mo, thereby improving ITO/IGZO contact quality with lowering the width of tunneling barrier. It should be noted that contact optimization is particularly important in vertical TFTs because contact resistance accounts for a large proportion in vertical short-channel devices.

Next, in order to achieve smaller footprint of our $4F^2$ 2T0C DRAM, we performed critical dimension (CD) scaling on vertical DG IGZO TFTs. Where CD is defined as the diameter of the circular channel region as shown in the Fig. 2a. Fig. 3a–c shows TEM

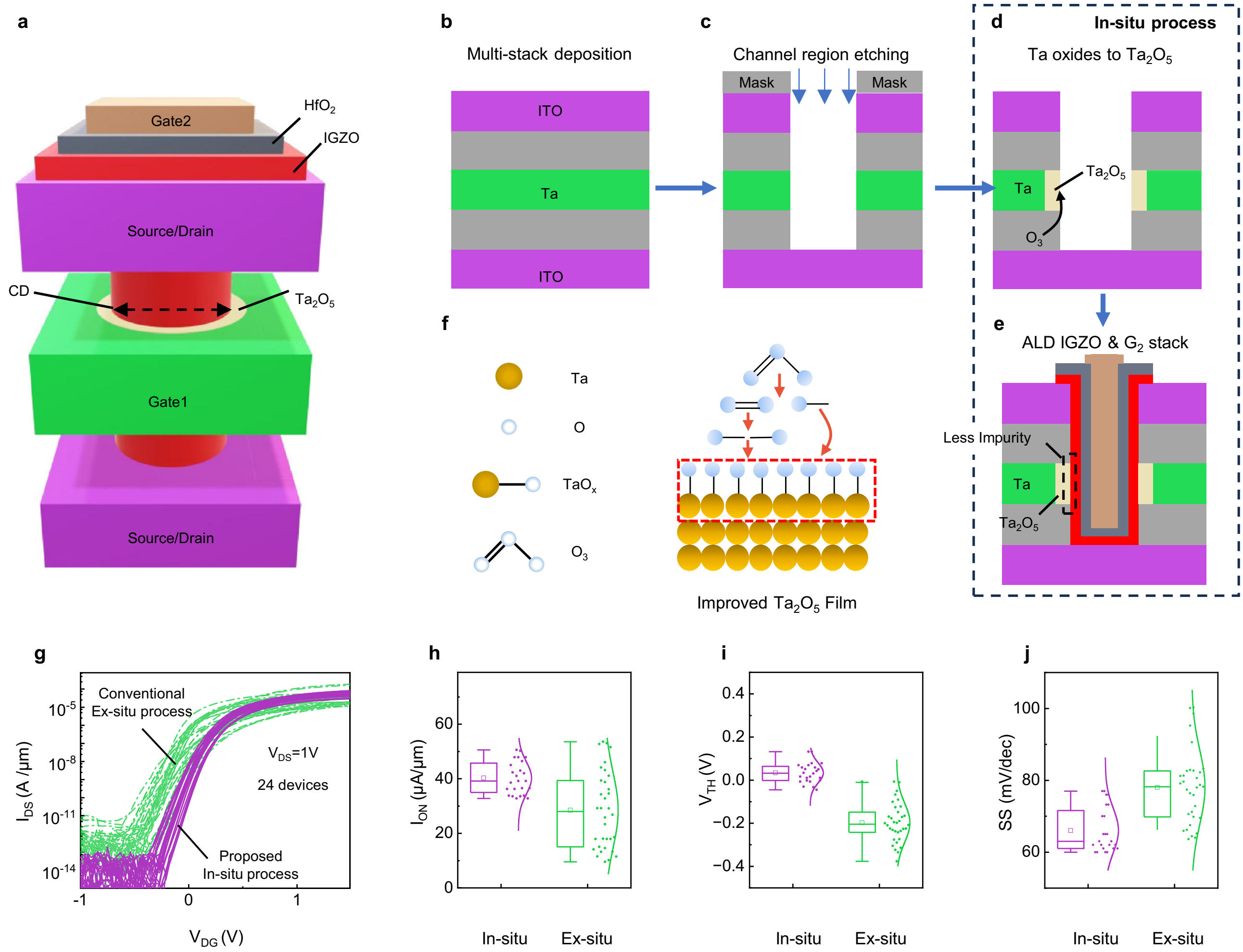

Fig. 2 | In-situ O_3 fabrication process of vertical dual-gate IGZO TFTs. **a** Schematic illustration of vertical dual-gate IGZO TFTs fabricated by the in-situ self-oxidation process. Key step of the in-situ O_3 fabrication process: **b** multi-stack deposition, **c** hole etching, **d** self-oxidation by O_3 under 250 °C, **e** ALD IGZO channel and second gate stack. Step (**d**, **e**) are carried out in one ALD chamber which avoid impurity. Low process temperature of 250 °C reduces the thermal budget. **f** Schematic illustration of Ta self-oxidation process under O_3 atmosphere. Stronger oxidative activity of O_3 result in better Ta_2O_5 film quality. **g** Statistical transfer characteristics comparison of 24 devices fabricated by in-situ O_3 fabrication process and ex-situ O_2 fabrication process. Extracted **h** I_{ON}, **i** V_{TH} and **j** SS from the transfer curve in (**g**). Low SS of 68 ± 5 mV/dec, I_{ON} of 45 ± 5 μA/μm and V_{TH} near to zero are achieved. Both the device performance and variations have been significantly improved with the in-situ process. (The figure depicts each data point and the corresponding distribution curve. Error bars ranger within the 1.5IQR and box limits are upper and lower quartiles. The square represents the mean, and the line represents the median. The data format is mean ± variance).

image of vertical DG IGZO TFTs with CDs of 4μm, 300 nm and 100 nm and the corresponding transfer characteristic comparison with CD scaling from 6μm to 100 nm (Fig. 3d). Current density and SS show no degradation as CD scaling down which demonstrates the scalability of the device at smaller footprint (Fig. 3e). For further scaling, performance of vertical IGZO DG TFTs with different L_{CH}, thickness of IGZO, and HfO_2 are shown in Supplementary Fig. 11. The performance changes during the scaling process are universal, which also indicates the good scalability. Thickness scaling of is further investigated by adjusting the process time of in-situ thermal oxidation as shown in the Supplementary Fig. 12 shows the optimized transfer characteristic with W_{CH}/L_{CH} of 500 nm/120 nm. Due to DG control with extremely low EOT, this device exhibits an ultra-low SS of 63 mV/dec and ultra-high on-state current of 50.3 μA/μm at $V_{DG} = V_{TH} + 1$ V and $V_{DS} = 1$ V satisfying the typical driving current in a 2T0C DRAM cell. And the threshold voltage of −0.04 V and a transconductance exceeding 100μS/μm at $V_{DS} = 1$ V are achieved in this device (Fig. 3f). Benefiting from the optimization of contact resistance, the output curves exhibit ohmic contacts in the linear region and saturation characteristics at relative higher V_{DS} region (Fig. 3g). The V_{TH} tuning capability is further investigated through testing the I_{DS}-V_{G2} characteristic with different G_1 bias. By applying negative voltage to G_1 (RWL), transfer curves shift positively which is desired for DG 2T0C DRAM readout. ΔV_{TH} shows linear dependence on both ΔV_{G1} and ΔV_{G2} demonstrating the well functioned V_{TH} tuning ability of our vertical DG TFT (Supplementary Fig. 13).

To evaluate the thermal stability, vertical DG IGZO TFTs are measured under bias temperature stress of $V_{DG} = \pm 2$ V and 85 °C to confirm the high reliability. Positive bias temperature stability (PBTS) result shown in the Fig. 3h and Supplementary Fig. 14 shows V_{TH} shift of 65 mV and 87.7 mV after dual-gate bias stress of 2 V for 3600 s at 25 °C and 85 °C which exhibit much smaller PBTS compared to the state-of-the-art VCTs reported so far. While the negative bias temperature stability (NBTS) in Fig. 3i and Supplementary Fig. 14 shows V_{TH} shift of −7mV and −22.6 mV after dual-gate bias stress of −2V for 3600 s at 25 °C and 85 °C which also has a significant advantage over other similar devices. Fig. 3j shows the transfer curves of vertical DG IGZO TFTs before and after conducting N_2 annealing for 30 mins at

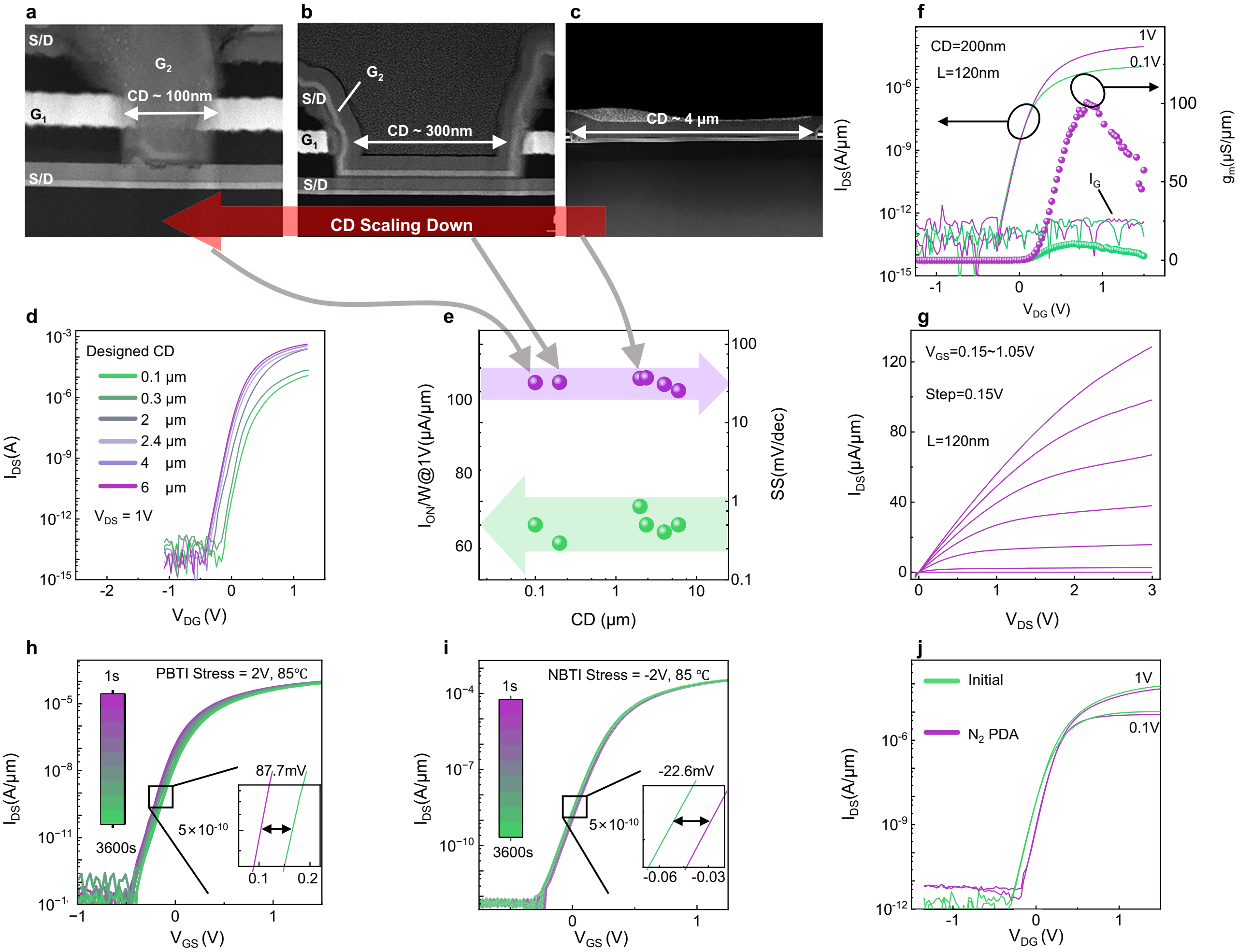

Fig. 3 | CD scaling and thermal stability assessment. TEM image of vertical DG IGZO TFTs with CD scaling from **c** 4 μm and **b** 300 μm to **a** 100 nm. Scale bar: 50 nm, 100 nm and 1 μm. **d** Transfer curves of vertical DG TFTs with CDs from 6 μm down to 100 nm. V_{DS} is set to be 1 V. **e** Extracted I_{ON} at $V_{DG} = 1$ V and subthreshold swing from the transfer curve in (**d**). The current density and SS maintain stability as CD scaling, demonstrating the excellent scaling potential in the DG IGZO TFTs. **f** transfer and **g** output curves of vertical DG IGZO TFTs with 120 nm channel length. I_{ON} of 50.3μA/μm@$V_{TH} + 1$ V and ultra-low SS of 63 mV/dec is achieved. **h** PBTS characteristics of vertical DG IGZO TFTs with 2 V DG stress for 1 h at 85 °C showing 87.7 mV V_{TH} shift. **i** NBTS characteristics with −2V DG stress for 1 h at 85 °C showing −22.6 mV V_{TH} shift. **j** Transfer characteristic of vertical DG IGZO TFTs before and after 300 °C N_2 post-deposition annealing with slight variation. These results validate the excellent thermal stability of the device, which is crucial in high-density memory.

300 °C show slight performance variation. We note that the V_{TH} is defined as V_{GS}@$I_{ON} = W/L$*100pA, the I_{ON} extracted at V_{GS} equals to $V_{TH} + 1$ V and SS is extracted for at least a range of two orders of channel current, following a same method in recent literature. We further conducted the benchmarking of I_{ON} as a function of SS in comparison with the state-of-the-art vertical TFTs based on oxides and two-dimensional materials reported so far (see Supplementary Table 1 for details)[34,35,37–46]. This comparison demonstrates the competitiveness and performance potential of vertical DG IGZO TFTs. It can be seen that the vertical DG IGZO TFTs achieved concomitantly both the highest I_{ON} and lowest SS.

4F^2 DG 2T0C cell with 4-bit storage

In order to demonstrate the functionality of the 2T0C bit-cell based on the vertical DG IGZO TFTs, we fabricated and evaluated planar interconnect DG 2T0C DRAM cell shown in Supplementary Fig. 15. In this planar DG 2T0C DRAM bit-cell, T_W/T_R within the same layer are interconnected through routing. The source of T_W is interconnected with G_2 of T_R and RWL is set on the G_1 of T_R for the consideration of DG read operation and undesired current path eliminating (Supplementary Fig. 15a). The readout current of this planar bit-cell illustrated in Supplementary Fig. 15c shows that the retention time of data ‘1’ is 270 s while the data ‘0’ can be hold over 500 s. The retention of data ‘1’ is defined as the time that V_{SN} decreases by 100 mV, while the retention of data ‘0’ is defined as the time that V_{SN} increases by 100 mV. The highlight characteristic of long retention time and dual-gate read operation suggest that vertical DG structure based on SASS process is suitable for high-density memory application.

We further realize 4F^2 DG 2T0C bit-cell through the proposed SASS process based on vertical DG IGZO TFTs. The DRAM operation modes have already demonstrated in our previous work[36]. In write stage, Data ‘1’ or ‘0’ through BL (1 V or 0 V) is written into SN by turning on T_W with WWL of 0.5 V. After finishing write operation, TW is turned off to keep the data in SN by applying −1.5 V to WWL. For read operation, RWL is biased with selected potential (0.5 V) to discriminate the data stored in SN. Remarkably different current of BL (I_{BL}) can be measured for data ‘1’ and ‘0’ (I_{DATA1} and I_{DATA0}) at $V_{BL} = 0.1$ V. Here, it should be noted that while the additional gate capacitance of the T_W can increase the storage capacity of the DRAM, a more negative voltage (−1.5 V) also needs to be applied to WWL to ensure the write transistor is turned off during the read stage. Although the T_R and T_W share the same channel film, their channel region are divided into

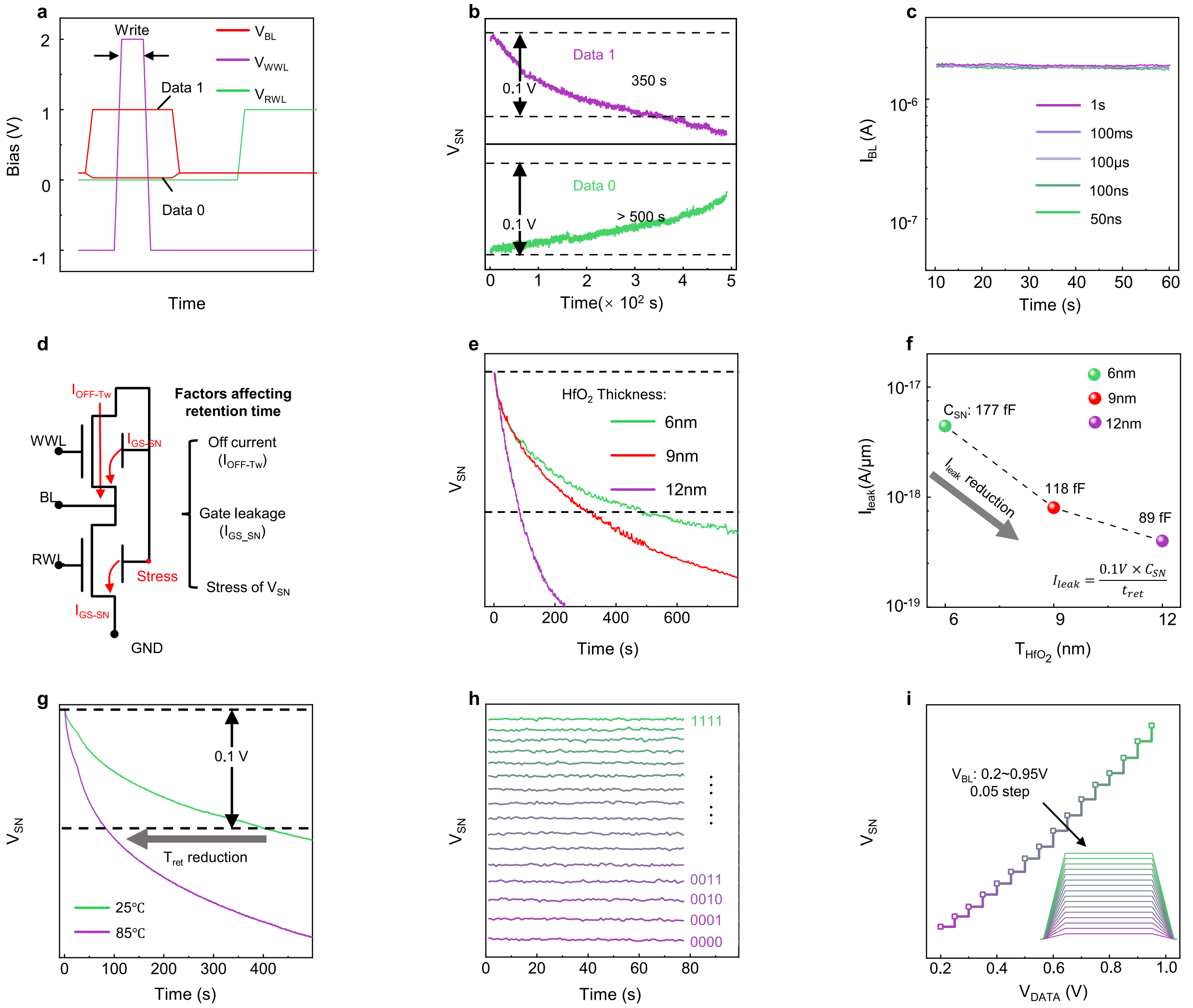

Fig. 4 | Performance of 4F^2 DG IGZO 2T0C cell. a Measurement setup of read/write operation. V_{DATA} for data '1'/data '0' are 1 V/0 V. Write speed is defined as the pulse width of V_{WWL}. **b** V_{SN}-Time characteristic of the fabricated 4F^2 DG 2T0C cell. 350 s and over 500 s retention time are achieved with 0.1 V V_{SN} drop. **c** Read current respond to the different pulse width of V_{WWL} range from 50 ns to 1 s. No attenuation of read current is observed, indicating the DG 2T0C cell achieve 50-ns write speed. **d** Circuit diagram describing the factors affecting data retention time in 2T0C cell which includes three parts: off-state current of write transistor $I_{DS\text{-}off\text{-}TW}$, gate leakage at SN $I_{GS\text{-}SN}$ and bias stress of V_{SN} **e** Retention characteristic of data '1' in vertical DG cell with different T_{HfO2} (6, 9, 12 nm). **f** Calculated I_{leak} current from the retention characteristic in (**e**). I_{leak} decreases as T_{HfO2} scaling due to the $I_{GS\text{-}SN}$ drop and the less positive ΔV_{TH} shifting with thicker gate insulator. **g** Retention characteristic of data '1' in vertical DG 2T0C cell with different operating temperature. **h** The multi-bit test of vertical DG 2T0C cell with V_{BL} varying from 0.2 to 0.95 V in 0.05 V step. 16 distinct read current are observed, which demonstrated the DG 4F^2 cell achieve 4-bit storage. **i** Read current as a function of V_{DATA}. Distinct 16 states can be clearly observed.

upper and lower portions within the IGZO channel, and they are not simultaneously activated according to the different operation. Therefore, there exist little crosstalk within T_R and T_W. Next, we evaluation the retention characteristic of the 4F^2 DG cell. The measurement setup and the corresponding bit line current (I_{BL}) are represented in Fig. 4a and retention time for data '1'/'0' show in Fig. 4b. The retention time of data '1' is 470 s while the data '0' can be hold over 500 s with a large current ratio over 300 s. The longer retention time may enhance from the increased gate capacitance enable by the dual gate structure of T_W. For fast write, we conducted a write operation on the vertical DG 2T0C cell. The pulse width of WWL (t_{write}) is set from 50 ns to 1 s. Fig. 4c shows the response read current with different t_{write}. Extracted I_{BL} is 1.52×10^{-6}, 1.53×10^{-6}, 1.55×10^{-6}, 1.56×10^{-6} and 1.58×10^{-6} A for t_{write} of 50 ns, 100 ns, 100us, 100 ms and 1 s, respectively. As t_{write} shortens, the·I_{BL} keeps almost same value, which indicates the DG DRAM cell in this work achieves a 10 ns write speed. Next, we analyses the leakage currents which influence the retention characteristic in DRAM cells. As shown in the Fig. 4e, f, the total leakage current I_{leak} that affects the retention characteristic in a vertical DG 2T0C cell includes two parts: off-state current of write transistor $I_{DS\text{-}off\text{-}TW}$ and gate leakage at SN $I_{GS\text{-}SN}$ as shown in the Fig. 4d. In addition to leakage current, the voltage on the storage node can also continuously stress the read transistor, causing a shift in the threshold voltage, which indirectly affects the data retention time. Besides the low $I_{DS\text{-}off\text{-}TW}$ of IGZO channel, low gate leakage $I_{GS\text{-}SN}$ is also important for improving the retention characteristics of the 2T0C. In our vertical DG 2T0C cell, the $I_{GS\text{-}SN}$ is mainly determined by the thickness of ALD HfO$_2$. To investigate this issue, we conducted the retention characteristic test in a vertical DG cell with different HfO$_2$ thicknesses. As shown in Fig. 4e, retention times with T_{HfO2} of 6, 9, 12 nm are 90, 300 and 440 s. Fig. 4f shows the I_{leak}

calculated by the formula:

$$T_{ret} = \frac{0.1V^{*}tC_{SN}}{I_{leak}} \quad (1)$$

which is 4.42×10^{-16}, 8×10^{-17} and 4×10^{-17} A/μm. The leakage current decreases in the 2T0C cell with thicker HfO_2 layer. We noted that the $I_{DS\text{-}off\text{-}TW}$ is unchanged with increasing T_{HfO2}. Furthermore, ΔV_{TH} result from PBS reduce as T_{HfO2} increasing which contribute in the retention promotion. Thus, the reduction of I_{leak} mainly results from the decrease of gate leakage $I_{GS\text{-}SN}$ and positive stress of V_{SN}. A decreasing $I_{GS\text{-}SN}$ results from a larger EOT_{HfO2} layer with thicker T_{HfO2}. Fig. 4g shows the temperature-dependent retention characteristic of the vertical DG 2T0C cell. T_{ret} of 90 s with I_{leak} of 1.3×10^{-16} A/μm at 85 °C and T_{ret} of 410 s with I_{leak} of 2.9×10^{-17} A/μm at 25 °C is achieved. We note that the increased I_{leak} at 85 °C mainly results from the increase of thermally activated carriers which contribute to the larger $I_{DS\text{-}off\text{-}TW}$ and $I_{GS\text{-}SN}$ and also result from the large ΔV_{TH} by positive stress of V_{SN} as temperature increasing. As further tests, we successfully conduct the 4-bit multi-bit operations as shown in the Fig. 4h, i. By writing different data voltages from 0.2 V to 0.95 V with a step of 0.05 V, 4-bit read current can be clearly observed with 16 distinct states (0000,0001, …, 1110,1111). The extracted read current of the 16 distinct states is proportional to V_{DATA} as shown in Fig. 4h, proving the validity of 4-bit operation with this vertical DG cell. This works shows small footprint of $4F^2$ and more reliable read operation of DG read scheme. The result suggested that as fabricated 3D integration DG 2T0C cell can exhibit basic read/write operation with multi-bit operation which contributed to high density DRAM application.

To further prove the feasibility of this cell, additional 9 retention characteristics of 3D DG cell are measure and display in Supplementary Fig. 16. All these bit-cells achieve the retention time of data '1' exceeding 100 s and the average value is 230 s. We noted that these similar retention characteristics, indicating the repeatability of the $4F^2$ 2T0C bit-cell. Finally, the performance benchmark of representative AOS-based 2T0C DRAM cells is summarized in Supplementary Table 2, showing obvious advantages of our 3D DG 2T0C bit-cell with smallest footprint, dual-gate read and multi-bit operation, respectively, with long retention time of 470 s. Although not superior than the previously reported planar-device-based 2T0C DRAM, the retention time of 100–500 s in this work demonstrates the highest reported for all vertical device-based 2T0C structures, with at least one decade improvement[17]. The main reason for decreased retention time in the vertical device-based design is due to increased discharge paths resulting from SN node overlapping with all the RWL, GND and BL lines. The retention time can be improved by scaling the overlapped area and optimizing the gate stack of SN node.

Finally, we investigate the effects of crosstalk such as the Row Hammer and Passing-gate effects for our $4F^2$ DG 2T0C cell by SPICE simulations. Supplementary Fig. 17a shows the read disturb due to the RWL-SN coupling (SN suffering from the electric coupling of neighboring RWL). Beneficial in our vertical DG cell design, all the cell capacitance at the SN (from grounded terminal, WWL, RWL and BL) contribute to stabilize the SN potential. Furthermore, a negative enough potential (V_L) can be provided to the unselected RWLs to reduce the disturbance of current as shown in the Supplementary Fig. 17b. Remarkably current difference is observed (read current of 3.8uA and 0.2uA for data '1' and data '0') for the array operation by SPICE simulations as reviewer suggested as shown in Supplementary Fig. 18a. Simulation results also provide further proof that disturbance impact can be reduced. As shown in Supplementary Fig. 18b, the current from all other unselected cells can be controlled below 1fA, which is several orders less than the current (uA level) from target cell.

Discussion

Based on self-oxidation and SASS process, a 3D integration DRAM cell scheme without photolithography misalignment proposed to improve the density of DRAM. With optimized performance, ultra-high I_{ON} and low SS was achieved. Moreover, the suggested high-density DRAM cell demonstrates fundamental read/write operations with extended retention time, ample storage margin and 4-bit multi-bit operation. This study presents a solution for achieving high-density DRAM, which can help storage-intensive applications, such as artificial intelligence, overcome storage bottlenecks.

Methods

Vertical DG IGZO TFT fabrication

The process flow showcasing the major process steps is shown in Supplementary Fig. 7. Firstly, a 20-nm-thick ITO was grown by RF magnetron sputtering as Source/Drain layer on clean SiO_2/Si substrate and patterned by an inductively coupled plasma (ICP) etching process. Then, a SiO_2/Ta/SiO_2/ITO stack was grown via RF sputtering with thickness of 40/40/40/30 nm in which two layers of SiO_2 ILD was used to isolation electrode, Ta and ITO layer was use for gate metal and Source/Drain electron. Secondly, continuous etching the above stack by ICP under the mask of the same photo-resist to form the circular channel region. Then, put the sample in the ALD chamber and annealed at 250 °C under ozone atmosphere for 1 h to self-align form the Ta_2O_5 insulator. After that, an IGZO/HfO_2/IZO gate stack with thickness of 6/9/25 nm was sequentially deposited by plasma-enhanced atomic layer deposition (PEALD) in one chamber. ICP dry etching and dilute HNO_3 was carried out to patterned the IGZO/HfO_2/IZO stack for device isolation. Finally, the SiO_2 was removed by dry etch process to expose the electrodes.

3D integration 2T0C cell fabrication

The process flow is similar to the vertical DG IGZO TFT. Firstly, a 20-nm-thick ITO was grown by RF magnetron sputtering as GND on clean SiO_2/Si substrate and patterned by an ICP etching process. Then, a SiO_2/Ta/SiO_2/ITO/SiO_2/Ta/SiO_2/ITO stack was grown via RF sputtering with thickness of 40/40/40/30/40/40/40/30 nm in which Ta layers was acted as RWL & WWL and ITO layers was acted as common BL & SN electron. Secondly, continuous etching the above stack by ICP under the mask of the same photo-resist to form the circular channel region. Then, put the sample in the ALD chamber and annealed at 250 °C under ozone atmosphere for 1 h to self-align form the Ta_2O_5 IG oxide of RWL & WWL. After that, an IGZO/HfO_2/IZO stack with thickness of 6/9/25 nm was sequentially deposited by PEALD at 250 °C. ICP dry etching and dilute HNO_3 was carried out to patterned the IGZO/HfO_2/IZO stack. Finally, a 10/30 nm Ti/Au dual-layer is deposited via electron beam evaporation (EBE) to connect the RT and WT and the SiO_2 was removed by dry etch process to expose the electrodes.

Material and device characterizations

The IGZO film was deposited using PEALD at 250 °C. O_3 plasma was selected as the oxidizing agent in the ALD process to prevent the impact of hydrogen on the IGZO film and In:Ga:Zn cycle ratio during the ALD process is 1:1:1. The cross-section TEM sample is cut by FEI Scios 2 dual-beam focused ion beam (FIB) system. The TEM images and EDX mapping were performed by using JEM ARM300F at 300 kV. I-V and I-T characteristic were measured at room temperature/85 °C and ambient atmosphere in a Signatone 1060 probe station with dark shield and a Keysight B1500A semiconductor parameter analyzer.

Data availability

Preliminary results from this study have been reported in the conference proceedings of the 2024 IEEE International Electron Devices Meeting (IEDM). The data generated in this study are provided in the Supplementary Information/Source Data file. Data are available from the corresponding authors upon request. Source data are provided with this paper.

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Author contributions

Ming L., L.L., A.N., C.Z., G.Y., Z.Z., Z.L., and F.L. conceived the research and designed the experiments. F.L. and Z.L. fabricated and measured devices. Menggan L., K.C., W.L., Z.W., X.Z., N.M., C. Lu, J.W., J.Y., L.W., D.G., and N.L. discussed the fabrication process and provided technical supports. F.L., Z.Z., G.Y., A.N., and L.L. co-wrote the paper. M.J., C. Liu, B.K., J.S., X.W., J.Z., Y.Y., and G.W. discussed the results and gave valuable suggestions. All authors commented and discussed the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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