nature communications

Article

https://doi.org/10.1038/s41467-025-68007-6

# High-$\kappa$ samarium oxysulfate dielectric for two-dimensional electronics with enhanced gate coupling

Received: 1 June 2025

Accepted: 15 December 2025

Published online: 29 December 2025

Check for updates

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Layered dielectric materials and their van der Waals (vdW) heterostructures offer high potential for next-generation two-dimensional (2D) electronic devices, but materials that combine a wide bandgap and high dielectric constant are rare. Here, we present the controllable synthesis of quasi-vdW layered samarium oxysulfate ($Sm_2O_2SO_4$) single crystals via a molten-salt-assisted chemical vapor deposition (CVD) method. These atomically thin crystals exhibit remarkable dielectric properties, including a wide bandgap (~5.54 eV), high dielectric constant (~18), robust breakdown voltage (>12 MV $cm^{-1}$) and good thermal reliability. By integrating ultrathin $Sm_2O_2SO_4$ nanoplates with 2D molybdenum disulfide ($MoS_2$) via vdW forces, we fabricate field-effect transistors (FETs) showing a subthreshold swing down to 65.2 mV $dec^{-1}$, hysteresis down to 5.4 mV, on/off current ratios of ~$10^9$, and gate leakage currents down to around $7 \times 10^{-7}$ A $cm^{-2}$. Furthermore, a high gate coupling ratio (GCR ~ 0.83) non-volatile memory device was developed based on the $MoS_2$/h-BN/MLG/$Sm_2O_2SO_4$/MLG heterostructure. The flash memory achieves ultrafast (~50 ns) programming/erasing operations, robust endurance (>2000 cycles) and long-term retention (>10 years). This work shows promising results for the integration of $Sm_2O_2SO_4$ as a high-$\kappa$ dielectric in future 2D devices, with implications for low-power, high-performance electronics.

Two-dimensional (2D) semiconductors, with high carrier mobility, tunable bandgaps, and atomic-scale thickness, are widely regarded as ideal channel materials for future technologies that aim to surpass silicon-based integrated circuits and memory computing architectures[1–3]. In recent years, floating-gate field-effect transistors (FGFETs) based on 2D materials have gained widespread attention[4–13]. 2D materials such as $MoS_2$, $ReSe_2$, $HfS_2$, and $MoTe_2$ demonstrate excellent electric field control, effectively reduce parasitic defect capture, and facilitate the scaling of memory and computing systems, thereby showing significant advantages in high-density integration[14,15]. However, the lack of high-quality blocking dielectric materials limits further improvements in low-power and ultrafast FGFET performance. Dielectrics must not only exhibit excellent electrical properties but also achieve low operating voltage, low leakage current, and stable thermal and electrical characteristics[16,17].

Conventional high-$\kappa$ oxides ($HfO_2$, $ZrO_2$, $Ta_2O_5$) enhance electrostatic control but are limited by atomic layer deposition (ALD) processes, which cause crystallization at the nanoscale and introduce

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interface defects, reducing device reliability[18–21]. Additionally, in-situ deposition may induce interface trap states, increase charge scattering, degrade carrier mobility, and elevate leakage current, restricting their applicability in 2D devices. Meanwhile, silicon-based floating-gate memory suffers from high tunneling barriers at the $Si/SiO_2$ interface and dangling bonds, leading to a low gate coupling ratio (GCR), high power consumption, and short data retention times[22–24]. High-quality single crystal dielectric materials such as *h*-BN, $Gd_2O_5$, $MgNb_2O_6$, $Eu_2SO_x$, and $Mn_3O_4$, due to their excellent interface quality, have been widely used in 2D electronic devices as vdW dielectric materials, preserving the intrinsic properties of 2D semiconductors[25–30]. Recently, all-2D floating-gate memory utilizing *h*-BN as a blocking layer has been demonstrated, achieving atomically sharp interfaces and enabling miniaturization for high-density integration[8]. However, its low dielectric constant ($\kappa = 2–4$) limits electrostatic control, preventing further scaling of the equivalent oxide thickness (EOT), and constrains GCR improvement, ultimately affecting storage efficiency. Furthermore, an ideal gate dielectric should possess a wide bandgap to suppress leakage current, reduce interface state density, and enhance breakdown strength. For example, perovskite strontium titanate ($SrTiO_3$) has an ultrahigh dielectric constant and holds promise for sub-1 nm EOT applications, but its relatively narrow bandgap (~3.2 eV <5 eV) leads to excessive leakage current, limiting its potential for future 2D CMOS applications[31,32]. Therefore, there is an urgent need to develop new dielectric materials with high GCR, a high dielectric constant, low leakage current, and stable interfaces to advance 2D electronics and storage technologies.

In this study, we report the successful synthesis of atomically thin samarium oxysulfate ($Sm_2O_2SO_4$) dielectric single crystals using a molten-salt-assisted chemical vapor deposition (CVD) method. This quasi-vdW layered $Sm_2O_2SO_4$ single crystal exhibits remarkable potential as a gate dielectric for 2D heterostructure devices due to its high dielectric constant (~18), wide bandgap (~5.54 eV), high breakdown field strength (>12 MV $cm^{-1}$), and excellent thermal and electrical stability. Molybdenum disulfide ($MoS_2$) with $Sm_2O_2SO_4$ gate dielectrics operates with minimal hysteresis of 5.4 mV, a subthreshold slope (SS) of 65.2 mV $dec^{-1}$, an on/off current ratio of $10^9$, a low top-gate leakage current of $7 \times 10^{-7}$ A $cm^{-2}$, and high operational reliability at 500 K. Furthermore, leveraging the wide bandgap and high dielectric performance of $Sm_2O_2SO_4$, we constructed a low-power (2.97 pJ) all-2D floating-gate memory device based on a $MoS_2$/*h*-BN/MLG/$Sm_2O_2SO_4$/MLG vdW heterostructure (here *h*-BN stands for hexagonal boron nitride and MLG stands for multilayer graphene), where $Sm_2O_2SO_4$ was employed as a blocking layer. The resulting FG device exhibits outstanding non-volatile memory performance, including a low-voltage storage window (<3 V), high on/off ratio (>$10^7$), long data retention (>10 years), stable endurance (>2000 cycles) and fast (~50 ns) programming/erasing operations. These characteristics stem from its high-$\kappa$ properties, which enhance GCR ( ~ 0.83), and the atomically sharp vdW interface. These findings highlight the potential of $Sm_2O_2SO_4$ as a promising high-$\kappa$ layered dielectric material for 2D nanoelectronics and high-GCR floating-gate memory devices.

## Results

### Controlled growth and structural characterization of $Sm_2O_2SO_4$

As shown in Fig. 1a, europium oxysulfate SmOSO crystallizes in the tetragonal lattice with an $_{224}I\bar{4}2m$ space group, and it possesses a quasi-vdW layered structure with a covalently saturated surface in the [001] direction. From the side view of the SmOSO structure, the crystal structure consists of alternating $[SmO]^+$ cationic layers and $[SO]^-$ anionic layers via electrostatic forces instead of vdW attractions. From the top view, the structure appears as consisting of multiple [SmO] units, where the Sm atoms form the framework and the O atoms occupy the central positions, with each Sm atom coordinated to two O atoms, creating a [SmO] subunit. Additionally, the [SO] group is symmetrically placed around the [SmO] units, with the S atom at the center and the four O atoms positioned around it in a tetrahedral arrangement.$_{22422^2 4^2 2222422}$

High-quality ultrathin $Sm_2O_2SO_4$ nanoplates were synthesized using the molten-salt-assisted chemical vapor deposition (CVD) system, employing mica as growth substrate, $Sm_2(SO_4)_3 \cdot xH_2O$ as the growth precursor and KI as eutectic melt (Fig. 1b and Supplementary Fig. 1 for details). During the melting process, molten salts promote the dissolution of precursors, ion diffusion, and the assembly of basic units, with nucleation and growth primarily occurring in the lateral direction based on the reaction process as follows: $Sm_2(SO_4)_3 \cdot xH_2O + 2H_2 + KI \rightarrow Sm_2O_2SO_4 + 2SO_2 + (2+x)H_2O + KI$. Optical microscopy (OM) images confirm that the $Sm_2O_2SO_4$ nanoplates exhibit a transparent rhombic-like shape and atomically thin nature, with maximum lateral sizes of 50 μm (Fig. 1c and Supplementary Fig. 2a). Supplementary Fig. 2c shows the atomic force microscope (AFM) image of a typical $Sm_2O_2SO_4$ nanoplate, which features atomically smooth surface and ultrathin thickness of ~5.2 nm. The crystal size and thickness can be commendably controlled by modulating the growth parameters (Supplementary Fig. 3). The statistical results, as shown in Supplementary Fig. 3c, f, and i, indicate that the lateral crystal sizes are mainly distributed in the range of 20-60 μm, with a concentration around 40 μm. Besides, the as-synthesized $Sm_2O_2SO_4$ nanoplates are prone to wrinkling when washing residual salts, indicating a weak adhesion force between nanoplate and mica substrate, originating from the vdW epitaxy mechanism (Supplementary Fig. 4)[29]. Therefore, ultrathin $Sm_2O_2SO_4$ nanoplates can be easily released from the growth substrate and transferred onto other target substrates or constructing artificial heterostructures. Density functional theory (DFT) calculations are performed to investigate the electronic band structure of layered $Sm_2O_2SO_4$. As plotted in Fig. 1d, $Sm_2O_2SO_4$ displays a large indirect band gap of ~5.67 eV, with the conduction band minimum (CBM) and valence band maximum (VBM) both located at the Γ and near the X points of the 2D Brillouin zone, respectively. The conduction band is made up hybridized Sm *p* and S *p* states associated with the empty O 1*s* lone pair, while the valence band consists mainly of S *p* states. Furthermore, we analysed the optical bandgap from the absorption spectrum using ultraviolet-visible spectroscopy and found that the bandgap of ultrathin $Sm_2O_2SO_4$ nanoplates is ~5.54 eV, which is higher than that of the most crystalline high-$\kappa$ dielectrics such as $SrTiO_3$ (3.2 eV)[32], $Bi_2SeO_5$ (3.9 eV)[33], $Sb_2O_3$ (4.06 eV)[34] and $Bi_2SiO_5$ (3.79 eV)[35]. To study the chemical structure and crystallinity of $Sm_2O_2SO_4$, Raman and Photoluminescence (PL) spectra measurements were conducted. As shown in Fig. 1e, the $Sm_2O_2SO_4$ crystal exhibits four vibrational modes ($\nu_1$, $\nu_2$, $\nu_3$ and $\nu_4$) corresponding to the free $[SO_4]^{2-}$ ions with $T_d$ symmetry, and two prominent peaks at 333.4 and 418.8 $cm^{-1}$, which are attributed to the Sm-O fundamental modes, consistent with previous experimental Raman results[36]. We systematically performed Raman spectroscopy on $Sm_2O_2SO_4$ crystals of different thicknesses (Supplementary Fig. 5). As the thickness decreases, the peaks ($\nu_1$, $\nu_2$, $\nu_3$ and $\nu_4$) become less pronounced, which can be attributed to the weaker intensities of four vibrational modes in few-layer $Sm_2O_2SO_4$ nanoplates. PL spectra of the bulk $Sm_2O_2SO_4$ crystal is recorded using excitation wavelength 532 nm in Supplementary Fig. 6a. Four peaks can be observed at 562 nm, 608 nm, 644 nm, and 658 nm, corresponding to the characteristic luminescent bands of the $Sm^{3+}$ ions, arising from the transitions of the $^4G_{5/2}$ state to the $^6H_{5/2}$, $^6H_{7/2}$ and $^6H_{9/2}$ multiplets, respectively. However, as the thickness decreases, the three peaks at 608 nm, 644 nm, and 658 nm become less pronounced, which can be attributed to the reduced luminous efficiency in few-layer $Sm_2O_2SO_4$ nanoplates due to enhanced surface effects and non-radiative recombination pathways[37,38]. Supplementary Fig. 6b shows the cathodoluminescence (CL) spectra of ultrathin $Sm_2O_2SO_4$ nanoplates transferred onto a $SiO_2/Si$ substrate. Two

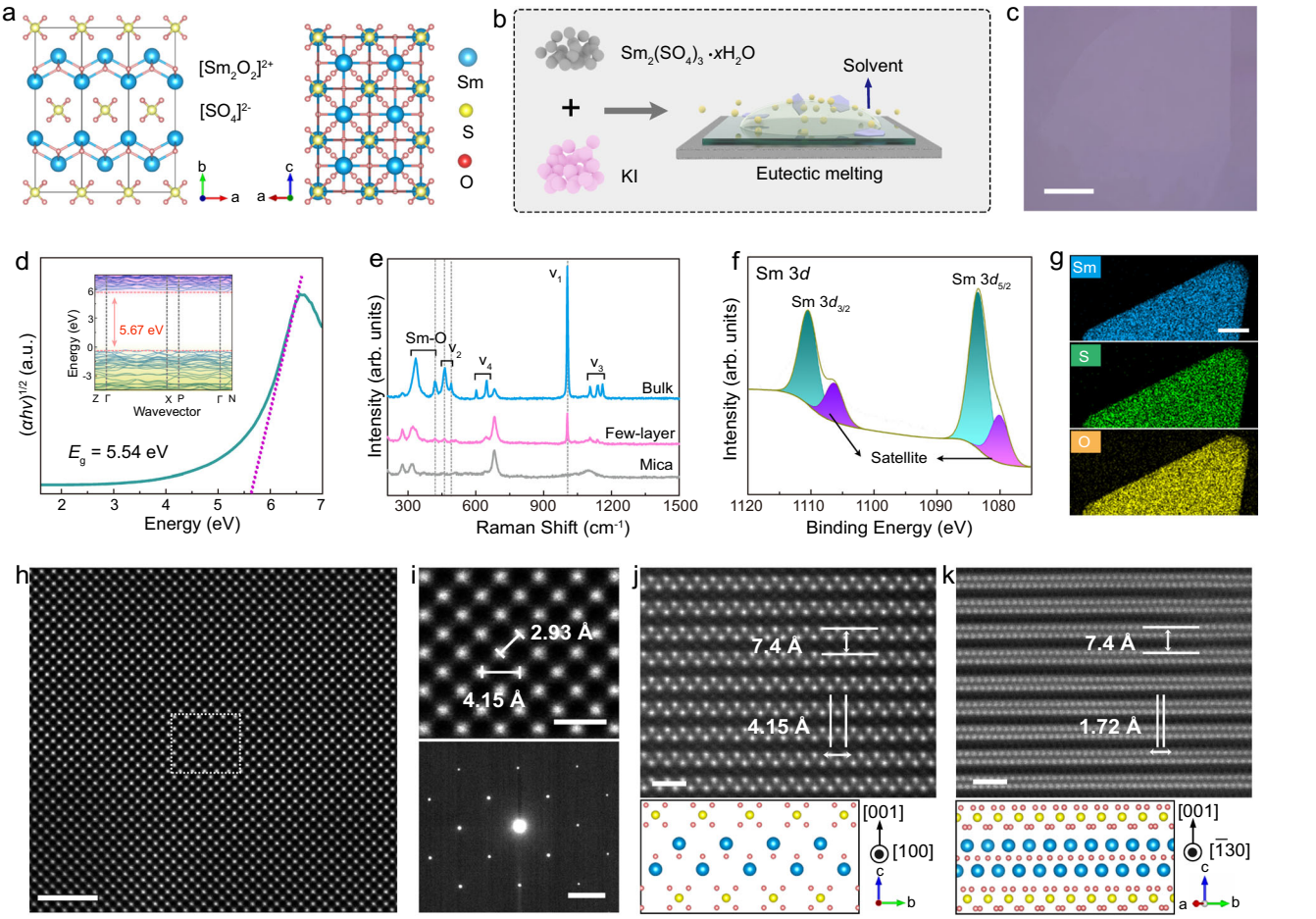


**Fig. 1 | Structure and characterization of quasi van der Waals (quasi-vdW) layered $Sm_2O_2SO_4$ single crystals. a**The crystal structure of SmOSO. Blue, yellow and red spheres represent Sm, S and O atoms, respectively. $_{224}$**b**Schematic of the strategy for the growth of layered SmOSO single crystals. $_{224}$**c**Optical microscopy (OM) image of SmOSO nanoplates. Scale bars: 10 μm. $_{224}$**d**The optical band gap ($E_g$) is determined to be ~5.54 eV from the Tauc plot of the ultraviolet-visible absorption spectrum, where $\alpha$, $h$and $v$are the absorption coefficient, Planck's constant, and the light frequency, respectively. Inset: The calculated electronic band structure of $Sm_2O_2SO_4$. **e** Typical Raman spectra of ultrathin SmOSO nanoplates transferred onto SiO/Si substrate acquired at room temperature. $_{2242}$**f**X-ray photoelectron spectroscopy (XPS) spectra of Sm 3 *d*orbitals. **g**The energy dispersive X-ray spectroscopy (EDS) elemental mapping images of SmOSO nanoplate. Scale bars: 0.5 μm. $_{224}$**h**The high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of SmOSO. Scale bars: 2 nm. $_{224}$**i**The high-magnification HAADF-STEM image (top) and selected-area electron diffraction (SAED) pattern (bottom) of SmOSO nanoplate. Scale bars: 0.5 nm and 5 nm. $_{224}$**j**, **k**Cross-sectional atomic-resolution HAADF-STEM images and corresponding atomic models of ultrathin SmOSO nanoplate taken along the zone axes of $_{224}$**j**[100], and **k** [1̄30]. Scale bars: 1 nm.

distinct peaks are observed at 606 nm and 652 nm, which correspond to the electronic transitions labeled $^6H_{7/2}$ and $^6H_{9/2}$ due to the f-f transitions of $Sm^{3+}$ ions. Additionally, the chemical states of ultrathin $Sm_2O_2SO_4$ nanoplates were analyzed using X-ray photoelectron spectroscopy (XPS) (Fig. 1f and Supplementary Fig. 7). The binding energies of 1083.5 and 1110.4 eV confirm the presence of $Sm^{3+}$ $3d_{5/2}$ and $Sm^{3+}$ $3d_{3/2}$, respectively. The O 1 s binding energies of 529.2 and 532.1 eV are attributed to Sm-O and $[SO_4]^{2-}$ species, while the S $2p_{3/2}$ binding energies of 168.9 and 170.1 eV are assigned to Sm-S.

Scanning transmission electron microscopy (STEM) studies are used to investigate more information about the crystal structure of the transferred ultrathin $Sm_2O_2SO_4$ nanoplates (Supplementary Fig. 8a). The typical high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) images of the rhombic $Sm_2O_2SO_4$ crystal (Fig. 1g and Supplementary Fig. 8b) along the [001] zone axis is shown in Fig. 1h and Supplementary Fig. 9a, b. The intuitive plan-view STEM images reveal a highly-crystallized tetragonal crystal structure with no atomic vacancies or lattice deformation. The lattice spacings are estimated to be ~4.15 and ~2.93 Å, as verified by the enlarged HAADF-STEM image (Fig. 1i), matching well with the structure of (100) and (110) plane of the tetragonal phase $Sm_2O_2SO_4$ crystal. Besides, the selected-area electron diffraction (SAED) pattern along the [001] zone axis shows the corresponding tetragonal structure. The energy dispersive X-ray spectroscopy (EDS) elemental mapping confirms the uniform distribution of Sm, S and O throughout the entire nanoplate (Supplementary Fig. 9c). To identify the layered characteristic in $Sm_2O_2SO_4$ single crystal, a nanoplate was cut using a focused ion beam (Supplementary Fig. 10), followed by atomic-resolution cross-sectional HAADF-STEM imaging. Figure 2j, k and Supplementary Fig. 11 show atomic-resolution STEM imaging along three-zone axes ([100], [1̄30]., and [110]) with a regular layered arrangement, as well as corresponding atomic models of $Sm_2O_2SO_4$. The alternative stacking of $[Sm_2O_2]^{2+}$ and $[SO_4]^{2-}$ layers with a layer space of 7.4 Å is observed, and the measured lattice fringes of 4.15, 2.93, and 1.72 Å can be attributed to the lattice planes of (010), (1$\bar{1}$0), and (310), respectively. These results indicate the successful fabrications of the 2D quasi-vdW layered $Sm_2O_2SO_4$ single crystal.

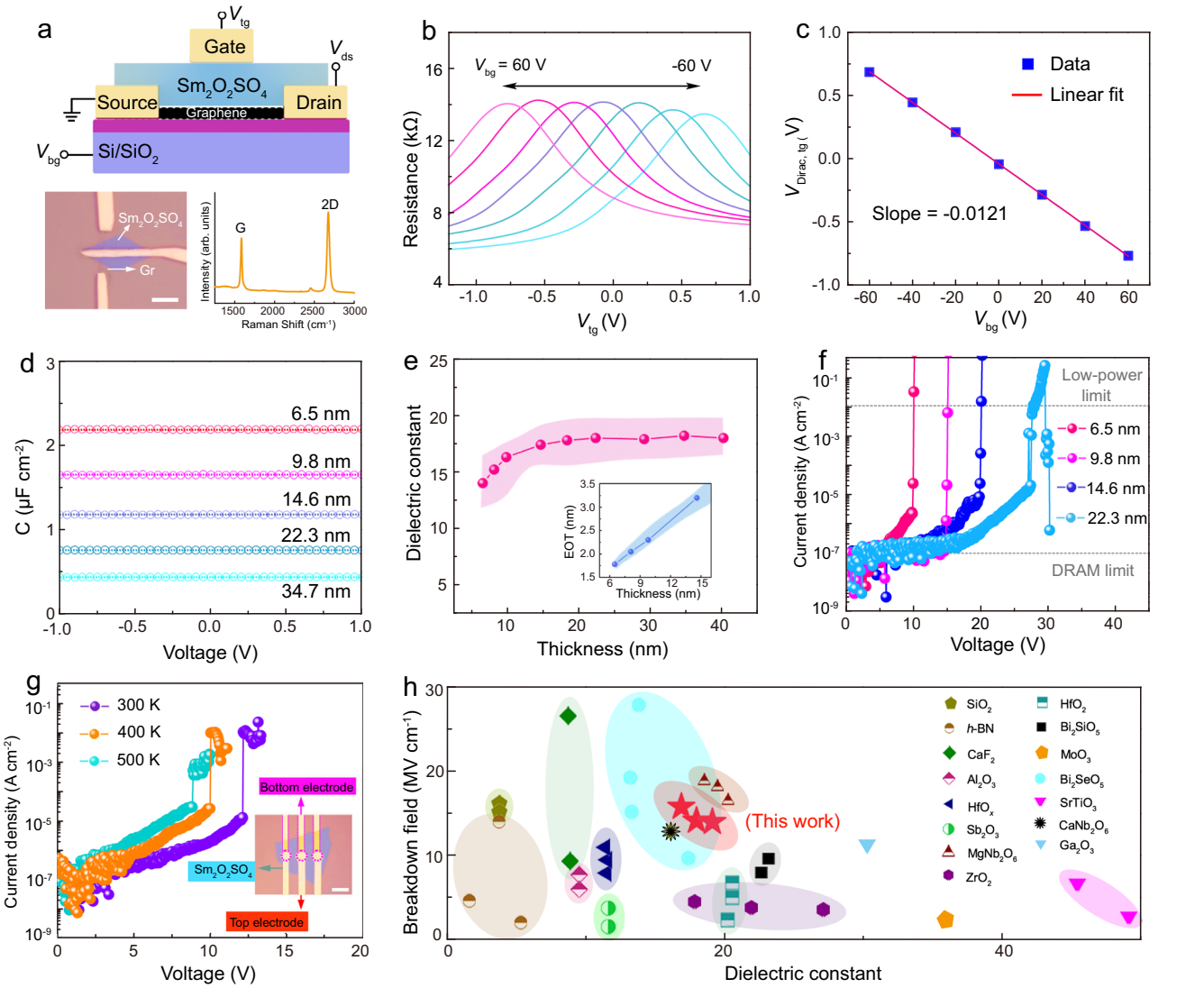


**Fig. 2 | Dielectric properties of quasi-vdW layered $Sm_2O_2SO_4$ single crystal.** **a** Schematic (top) and OM image (left bottom) and Raman spectroscopy (right bottom) of the double-gate graphene (Gr) field-effect transistor (FET) with the $Sm_2O_2SO_4$ top-gate dielectric on $SiO_2$/Si substrate (here $V_{tg}$, $V_{bg}$ and $V_{ds}$ represent the top-gate voltage, back-gate voltage, and drain-to-source voltage, respectively). Scale bars: 5 μm. **b** Total resistance of a typical dual-gate graphene FET as the function of $V_{tg}$ at different $V_{bg}$. **c** $V_{bg}$-dependent top-gate Dirac point voltages of the dual-gate graphene FET. **d** Thickness-dependent capacitance–voltage (*C-V*) measurements of $Sm_2O_2SO_4$ nanoplates at measurement frequency of 100 kHz. **e** Thickness-dependent dielectric constant of $Sm_2O_2SO_4$ measured by the *C-V* method. Inset: thickness dependent equivalent oxide thickness (EOT) of $Sm_2O_2SO_4$. **f** Current leakage and breakdown characteristics of $Sm_2O_2SO_4$ nanoplates measured by metal-insulator-metal (MIM) devices with thicknesses ranging from 6.5 to 22.3 nm. The dashed lines mark the limits for various electronic applications. DRAM, dynamic random access memory. **g** The breakdown field of $Sm_2O_2SO_4$ at different temperatures. Inset: OM image of the MIM device. Scale bars: 5 μm. **h** Breakdown field versus effective dielectric constant of ultrathin $Sm_2O_2SO_4$, compared with various dielectric materials[18,20,26,27,32–35,41–43,53–55].

## Dielectric properties of $Sm_2O_2SO_4$

Dielectric constant, and breakdown field strength are key parameters that determine the performance of dielectric materials. To evaluate the dielectric properties of layered $Sm_2O_2SO_4$ single crystals, dual-gate graphene FETs were fabricated by integrating graphene channels with ultrathin $Sm_2O_2SO_4$ nanoplates on a p-Si substrate with a 285 nm $SiO_2$ capping layer (Fig. 2a). The thicknesses of $Sm_2O_2SO_4$ (15 nm) and graphene (single layer) were determined by AFM and Raman spectroscopy, respectively (Fig. 2a and Supplementary Fig. 12). In this setup, $Sm_2O_2SO_4$ and $SiO_2$ serve as the top- and back-gate dielectrics, respectively. The charge carriers in the graphene channel can be controlled simultaneously by applying top- and back-gate voltages[28,30,39,40]. The top-gate Dirac point voltage ($V_{Dirac,\ tg}$) can be modulated by the back-gate voltage ($V_{bg}$), as shown in Fig. 2b. Using a parallel plate capacitor model for the top- and back-gate, the slope of $V_{Dirac,\ tg}$ with respect to $V_{bg}$ corresponds to the ratio of the back-gate capacitance to the top-gate capacitance ($C_{SiO_2}/C_{Sm_2O_2SO_4}$), as expressed in the following equation:

$$\frac{C_{SiO_2}}{C_{Sm_2O_2SO_4}} = \frac{\varepsilon_{SiO_2} t_{Sm_2O_2SO_4}}{\varepsilon_{Sm_2O_2SO_4} t_{SiO_2}} \quad (1)$$

where $\varepsilon_{Sm_2O_2SO_4}$ and $\varepsilon_{SiO_2}$ (3.9) are the dielectric constants of $Sm_2O_2SO_4$ and $SiO_2$, respectively, and $t_{Sm_2O_2SO_4}$ and $t_{SiO_2}$ are their respectively thicknesses, we obtain the dielectric constant of 16.9 for 15-nm-thick $Sm_2O_2SO_4$ from this device (Fig. 2c). To obtain the effective dielectric constant of $Sm_2O_2SO_4$ more precisely, more dual-gate graphene FETs are fabricated using $Sm_2O_2SO_4$ with various thicknesses as the top-gate dielectric (Supplementary Fig. 13).

Additionally, the parallel-plate capacitor device with ertical metal-insulator-metal (MIM) structure were also constructed to characterize the dielectric properties of $Sm_2O_2SO_4$ (Supplementary Fig. 14a). In this

setup, the $Sm_2O_2SO_4$ layer was sandwiched between two vertically stacked Cr/Au electrodes on a quartz substrate. The corresponding capacitance–voltage (*C-V*) measurements at various frequencies (*f*) are shown in Supplementary Fig. 14b. The effective permittivity ($\varepsilon_{eff}$) can be calculated calculated using the following equation:

$$C_{eff} = \frac{A\varepsilon_0\varepsilon_{eff}}{t} \quad (2)$$

in which $C_{eff}$ is the measured capacitance, $A$ is the effective area, $t$ is the thickness of the $Sm_2O_2SO_4$ layer, and $\varepsilon_0$ is the vacuum permittivity. Thus, the $Sm_2O_2SO_4$ nanoplate with a thickness of 14.6 nm demonstrated a high $\varepsilon_{eff}$ of 17.8, which is much higher than that of 2D hexagonal boron nitride (*h*-BN) (~5)[25] and comparable with that of traditional high-$\kappa$ oxide dielectrics such as $HfO_2$[41], $ZrO_x$[42] and $Al_2O_3$[43]. As shown in Fig. 2d and Supplementary Fig. 15, the capacitance exhibited a significant dependence on the thickness of the $Sm_2O_2SO_4$ nanoplates. Correspondingly, the $\varepsilon_{eff}$ of $Sm_2O_2SO_4$ with different thicknesses is plotted in Fig. 2e, which shows a decreasing trend as the thickness reduces and can be well described by the typical 'dead layer' model due to the existence of interfacial capacitance (Supplementary Fig. 16)[44,45]. The corresponding EOT for $Sm_2O_2SO_4$ can be calculated by the following equation:

$$EOT = \frac{3.9t}{\varepsilon_{eff}} \quad (3)$$

where 3.9 is the dielectric constant of silicon oxide. Notably, the EOT shows a near-linear relationship with the $Sm_2O_2SO_4$ thickness, implying that a 1.7 nm EOT can be achieved with a thickness of 6.5 nm nanoplate (Fig. 2e).

Beyond the dielectric constant, a low leakage current and high breakdown strength ($E_{bd}$) of dielectric materials are also important performance parameters for reducing device power consumption[46–48]. The $Sm_2O_2SO_4$ nanoplates sandwiched between Cr/Au electrodes demonstrate the large $E_{bd}$ in the range 1215 MV $cm^{-1}$ (Fig. 2f), almost triple that of perovskite $SrTiO_3$ membranes[32], which are significantly higher than the required by the International Technology Roadmap for Semiconductors (ITRS)[49]. The thermal stability and electrical reliability of $Sm_2O_2SO_4$ nanoplates were also evaluated, as these properties are critical for ensuring their performance in device applications. To ensure the reliability of the breakdown field strength results, we performed at least three independent measurements on different samples, as shown in Supplementary Fig. 17. All experimental results indicate that the breakdown field strength exceeds 10 MV/cm for samples of different thicknesses. Thanks to its high crystallinity and wide bandgap, the $Sm_2O_2SO_4$ nanoplates maintain a high breakdown field strength of up to 10 MV/cm even at a high testing temperature of 500 K, demonstrating the robust breakdown performance of $Sm_2O_2SO_4$ at various thicknesses. They exhibited a low leakage current of the order of $10^{-2}$ A $cm^{-2}$ under 7.5 MV $cm^{-1}$ (Fig. 2g). Low leakage current can be attributed to the well-defined vdW gap, which primarily improves leakage and stability by introducing an additional barrier at the interface to extend the carrier tunneling path, suppressing the interference of interfacial defects with charge transport, and alleviating stress concentration induced by lattice or thermal mismatch. To further confirm the potential of $Sm_2O_2SO_4$ as a dielectric, the relationship between the breakdown field strength and corresponding dielectric constant of currently reported dielectrics was summarized in Fig. 2h. Given the superior dielectric properties of crystalline $Sm_2O_2SO_4$ nanoplate, it is a promising insulating candidate for integration into high-performance FETs with 2D semiconductor channels.

## High-performance 2D FETs with $Sm_2O_2SO_4$ as gate insulator

To investigate the dielectric modulation effect of $Sm_2O_2SO_4$, $MoS_2$ FETs with $Sm_2O_2SO_4$ as the top-gate dielectric were fabricated using the mechanical stacking method. (Supplementary Fig. 18). The device structure is shown schematically in Fig. 3a. The $Sm_2O_2SO_4/MoS_2$ top-gate FET was fabricated on a $SiO_2/Si$ substrate, utilizing Cr/Au as the source and drain electrodes. To ensure that Cr/Au exhibits a low contact resistance, we extracted its contact resistance $R_c$ of 0.97 kΩ·μm using the TLM method, demonstrating reliable ohmic contact (see Supplementary Note 1 and Supplementary Fig. 19). It is important to emphasize that the focus of this work is not on the scaling of contact resistance. The output curves of the $Sm_2O_2SO_4/MoS_2$ FET show excellent gate control, as evidenced by the linear $I_{ds}$-$V_{ds}$ curve at low $V_{ds}$ and saturation at high $V_{ds}$, and exhibit a good ohmic contact between the electrodes and $MoS_2$ (Fig. 3b). The corresponding transfer curves demonstrates a high on/off ratio of $10^7$ and low gate leakage currents as low as $7 \times 10^{-7}$ A $cm^{-2}$ across a $V_{tg}$ sweep from −1.0 to 1.0 V (Fig. 3c). There was a sharp increase in drain current in the subthreshold region, with an average subthreshold slope (SS) of ~65.2 mV $dec^{-1}$ and a low drain-induced barrier lowering (DIBL) value of ~21 mV/V (Supplementary Fig. 20). Particularly, remains close to 60 mV $dec^{-1}$ across more than two orders of magnitude of the drain-source current and stays below 100 mV $dec^{-1}$ over three orders of magnitude of $I_{ds}$ (Fig. 3d). More importantly, we also investigated the thermal stability and electrical reliability of the $Sm_2O_2SO_4/MoS_2$ FETs. For a typical $MoS_2$ FET device, the on/off current states could be well maintained even after being stored in air for 1 month, with an insignificant shift in threshold voltage (Supplementary Fig. 21). Benefitting from the high-quality interface with the low interfacial defect density between the $Sm_2O_2SO_4$ and $MoS_2$, the devices had an negligible hysteresis as low as 5.4 mV in the $I_{ds}$-$V_{tg}$ curve (Fig. 3e), ensuring the operational stability. The thermal stability of the dielectric properties in single-crystalline $Sm_2O_2SO_4$ allowed the $MoS_2$ FET device to maintain consistent performance without noticeable degradation even at a testing temperature of 500 K, exhibiting a small hysteresis width $\Delta V_{tg}$ of no more than 24.4 mV (Fig. 3e, Supplementary Fig. 22).

To further validate the performance of the $Sm_2O_2SO_4$-based top-gate FET devices, we fabricated $MoS_2$ transistors with higher on-state currents. Using high-quality $MoS_2$ single crystals (as shown in Supplementary Fig. 23), we have fabricated $MoS_2$ FETs that achieve a switching ratio of up to $10^9$. We further extracted the transconductance and mobility of the devices, with a maximum transconductance of approximately 38 μS/μm and a maximum mobility of around 81 $cm^2V^{-1}$ $s^{-1}$. These results confirm that, under conditions of lower defect density and higher crystal quality, the $MoS_2$ FET devices with $Sm_2O_2SO_4$ as the gate dielectric demonstrate good electrical performance, further validating the positive impact of material and process optimization on device performance. When the channel length of $MoS_2$ FETs is reduced to 100 nm, $Sm_2O_2SO_4$ demonstrates good electrical performance as a gate dielectric (Supplementary Fig. 24). Electrical statistics show that all devices exhibit steep subthreshold slopes (Supplementary Fig. 25), with the on/off ratio and field-effect mobility following a Gaussian distribution, averaging $7 \times 10^6$ and 48.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$, respectively. The key parameters for transistors, such as on/off ratio, SS, hysteresis, EOT and $E_{bd}$, listed in Supplementary Table 1, highlight the great potential of $Sm_2O_2SO_4$ single crystals for application in 2D electronics. These results demonstrate that the $MoS_2$ FETs gated with $Sm_2O_2SO_4$ dielectrics exhibit excellent thermal stability and electrical reliability.

In the microelectronics industry, traditional amorphous oxide dielectrics are typically integrated with semiconducting channels using ALD method, which often induces a substantial density of defects at the dielectric/semiconductor interface due to uncontrolled chemical bonding. These defects lead to the formation of border traps, which capture charge during device operation, resulting in increased

https://doi.org/10.1038/s41467-025-68007-6

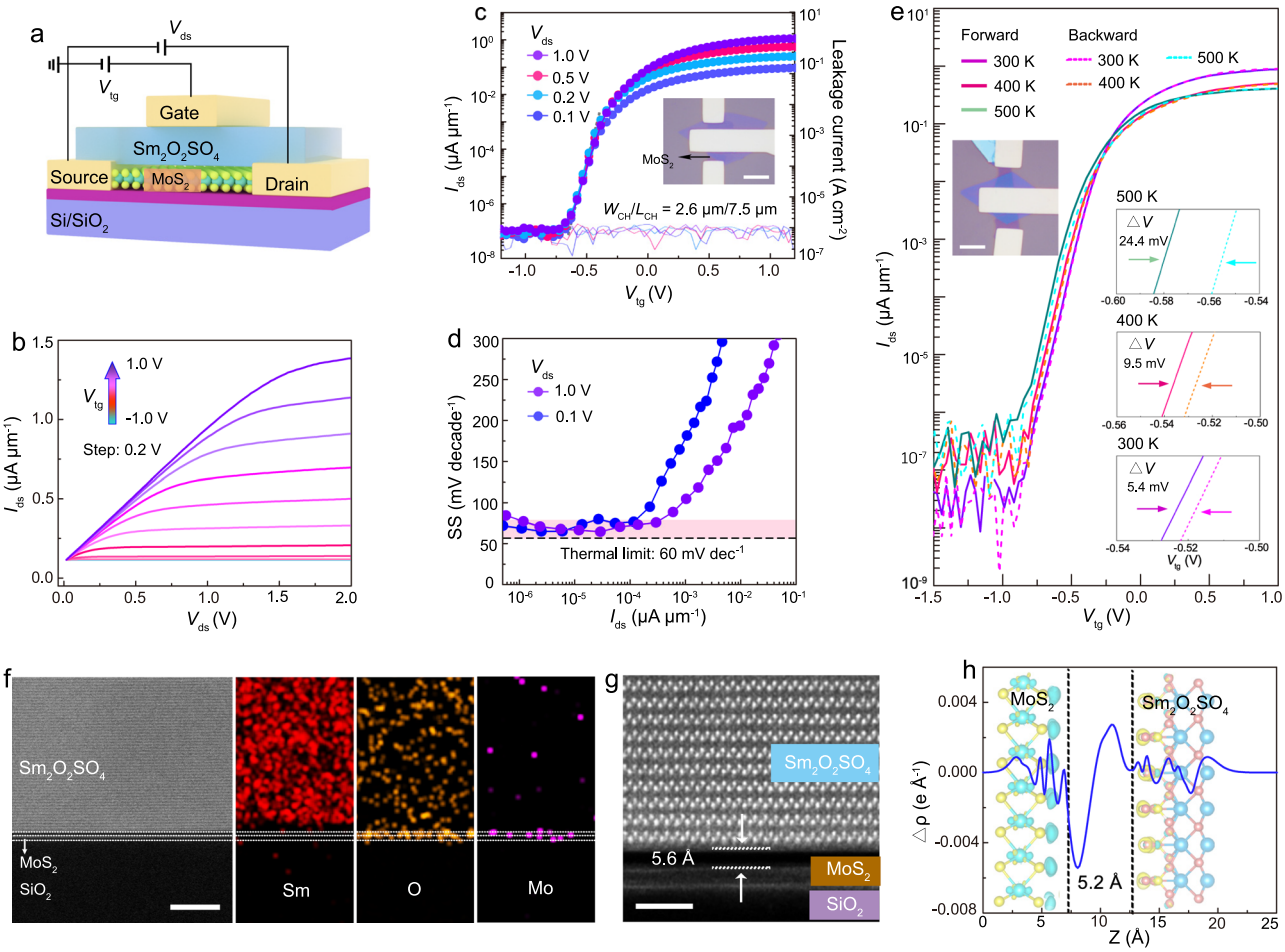


**Fig. 3 | Electrical characteristics of $MoS_2$ FETs based on high-$\kappa$ $Sm_2O_2SO_4$ dielectrics. a** Schematic of the top-gated $MoS_2$ FETs. **b**, **c** The output curves and transfer curves of a typical $MoS_2$ FET with $Sm_2O_2SO_4$ top gate. Inset: OM image of $Sm_2O_2SO_4/MoS_2$ FET. (channel width/channel length: $W_{CH}/L_{CH}$ = 2.6 μm/7.5 μm, $MoS_2$ thickness: 3.1 nm). Scale bars: 5 μm. **d** SS versus $I_{ds}$ extracted from the transfer curves. The dashed line marks 60 mV dec$^{-1}$. **e** The transfer curves curves of the same device measured at 300, 400 and 500 K. Insets: corresponding hysteresis widths and OM image of $Sm_2O_2SO_4/MoS_2$ FET. Scale bars: 5 μm. **f**, **g** EDS elemental mapping images and a cross-sectional STEM image of the a $Sm_2O_2SO_4/MoS_2$ heterointerface. Scale bars: 10 and 1 nm. **h** Plane-averaged differential charge density of the $Sm_2O_2SO_4/MoS_2$ vdW heterostructure as a function of position along z direction.

subthreshold swing, wider hysteresis, and threshold voltage shift. The interfacial microstructure of top-gated $MoS_2$ FET was analyzed by cross-sectional STEM image and EDS mapping. Figure 3f and Supplementary Fig. 26, the $Sm_2O_2SO_4/MoS_2$ shows a uniform layer thickness and clean, flat surfaces with a typical vdW gap. Atomic-resolution HAADF-STEM image in Fig. 3g exhibits a vdW gap of ~5.6 Å without any structural disorder, indicating a perfect interface with low carrier tunneling probability. The interface trap density ($D_{it}$) was extracted based on the following equation:

$$SS = \ln(10)\frac{k_B T}{q}\left(1+\frac{qD_{it}}{C_G}\right) \quad (4)$$

where $k_B$ is Boltzmann constant, $T$ is absolute temperature, $q$ is the elementary charge and $C_G$ is the gate capacitance. A low $D_{it}$ value of $4.87\times10^{11}$ cm$^{-2}$ eV$^{-1}$ can be achieved, which demonstrates its superiority compared to previously reported 2D $MoS_2$ FETs with conventional oxides (Supplementary Table 2). To investigate the vdW interface between the $Sm_2O_2SO_4$ dielectric and the $MoS_2$ channel, a differential charge density calculation was carried out on the $Sm_2O_2SO_4/MoS_2$ heterostructure using DFT calculations. As shown in Fig. 3h, there is no charge accumulation at the $Sm_2O_2SO_4/MoS_2$ interface, indicating the absence of bonding interactions between $Sm_2O_2SO_4$ and $MoS_2$. Additionally, from the planar-averaged electron density difference curve, the average vdW gap is 5.2 Å, which is consistent with the cross-sectional atomic-resolution HAADF-STEM data. This value is significantly larger than the combined covalent radii of both O and S atoms, further supporting the existence of a vdW contact.

## Non-volatile FG memory based on $MoS_2$/*h*-BN/MLG/$Sm_2O_2SO_4$/MLG

Floating gate (FG) memory, as a classic non-volatile storage technology, has been a research focus due to its high storage density, low power consumption, and excellent data retention capabilities[17]. However, conventional silicon-based FG memory suffers from high tunneling barriers and dangling bond issues at the $Si/SiO_2$ interface, leading to slow operation, increased power consumption, and limited data retention[5,50–52]. 2D layered atomic-scale sharp high-$\kappa$ dielectric materials, with their outstanding electrical properties and high stability, have emerged as promising alternatives to $SiO_2$. They can effectively enhance the GCR of FG memory while enabling miniaturized integration[6,8,10]. A high GCR translates to faster programming, a larger memory window, lower power consumption, extended data retention, and low-voltage operation. We have leveraged the high dielectric constant and wide bandgap characteristics of $Sm_2O_2SO_4$ to successfully fabricate a high-GCR FG memory device based on a $MoS_2$/*h*-BN/MLG/$Sm_2O_2SO_4$/MLG vdW heterostructure, where the channel material $MoS_2$, tunneling *h*-BN, floating gate MLG, blocking $Sm_2O_2SO_4$ and

https://doi.org/10.1038/s41467-025-68007-6

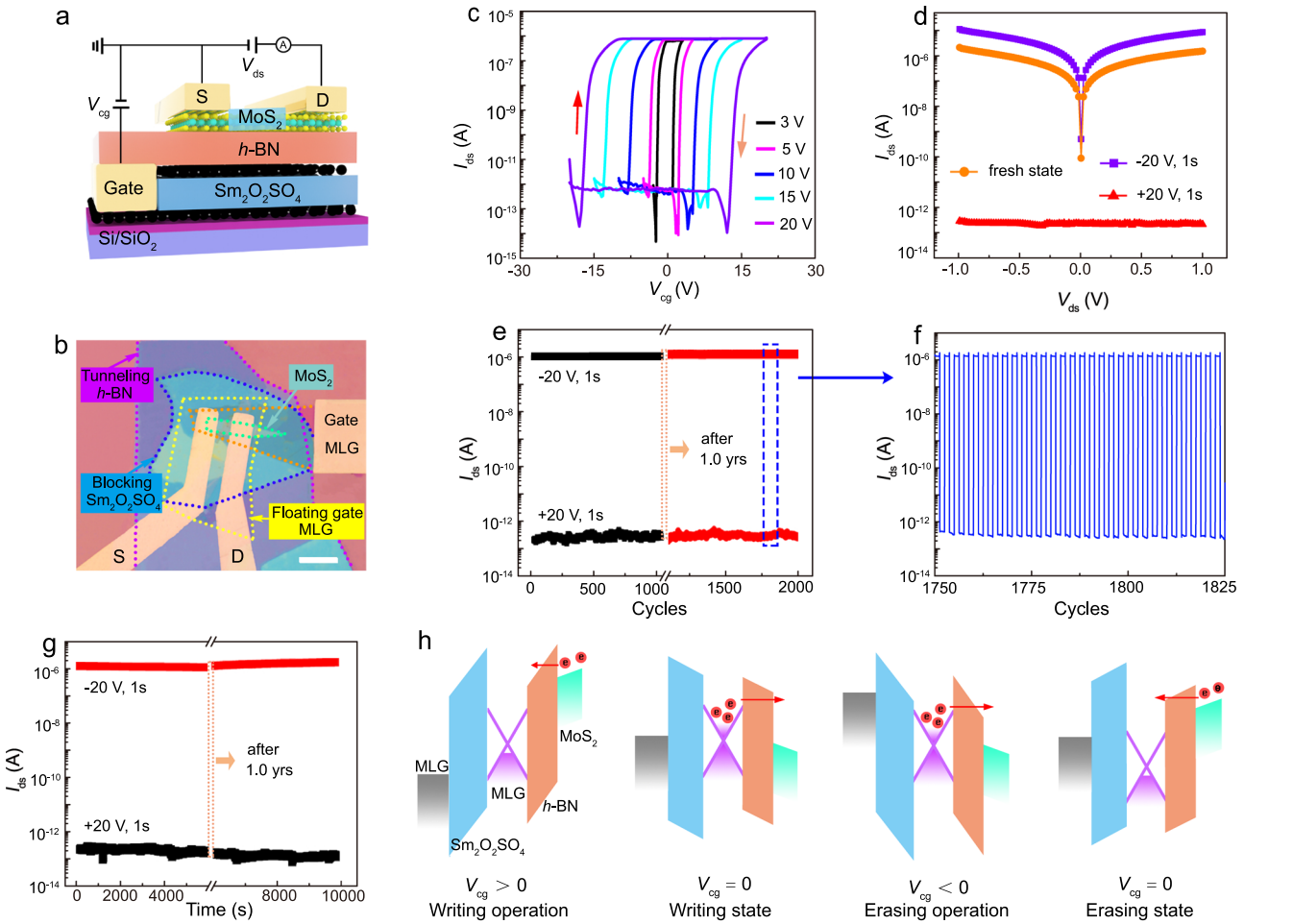


**Fig. 4 | Electrical characterizations and memory performances of the ultrafast floating gate nonvolatile memory device. a** Schematic diagram of the nonvolatile memory device. The functional layers from top to bottom are the channel material $MoS_2$, tunneling hexagonal boron nitride (*h*-BN), floating gate multilayer graphene (MLG), blocking $Sm_2O_2SO_4$ and control gate MLG. **b** Optical image of a memory device based on the $MoS_2$/*h*-BN/MLG/$Sm_2O_2SO_4$/MLG heterostructure. Scale bars: 5 μm. **c** Transfer curves of the device under bidirectional sweeping of different control gate voltage ($V_{cg}$) values and a $V_{ds}$ of 0.1 V, step: 200 mV/s. **d** Output characteristic curves of the device under the fresh state (no charge in the floating gate, orange), off-state and on-state (after a 1-second-wide voltage pulse of +20 V and −20 V applied to MLG control gate, red and purple) configurations. **e** Endurance performance of the nonvolatile memory device for 2000 cycles, showing the robustness of the all-2D-materials based nonvolatile memory device. **f** The real-time variation of the channel current value for multiple cycles as highlighted in **e** with the blue dashed box. **g** The retention characteristics of the device keep almost unchanged after 1.0 year. **h** Schematic energy-band diagrams of the nonvolatile memory device for writing and erasing program.

control gate MLG from top to bottom, respectively (Fig. 4a and Supplementary Fig. 27, 28). The corresponding OM image of the FG memory device is provided in Fig. 4b. With this configuration, our fully 2D memory device achieves a GCR as high as ~0.83 (further explained in the Supplementary Note 2), significantly exceeding that of silicon-based flash memory (0.49-0.57) and the state-of-the-art FG FET using *h*-BN as the blocking layer (0.6)[6,8,10]. Figure 4c exhibits the transfer curves obtained by scanning the control gate voltage ($V_{cg}$) from negative to positive values and then back to negative values, under a drain-source bias maintained at 0.1 V. A significant clockwise memory window ($\Delta V$) increases almost linearly with the maximum $V_{cg}$ (Supplementary Fig. 29), where $\Delta V$ is defined as the difference between the positive and negative $V_{th}$ offsets. Notably, even at $V_{cg} < 3$ V, a memory window exceeding 3.4 V is achieved, attributed to the high-$\kappa$ $Sm_2O_2SO_4$ enhancing GCR and effectively increasing the tunneling field in the *h*-BN layer. The output curves at different control voltages are shown in Fig. 4d. The output characteristic curve of the FG memory device (purple curve, fresh state) under no control gate voltage pulse exhibits a typical on-state with symmetric current due to initial doping of $MoS_2$, also indicating a good ohmic contact at Cr/Au and $MoS_2$ interfaces. When a positive voltage pulse (+20 V, 1 s width) is applied to the MLG control gate, the electrons are injected from the $MoS_2$ channel into the floating-gate MLG through the tunneling layer *h*-BN and are blocked by the blocking $Sm_2O_2SO_4$ layer. This causes a redistribution of the charge in the top $MoS_2$ layer, leading to the device entering the off-state. On the contrary, when a negative control gate voltage pulse is applied, the holes are injected into the floating-gate MLG, causing a change in the floating gate charge, which modulates the electrical properties of the top $MoS_2$ layer. As a result, the device enters the on-state, exhibiting higher conductivity.

More importantly, our devices operated with excellent long-term memory stability and electrical reliability. The endurance performanceof FG memory device is validated by repeatedly programming and erasing the $MoS_2$/*h*-BN/MLG/$Sm_2O_2SO_4$/MLG vdW heterostructure (Fig. 4e), which shows that the on and off states of the current could be well maintained even after operating for more than 1000 cycles. Additionally, after 1.0 year, the repeated programming and erasing of the FG memory device for another 1000 cycles reveals no apparent change in either the program and erase states, demonstrating excellent durability and stability. Figure 4f shows an enlarged real-time memory state, indicating a stable transition between high and low current states. To verify the reliability of $Sm_2O_2SO_4$ as a blocking

dielectric, the maximum allowable voltage of 20 V was used as the operating voltage. After writing (+20 V) and erasing (-20 V) with a pulse duration of 1 s, the on/off ratio remained ~$10^6$ after 6000 s under a fixed $V_{ds}$ of 0.1 V at $V_{cg}$ = 0 V (Fig. 4g), indicating a low back-tunneling probability by using $Sm_2O_2SO_4$ as the blocking layer. Even after 1.0 year, the two current states characteristics of FG memory device show almost no changes. Additionally, we further evaluated the device's fast programming/erasing performance (Supplementary Fig. 30). The results demonstrate that the device is capable of performing programming and erasing operations within nanosecond timescales (55.9 ns for erasing and 54.2 ns for programming), showing clear and stable state transitions. We further evaluated its energy efficiency, and the calculation results show that the energy consumption per pulse is 2.97 pJ (detailed in Supplementary Note 3). To further validate the long-term stability of the $Sm_2O_2SO_4$-based floating-gate memory, we conducted testing using the Arrhenius method[6]. The results indicate that the memory exhibits over 10 years of stability, with a characteristic temperature of 179.2 °C and an activation energy of 2.03 eV (Supplementary Fig. 31 and Supplementary Note 4). Figure 4h illustrates the writing and erasing mechanisms of the device. When a positive pulse ($V_{cg} > 0$ V) is applied, electrons primarily tunnel from the $MoS_2$ channel into the MLG floating gate via Fowler–Nordheim (FN) tunneling. The $Sm_2O_2SO_4$ blocking layer effectively shields the control gate electric field, facilitating electron accumulation and stable storage. Conversely, when a negative pulse ($V_{cg} < 0$ V) is applied, the electrons in the floating gate tunnel back to the $MoS_2$ channel through FN tunneling, restoring the erased state. As shown in Supplementary Table 3, we compared the key performance of our device with other advanced 2D floating-gate memory devices. Our results demonstrate that the fully 2D high-GCR FG FET structure based on high-$\kappa$ $Sm_2O_2SO_4$ can overcome the low-power and low-GCR integration bottlenecks of conventional flash memory, holding potential for the development of next-generation low-power, fast non-volatile memory technologies.

In summary, we have shown that 2D crystalline high-$\kappa$ $Sm_2O_2SO_4$ dielectric can be synthesized via a molten-salt-assisted CVD method on a mica substrate. The ultrathin $Sm_2O_2SO_4$ nanoplates have atomically flat surfaces, wide bandgap, high dielectric constants, and large breakdown strength, which could make it a potential dielectric for 2D FETs and other storage devices. Top-gated $MoS_2$ FETs using $Sm_2O_2SO_4$ as the dielectric exhibited an $I_{on}/I_{off}$ ratio of $10^9$, a negligible hysteresis of 5.4 mV, a steep SS of 65.2 mV $dec^{-1}$, and a low top-gate leakage current of $7 \times 10^{-7}$ A/cm$^2$. Furthermore, we demonstrated the use of $Sm_2O_2SO_4$ dielectric as a blocking layer in FG memory, verifying the feasibility of miniaturized integration and low power consumption in 2D high-GCR FG devices. The dielectric properties of ultrathin crystalline $Sm_2O_2SO_4$ nanosheets provide potential opportunities for developing low-power, fast electronic devices using the vdW integration strategy.

## Methods

### Synthesis and transfer of ultrathin $Sm_2O_2SO_4$ nanoplates

2D $Sm_2O_2SO_4$ single crystals were obtained by a molten-salt-assisted CVD system, which equipped with a 2-inch diameter quartz tube. $Sm_2(SO_4)_3 \cdot xH_2O$ powders (purity 99.9%, Aladdin) and KI powders (purity 99.9%, Aladdin) were dispersed on fluorophlogopite mica ($KMg_3(AlSi_3O_{10})F_2$) substrate and placed in the center of the furnace as the reactant and solvent. Prior to the growth process, the furnace was purged with ultra-high purity argon (Ar) gas at a flow rate of 500 sccm for 10 minutes to eliminate residual oxygen. Then, the system was heated from room temperature to 680 °C in 15 min and maintained for 10 min for ultrathin nanoplates growth at the Ar/$H_2$ carrier gas with the flow rate of 80/20 sccm. After growth, the ultrathin nanoplates were transferred onto a target substrate via the polystyrene (PS) assisted transfer method, as shown in Supplementary Fig. 7. Firstly, PS solution was spin-coated on the mica with grown ultrathin nanoplates, followed by drying at 80 °C for 5 minutes. Then, the PS-capped substrate was placed in deionized water and then the PS film with ultrathin nanoplates was carefully lifted off the mica. Subsequently, the film was attached onto the target substrates (such as copper grid and silicon substrate). Finally, after drying on a hot plate with 80 °C for 2 min, the PS layer was removed by hot acetone (70 °C for 10 min), completing the transfer of the ultrathin nanoplates.

### Material characterization

The morphology and thickness characteristics of the ultrathin nanoplates were characterized by OM (Nikon instrument ECLIPSE LV150N) and AFM (Bruker Dimension Icon), respectively. Raman and PL spectra were recorded using a micro-Raman spectrometer (LabRAM HORIBA) with a 532 nm excitation laser source. The chemical composition and crystal microstructure were investigated through XPS (250Xi ESCALAB), TEM (JEM-ARM200F, JEOL), STEM (FEI-Titan Cubed Themis G2 300). The bandgap of ultrathin nanoplates was characterized by the ultraviolet-visible absorption spectrometer (Mstarter ABS).

### Density functional theory calculations

All DFT calculations were conducted using the Vienna ab initio simulation package (VASP). The exchange-correlation interactions were described using the Perdew–Burke–Ernzerhof (PBE) form of the generalized gradient approximation (GGA). The interactions between ion cores and valence electrons were treated using the projector augmented wave (PAW) method. A plane-wave cutoff energy of 500 eV was set to ensure convergence and accuracy. For geometry optimization, a Γ-centered 3 × 3 × 1 Monkhorst-Pack k-point grid was used, and all structures were fully relaxed until the residual forces on each atom were below 0.01 eV/Å. To prevent spurious interactions between periodic images in the vertical direction, a vacuum layer larger than 20 Å was introduced. After structural relaxation, the band gap was calculated using a denser 6 × 6 × 3 k-point mesh.

### Device fabrication and measurements

To fabricate the metal-insulator-metal (MIM) capacitors, bottom electrodes (5/50 nm Cr/Au) were first patterned on quartz substrates via electron beam lithography (EBL) followed by electron beam evaporation. Subsequently, $Sm_2O_2SO_4$ nanoplates were transferred onto the patterned bottom electrodes using a PS and polydimethylsiloxane (PDMS)-assisted transfer technique on a 2D material transfer platform. Finally, top electrodes composed of Cr/Au (5/50 nm) were defined through a second EBL patterning and electron beam evaporation process.

For the Gr and $MoS_2$ FETs, mechanically exfoliated Gr and $MoS_2$ flakes were transferred onto a $SiO_2$/Si substrate, followed by the transfer of grown $Sm_2O_2SO_4$ nanoplates onto the Gr and $MoS_2$ flakes, respectively. After that, Cr/Au (5/50 nm) electrodes were deposited using standard EBL and electron beam evaporation. The fabrication process for the FG memory devices, apart from the use of graphene as the bottom-gate electrode, was largely identical to that of the FETs. Specifically, the graphene stripes through mechanical exfoliation from bulk graphite crystals are firstly transferred on a $SiO_2$/Si substrate as a bottom-gate electrode. Then, $Sm_2O_2SO_4$, graphene, BN, and $MoS_2$ layers were sequentially transferred onto the back-gate electrode using a 2D material transfer platform. Finally, the Cr/Au source-drain electrodes were fabricated on it by EBL and electron beam evaporation process.

Electrical characterizations of the MIM capacitors, FETs, and FG memory devices were carried out using a semiconductor parameter analyzer (Keithley 4200) equipped with capacitance-voltage measurement modules, in a vacuum probe station (TTPX, Lake Shore) with a base pressure of approximately $10^{-4}$ Torr. All electrical measurements were performed at room temperature unless otherwise stated.

## Data availability

The Source Data underlying the figures of this study are available with the paper. All raw data generated during the current study are available from the corresponding authors upon request. Source data are provided with this paper.

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## Acknowledgements

This work was supported by the National Natural Science Foundation of China (Nos. 62575285, 92580123 to W.L., Nos. 52372240 and Nos. U23A2094 to Q.C.), the China Postdoctoral Science Foundation (Nos. 2023M733495 to C.J., Nos. 2025M770054 to Q.J.), the Self-deployment Project Research Program of Haixi Institutes, Chinese Academy of Sciences (Nos. CXZX631 2022-GH09 to W.L.), and the Self-deployed Key Project of State Key Laboratory of Functional Crystals and Devices (GNJT-2025-ZD06 to W.L.).

## Author contributions

W.L. conceived the original idea and supervised the entire project. J.Y. and C.J. contributed equally to the work. J.Y. and C.J. completed all the experiments together with Q.J., Q.C. and Y.G. helped to conduct the testing and analysis of capacitor devicesed. J.K. co-supervised the entire project and provided constructive suggestions. All authors participated in scientific discussions.

## Competing interests

The authors declare no competing interests.

## Additional information

**Supplementary information** The online version contains supplementary material available at https://doi.org/10.1038/s41467-025-68007-6.

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**Peer review information** *Nature Communications* thanks Cheng-Yan Xu, Yu Zhou, and the other, anonymous, reviewer for their contribution to the peer review of this work. A peer review file is available.