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Intrinsically stretchable 2D MoS_2 transistors

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Intrinsically stretchable electronics is rapidly emerging as a transformative platform for next-generation electronics, offering novel form factors and enhanced capabilities. Herein, we report high-performance intrinsically stretchable thin-film transistors based on two-dimensional semiconducting flakes. Our n-type molybdenum disulfide transistors exhibit a maximum field-effect mobility up to 12.5 $cm^2V^{-1}s^{-1}$ (average 8 $cm^2V^{-1}s^{-1}$) and an on/off current ratio above 10^7, even under 20% strain, and demonstrate stable performance during cyclic stretching tests. Structural analysis revealed that mechanical strain was accommodated via interflake motions; the flakes are connected by weak van der Waals bonds, enabling effective stress relaxation within the transistor channel. Furthermore, charge transport from the source to the drain in the channel remains robust as long as the vertical interconnection between the flakes and the substrate is maintained under stretching. This strain accommodation mechanism offers a generalizable pathway for integrating van der Waals semiconductors into stretchable electronics and addresses the critical lack of high-performance stretchable n-type materials for complementary metal-oxide–semiconductor integration, paving the way for logically capable and scalable deformable systems.

Wearable electronics, soft robotics, and stretchable displays require electronic components, particularly stretchable transistors with active layers that can deform uniformly under strain without relying on engineered structural motifs such as serpentine or Kirigami designs[1,2]. Intrinsically stretchable architectures offer distinct advantages, including simple layouts and good compatibility with scalable manufacturing techniques, such as printing and photolithography. Despite substantial research progress, intrinsically stretchable transistors reported to date rely on a limited number of semiconductor materials. First, conjugated polymers with flexible backbones are used either in their neat form or as composites with elastomers[3–6]. Although stretchability can be achieved by suppressing crystallinity or aggregation, both of which hinder deformation, these strategies often reduce the electrical performance, resulting in materials that have limited applicability in high-performance electronic systems. The second category includes single-walled carbon nanotube (SWCNT)-based composites, which maintain percolative pathways under moderate strain and have recently demonstrated high charge-carrier mobility and mechanical durability[7–9]. However, the relatively high off-state current due to the imperfect separation of metallic and semiconducting SWCNTs, anisotropic charge-transport characteristics arising from the one-dimensional structure, and the lack of robust n-type dopants present significant challenges for large-area complementary metal–oxide–semiconductor (CMOS) implementation.

Recently, two-dimensional (2D) van der Waals (vdW) materials have shown promise for use in ultraflexible electronic devices owing to their atomic-level thickness and high carrier mobility[10–13]. As a representative 2D material, MoS_2 offers n-type semiconducting properties[14,15]. However, its monolayer form is mechanically rigid[16], making it unsuitable for intrinsically stretchable devices. Solution-processed MoS_2 flakes provide

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a practical alternative, combining large-area processability with inherent mechanical deformability through interflake sliding and rearrangement under strain[17,18]. This mechanical behavior, demonstrated through molecular dynamics simulations and experiments with thin-film configurations[19–21], highlights the potential of MoS_2 flakes as active materials for intrinsically stretchable electronics.

Despite the development of potential materials, intrinsically stretchable field-effect transistors (FETs) based on 2D materials have not yet been reported. In-depth studies on the fundamental strain accommodation mechanisms of vdW architectures are essential to facilitate their integration into practical stretchable electronic systems. In addition, the development of CMOS circuits composed of n- and p-MOS transistors is necessary to scale intrinsically stretchable electronics into a high-performance, commercially viable technology. While intrinsically stretchable p-type semiconductors have steadily advanced, limited progress in their n-type counterparts has been achieved owing to the limitations of conjugated polymers and SWCNT-based materials.

Here, we report high-performance, intrinsically stretchable n-type FETs based on 2D MoS_2 flakes that exhibit both high electron mobility and high on/off ratios (Fig. 1). Transistor arrays fabricated on industry-standard 8-inch wafers using conventional photolithography processes achieved electron mobilities up to 12.5 $cm^2\,V^{-1}\,s^{-1}$ (average 8 $cm^2\,V^{-1}\,s^{-1}$) and on/off ratios above 10^7. The devices maintained their field-effect mobility (μ_{FET}) under 20% strain regardless of the stretching direction and demonstrated stable performance in cyclic stretching tests. The stress variations in the MoS_2 flakes were analyzed in detail using Raman mapping to determine the underlying deformation mechanisms during stretching. This study provides a foundation for developing FETs based on other vdW semiconductors, enabling the integration of transition metal dichalcogenide flakes, thereby accelerating the development of high-performance intrinsically stretchable circuits.

Results

Fabrication of transistor array

The structure of the intrinsically stretchable MoS_2 FET is shown in Fig. 2a. It features a bottom-gate, bottom-contact architecture. Styrene-ethylene-butylene-styrene (SEBS) block copolymer was used as the stretchable substrate and encapsulation material, while poly(-acrylonitrile-co-butadiene) (NBR) and SEBS were used as the dielectric layer. These elastomer polymers were crosslinked to enhance mechanical stability (Supplementary Fig. 1). As a stretchable gate, source, and drain electrode, Au was deposited slowly onto the elastomer surfaces to form an interpenetrating network-like morphology. During this process, Au atoms diffused into the free volume of the polymer, leading to the nucleation of Au clusters that became firmly anchored within the bulk.

MoS_2 ink was prepared by dispersing electrochemically exfoliated MoS_2 flakes in isopropyl alcohol (IPA). The UV-Vis absorption spectrum of the ink exhibits distinct excitonic peaks at 438, 613, and 675 nm, confirming the presence of high-quality semiconducting MoS_2 flakes (Supplementary Fig. 2). Coating the ink onto a substrate revealed that the flakes had an average lateral size of 1.16 μm, with more than half of them being around ~2.2 nm thick. Raman spectroscopy confirmed that these flakes corresponded to three-layer MoS_2, exhibiting characteristic peaks at 384.3 cm^{-1} (E_{2g}) and 405.8 cm^{-1} (A_{1g})[22]. After three spin-coating steps for full film coverage of the FET channel, the Raman spectrum exhibited peaks at 382.9 cm^{-1} (E_{2g}) and 407.1 cm^{-1} (A_{1g}), consistent with bulk properties of MoS_2. TEM imaging over an area of approximately 50 × 50 μm^2 revealed that the channel thickness varied, with thin regions consisting of 4–6 layers of MoS_2 and thick regions with up to 30 layers. (Supplementary Fig. 3).

To fabricate FET channels, as-coated MoS_2 films were subjected to bis(trifluoromethane)sulfonamide (TFSI)-based strong-acid treatment and annealing at 200 °C to reduce unintentional n-doping[23] (Supplementary Fig. 4). However, these processes pose a challenge for stretchable FETs, because the elastomer substrate can be easily damaged by acids and heat. To address this, we employed a transfer method in which MoS_2 was first coated, treated with acid, and annealed on an oxide substrate, such as SiO_2, and then transferred onto a stretchable FET platform (Supplementary Fig. 5). The MoS_2 layer was spontaneously delaminated from the substrate in an aqueous environment due to the difference in hydrophilicity between the oxide surface and MoS_2, enabling transfer. Further analyses confirmed that MoS_2 retained its properties after transfer. Raman spectroscopy

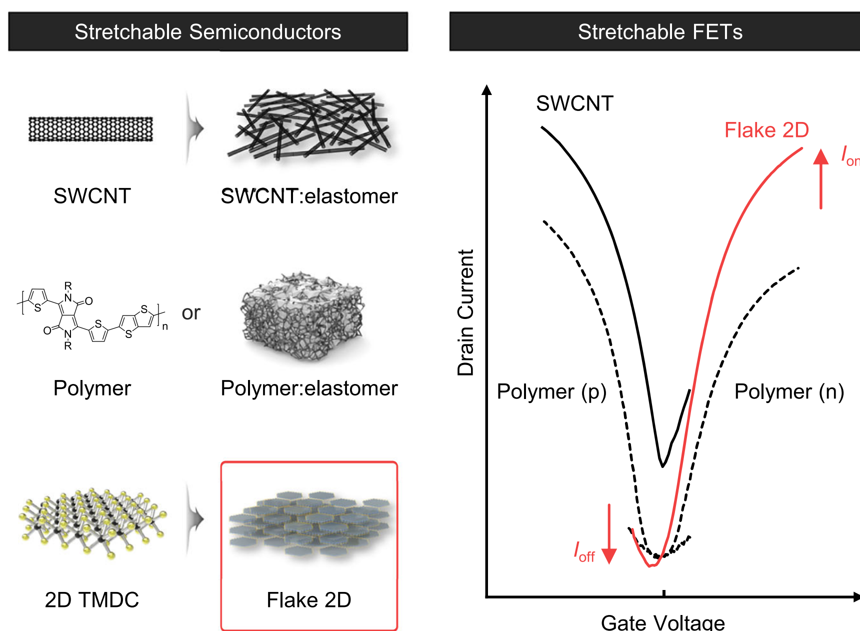

Fig. 1 | Intrinsically stretchable semiconductor materials and transfer characteristics of their field-effect transistors (FETs). Single-walled carbon nanotubes (SWCNT)-based composites, polymer semiconductors with or without elastomer blending, and flake-type transition metal dichalcogenide (TMDC) materials enable p- and n-type stretchable transistors with distinct on-current (I_{on}) and off-current (I_{off}) characteristics.

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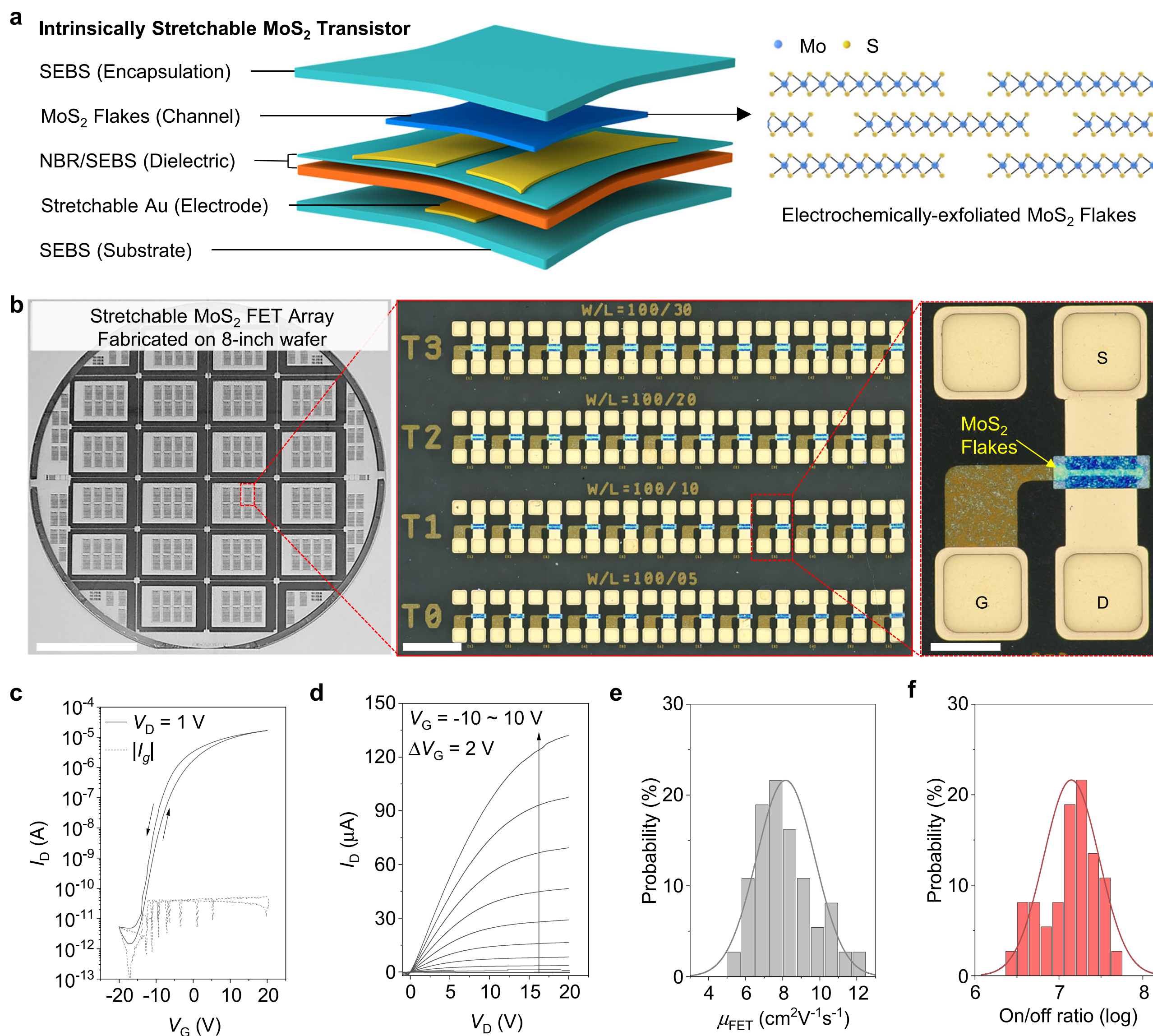

Fig. 2 | Eight-inch wafer-scale intrinsically stretchable MoS_2 transistor array. **a** Schematic of the transistor structure. SEBS denotes styrene-ethylene-butylene-styrene, and NBR denotes poly(acrylonitrile-co-butadiene). **b** Photograph and optical microscopy images of the transistor array on an 8-inch wafer. Scale bars: 60 mm (left), 500 μm (middle) and 100 μm (right). Representative **c** transfer and **d** output characteristics of the transistors with channel width/length = 100/10 μm. I_D and V_D denote the drain current and drain voltage, respectively, while I_g and V_G denote the gate leakage current and gate voltage. Distribution of **e** field-effect mobility (μ_{FET}) and **f** on/off ratios obtained from the transfer characteristics of 36 individual transistors. The solid lines present Gaussian distributions fitted to the data.

showed no shift in the E_{2g} and A_{1g} peaks of MoS_2 and no MoO_3-related peaks, indicating no oxidation or damage during transfer (Supplementary Fig. 6a). FET characterization also confirmed that the off-current and μ_{FET} were similar before and after transfer (Supplementary Fig. 6b, c).

The choice of gate dielectric plays a crucial role in achieving a high on/off ratio and low operating voltage with intrinsically stretchable MoS_2 transistors (Supplementary Fig. 7). In preliminary tests, FETs with a crosslinked thick SEBS dielectric (~500 nm, κ of 2.17 at 1 kHz) required high gate voltages to turn on, and exhibited poor switching behavior and a low on-current (13.4 μA at V_G = 80 V). This is mainly attributed to the low dielectric constant (κ) of SEBS, which results in a low gate capacitance and weak electrostatic control of the MoS_2 channel. In contrast, when a bilayer dielectric structure (κ of 5.12 at 1 kHz) composed of cross-linked SEBS (~ 90 nm) and NBR (~ 200 nm) was used, the operating voltage was significantly reduced to 20 V, and the on/off current ratio was above 10^7. This enhanced switching performance is attributed to the incorporation of NBR, a high-κ dielectric material that increases the overall gate capacitance and strengthens the electrostatic control over the MoS_2 channel. This enables efficient carrier accumulation in the on-state and suppresses leakage in the off-state, resulting in low-voltage operation, higher on-current (17.4 μA at V_G = 20 V), and improved on/off ratio. These findings underscore the crucial role of high-κ dielectrics in intrinsically stretchable MoS_2 transistors, enabling reliable low-voltage and high-performance operation.

To ensure the stretchability of the source and drain electrodes formed on top of the gate dielectric, it was essential to use an NBR/SEBS bilayer rather than an NBR single layer (Supplementary Fig. 8). Au electrodes deposited directly onto NBR exhibited poor stretchability due to the higher modulus and reduced fraction of soft elastomeric segments in NBR compared to SEBS. This mechanical rigidity likely limits the formation of well-defined compliant microcrack networks that are critical for maintaining electrical conductivity under strain. To

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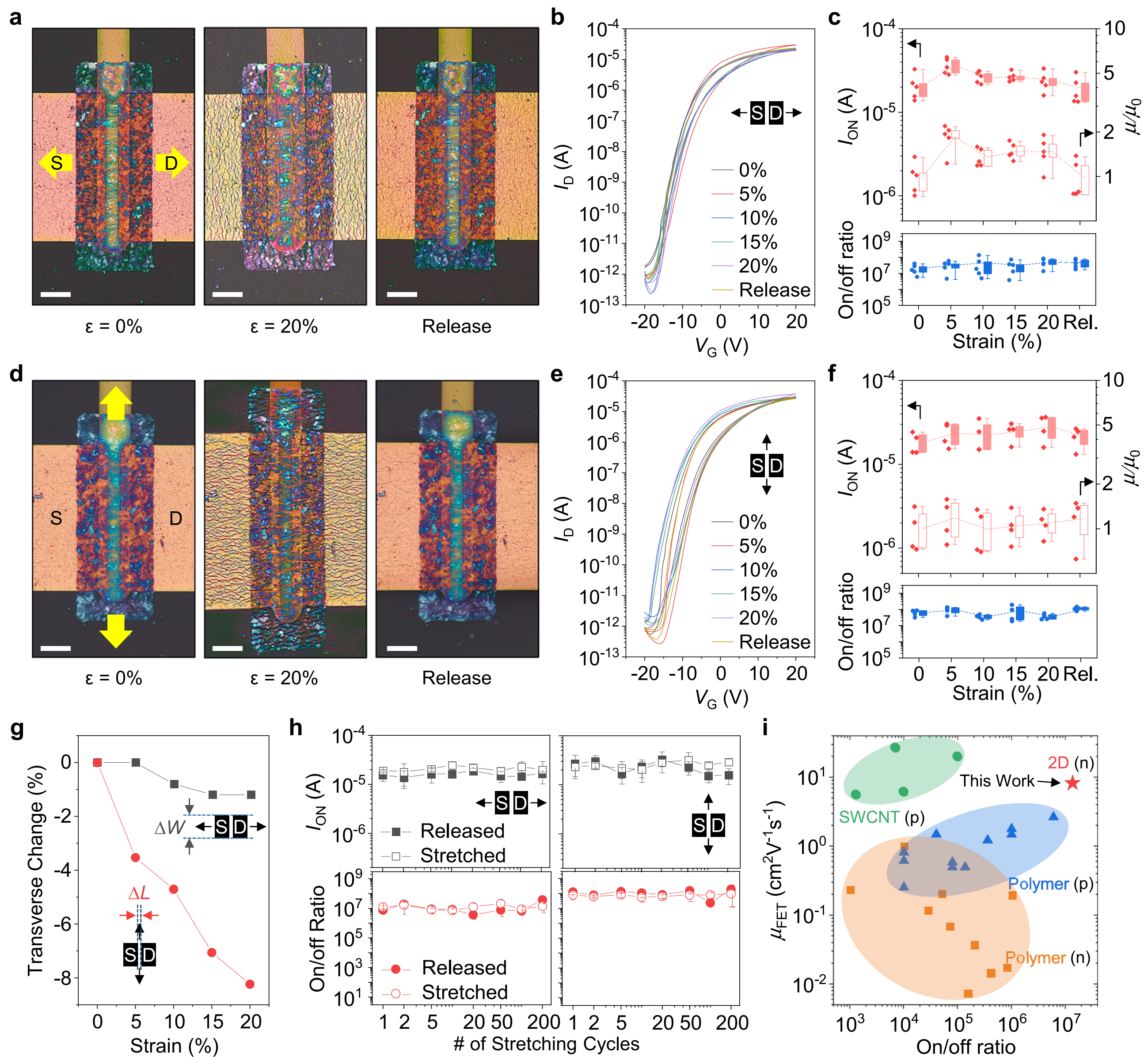

Fig. 3 | Electrical and mechanical properties of intrinsically stretchable MoS_2 transistors under strain. **a** Optical microscopy images, **b** transfer characteristics, and **c** changes in on-current (I_{ON}), μ_{FET}, and on/off ratio under stretching along the charge-transport direction. S and D denote the source and drain electrodes, respectively. Scale bar: 20 µm. **d** Optical microscopy images, **e** transfer characteristics, and **f** changes in on-current, μ_{FET}, and on/off ratio under stretching perpendicular to the charge-transport direction. Scale bar: 20 µm. For (**c**, **f**) data are presented as box-and-whisker plots (4–5 devices), where the box denotes the 25th–75th percentiles and the whiskers indicate the minimum and maximum values. **g** Transverse dimensional changes as a function of applied strain. ΔW and ΔL represent the changes in the channel width and length, respectively. **h** On-current and on/off ratio values during 200 stretch–release cycles. Error bars represent the standard deviation obtained from 5 independent measurements. **i** Comparison of electrical performance with previously reported intrinsically stretchable transistors[3,5–9,24,30–47]. The channel width and length for all evaluated devices are 100 µm and 10 µm, respectively.

address this limitation, a thin SEBS coating was introduced on top of the NBR layer to improve the stretchability of the cracked Au electrodes. Because SEBS is a low-κ dielectric, increasing its thickness undesirably increases the operating voltage of the device. Therefore, the design objective was to minimize SEBS thickness while ensuring adequate electrode stretchability. Through optimization aimed at achieving a strain of at least 50% at a resistance change of $R/R_0 = 10$, the optimal SEBS thickness was determined to be 91 nm (Supplementary Fig. 8c, d). Importantly, this optimized dielectric layer exhibited robust leakage current characteristics even under applied strains of up to 50% (Supplementary Fig. 9).

Based on the optimized processing conditions, an intrinsically stretchable MoS_2 transistor array was fabricated on an 8-inch wafer using conventional photolithography. Representative images of the array are shown in Fig. 2b. The transfer and output characteristics exhibited typical n-type behaviors (Fig. 2c, d). Measurements from 36 individual devices yielded an average μ_{FET} of 8.16 $cm^2 V^{-1} s^{-1}$, with a maximum of 12.16 $cm^2 V^{-1} s^{-1}$. The devices also exhibited a high on/off ratio, averaging greater than 10^7 (Fig. 2e, f, Supplementary Fig. 10).

Electrical characterization under strain

The electrical characteristics of the intrinsically stretchable MoS_2 transistor were evaluated under stretching parallel or perpendicular to the charge-transport direction. The definition of strain depends on the direction; for stretching parallel to charge transport, the strain corresponds to changes in channel length, whereas for perpendicular

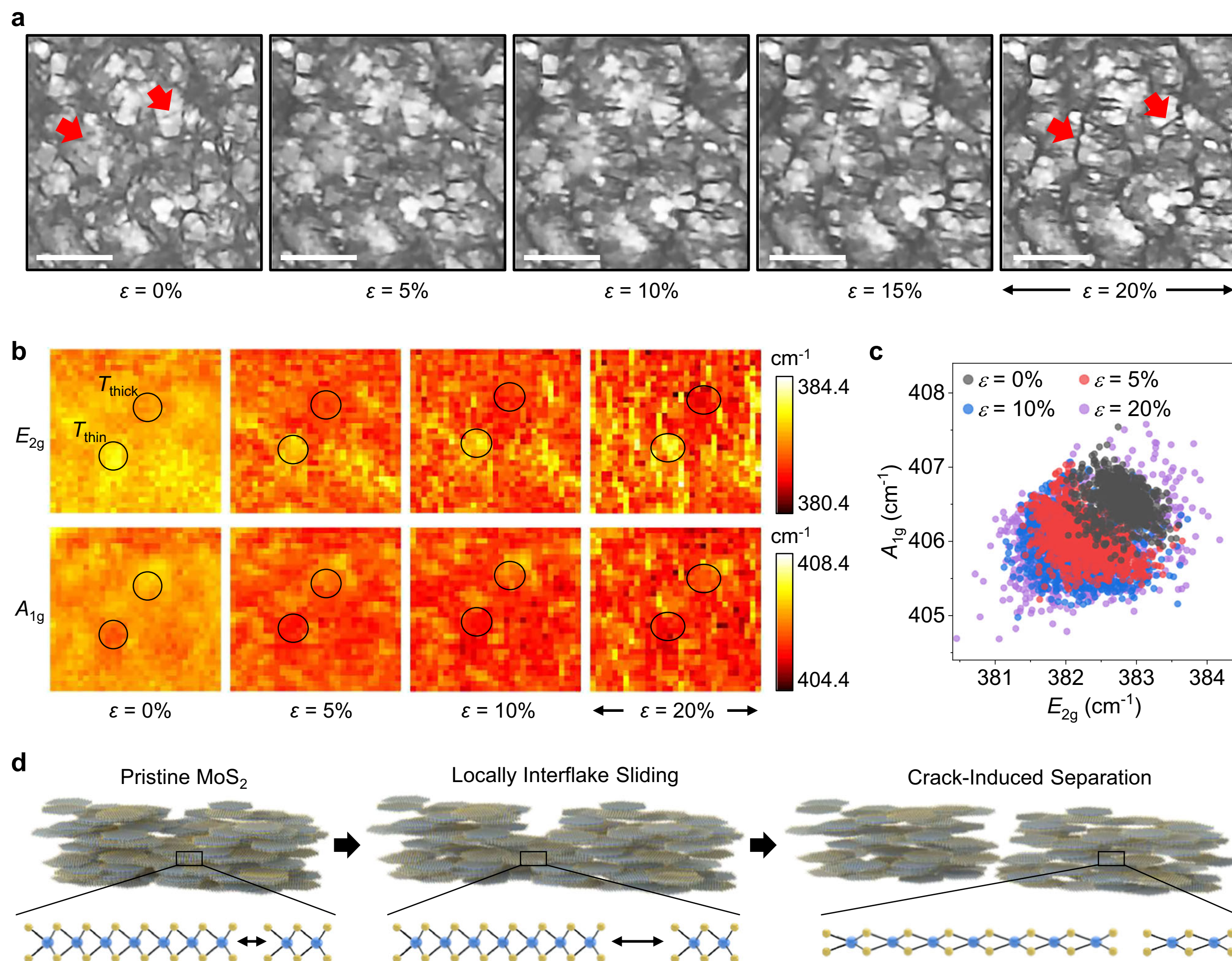

Fig. 4 | Structural characterization of MoS_2 under strain. a Optical microscopy images of MoS_2 flake-based thin films under increasing strain. Red arrows indicate the formation of strain-induced cracks. Scale bars: 10 µm. **b** Spatially resolved Raman peak positions mapped over a 30 µm × 30 µm area under different strains. The circles indicate representative regions of thicker (T_{thick}) and thinner (T_{thin}) MoS_2 layers. **c** Corresponding Raman E_{2g} versus A_{1g} plot. **d** Schematic of the proposed strain-induced structural-evolution mechanism.

stretching, it reflects changes in channel width. The strain-dependent capacitance values used to extract the μ_{FET} are presented in Supplementary Fig. 11. When the device is stretched parallel to the transport direction (Fig. 3a–c, Supplementary Fig. 12), applying 5% strain led to a 73% increase in on-current and 83% increase in μ_{FET} compared to the unstrained device. This is notable because many previously reported stretchable transistors exhibit a reduced on-current under similar strains owing to the geometric elongation of the channel[3,7,8,24]. This performance enhancement is likely due to tensile stress-induced modulation of the electronic structure of the MoS_2 channel. Previous experimental and theoretical studies reported stress-dependent electronic properties of 2D semiconductors, including MoS_2; applying tensile stress to monolayer MoS_2 reduces the effective mass of electrons in the K-valley and increases the energy difference between the K- and Q-valleys, thereby suppressing electron–phonon intervalley scattering and enhancing electron μ_{FET}[25–28]. When the strain was increased to 5%, our device showed the highest on-current and μ_{FET} values, which decreased slightly up to 20% strain due to degradation of the percolation network beyond moderate strain levels, but remained higher than the values obtained at 0%. Importantly, the on-current returned to its initial level upon release, and the transfer curve maintained an on/off ratio of approximately 10^7 without any performance degradation during stretching and release. Analysis of contact resistance using the transfer line method reveals that while contact resistance increases with strain, it remains negligible compared to the total device resistance. It means that the variation in contact resistance is not the dominant factor driving the observed changes in μ_{FET} (Supplementary Fig. 13). However, at strains of 25–30%, both the on-current and μ_{FET} declined significantly and did not recover after release. This suggests that the percolation pathways were irreversibly disrupted beyond the critical strain level (Supplementary Fig. 14). When stretched perpendicular to the transport direction (Fig. 3d–f, Supplementary Fig. 15), the device exhibits enhanced performance, although it was less pronounced. At 5% strain, the on-current increased by 29%, and μ_{FET} improved by 18% relative to the unstretched state. Under 20% strain, the on-current was slightly enhanced, while μ_{FET} remained similar to the original value. The electrical performance returned to the baseline upon release, with an on/off ratio above 10^7. No significant difference was observed in the subthreshold swing values during the 20% strain and release process, independent of the stretching direction (Supplementary Fig. 16).

To better understand the origin of these direction-dependent behaviors, we analyzed the changes in the channel dimensions under strain (Fig. 3g, Supplementary Fig. 17). Under perpendicular stretching, the channel exhibits a more pronounced transverse contraction. For example, at 5% perpendicular strain, the transverse dimension decreases by approximately 3.5%, whereas it remains similar under parallel stretching. Even at 20% strain, transverse contraction is only

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−1.2% for parallel stretching, compared to −8.2% for perpendicular stretching. This suggests that under perpendicular stretching, higher compressive stress in the transverse direction reduces the net tensile stress experienced by the MoS_2 channel, thereby diminishing the degree of on-current enhancement. These results are consistent with previous reports of compressive stress reducing electron mobility[29].

Both the parallel and perpendicular stretching modes exhibit stable performance under cyclic loading, maintaining the initial on-current and on/off ratio for over 200 cycles at 15% strain (Fig. 3h, Supplementary Fig. 18). Under parallel stretching, the on-current in the stretched state remained consistently higher than that in the released state, suggesting that the cyclic stress reversibly modulates the device characteristics. Compared to previously reported intrinsically stretchable transistors[3,5–9,24,30–47], our devices achieve high on/off ratios (Fig. 3i). Notably, these *n*-type transistor devices demonstrate significantly better performance than conjugated polymer *n*-type devices. The observed μ_{FET} values are close to those of high-performance *p*-type transistors based on SWCNTs. Therefore, flake-based 2D semiconductors could enable the development of high-performance n-type stretchable transistors, potentially accelerating the development of fully stretchable electronic systems.

Structural characterization under strain

To gain deeper insight into the strain-induced modulation of the electrical properties, we investigated the morphology and chemical structure of MoS_2 flake-based thin films using optical microscopy (OM) and spatially resolved Raman mapping, respectively. The OM images show that the number of cracks in the MoS_2 film increases with the applied strain (Fig. 4a). Up to 5% strain, the film remains intact without observable cracking. At 10% strain, cracks appear due to fracture within individual flakes or by the widening of interflake gaps, leading to the formation of a distributed microcrack network. As the strain increases further, both the number of cracks and their spacing continue to increase.

To more precisely examine stress distribution and crack formation, spatially resolved Raman mapping was performed over a 30 μm × 30 μm area with a step size of 1 μm (Fig. 4b, Supplementary Figs. 19, 20). The same region was repeatedly measured under increasing strain levels, enabling direct tracking of the shifts in the E_{2g} and A_{1g} phonon modes. At 0% strain, spatial variations in the Raman shift are observed across the spin-coated MoS_2 film owing to thickness differences. Within the mapped region, the E_{2g} peak position ranges from 381.9 to 383.6 cm^{-1}, whereas the A_{1g} peak varies from 405.7 to 407.5 cm^{-1}. Considering the OM images, the thinner regions exhibit higher E_{2g} and lower A_{1g} peak positions, consistent with previously reported thickness-dependent Raman behavior[22]. The representative thick and thin domains are defined as T_{thick} and T_{thin}, respectively, with areas of 22.49 and 18.74 μm^2, respectively. As the strain increases, the E_{2g} and A_{1g} peaks redshift, which is consistent with the buildup of tensile stress in the MoS_2 lattice[26,27]. In T_{thick}, the average E_{2g} and A_{1g} peaks shift by 1.03 and 0.73 cm^{-1}, respectively, confirming the presence of local tensile loading. In contrast, T_{thin} exhibits minimal peak shifts (0.29 cm^{-1} for E_{2g} and 0.57 cm^{-1} for A_{1g}), suggesting that interflake sliding occurs more readily, allowing strain to be released without significant stress accumulation. Above 10% strain, the Raman maps indicate crack formation. Although the peaks were mostly red-shifted with increasing strain prior to crack initiation, in the regions where cracks appeared, the Raman peaks shifted back toward higher frequencies. This implies local stress release, although contributions from defect formation or edge effects associated with the crack sites cannot be excluded[48]. A scatter plot of the E_{2g} versus A_{1g} peak positions further confirms the overall Raman redshift with increasing strain (Fig. 4c).

Correlating the Raman and morphological observations with electrical performance shows that the changes in μ_{FET} under strain are closely related to the stress state and crack evolution in the MoS_2 channel. For example, under 5% strain applied parallel to the charge-transport direction, μ_{FET} increases by 83%. This significant enhancement is attributed to the tensile stress enhancing carrier transport, while the lack of cracks preserves the percolation pathway. At 10–20% strain, although tensile stress tends to increase, crack formation begins to degrade the percolation pathway, resulting in reduced μ_{FET} compared to the 5%-strain case. Beyond 25% strain, irreversible electrical degradation occurs, likely due to extensive crack formation and the loss of conductive pathways. Taken together, the electrical, morphological, and spectroscopic analyses reveal a strain-dependent mechanical response in the MoS_2 flake-based thin films. As illustrated in Fig. 4d, the thin regions accommodate deformation through interflake sliding and remain largely unstrained. In thicker domains, tensile stress accumulates under strain and eventually exceeds a critical threshold, resulting in crack formation and local mechanical degradation. These insights provide a fundamental understanding of the strain management in 2D materials and lay the foundation for the development of next-generation stretchable electronic devices.

Discussion

We demonstrated high-performance, mechanically robust, and intrinsically stretchable transistors based on 2D vdW MoS_2 flakes, an emerging material that has yet to be fully validated for these applications. The flake-based n-type transistors exhibit high μ_{FET} and low off-current, overcoming the long-standing limitations demonstrated by stretchable n-type devices. By integrating carefully selected gate dielectrics with wafer-compatible photolithography processes, we successfully fabricated stretchable thin-film transistor arrays with stable electrical performance under high strains. This study establishes 2D flake-based n-type semiconductors as a crucial platform for developing high-performance complementary circuits, marking a significant step toward the practical application of intrinsically stretchable electronics.

Despite the initial promising results, further improvements are required to extend the mechanical resilience of the stretchable transistors beyond 20% strain. A closer examination revealed that two aspects are particularly critical: the intrinsic properties of the flake film and the semiconductor–electrode interface. Maintaining overlapping flakes is crucial for the channel performance. Raman mapping showed that stress accommodation differs markedly between thick and thin regions, with local thickness variations acting as crack initiation sites that undermine stretchability. Therefore, improving film uniformity is an easy and effective route for enhancing strain tolerance. Furthermore, using larger flakes could help sustain percolation pathways even when the strain becomes localized. We experimentally confirmed that increasing the flake size enhances the mechanical durability of the percolating network (Supplementary Fig. 21). Notably, MoS_2 flake films are capable of sustaining strains of up to ~50% without electrical disconnection[19], suggesting that the 20% strain limit observed for our devices is not governed by the film itself but by interfacial failure. Microscopic inspection revealed that cracks preferentially nucleate near the MoS_2/Au contacts, highlighting the vulnerability of the semiconductor–electrode interface to tensile stress. This interfacial weakness seems to be the dominant bottleneck preventing the devices from reaching the intrinsic strain capacity of the 2D film (Supplementary Fig. 22). Taken together, these findings emphasize that advancing 2D flake-based stretchable transistors depends on refining thin-film uniformity and increasing flake size to minimize strain localization within the channel, and engineering more resilient semiconductor–electrode interfaces to suppress crack formation at the contacts. Overcoming these limitations is essential to push the stretchability of devices closer to the inherent mechanical limits of vdW semiconductors and enable their reliable integration into deformable electronic devices.

Methods

Fabrication of MoS_2 ink

MoS_2 ink was prepared using the electrochemical exfoliation method in a two-electrode system. MoS_2 crystals (SPI Supplies) and graphite rods were used as the cathode and anode, respectively, and tetraheptylammonium bromide (99%, Aldrich) dissolved in acetonitrile (99%, Aldrich) at a concentration of 4 mg/mL was used as the electrolyte. Intercalation was performed by applying a direct current of 0.01 A for 1 h. The intercalated MoS_2 crystals were then lightly washed with ethanol (99.5%, anhydrous, Aldrich) and immersed in a solution of polyvinylpyrrolidone (PVP, average molecular weight ~40,000, Aldrich, 8 mg/mL) dissolved in N,N-dimethylformamide (DMF, anhydrous, 99.8%, Aldrich). The mixture was sonicated for 30 min to effectively disperse the MoS_2 flakes in the solution. To isolate the MoS_2 flakes, a two-step centrifugation process was performed. Initially, centrifugation at a low speed (440 x *g*, 15 min, 4 °C) was conducted to remove large particles and impurities, and the supernatant was collected. The supernatant was then subjected to high-speed centrifugation (24,000 x *g*, 15 min, 4 °C) to obtain the precipitated MoS_2 flakes. The precipitate was redispersed in IPA. The high-speed centrifugation step was repeated at least three times to effectively remove the residual PVP, resulting in purified MoS_2 flakes. To fabricate the MoS_2 FETs, the ink concentration was adjusted such that a 100-fold diluted sample showed an absorbance of 2.2 by UV-Vis spectroscopy, ensuring optimal conditions for spin coating.

Fabrication of stretchable MoS_2 transistors

An 8-inch glass substrate was first cleaned using O_2 plasma and spin-coated with a 10 wt% dextran (average molecular weight ~ 70,000, Aldrich) solution in deionized water at 1500 rpm for 20 s to serve as a sacrificial layer, followed by annealing at 180 °C for 15 min. A 4 wt% solution of SEBS (H1052, Asahi KASEI) in toluene (99.8%, anhydrous) was then prepared, with bis (6-((4-azido-2,3,5,6-tetrafluorobenzoyl) oxy)hexyl)decanedioate (C_{10}-azido) added as a crosslinking agent at 4 wt% compared to the SEBS content. The solution was spin-coated onto the prepared surface at 1000 rpm for 60 s to form the substrate of the stretchable transistor, followed by curing under 254 nm UV light at a power density of 10 mW/cm^2 for 1400 s, followed by annealing at 120 °C for 1 h. A stretchable gate electrode was fabricated by forming a cracked Au electrode using a lift-off process. Au was deposited to a thickness of 75 nm using a thermal evaporator at a very slow rate of 0.1 Å/s, enabling the Au to penetrate the substrate and achieve stretchability.

The stretchable gate dielectric is composed of two layers. The first layer was prepared using a 30 mg/mL NBR solution in cyclohexanone (99%, Aldrich), with C_{10}-azido as the crosslinking agent, added at 4 wt% relative to the NBR content. The NBR solution was spin-coated at 3000 rpm for 90 s, followed by an additional spin at 4000 rpm for 20 s. The coated film was exposed to 254 nm UV light at a power density of 10 mW/cm^2 for 370 s and annealed at 150 °C for 1 h, resulting in a thickness of approximately 200 nm. The second layer was formed by coating the NBR layer with SEBS (H1052, Asahi KASEI). A 10 mg/mL SEBS solution in toluene (99.8%, anhydrous) was prepared with C_{10}-azido added as a crosslinking agent at 4 wt% relative to the SEBS content. This solution was spin-coated at various speeds to control the thickness. The coated film was cured by exposure to 254 nm UV light at a power density of 10 mW/cm^2 for 25 s, followed by annealing at 120 °C for 1 h, yielding a thickness of approximately 60–145 nm.

To complete the bottom-gate/bottom-contact structure, stretchable source and drain electrodes were fabricated using the same process as the gate electrode by depositing a 50 nm-thick Au layer. An MoS_2 thin film, initially fabricated on a rigid substrate (e.g., SiO_2/Si), was then transferred onto a stretchable transistor. MoS_2 was patterned using a negative photoresist (PolyPR-1, U Chem) to minimize the damage to the polymer substrate, followed by etching with CF_4 plasma (20 mTorr, 100 W, 30 s). For encapsulation, two types of SEBS (H1221 and H1052, Asahi KASEI) were prepared as 40 mg/mL solutions and sequentially spin-coated at 1000 rpm for 180 and 360 s, respectively. Each layer was annealed at 80 °C for 3 or 10 min.

Fabrication and transfer of MoS_2 films

A SiO_2 (300 nm)/Si substrate was cleaned and treated with an O_2 plasma (50 sccm, 100 W, and 100 s). MoS_2 ink dispersed in IPA was spin-coated onto the substrate at 1000 rpm for 60 s, followed by annealing at 100 °C for 5 min. This process was repeated three times to ensure sufficient MoS_2 coverage, resulting in the formation of a 10–20 nm-thick MoS_2 film. To treat sulfur vacancies, the MoS_2 film was immersed in a 10 mg/mL solution of TFSI (95%, Aldrich) in 1,2-dichloroethane (99.8%, anhydrous) and treated at 80 °C for 1 h. The film was then annealed at 200 °C for 1 h in an N_2-purged glove box to remove residual solvent and improve interflake contact.

For the transfer process, a supporting layer of polymethyl methacrylate (PMMA; 950 PMMA C2, MicroChem) was spin-coated onto the MoS_2 film at 1000 rpm for 60 s and annealed at 180 °C for 1 min. To enable the natural separation of the MoS_2 film from the SiO_2 layer, the sample was immersed in deionized water. To facilitate the handling of the released MoS_2 film, polypropylene tape was applied to the edges of the film, leaving the central area untouched. The released film was then transferred onto a stretchable substrate, which was heated at 50 °C for 20 min to evaporate the residual water and improve the adhesion between the film and substrate. Finally, the PMMA support layer and the polypropylene tape were removed by rinsing the substrate with acetone and IPA, followed by drying with nitrogen gas.

Characterization

OM images were acquired using an Olympus DSX1000 microscope. The electrical properties of the FETs were evaluated using a Keithley 4200 semiconductor characterization system under vacuum conditions near 10^{-3} Torr. The μ_{FET} values were obtained from the linear region of the transfer curves: $\mu_{FET} = (L/WC_{ox}V_D)/(\partial I_D/\partial V_G)$, where I_D is the drain current, C_{ox} is the dielectric capacitance per unit area, W and L are the channel width and length, respectively, V_G is the gate voltage, and V_D is the drain voltage. C_{ox} values were determined using an Agilent 4284 A precision LCR meter. The UV-Vis absorption spectra were measured using a Shimadzu UV-3600 Plus UV-Vis-NIR spectrophotometer. The photoluminescence was measured using an F-7000 fluorescence spectrophotometer. Atomic force microscopy topographies were obtained using a Bruker Dimension XR microscope. Raman imaging was performed using an InVia Raman microscope (Renishaw, UK). An excitation source with a wavelength of 514 nm was used. All Raman images were acquired at 50 × magnification with an excitation power density of approximately 2 mW cm^{-2} and a 2400 mm^{-1} grating.

Data availability

Relevant data supporting the key findings of this study are available within the article and the Supplementary Information file. All raw data generated during the current study are available from the corresponding authors upon request.

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Author contributions

Y.-Y. N. and G.H.L. conceived the study. K.K. performed the experiments and analyzed the data. Y.K. and H. Kang assisted with array fabrication. C.J. performed Raman mapping. S.H., J.-Y.K., J.Y.J., and S.-G.K. assisted with the characterization and device measurements. T.Z., G.B., H. Kim, Y.L., J.S., S.-J.L., and B.-L.L. assisted in the synthesis and characterization

of the 2D flake solution. G.H.L. and T.-G.K. oversaw the project. K.K., Y.-Y.N., and G.H.L. wrote the manuscript, and all authors contributed to discussions.

Competing interests
The authors declare no competing interests.

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