Nature Communications

https://doi.org/10.1038/s41467-026-70108-9

Article in Press

Atomically sharp heteroepitaxial Hf_2C edge contacts enabling barrier-free carrier injection in 2D $HfSe_2$ semiconducting channels

Received: 19 November 2025

Accepted: 18 February 2026

Cite this article as: Bhin, G., Kang, T., Jin, J.W. *et al.* Atomically sharp heteroepitaxial Hf_2C edge contacts enabling barrier-free carrier injection in 2D $HfSe_2$ semiconducting channels. *Nat Commun* (2026). https://doi.org/10.1038/s41467-026-70108-9

Gihyeon Bhin, Taeho Kang, Jeong Won Jin, Sangmin Ji, Seung Yong Lee, Chang Yong Park, Ji Hwan Lee, Saeroonter Oh, Ji-Sang Park, Young Jae Song & Sungjoo Lee

Atomically sharp heteroepitaxial Hf_2C edge contacts enabling barrier-free carrier injection in 2D $HfSe_2$ semiconducting channels

Gihyeon Bhin[1,2†], Taeho Kang[1,2†], Jeong Won Jin[3], Sangmin Ji[1,2], Seung Yong Lee[1,2], Chang Yong Park[1,2], Ji Hwan Lee[4], Saeroonter Oh[5], Ji-Sang Park[1,2,6], Young Jae Song[1,2,6,7,8*], and Sungjoo Lee[1,2,6 *]*

[1]SKKU Advanced Institute of Nanotechnology (SAINT), Sungkyunkwan University, Suwon 16419, Korea

[2]Department of Nano Science and Technology, Sungkyunkwan University, Suwon 16419, Korea

[3]Department of Energy Science, Sungkyunkwan University, Suwon 16419, Korea

[4]Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, 16419, Korea

[5]Department of Semiconductor Convergence Engineering, Sungkyunkwan University, Suwon, 16419, Korea

[6]Department of Nano Engineering, Sungkyunkwan University, Suwon 16419, Korea

[7]Center for 2D Quantum Heterostructures, Institute for Basic Science (IBS), Suwon 16419, Korea

[8]Department of Physics, Sungkyunkwan University, Suwon 16419, Korea

†These authors contributed equally to this work.

*Correspondence: leesj@skku.edu

Abstract

Achieving high-quality source/drain contacts in two-dimensional (2D) semiconductors remains challenging due to Fermi-level pinning induced by metal-induced gap states (MIGS). Here, we demonstrate an atomically sharp $Hf_2C/HfSe_2$ edge contact formed via a laterally directed chemical conversion, driven by catalyst-assisted hydrodeselenization and carbonization under epitaxial alignment. Classical and *ab initio* molecular dynamics elucidate the atomistic mechanism of heteroepitaxial interface formation. Scanning tunneling microscopy and spectroscopy measurements confirm suppressed MIGS at the heteroepitaxial interface, indicating an electronically transparent junction. Electrical measurements reveal a near-zero Schottky barrier height (≈5 meV) and reduced contact resistance (≈475 Ω·μm) when compared with previously reported 2D edge-contact systems. When co-integrated with a van der Waals-integrated native high-κ HfO_2 gate dielectric within a single $HfSe_2$ channel, the devices exhibit a subthreshold swing of 62 mV/dec and on-state current density of 920 μA/μm. This integrated platform

establishes a scalable design framework that couples contact and gate-stack engineering for next-generation 2D logic technologies.

Introduction

As outlined in the International Roadmap for Devices and Systems (IRDS), two-dimensional (2D) semiconductors are considered promising channel innovations for sub-1-nm logic nodes[1], due to their intrinsic advantages, particularly in terms of strong immunity to short-channel effects and the potential for high on-off current ratios[2]. These merits originate from their atomically thin nature, low dielectric permittivity, dangling-bond-free surface, moderate density of states, favorable effective mass, and efficient in-plane thermal dissipation[3,4]. Translating these intrinsic advantages into practical device performance, however, requires the formation of high-quality junctions with atomically clean and crystallographically coherent interfaces. In particular, the source/drain contact is critical; achieving low contact resistance (R_C) approaching the quantum limit is essential for efficient carrier injection and for sustaining high drive current in aggressively scaled logic technologies[5]. However, achieving high-quality contacts in 2D semiconductors remains a long-standing and fundamental challenge, primarily due to Fermi-level pinning (FLP) at the metal–2D semiconductor interface, which originates from metal-induced gap states (MIGS). During conventional metal deposition, the metal wavefunction penetrates into the bandgap of the 2D semiconductor, generating interface states localized near the charge-neutrality level and thereby strongly pinning the metal Fermi level[6,7]. Structural and chemical perturbations introduced during deposition—such as chalcogen vacancies, interstitial incorporation, interfacial strain, and metal–chalcogen reactions—further increase the density of interfacial states[8]. As a result, the Schottky barrier height (SBH) becomes largely insensitive to the metal work function, deviating from the ideal Schottky–Mott limit and severely limiting efficient carrier injection across metal–2D semiconductor junctions[9].

To address these limitations, a variety of contact-engineering strategies have been explored, including doping, van der Waals (vdW) contacts, and semimetal contacts. Doping approaches aim to emulate the heavily doped source/drain regions in silicon technology, where high doping concentrations narrow the depletion width and enable direct carrier tunneling into the band edges, thereby facilitating near-ohmic contact formation. For example, atomic-layer yttrium doping of MoS_2 has been shown to induce a silicide-like metallic phase, yielding an R_C as low as 69 $\Omega \cdot \mu m$[10]. Despite such promising results in tailored systems, the intrinsically high dopant ionization energies and the atomically thin nature of 2D semiconductors fundamentally limit dopant solubility, generally leading to structural defects and deep-level traps that degrade contact performance[11]. Moreover, in 2D semiconductors, the depletion width at the interface

depends only weakly on carrier concentration, making it difficult to realize true ohmic behavior through tunneling alone. Alternatively, non-disruptive approaches such as charge-transfer doping and interfacial dipole engineering have also been proposed, enabling localized carrier accumulation via spontaneous Fermi-level equilibration without introducing structural disorder[12]. However, these methods are highly sensitive to ambient conditions and typically require full encapsulation, posing significant challenges for scalable integration and long-term stability[13].

vdW contacts—first demonstrated by Liu *et al*. using dry-transferred metal electrodes[14]—offer a promising pathway to mitigating FLP by physically decoupling the metal–2D semiconductor interface, thereby minimizing interface disorder and suppressing the formation of MIGS. Nevertheless, the inherent tunneling barrier imposed by the vdW gap fundamentally limits carrier injection by reducing the spatial overlap between the metal and 2D semiconductor wavefunctions, even when favorable band alignment is present[15]. More recently, semimetal contacts have emerged as a frontier strategy, leveraging their low density of states near the Fermi level to intrinsically suppress MIGS and mitigate FLP. Shen *et al*. demonstrated that bismuth (Bi) contact to monolayer MoS_2 results in a near-zero SBH and reduced R_C of ≈123 Ω·μm, maintaining linear transport behavior even at cryogenic temperatures[16]. Li *et al*. further advanced this approach by forming oriented antimony (Sb) interfaces, achieving coherent band hybridization across the interface and R_C values approaching the quantum limit (≈42 Ω·μm)[17]. However, such elemental semimetals inherently possess material constraints that hinder their practical use in advanced device integration. Specifically, Bi has a melting point below 300 °C, and Sb exhibits high atomic diffusivity[18], making both incompatible with the stringent thermal budget and reliability requirements of back-end-of-line processes[19]. Their propensity for metal diffusion further exacerbates integration challenges, particularly as diffusion control has become a critical reliability issue in modern industrial contact integration processes.

Despite remarkable progress in contact engineering for 2D semiconductors, most state-of-the-art approaches still rely on top-contact geometries. As device dimensions enter the extremely scaled regime, the contact length (L_C) proportionally shrinks, leading to insufficient transfer length (L_T) and pronounced current crowding, which exponentially increases the R_C[20]. Edge-contact architecture has therefore attracted considerable attention, as they enable in-plane carrier injection with nanometer-scale L_T. Early demonstrations formed such contacts by plasma etching to expose the 2D semiconductor edge prior to metal deposition[21], validating the conceptual advancement of edge injection but inevitably generating interfacial disorder that induces FLP and non-ideal Schottky barriers. To mitigate interfacial damage,

subsequent strategies such as epitaxial lateral junctions and thermally induced on-device phase engineering have been proposed[22,23]. However, these approaches still suffer from unacceptably high R_C and inherent limitations in achieving precise, localized stoichiometry, which remain fundamental bottlenecks to scalable integration. More fundamentally, such approaches are incompatible with the evolution toward multi-sheet systems, where the physical underlap between the contact and the gated channel becomes a non-negligible component of the total series resistance[3]. This parasitic resistance introduces an additional voltage drop between the contact and the active channel region, lowering the effective gate overdrive and partially offsetting the gains from R_C reduction and ultimately constraining overall supply voltage scaling. Hence, establishing and understanding a genuinely laterally directed, high-quality edge contact to 2D semiconductors is essential for advancing contact engineering beyond the current limits.

In this work, we present an interface-engineered strategy for integrating an atomically sharp-edge-embedded contact in a 2D semiconductor. By inducing simultaneous edge-initiated hydrodeselenization and carbonization of $HfSe_2$ under thermally and catalytically activated conditions via a controllable chemical vapor deposition (CVD) process—thereby converting $HfSe_2$ into Hf_2C—an atomically sharp heteroepitaxial interface was achieved. *Ab initio* molecular dynamics (AIMD) simulations based on density functional theory (DFT) further elucidated the atomistic mechanism of edge-initiated heteroepitaxial interface formation and the evolution of directionally oriented atomic configurations. Furthermore, we employed scanning tunneling microscopy/spectroscopy (STM/STS) and Kelvin probe force microscopy (KPFM) to investigate the local density of states (LDOS) and work function. These measurements revealed the metallic nature of Hf_2C with a work function of ≈4 eV, distinct from the semiconducting $HfSe_2$. Notably, line STS (LSTS) directly confirmed suppressed MIGS across the heteroepitaxial junction, providing critical insight for heteroepitaxial contact engineering. The high-quality $Hf_2C/HfSe_2$ interface was further demonstrated by the fabricated $Hf_2C/HfSe_2$ field-effect transistors (FETs), which exhibited a near-zero SBH (≈5 meV) and a reduced R_C (≈475 Ω·μm), outperforming previously reported 2D semiconductor-based edge-contact technologies. To further demonstrate the potential of the proposed edge-contact, FETs with a gate length (L_g = 200 nm), incorporating a vdW interface-integrated native high-κ dielectric (HfO_2) within a single $HfSe_2$ channel were fabricated, exhibiting a nearly ideal subthreshold swing (SS) of 62 mV/dec at room temperature (300 K) along with a high on/off ratio (≈10^8). The obtained on-state current density (I_{on}) reaches up to 920 μA/μm at a drain bias (V_{DS}) = 1 V, surpassing the projected IRDS targets. These results underscore the

pivotal role of atomically engineered edge-contacts in achieving low R_C, representing a major step toward scalable contact engineering and the integration of 2D semiconductor logic architectures beyond silicon.

Results

Atomically sharp heteroepitaxial edge-embedded $Hf_2C/HfSe_2$ lateral junction

Figure **1a** presents a schematic of the heteroepitaxial lateral edge-contact structure of the $Hf_2C/HfSe_2$ heterojunction studied in this work. A pristine $HfSe_2$ flake (≈ 40 nm) was prepared and selectively converted into a 2D metallic carbide (Hf_2C) via edge-initiated hydrodeselenization and carbonization under a thermally activated process with CH_4 and H_2 gas injection. The detailed experimental conditions and procedures are provided in the Methods section and Supplementary Fig. 1. This edge-initiated chemical conversion process[24] is schematically illustrated in Fig. **1b.** Under a CH_4/H_2/Ar gas atmosphere, molecular H_2 dissociates into reactive H° radical on the catalyst surface, which selectively cleave the weak Hf–Se bonds exposed at the edges of $HfSe_2$. The liberated Se atoms react with H° radicals to produce volatile H_2Se molecules that desorb from the surface. Simultaneously, CH_3° radicals generated from CH_4 decomposition occupy the Se vacancies created during this hydrodeselenization process and bond with exposed Hf atoms, leading to the formation of Hf–C bonds and subsequent Hf_2C conversion. As the reaction progresses, this lateral conversion front propagates inward from the edges, yielding a well-defined heteroepitaxial $Hf_2C/HfSe_2$ interface. The converted Hf_2C area can be controlled by adjusting the reaction time (Supplementary Fig. 2).

By employing the proposed methodology, the formation of the $Hf_2C/HfSe_2$ heterojunction was experimentally demonstrated, as evidenced by the cross-sectional scanning transmission electron microscopy (STEM) image and the corresponding energy-dispersive spectroscopy (EDS) elemental mapping (Fig. **1c**). The EDS mapping clearly reveals a distinct boundary between the C and Se elements, consistent with the STEM contrast, thereby confirming the formation of a well-defined interface between Hf_2C and $HfSe_2$ (see Supplementary Figs. 6-8 for additional material characterization details). The fast Fourier transform patterns further verify the layered-crystalline structure of $HfSe_2$ together with the crystallographically oriented Hf_2C, consistent with other layered transition-metal carbides[25] (see also Supplementary Fig. 3). Notably, the enlarged cross-sectional STEM image of the dashed-square region in Fig. **1c** clearly reveals an edge-embedded heteroepitaxial junction, demonstrating the formation of an atomically sharp interface between Hf_2C and $HfSe_2$ achieved through the edge-initiated chemical

conversion process (Fig. **1d**). The converted Hf_2C region exhibits a lattice spacing of 2.25 Å, whereas $HfSe_2$ retains its characteristic 6.1 Å spacing, accompanied by an interfacial lattice tilting of ≈150°, consistent with the mechanistic study discussed in the following section. Additional structural analysis—confirming atomically sharp interfaces on both the right and left sides and revealing the top-view morphology of the $Hf_2C/HfSe_2$ heterojunctions—further verifies the formation of an atomically sharp interface (Supplementary Figs. 4 and 5). These comprehensive structural and materials characterizations verify the formation of a high-quality, atomically sharp $Hf_2C/HfSe_2$ heteroepitaxial interface, thereby establishing a robust laterally configured heterojunction within the 2D semiconductor channel. The scalability of the proposed methodology toward uniform wafer-scale integration can be investigated by coupling it with established wafer-scale channel-formation routes, while maintaining compatibility with standard lithography and enabling a practical overlay-tolerance window through a globally controlled, self-aligned conversion step.

Atomistic mechanism of heteroepitaxial $Hf_2C/HfSe_2$ interface formation

To investigate the growth mechanism of $Hf_2C/HfSe_2$ upon the introduction of C atoms, we performed classical molecular dynamics (CMD) simulations by employing machine-learned potentials, as shown in Fig. **2a,b** (see Methods section for details). The simulation was initiated with a pristine $HfSe_2$ crystal. To simulate the edge-initiated chemical conversion process, we iteratively performed 97 cycles of modification and CMD simulation. For each cycle, one C atom was substituted for every four Se atoms removed from the left side of the $HfSe_2$ slab. Starting from the initial structure, the output structure from each step was used as the input for the next iteration. Our results reveal that, when a C atom initially replaces a Se atom, the C atom bonds with three Hf atoms, but as more Se atoms are removed, it becomes surrounded by more Hf atoms, and finally, it is surrounded by six Hf atoms, as in the bulk structure (Supplementary Fig. 11a). As the coordination number of the Hf atom changes from 6 to 3, the newly formed Hf_2C layer possesses a distinct crystal structure from the parent $HfSe_2$ with a thinner thickness (Supplementary Fig. 11b), consistent with our experimental results (Supplementary Figs. 9 and 10), and furthermore, a significant tilting of the Hf_2C layers with respect to the $HfSe_2$ is observed at the interface. To further investigate the atomic structure and identify a more precise, stable configuration of the interface, we performed AIMD simulations (see Supplementary Video). The initial configuration for the AIMD simulation was constructed by taking the $HfSe_2$ crystal structure and substituting a portion of the Hf and Se atoms with C and Hf atoms, respectively, thereby creating a Hf_2C region within the $HfSe_2$ matrix.

Following this, an AIMD simulation and subsequent structure relaxation were performed to find a plausible interface structure. The resulting atomic configuration reveals a tilting of the hafnium (Hf) layer, which is consistent with the observations from our CMD simulations. When viewed along the plane of the 2D $HfSe_2$ layer, the interfacial lattice tilting is measured to be ≈150° (Fig. **2c**), whereas an observation along the c-axis reveals a tilting of ≈165° for the Hf layer (Fig. **2d**). This structural rotation results from the formation of more Hf-Se bonds at the interface, which is associated with the increased Hf density in the Hf_2C layers.

Electronic characterization of $Hf_2C/HfSe_2$ interface

To investigate the local electronic structure and directly probe for MIGS, we performed high-resolution STM/STS measurements to map the LDOS at the $Hf_2C/HfSe_2$ lateral heterojunction. A key advantage of the lateral architecture is that it enables direct in-plane STM/STS analysis across the interface, as illustrated in Fig. **3a**. An STM tip is scanned from the Hf_2C region to the $HfSe_2$ region across the heterojunction. Figure **3b** shows a typical STM image of the junction, which exhibits the bright Hf_2C region against the relatively darker $HfSe_2$ region, with the white arrow indicating the lateral location along which line spectroscopy was performed. This topographic contrast indicates a higher LDOS near the Fermi level for Hf_2C. The point-specific differential conductance (dI/dV) spectra (Fig. **3c**) reveal the LDOS for both Hf_2C and $HfSe_2$. The $HfSe_2$ exhibits a bandgap of approximately 1.1 eV and displays typical n-type semiconducting characteristics, consistent with its known electronic behavior[26]. In contrast, Hf_2C demonstrates a metallic LDOS profile with no bandgap, evidencing its metallic nature. This spectroscopic evidence underscores the distinct electronic properties of the two materials. To investigate the lateral heterojunction in detail, spatially resolved LSTS was performed following the white arrow in Fig. **3b**. The resulting LSTS mapping (Fig. **3d**) presents the evolution of the LDOS across the $Hf_2C/HfSe_2$ interface. The LSTS result demonstrates an exceptionally sharp transition between the metallic LDOS characteristic of Hf_2C and the semiconducting LDOS of $HfSe_2$. Crucially, there are no detectable in-gap states within the $HfSe_2$ bandgap at the interface. This abrupt electronic change and clear preservation of the bandgap at the junction confirm the suppressed MIGS, indicating the formation of a well-defined and electronically clean structure. These results are further corroborated by first-principles DFT calculations of the electronic band structure (Supplementary Fig. 13). These findings provide direct experimental evidence for the realization of suppressed MIGS at the $Hf_2C/HfSe_2$ interface. On the basis of the experimentally resolved interfacial electronic structure, the electron energy barrier can be determined

from the measured work function of Hf_2C (≈4 eV) obtained by KPFM analysis (Supplementary Fig. 14) together with the known electron affinity of $HfSe_2$[27], indicating barrier-less carrier injection at the interface and the formation of an ohmic contact (Supplementary Fig. 15).

Electrical characterization of $Hf_2C/HfSe_2$ interface

To elucidate the contact properties between Hf_2C and $HfSe_2$, electrical characterization was performed, as detailed in the Methods section. Prior to evaluating the electrical contact characteristics of the $Hf_2C/HfSe_2$ heterojunction, the intrinsic electrical properties of Hf_2C were examined, confirming its purely metallic nature consistent with the LDOS results (Fig. **3c** and Supplementary Fig. 16). Figure **4a** compares the transfer characteristics of Hf_2C- and Ti/Au-contacted $HfSe_2$ FETs with a 40-nm-thick $HfSe_2$ channel (see Supplementary Fig. 17 for the Au-only-contacted device characteristics). The $Hf_2C/HfSe_2$ FET exhibits markedly enhanced conduction with an improved I_{on}, in contrast to the Ti/Au-$HfSe_2$ FET. Moreover, the $Hf_2C/HfSe_2$ interface shows linear output characteristics at both room and low temperatures (Fig. **4b** and Supplementary Fig. 18), indicative of efficient carrier injection across the interface. The linear output behavior observed under various on-state gate-bias conditions further confirms the stable ohmic contact behavior at the $Hf_2C/HfSe_2$ interface (Fig. **4c**). Similar results are also observed in devices with scaled channel lengths (Supplementary Fig. 19). In contrast, the Ti/Au-$HfSe_2$ FET exhibits nonlinear output characteristics (see Supplementary Fig. 20 for details), reflecting the presence of a potential barrier, consistent with previous reports on Schottky- or interfacial-layer-limited contacts[28]. To further validate the contact nature, temperature-dependent transfer characteristics were measured for both $Hf_2C/HfSe_2$ and Ti/Au-$HfSe_2$ FETs (Fig. **4d**). For the $Hf_2C/HfSe_2$ FET, enhanced phonon scattering at elevated temperatures reduces the I_{on}, whereas the suppression of scattering at lower temperatures enables more efficient carrier transport, resulting in a higher I_{on}— consistent with the ohmic contact behavior reported in previous studies[29]. By contrast, the Schottky-type Ti/Au-$HfSe_2$ FET exhibits thermally activated transport behavior. At low temperatures, insufficient thermal energy limits carrier injection across the barrier, leading to a reduced I_{on}, while at higher temperatures, increased thermal excitation enables carriers to surmount the SBH, thereby enhancing the conduction. To quantitatively evaluate the barrier height of $Hf_2C/HfSe_2$ interface, the SBH was extracted from temperature-dependent transfer characteristics using the Arrhenius plot (Fig. **4e**), following the thermionic emission model, $I_{DS} = A^*_{2D}T^2\exp(-\varphi_B/k_BT)$, where $A^*_{2D} = q(8\pi k_B^3 m^*)^{1/2}/h^2$, φ_B is the effective barrier height, k_B is the Boltzmann constant, q is the elementary charge, m^* is the effective carrier mass, T is the absolute temperature, and h is Planck's

constant[30]. The extracted SBH was found to be suppressed (≈5 meV), demonstrating nearly barrierless contact consistent with the electronic demonstration discussed above. Figure **4f** compares the nonlinearity factor (N) of the $HfSe_2/Hf_2C$ and Ti/Au-$HfSe_2$ FETs, obtained from their output characteristics. For quantitative assessment, N was estimated using the differential relation[31], $N = [(V/I)\,(dI/dV)] - 1$, which represents the deviation from the linear regime ($N = 0$). This formulation is closely related to a curvature-based definition, $N = (d^2I/dV^2)/[2(dI/dV)]$, but provides greater numerical stability for experimental data analysis[31]. An increase in N corresponds to enhanced nonlinearity, indicating a higher potential barrier at the interface. As shown in the inset of Fig. **4f**, $N \approx 0$ was maintained across all V_{DS} ranges and throughout the entire temperature range, confirming ohmic contact behavior originating from the atomically sharp interface-integrated edge contact. In contrast, the Ti/Au-$HfSe_2$ FET exhibited a pronounced nonlinearity factor of approximately $N \approx 3$, characteristic of Schottky-type contact behavior. Furthermore, the R_C, extracted using the transfer-length method, exhibited a reduced R_C of ≈475 Ω·μm (Fig. **4g** and Supplementary Fig. 21). Similar results were also obtained upon scaling the channel length and thickness (down to bilayer), further confirming stable ohmic contact behavior and the benefits of the proposed $Hf_2C/HfSe_2$ edge-contact geometry (Supplementary Figs. 22 and 23). This performance surpasses that of recently reported edge-contact systems based on 2D semiconductors[21-24,32-36], demonstrating the superior contact performance of the $Hf_2C/HfSe_2$ interface (Fig. **4h** and Supplementary Table 1). A current-density plot as a function of 2D-channel thickness for reported edge-contacted devices is also provided in Supplementary Fig. 24. To further demonstrate the intrinsic advantage of the proposed edge contact, we examined the transfer characteristics of devices with varying L_C (Fig. **4i**). For the $Hf_2C/HfSe_2$ edge contact, devices with different L_C exhibit nearly identical I_{on}, indicating a genuine edge profile and pure in-plane carrier injection, as the current remains invariant with changes in L_C. In contrast, for the Ti/Au-$HfSe_2$ top-contact architecture, reducing L_C results in a pronounced degradation in device performance, particularly when L_C becomes shorter than the L_T (30–40 nm for 2D semiconductors)[37], which defines the characteristic distance over which most carriers are injected (see Supplementary Fig. 25 for details).

Electrical performance of Hf_2C-HfO_2 co-integrated $HfSe_2$ FET

To demonstrate the scalability and practical integration of the proposed edge-embedded contact architecture, we further implemented a co-integrated $HfSe_2$ FET (Fig. **5a**), in which an atomically sharp Hf_2C edge contact and a vdW interface-integrated native HfO_2 gate dielectric were simultaneously incorporated within a single $HfSe_2$ channel (≈15 nm) with a gate length (L_g) of 200 nm (Fig. **5b**). The

detailed fabrication procedures are provided in the Methods section and Supplementary Fig. 1. To evaluate the device performance, transfer characteristics were measured under various V_{DS} (Fig. **5c**). The co-integrated $HfSe_2$ FET exhibited an enhanced I_{on} of up to 920 μA/μm at V_{DS} = 1 V, along with a near-ideal SS value of 62 mV/dec (over four orders of $I_{DS,}$ where I_{DS} denotes the drain-to-source current) at room temperature (300 K), a high on/off current ratio (≈10^8), and a low gate leakage current (≈10^{-6} A/cm^2). Furthermore, negligible gate hysteresis (≈2.8 mV), which is closely associated with dielectric and interfacial trap states[38], confirms the effective suppression of charge trapping at the vdW interface and within the HfO_2 dielectric layer (Supplementary Figs. 26a and 27). Comparable field-effect mobility to that reported for MoS_2 upon channel-thickness scaling[39,40] was also observed (Supplementary Figs. 35-37). Detailed electrical and interfacial characterization of the vdW interface-integrated gate stack is provided in Supplementary Figs. 28-30. In addition, highly reproducible device performance was confirmed across 20 identically processed co-integrated $HfSe_2$ FETs, all showing consistent I_{on} values (Fig. **5d**). Device statistics and a summary of key performance metrics are also provided in Supplementary Fig. 31 and Supplementary Table 2. For stability evaluation, within the repeated dual-direction transfer sweep of 200 cycles, the co-integrated $HfSe_2$ FET exhibited negligible variation in I_{on}, suggesting the robust and clean interface between Hf_2C and $HfSe_2$ (Fig. **5e**). The thermal stability and reliability of the co-integrated $HfSe_2$ FETs were further assessed through thermal cycling and bias–temperature stress test (Supplementary Figs. 32 and 33). The improved current drive primarily arises from the seamless lateral conversion of $HfSe_2$ into Hf_2C from the channel edge, producing an atomically coherent interface that effectively suppresses MIGS, unlike conventional deposited metal contacts. This advancement not only surpasses the projected IRDS targets but also achieves performance comparable to the most advanced contact technologies reported to date (Fig. **5f**)[1,16,17,20,41-48]. Co-integrated $HfSe_2$ FETs with an atomically thin bilayer channel also achieved improved electrostatic control while preserving carrier-injection efficiency, offering a scaling demonstration that is technologically relevant to the channel-thickness regime of state-of-the-art Si nanosheet nodes (Supplementary Fig. 34). To further assess the intrinsic drive capability beyond the DC limit, pulsed measurements with150-ns drain pulses were conducted (Fig. **5g**). While the device exhibited an I_{on} of 920 μA/μm under DC operation, the pulsed I_{on} increased to 1070 μA/μm at V_{DS} = 1 V, accompanied by a delayed onset of the saturation regime. This enhancement is attributed to the suppression of self-heating and hot-electron trapping[49], which delays the velocity saturation, facilitated by the atomically coherent $Hf_2C/HfSe_2$ interface, thereby more closely reflecting the intrinsic current-driving capability relevant to circuit operation. Based on the measured I_{on} values, the intrinsic gate delay was estimated to be 35 ps at 920 μA/μm and 18.8 ps at 1070 μA/μm (Supplementary

Fig. 26b), which is comparable to advanced Si FETs and industrial roadmap targets. Further optimization toward ultimate scaling while maintaining functional device operation will be pursued in future work, guided by sub-50-nm device simulations (Supplementary Fig. 38) and gate-stack engineering (e.g., EOT scaling via thinner dielectrics and/or higher-κ materials). Collectively, these results underscore that the Hf_2C/$HfSe_2$ edge-contact, when co-integrated with a high-κ HfO_2 gate stack, offers a scalable and high-performance contact architecture capable of delivering high drive current, low power consumption, and the possibility of circuit-level applicability—establishing a promising platform for next-generation 2D semiconductor logic technologies.

Discussion

In conclusion, we have demonstrated a heteroepitaxial edge-embedded contact strategy that enables the formation of an atomically sharp interface between Hf_2C and $HfSe_2$. Through laterally directed chemical conversion via hydrodeselenization and carbonization, $HfSe_2$ was seamlessly transformed into Hf_2C, yielding a structurally coherent interface. Both classical and *ab initio* MD simulations clarified an edge-initiated propagation pathway and lattice tilting at the Hf_2C/$HfSe_2$ interface, elucidating the atomistic origin of the heteroepitaxial alignment. Electronic characterization using STM/STS directly revealed a suppressed MIGS within the $HfSe_2$ bandgap after the conversion process, as evidenced by the LDOS, validating the realization of an electronically transparent interface. Corresponding electrical measurements further established a nearly barrier-free contact with a SBH of ≈5 meV and the reduced R_C of ≈475 Ω·μm—outperforming recently reported edge-contact systems based on 2D semiconductors. When co-integrated with a vdW interface-integrated high-κ native HfO_2 gate dielectric within a single $HfSe_2$ channel, the resulting co-integrated $HfSe_2$ FETs exhibited an enhanced I_{on} (≈920 μA/μm), and near-ideal SS (62 mV/dec) at room temperature. These results collectively demonstrate that the atomically engineered Hf_2C/$HfSe_2$ edge contact not only mitigates fundamental FLP but also enables scalable integration with high-κ dielectrics for low-power and high-drive 2D logic architectures. This work provides a framework for interface-engineered contact technologies, paving the way for efficient carrier injection and scalable device architectures beyond conventional silicon technology.

Methods

Fabrication of the fully converted Hf_2C

Initial $HfSe_2$ flakes (≈40 nm) were mechanically exfoliated using Scotch tape and dry-transferred onto the cleaned SiO_2/p^+-Si substrates. All exfoliation and transfer processes were carried out in an Ar-filled glove box, where the O_2 and H_2O concentrations were maintained below 0.1 ppm to prevent oxidation and contamination. Prior to the conversion process, the $HfSe_2$ flakes were patterned into elongated square regions (5 μm × 3 μm) using inductively coupled plasma etching to define the conversion area. Edge-initiated conversion of $HfSe_2$ into Hf_2C was performed in a low-pressure chemical vapor deposition (CVD) system operating at 2.0×10^{-4} Torr. The samples were placed beneath folded Cu foil (99.9%, Alfa Aesar) and positioned at the center of a 4-inch quartz tube furnace. The quartz tube was first purified at 800 °C under a 100 sccm Ar flow for 1 h to remove residual contaminants. After cooling, the chamber atmosphere was stabilized under a CH_4 (100 sccm), H_2 (5 sccm) and Ar (100 sccm) gas mixture. The temperature was then raised to 800 °C and maintained for 2 h to initiate the chemical conversion process and achieve the full conversion into Hf_2C. Following the reaction, the system was cooled to room temperature at a rate of 4.75 °C/min under continuous gas flow. The conversion rate of the Hf_2C was estimated to be ≈41.5 nm/min (2.5 μm/h) toward the flake center (Supplementary Figs. 9 and 10).

Fabrication of the $Hf_2C/HfSe_2$ edge-contact

Prior to the conversion process, the ≈40 nm $HfSe_2$ flakes were patterned into elongated square regions (5 μm × 3 μm) using inductively coupled plasma etching to define the conversion area. Selective conversion to realize the $Hf_2C/HfSe_2$ heteroepitaxial interface was achieved using a lithographically defined SiO_2 mask layer. Electron-beam lithography (EBL) was used to pattern the regions to be protected, followed by deposition of a 180 nm-thick SiO_2 layer using electron-beam deposition (EBD). The conversion process was then repeated under identical CVD conditions, with the temperature held at 800 °C for 1 h under a $CH_4/H_2/Ar$ gas flow (100/5/100 sccm). The masked regions remained as pristine $HfSe_2$, whereas the exposed areas were converted into Hf_2C, resulting in the formation of a lateral $Hf_2C/HfSe_2/Hf_2C$ heterostructure. All structural and compositional characterizations were performed on samples fabricated using this procedure.

Fabrication of the $Hf_2C/HfSe_2$ FET

Following the same fabrication procedure used for the $Hf_2C/HfSe_2$ edge-contact structures, Ti (10 nm)/Au (40 nm) source and drain electrodes were deposited by EBD under a high vacuum of 4×10^{-7} Torr. All electrical measurements of the $Hf_2C/HfSe_2$ devices were performed on samples fabricated using this

process.

Fabrication of the $HfO_2/HfSe_2$ gate-stack

$HfSe_2$ flakes were mechanically exfoliated using Scotch tape and dry-transferred onto the cleaned substrates. All exfoliation and transfer processes were conducted inside a glove box under controlled conditions to prevent ambient contamination, where both O_2 and H_2O concentrations were maintained below 0.1 ppm. To form HfO_2 as a high-κ gate dielectric with a vdW interface on $HfSe_2$, O_2 plasma oxidation was carried out at a power of 10 W with an O_2 flow rate of 5 sccm and a chamber pressure of 470 mTorr under fixed process conditions[50,51]. The thickness of the converted HfO_2 layer was controlled by adjusting the plasma exposure time and the initial thickness of pristine $HfSe_2$, based on an oxidation rate of ≈2.1 nm/min (see Supplementary Fig. 20 for details).

Fabrication of the Hf_2C-HfO_2 co-integrated $HfSe_2$ FET

All process parameters for carbonization and plasma oxidation were identical to those described above. ≈40 nm-thick $HfSe_2$ flakes were transferred onto the SiO_2/p^+-Si substrate. Prior to the device fabrication process, the $HfSe_2$ flakes were patterned into elongated square regions using inductively coupled plasma etching to define the conversion area. Subsequently, polymethyl methacrylate (PMMA) 495 and 950 layers were spin-coated at 2000 rpm for 5 s and 4000 rpm for 35 s, respectively, followed by baking at 180 °C for 2 min on a hot plate. A SiO_2 masking layer was then partially deposited on the $HfSe_2$ surface by the EBL and EBD process. During the subsequent CVD process, the exposed regions of $HfSe_2$ were laterally converted into Hf_2C, whereas the areas covered by SiO_2 remained unreacted. After carbonization, the SiO_2 masking layer was removed by a peel-off process, yielding a lateral $Hf_2C/HfSe_2/Hf_2C$ heteroepitaxial structure. A PMMA layer was then once again applied, and EBL was employed to expose the unconverted channel region previously protected by the SiO_2 mask. Partial vertical oxidation of the exposed region was performed by O_2 plasma, yielding ≈10 nm of HfO_2. Through this process, a FET was realized in which the atomically sharp interface-integrated $Hf_2C/HfSe_2$ edge-contact and the vdW interface-integrated $HfO_2/HfSe_2$ gate-stack were co-integrated within a single $HfSe_2$ channel. Finalelectrodes0 nm)/Au (40 nm) source and drain electrodes and a 20 nm-thick Au top-gate electrode were deposited by EBD under high-vacuum conditions (4×10^{-7} Torr). The overall fabrication process flow and corresponding OM images are shown in Supplementary Fig. 1.

Sample characterization

OM (Olympus, BX51M) and FE-SEM (JEOL, JSM7500F) were used to observe the sizes and colors of

the prepared samples and fabricated devices. Raman spectroscopy at an excitation wavelength of 523 nm was used to characterize $HfSe_2$, Hf_2C and HfO_2. The thickness of the flakes was determined using an atomic force microscope (AFM, Park Systems Corp., NX-10) in the non-contact mode with PPP-NCHR probe tips (nanosensors). The work function of Hf_2C was also measured using the same AFM equipment. A scanning rate of 0.2 Hz with 256 scanning lines was used. The measurements utilized an Au-coated tip (HQ:NSC36/Cr-Au, Cantilever type B, MikroMasch). The tip had a nominal radius below 35 nm and a height of 15 μm. Three cantilevers were present per chip, with typical properties: force constant 2 N/m, resonance frequency 130 kHz, and cantilever length 90 μm. The 30 nm Au coating with a 20 nm Cr sublayer ensures both electrical conductivity and laser reflectivity. The cross-sections were observed using transmission electron microscopy (TEM, JEOL, TEM2100F) at an accelerating voltage of 200 kV. X-ray photoelectron spectroscopy (XPS, MultiLab 2000, Thermo VG, Mg Kα source) was employed to analyze the chemical states and composition, with the binding energy calibrated to the C 1s peak at 284.8 eV.

Electrical characterization

All the electrical measurements were performed in a probe station (MSTECH) with a vacuum pressure of 10^{-6} torr using a semiconductor analyzer (Keithley 4200). A Keithley 4200 instrument was used to provide the supply voltage to all the devices in this study. Pulsed I–V measurements were carried out using the 4225-PMU and 4225-RPM modules with Keithley 4200.

Electronic characterization

STM/STS experiments were carried out in a commercial LT-STM (Omicron, Germany) with a base pressure of approximately 10^{-10} Torr. All the STM/STS measurements were performed at room temperature. Electrochemically etched tungsten tips were used after the removal of surface oxide by electron bombardment in the ultrahigh vacuum chamber. STM images were acquired in the constant-current mode, and the bias voltages were applied to the sample with respect to the STM tip. The dI/dV spectra were collected by using the standard lock-in technique with a voltage modulation of 50 mV and frequency of 817 Hz. For STM measurements, a 50 nm-thick Au electrode was deposited on the substrate using EBD to provide electrical contact to the sample.

Computational details

Classical molecular dynamics simulations were performed using the Atomic Simulation Environment (ASE)[52]. The interatomic interactions were described using a pre-trained machine learning interatomic potential, specifically the Machine Learning Atomic Cluster Expansion (MACE) model (mace-mp-0b3-

medium)[53]. Molecular dynamics simulations were performed using the NVT (canonical) ensemble. The system temperature was maintained at around 1000 K using a Langevin thermostat (Supplementary Fig. 12). Each molecular dynamics simulation was run for 500 steps with a time step of 1 fs, corresponding to a total simulation time of 0.5 ps. $HfSe_2$ on the right side (c.a. 10 Å) were kept fixed to maintain the bulk structure. Following the CMD simulation, the final atomic structure was fully optimized using the Broyden–Fletcher–Goldfarb–Shanno algorithm until the residual forces on all atoms were converged to below 0.01 eV/Å. To predict the interface structure between $HfSe_2$ and Hf_2C, we performed spin-polarized DFT calculations using the Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional[54]. The interactions between ions and electrons were described by the Projector Augmented-Wave (PAW) method[55], as implemented in Vienna *Ab initio* Simulation Package (VASP)[56]. For a better description of dispersion interactions, DFT-D3 method with Becke-Johnson damping function was used[57]. The initial interface structure was prepared by building a supercell of $HfSe_2$ and substituting Hf and Se atoms in the middle for C and Hf atoms, respectively. We performed *ab initio* molecular dynamics simulations using an NVT ensemble with a Nosé–Hoover thermostat to maintain a constant temperature of 500 K[58]. The simulations were run for a total of 1500 fs, with a time step of 1 fs. The energy cutoff for the plane waves was set to 400 eV. After the AIMD simulation, we further optimized the cell parameters using a higher energy cutoff of 500 eV until the residual forces become less than 0.03 eV/Å.

Data availability

Data supporting the findings of this work are provided in the paper and/or the Supplementary Information. Other relevant data can be obtained from the corresponding authors upon request.

References

1. International Roadmap for Devices and Systems (IRDS). *More Moore* (IEEE, 2024).

2. Kim, K. S. *et al.* The future of two-dimensional semiconductors beyond Moore's law. *Nat. Nanotechnol.* **19**, 895–906 (2024).

3. Pal, A. *et al.* Three-dimensional transistors with two-dimensional semiconductors for future CMOS scaling. *Nat. Electron.* **7**, 1147–1157 (2024).

4. Cao, W. *et al.* The future transistors. *Nature* **620**, 501–515 (2023).

5. Wang, Y. *et al.* Critical challenges in the development of electronics based on two-dimensional transition metal dichalcogenides. *Nat. Electron.* **7**, 638–645 (2024).

6. Wang, Y. *et al.* Making clean electrical contacts on 2D transition metal dichalcogenides. *Nat. Rev. Phys.* **4**, 101–112 (2022).

7. Liu, X. *et al.* Fermi level pinning dependent 2D semiconductor devices: Challenges and prospects. *Adv. Mater.* **34**, 2108425 (2022).

8. Noori, K. *et al.* Origin of contact polarity at metal–2D transition metal dichalcogenide interfaces. *npj 2D Mater. Appl.* **6**, 73 (2022).

9. Park, S. *et al.* The Schottky–Mott rule expanded for two-dimensional semiconductors: influence of substrate dielectric screening. *ACS Nano* **15**, 14794–14803 (2021).

10. Jiang, J. *et al.* Yttrium-doping-induced phase-transition technology for forming perfect ohmic contact in two-dimensional MoS_2 transistors. *Nat. Electron.* **7**, 545–556 (2024).

11. Cui, X. *et al.* Multi-terminal transport measurements of MoS_2 using a van der Waals heterostructure device platform. *Nat. Nanotechnol.* **10**, 534–540 (2015).

12. Pack, J. *et al.* Charge-transfer contacts for the measurement of correlated states in high-mobility WSe_2. *Nat. Nanotechnol.* **19**, 948–954 (2024).

13. Wang, Y. *et al.* Surface charge transfer doping for two-dimensional semiconductor-based electronic and optoelectronic devices. *Nano Res.* **14**, 1682–1697 (2021).

14. Liu, Y. *et al.* Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions. *Nature* **557**, 696–700 (2018).

15. Duflou, J. R. *et al.* Fundamentals of low-resistive 2D-semiconductor metal contacts. *npj 2D Mater. Appl.* **7**, 42 (2023).

16. Shen, P.-C. *et al.* Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **593**, 211–217 (2021).

17. Li, W. *et al.* Approaching the quantum limit in two-dimensional semiconductor contacts. *Nature* **613**, 274–279 (2023).

18. Bruggeman, G. A. & Roberts, J. A. The diffusion of antimony in α-iron. *Metall. Trans. A* **6**, 755–760 (1975).

19. Kim, J.-S. *et al.* Addressing interconnect challenges for enhanced computing performance. *Science* **386**, eadk6189 (2024).

20. Cheng, Z. *et al.* Distinct contact scaling effects in MoS_2 transistors revealed with asymmetrical contact measurements. *Adv. Mater.* **35**, e2210916 (2023).

21. Cheng, Z. *et al.* Immunity to contact scaling in MoS_2 transistors using in situ edge contacts. *Nano Lett.* **19**, 5077–5085 (2019).

22. Song, S. *et al.* Atomic transistors based on seamless lateral metal–semiconductor junctions with a sub-1-nm transfer length. *Nat. Commun.* **13**, 4916 (2022).

23. Liu, X. *et al.* On-device phase engineering. *Nat. Mater.* **23**, 1363–1369 (2024).

24. Jeon, J. *et al.* Epitaxial synthesis of molybdenum carbide and formation of a Mo_2C/MoS_2 hybrid structure via chemical conversion of molybdenum disulfide. *ACS Nano* **12**, 338–346 (2018).

25. Qin, T. *et al.* Recent progress in emerging two-dimensional transition metal carbides. *Nano-Micro Lett.* **13**, 183 (2021).

26. Mleczko, M. J. *et al.* $HfSe_2$ and $ZrSe_2$: Two-dimensional semiconductors with native high-κ oxides. *Sci. Adv.* **3**, e1700481 (2017).

27. Yao, Q. *et al.* Nanoscale investigation of defects and oxidation of $HfSe_2$. *J. Phys. Chem. C* **122**, 25498–25505 (2018).

28. Wang, J. *et al.* High mobility MoS_2 transistor with low Schottky barrier contact by using atomic thick h-BN as a tunneling layer. *Adv. Mater.* **28**, 8302–8308 (2016).

29. Li, X. *et al.* One-dimensional semimetal contacts to two-dimensional semiconductors. *Nat. Commun.* **14**, 111 (2023).

30. Trushin, M. *et al.* Theory of thermionic emission from a two-dimensional conductor and its application to a graphene–semiconductor Schottky junction. *Appl. Phys. Lett.* **112**, 171109 (2018).

31. Mondal, A. *et al.* Low ohmic contact resistance and high on/off ratio in transition metal dichalcogenides field-effect transistors via residue-free transfer. *Nat. Nanotechnol.* **19**, 34–43 (2024).

32. Han, S. S. *et al.* Reversible transition of semiconducting $PtSe_2$ and metallic $PtTe_2$ for scalable all-2D edge-contacted FETs. *Nano Lett.* **24**, 1891–1900 (2024).

33. Schneider, D. S. *et al.* CVD graphene contacts for lateral heterostructure MoS_2 field-effect transistors. *npj 2D Mater. Appl.* **8**, 35 (2024).

34. Xu, X. *et al.* Seeded 2D epitaxy of large-area single-crystal films of the van der Waals semiconductor 2H $MoTe_2$. *Science* **372**, 195–200 (2021).

35. Luo, L. *et al.* Ultra-low power consumption flexible sensing electronics by dendritic bilayer MoS_2. *InfoMat* **6**, e12605 (2024).

36. Choi, H. *et al.* Edge contact for carrier injection and transport in MoS_2 field-effect transistors. *ACS Nano* **13**, 13169–13175 (2019).

37. Liu, Y. *et al.* Low-resistance metal contacts to encapsulated semiconductor monolayers with long transfer length. *Nat. Electron.* **5**, 579–585 (2022).

38. Illarionov, Y. Y. *et al.* Energetic mapping of oxide traps in MoS_2 field-effect transistors. *2D Mater.* **4**, 025108 (2017).

39. Ha, V.-A. & Giustino, F. High-throughput screening of 2D materials identifies p-type monolayer WS_2 as potential ultra-high mobility semiconductor. *npj Comput. Mater.* **10**, 229 (2024).

40. Sebastian, A. *et al.* Benchmarking monolayer MoS_2 and WS_2 field-effect transistors. *Nat. Commun.* **12**, 693 (2021).

41. Ghani, T. *et al.* A 90-nm high volume manufacturing logic technology featuring novel 45-nm gate length strained silicon CMOS transistors. In *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, 11.16.1–11.16.3 (IEEE, 2003).

42. Thompson, S. *et al.* A 90-nm logic technology featuring 50-nm strained silicon channel transistors, 7 layers of Cu interconnects, low-κ ILD, and 1 μm^2 SRAM cell. In *2002 IEEE International Electron Devices Meeting*, 61–64 (2002).

43. Tang, J. *et al.* Low-power 2D gate-all-around logics via epitaxial monolithic 3D integration. *Nat. Mater.* **24**, 519–526 (2025).

44. Tan, C. *et al.* 2D fin field-effect transistors integrated with epitaxial high-κ gate oxide. *Nature* **616**, 66–72 (2023).

45. English, C. D. *et al.* Improved contacts to MoS_2 transistors by ultra-high vacuum metal deposition. *Nano Lett.* **16**, 3824–3830 (2016).

46. Schranghamer, T. F. *et al.* Ultrascaled contacts to monolayer MoS_2 field-effect transistors. *Nano Lett.* **23**, 3426–3434 (2023).

47. Wu, W. C. *et al.* Scaled contact length with low contact resistance in monolayer 2D channel transistors. In *2023 IEEE Symposium on VLSI Technology and Circuits*, 1–2 (IEEE, 2023).

48. Smets, Q. *et al.* Ultra-scaled MOCVD MoS_2 MOSFETs with 42 nm contact pitch and 250 μA/μm drain current. In *2019 IEEE International Electron Devices Meeting (IEDM)*, 23.22.1–23.22.4 (IEEE, 2019).

49. Nathawat, J. *et al.* Transient hot-carrier dynamics and intrinsic velocity saturation in monolayer MoS_2. *Phys. Rev. Mater.* **4**, 014002 (2020).

50. Kang, T. *et al.* High-κ dielectric (HfO_2)/2D semiconductor ($HfSe_2$) gate stack for low-power steep-switching computing devices. *Adv. Mater.* **36**, 2312747 (2024).

51. Kang, T. *et al.* High-κ dielectric van der Waals integration on 2D semiconductors for three-dimensional complementary logic systems. *Nat. Commun.* **16**, 11648 (2025).

52. Larsen, A. H. *et al.* The atomic simulation environment—a Python library for working with atoms. *J. Phys.: Condens. Matter* **29**, 273002 (2017).

53. Batatia, I. *et al.* MACE: Higher Order Equivariant Message Passing Neural Networks for Fast and Accurate Force Fields. *Adv. Neural Inf. Process. Syst.* **35**, 11423–11436 (2022).

54. Perdew, J. P. *et al.* Generalized Gradient Approximation Made Simple. *Phys. Rev. Lett.* **77**, 3865 (1996).

55. Blöchl, P. E. *et al.* Projector augmented-wave method. *Phys. Rev. B* **50**, 17953 (1994).

56. Kresse, G. *et al.* From ultrasoft pseudopotentials to the projector augmented-wave method. *Phys. Rev. B* **59**, 1758 (1999).

57. Grimme, S. *et al.* A consistent and accurate *ab initio* parametrization of density functional dispersion correction (DFT-D) for the 94 elements H–Pu. *J. Comput. Chem.* **32**, 1456 (2011).

58. Nosé, S. *et al.* A unified formulation of the constant temperature molecular dynamics methods. *J. Chem. Phys.* **81**, 511–519 (1984).

Acknowledgement

This research was supported by the Basic Science Research Program through the National Research Foundation of Korea and was funded by the Korean Government (MSIP) (Grant No. RS-2023-00281048, RS-2025-00512822). This work was supported by Samsung Research Funding & Incubation Center of Samsung Electronics under Project Number SRFC-MA2501-01. This study was supported by Samsung Electronics Co. Ltd. (IO251217-14774-01).

Author contributions

G.B. and T.K. conceived and designed the experiments. G.B. and T.K. prepared the materials, characterized the samples, fabricated the devices, and performed the electrical characterization with assistance from S.Y.L. and C.Y.P.. J.-S.P. performed the first principles and *ab initio* molecular dynamics simulations and contributed to the mechanistic interpretation of the interface reactions. J.W.J. conducted the STM/STS analysis, and S.J. carried out the KPFM measurements. Y.J.S. supervised the STM/STS and KPFM analyses. S.O. and J.H.L. performed the device simulations and assisted in analyzing the electrical characteristics. S.L., G.B. and T.K. analyzed the data and co-wrote the manuscript with input from all authors. S.L. supervised the overall project.

Competing interests

The authors declare no competing interests.

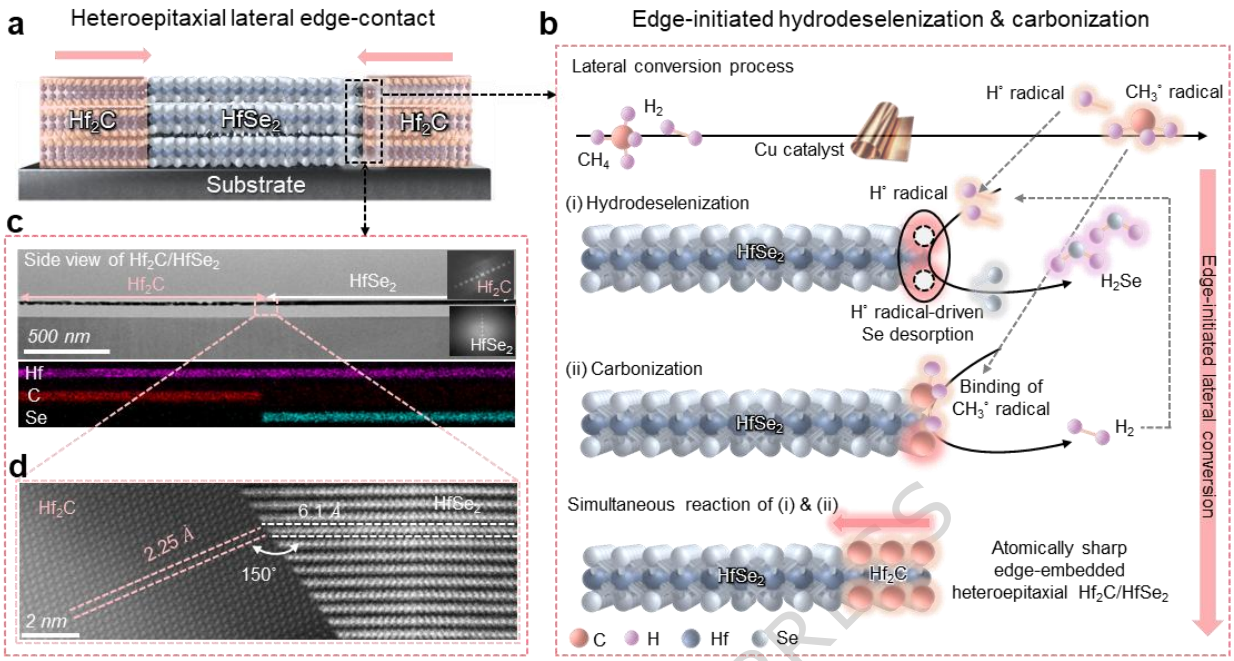

Figure 1. Structural demonstration of the atomically sharp lateral edge-embedded Hf_2C within $HfSe_2$. a, Schematic illustration of the $Hf_2C/HfSe_2$ lateral edge-contact studied in this work. The pale pink dashed box indicates an enlarged view of the black dashed box (the $Hf_2C/HfSe_2$ junction) and the formation process illustration. **b,** Process schematic of the heteroepitaxial edge-contact formation of $Hf_2C/HfSe_2$ via simultaneous edge-initiated hydrodeselenization and carbonization. **c,** Cross-sectional scanning transmission electron microscopy (STEM) image and the corresponding energy-dispersive X-ray spectroscopy (EDS) mapping of the $Hf_2C/HfSe_2$ heteroepitaxial structure. Inset: fast Fourier transform (FFT) pattern of each domain. **d,** High-resolution STEM image from the pink dashed-square region, showing an atomically sharp heteroepitaxial interface between Hf_2C and $HfSe_2$ with a lattice tilting of ≈150˚.

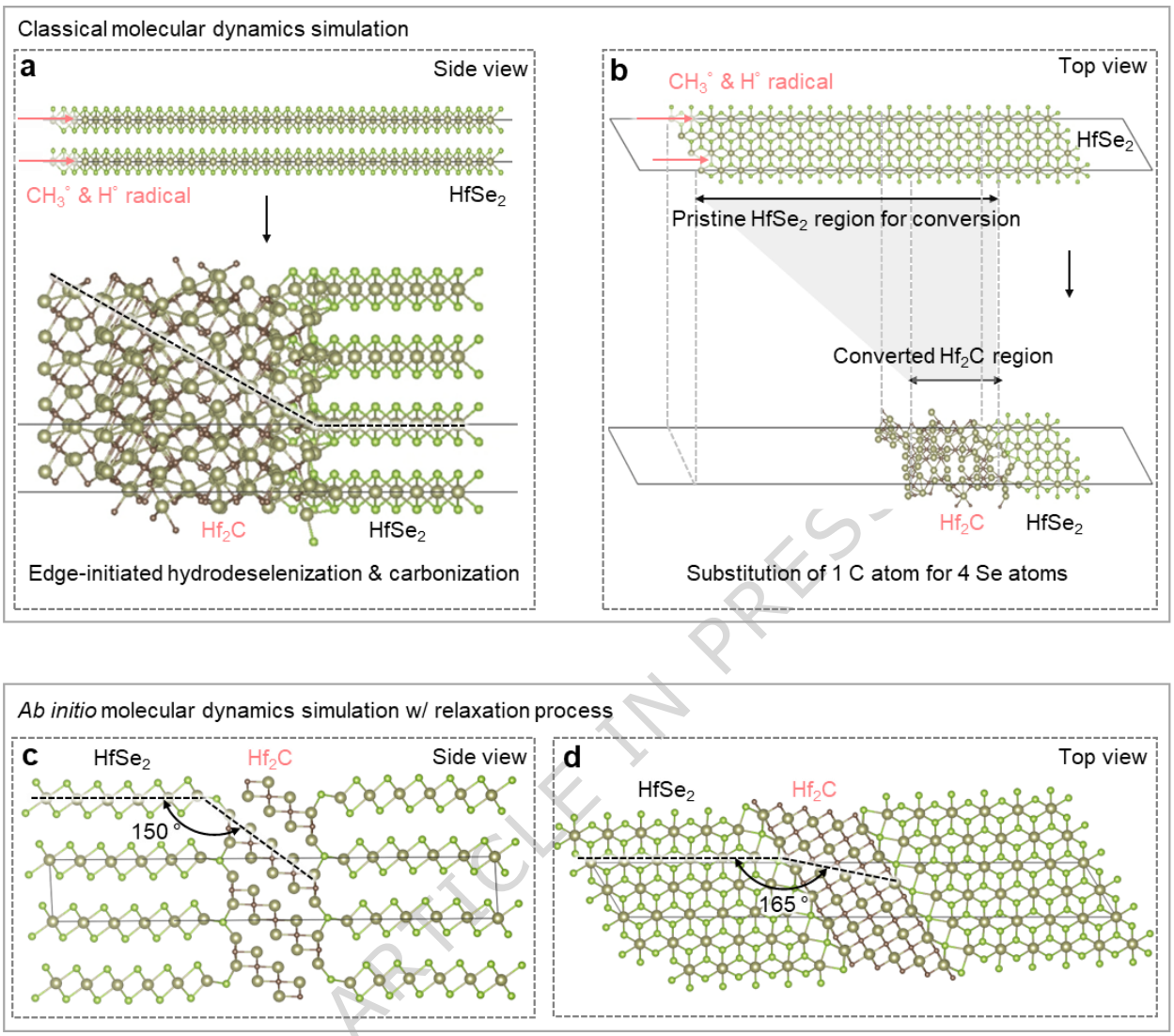

Figure 2. Molecular dynamics (MD) simulation of the heteroepitaxial $HfSe_2/Hf_2C$ interface formation flow and the interfacial angle difference formed via chemical lateral conversion. a,b, $Hf_2C/HfSe_2$ interface formation mechanism simulated by classical MD simulations. **c,d,** *Ab initio* MD simulations for predicting the stable $Hf_2C/HfSe_2$ interface structure.

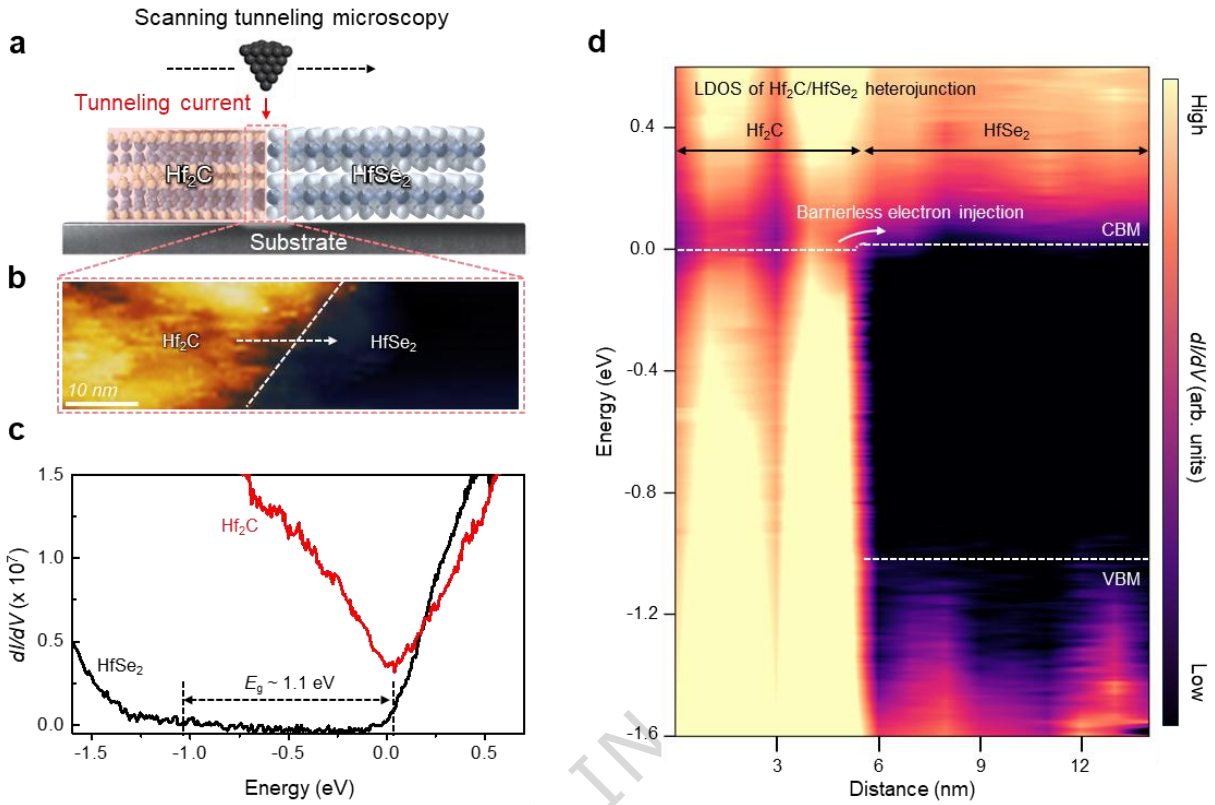

Figure 3. Electronic structure of the $Hf_2C/HfSe_2$ heterojunction. a, Schematic illustration of the lateral heterojunction composed of metallic Hf_2C and semiconducting $HfSe_2$, with a scanning tunneling microscopy (STM) tip scanning laterally across the interface for STM/scanning tunneling spectroscopy (STS) measurements. **b,** STM image distinguishing the brighter Hf_2C region from the relatively darker $HfSe_2$ domains (measured along a line across the pale pink dashed box). The white arrow indicates the direction of the line-scan STS acquisition across the $Hf_2C/HfSe_2$ heterojunction. Measurement condition: V_{bias} = 1.5 V and I = 300 pA, where V_{bias} denotes the applied bias voltage during scanning and I represent the tunneling current. **c,** Differential conductance (dI/dV) spectra, corresponding to the local density of states (LDOS), obtained from each domain. $HfSe_2$ (black) exhibits typical n-type semiconducting behavior with a clear bandgap, whereas Hf_2C (red) shows metallic LDOS without a gap. **d,** The measured line-scan STS map across the $Hf_2C/HfSe_2$ heterojunction, revealing an abrupt transition from metallic to semiconducting LDOS without detectable in-gap states. This distinct transition evidences a suppressed metal-induced gap states (MIGS) formation and a negligible barrier for electron injection at the atomically coherent interface. The color scale in the plot is logarithmic to improve dynamic range without affecting the qualitative features of the spectra.

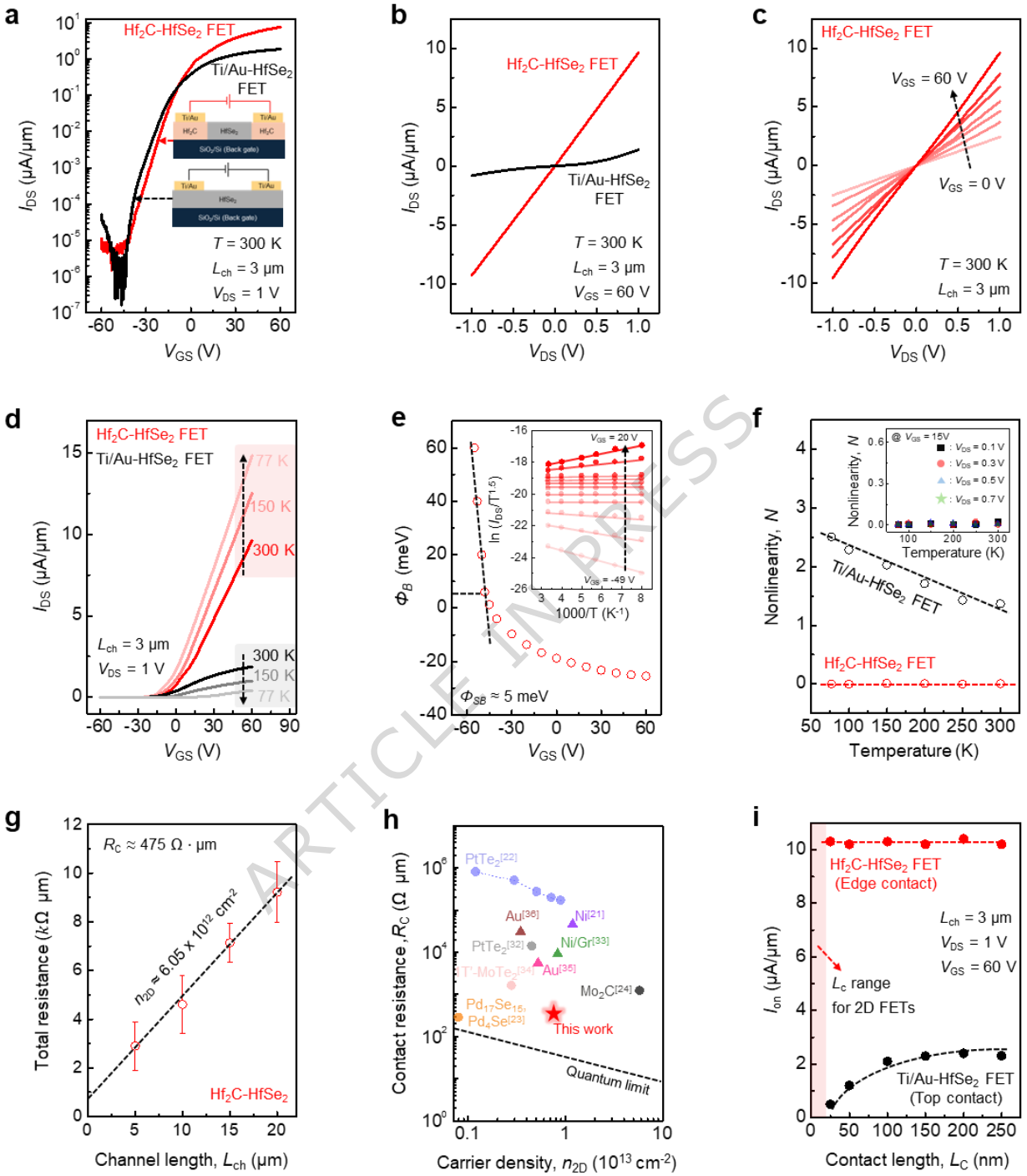

Figure 4. Electrical characterization of $Hf_2C/HfSe_2$ edge contact. a, Comparison of transfer characteristics between Hf_2C (red)- and Ti/Au (black)-contacted $HfSe_2$ field-effect transistors (FETs). The current was normalized by a channel width of 2.5 μm. T: temperature; L_{ch}: channel length; V_{DS}: drain-source voltage; V_{GS}: gate-source voltage; I_{DS}: drain-source current. Inset: schematic of the measured device with a SiO_2 (285 nm) back gate used for analysis ($HfSe_2$ = 40 nm). **b,** Comparison of output

characteristic linearity between the $Hf_2C/HfSe_2$ structure (ohmic) and the Ti/Au-$HfSe_2$ structure (Schottky). **c,** Linear output characteristics of the $Hf_2C/HfSe_2$ FET measured at 300 K, showing ohmic behavior across back-gate voltages from 0 V to 60 V. **d,** Comparison of temperature-dependent (77–300 K) transfer characteristics between $Hf_2C/HfSe_2$ FET and Ti/Au-$HfSe_2$ FET, exhibiting typical ohmic and Schottky behavior, respectively. **e,** Electron barrier height (Φ_B) of the $Hf_2C/HfSe_2$ edge contact. Inset: Arrhenius plot obtained from temperature-dependent transfer curves at various gate voltages. **f,** Nonlinearity factor (N) extracted from the output characteristics of the $Hf_2C/HfSe_2$ FET, compared with that of the Schottky-type Ti/Au-$HfSe_2$ FET, measured at V_{DS} = 0.5 V and $V_{GS} - V_{th}$ = 15 V. Here, V_{th} represents the threshold voltage. Inset: extracted N values at various V_{DS}, showing $N \approx 0$ for the $Hf_2C/HfSe_2$ FET. **g,** Contact resistance (R_C) of $HfSe_2$ FET with Hf_2C edge contact under various L_{ch}. The R_C values were extracted ($2R_C$ = y-intercepts of R_T, R_T = total resistance) from $Hf_2C/HfSe_2$ devices using the transfer-length method (TLM). Error bars represent the standard deviation of measurements from 10 TLM samples. **h,** Benchmark of R_C versus carrier density (n_{2D}) for various edge-contact technologies with 2D semiconductors (Circles denote chemically converted embedded edge contacts, whereas triangles denote deposited edge contacts)[21-24,32-36]. **i,** Comparison of on-state current density (I_{on}) behavior for different contact length (L_C) between the edge-contact and top-contact architectures (L_C = 30, 50, 100, 150, 200, and 250 nm).

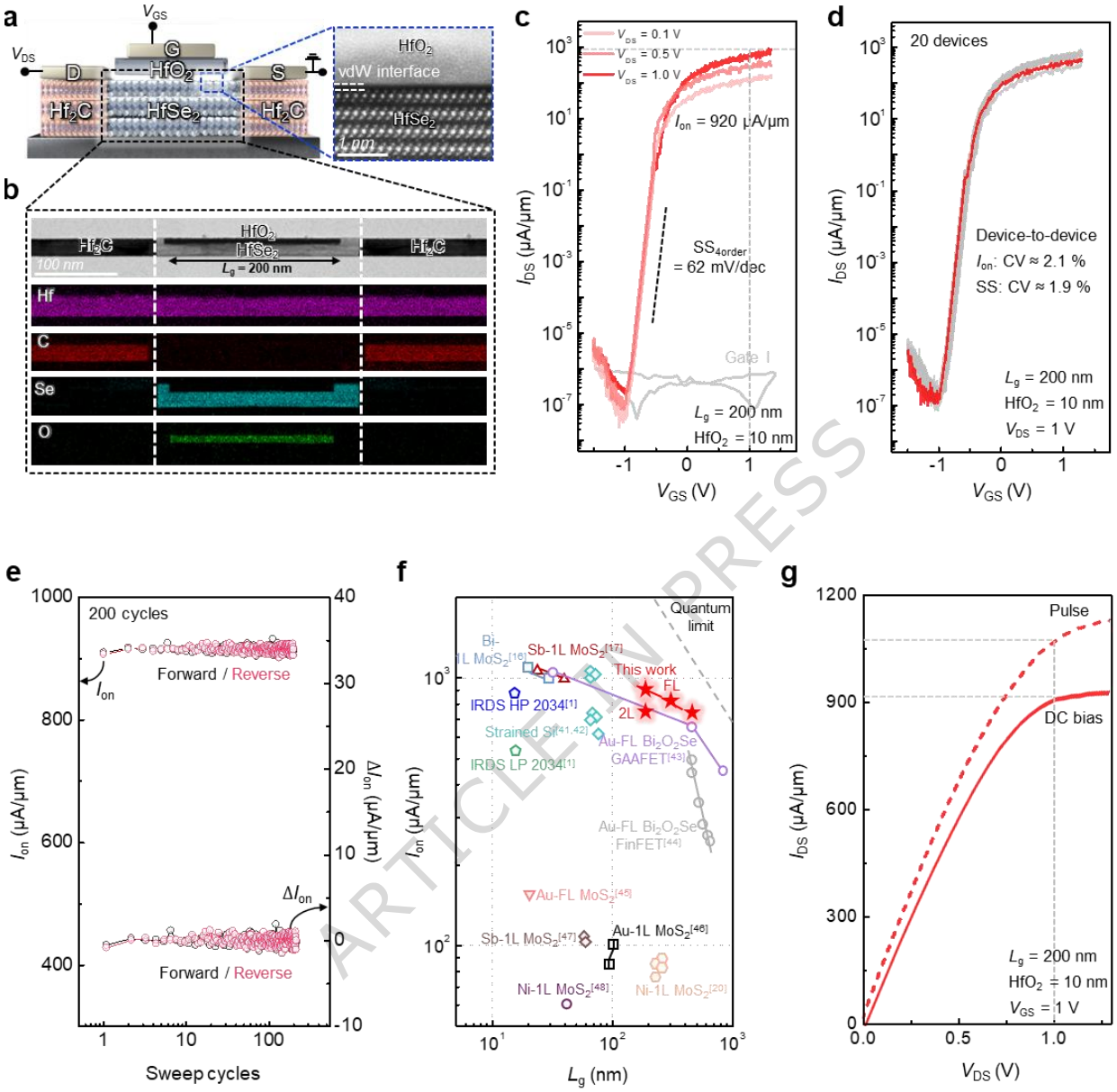

Figure 5. Electrical characteristics of Hf_2C edge-contact and van der Waals (vdW) interface HfO_2 co-integrated $HfSe_2$ FET. a, Schematic illustration of the co-integrated $HfSe_2$ FET. Right: high-resolution cross-sectional STEM image showing the atomically flat vdW interface between the native high-κ HfO_2 gate dielectric and $HfSe_2$ channel. **b,** Cross-sectional image of a co-integrated $HfSe_2$ FET with a gate length (L_g) of 200 nm and the corresponding elemental mapping obtained from EDS analysis ($HfSe_2$ = 15 nm, HfO_2 = 10 nm, and Hf_2C = 25 nm). **c,** Transfer characteristics of the co-integrated $HfSe_2$ FET measured at various V_{DS} values, exhibiting an I_{on} of 920 μA/μm, a subthreshold swing (SS) of 62 mV/dec at room temperature (300 K), and an on-off ratio of 10^8. The current was normalized by a channel width of 2.5 μm. Gate sweep rate = 0.01 V/s. **d,** Cumulative transfer characteristics of 20 co-integrated

$HfSe_2$ FETs, with the median curve highlighted in red. CV denotes the coefficient of variation (σ/μ), where σ is the standard deviation and μ is the mean of the extracted device parameter, representing the device-to-device variability. **e,** Absolute values (left axis) and the relative fluctuation (right axis) of I_{on} in 200 dual-direction gate-sweep cycles. Purple and black dots denote reverse and forward sweeps, respectively. **f,** Benchmark of I_{on} versus L_g for co-integrated $HfSe_2$ FETs, compared with recently reported planar FET with advanced contact technologies, FinFET, and GAAFET based on 2D semiconductors (1L: monolayer channel, 2L: bilayer channel, FL: few-layer channel)[16,17,20,41-48]. High-performance (HP) and low-power (LP) targets projected by IRDS are also included[1]. **g,** Output characteristics of the co-integrated $HfSe_2$ FET. Solid and dotted curves correspond to the DC and pulsed current-voltage measurements, respectively.

Editorial Summary

The fabrication of Ohmic contacts for 2D transistors remains challenging. Here, the authors report the synthesis of atomically sharp $Hf_2C/HfSe_2$ edge contacts for the realization of high-performance short-channel 2D $HfSe_2$ transistors with contact resistance down to 475 Ω·μm.

Peer review information: *Nature Communications* thanks Lingan Kong, Tara Peña, and Chenguang Qiu for their contribution to the peer review of this work. A peer review file is available.