Nature Communications

https://doi.org/10.1038/s41467-026-71446-4

Article in Press

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Received: 22 October 2025

Accepted: 23 March 2026

Cite this article as: Sestoft, J.E., Jensen, T.K., Flodgren, V. *et al.* Nanoscale photonic artificial neuron with biological signal processing. *Nat Commun* (2026). https://doi.org/10.1038/s41467-026-71446-4

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Nanoscale photonic artificial neuron with biological signal processing

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Abstract

Neuromorphic hardware can mitigate the unsustainable energy demand of artificial intelligence infrastructure. Photonic approaches provide high speed, low energy, and high connectivity but existing solutions have large circuit footprints which limits scaling potential and they miss key biological functions, like inhibition. We report a nano-optoelectronic artificial neuron with at least 100-fold reduced circuit footprints compared to existing approaches and picowatt-level operating power. The device deterministically integrates excitatory and inhibitory inputs, performs a nonlinear transfer operation, and exhibits biologically relevant temporal dynamics. Neural weighting is implemented via tunable input gains, enabling controlled summation and thresholding. The architecture is compatible with commercial silicon technology, supports multi-wavelength operation, and can be used for both computing and optical sensing. This work paves the way for two important research paths: photonic neuromorphic computing with

nanosized footprints and low power consumption, and adaptive optical sensing, using the same architecture as a compact, modular front end.

Introduction

The rising energy demand of artificial intelligence infrastructure is not sustainable.[1] Neuromorphic hardware offers encouraging solutions to this problem by mimicking the energy-efficient biological brain.[2, 3] Many different hardware solutions have been suggested, but photonic components are especially promising in terms of speed and power-efficiency[4, 5] and similar computing hardware can also serve as optical signaling/sensory systems. However, many still lack one or more essentials,[4–7] like: (i) miniaturized building blocks for high density integration; (ii) excitation and inhibition in the same device; (iii) linear fan-in (summation) and tunable nonlinear activation; (iv) low optical energy per operation; (v) controlled device-to-device variation and simple tunable weighting; (vi) wavelength selectivity for routing; and (vii) CMOS-compatible materials and processing, with a clear path to all-optical and on-chip links. For optical sensory systems many of the same demands are highly relevant in order to mimic the exceptional analytical power of the biological retina. This includes contrast resolution over many orders of magnitude of background light, excellent dynamic range and edge resolution. For intensity adaptation and edge sharpening inhibition plays an important role.[8–10]

Here we combine three semiconductor nanowires to construct an artificial optical/electronic (O/E) neuron, that fulfills these requirements. The active area is 30-90 μm^2 (at least 100 times smaller than prior on-chip photonic activators)[7, 11, 12] it provides both excitation and inhibition, sums concurrent optical inputs, and provides sigmoid activation functionality. It operates at pico-watt optical powers, shows millisecond-scale responses with 0.1-1 s recovery, is responsive across multiple wavelengths, offers voltage–tunable sensitivity/weighting and modelling projects that it can support $\sim$ 1 GHz operation speeds.[12] Compared with planar photonic platforms, our nanowire node provides an exceptionally high absorption cross-section per footprint together with bandgap-, geometry- and orientation-controlled wavelength and polarization selectivity. Nanowire technologies are highly refined and employed in many different technology areas (e.g. quantum computing[13] and solar cells[14]) and the nodal architecture allows for combinations of diverse functionalities in a modular fashion, while being CMOS-compatible.[15–17]

Results

Architecture, spatial mapping and nonlinear activation

The functionality and circuit diagram of the neuron are illustrated in Fig. 1 **a**. In line with previous work in neuromorphic photonics,[18–20] we use the term neuron below to denote an artificial neuron-like node that sums optical inputs and evaluate them

via a nonlinear, sigmoidal function to define an output. This includes excitatory/inhibitory signal inputs and a leaky internal memory state in the summations stage. As excitatory and inhibitory optical receivers, we use two nanowire photodiodes and short their anode and cathode together by a metallic lead. The electron-hole pairs generated by the photodiodes are summed on this lead and provide charge to a gate affecting the electronic conductance of a nanowire field effect transistor (FET). In Fig. 1 **b** we show an electron micrograph of a measured neuron device. We use InP nanowires with highly doped p-i-n junctions as photodiodes and connect the p-doped and n-doped regions of the two nanowires by Ti/Au leads. The lead is extended to a predefined Ti/Au lead partially covered by HfO_2 serving as a high-κ dielectric insulator. It is electrically isolated from an intrinsic InAs nanowire contacted in the same processing step as the InP nanowires. We denote the two InP nanowires 'p-gate' and 'n-gate' depending on which doping polarity is connected to the gate. All nanowires are positioned deterministically using a micromanipulator needle to predefined sites, with a placement precision on the order of hundreds of nanometres.[21] To probe the nanowire-based neuron devices, we use (1) optical-beam-induced current (OBIC) on the photodiodes and (2) ac lock-in conductance measurements on the FET. The OBIC setup comprises a piezo stage and an optical microscope receiving a single mode laser fiber (663 nm) and uses a 100x objective lens to achieve a beam spot size of approximately 0.8 µm. This setup allows us to record time-resolved conductance modulations across the transistor nanowires as a function of optical beam position and illumination power. See Methods and Supplementary Note 1, for details on device operation and measurement setup.

To demonstrate neural excitation and inhibition of the nanowire neuron, we first probe the device in terms of space- and optical power-resolved measurements using a single light source. In Fig. 1 **c**, we plot the conductance change (ΔG) across the nanowire FET as a function of beam spot position, as indicated by the dashed line in **b**. The laser diode is kept at a constant illumination power of 43 pW, placing the device in the saturated regime (see Fig. 1**d**). A voltage (V_G = -3 V) is applied to the n-gate InP nanowire bringing both InP diodes into reverse bias, improving photosensitivity. The beam spot is moved back and forth between the two pin-doped nanowires in oscillatory motion. Here we observe an increase in conductance (excitation) when the laser spot approaches the p-gate and a decrease (inhibition) when approaching the n-gate. The horizontal dashed line corresponds to the background conductance measured in dark conditions. Inhibition and excitation arises when one the two photodiodes receives incident photons generating electron-hole pairs. Depending on which end of the InP nanowire, and hence which doping polarity, is connected to the metal gate, illumination leads to an accumulation of either positive or negative charge on the gate. This photogenerated charge induces an effective gate voltage that electrostatically modulates the carrier concentration in the InAs nanowire. Here increase in positive charge increases carrier density (excitation), while an increase in negative charge lowers carrier density (inhibition). We control for reproducibility by performing these measurements for two distinct piezo-stage-stepping speeds. The traces overlap, however, faster operation may introduce hysteresis. These measurements demonstrate optically-controlled conductance modulations akin to biological neural excitation and

inhibition, and mimics light signal based synaptic communication originating from multiple on-chip or off-chip sources.

Next, we fix the beam spot position on the excitatory p-gate nanowire and record the change in conductance versus optical power (Fig. 1 **d**). For lower ranges of input power (∼6-12 pW) the device exhibits a significant quasi-linear conductance increase that saturates for lasing powers above ∼60 pW. The sigmoid-like dependence of the device conductance versus optical power is highly suitable for neural thresholding and activation functionality, providing the crucial nonlinear part in neural networks.[22] Assuming continuous illumination we find the lower bound of operation powers to be on the order of picowatts (Supplementary Note 2). Activation functions from additional devices are shown in Supplementary Note 3. As discussed later, weighting of individual optoelectronic nanowire neurons can be achieved by tuning their optical sensitivity using specific V_G values modulating their activation curves.

Summing multiple optical inputs

To investigate optical input summation, we perform measurements on both the n- and p-gates simultaneously. First, the neuron device is transitioned to an excited/inhibited state by selectively illuminating either the p- or n-gate. These states are arbitrarily defined as neuron conductance ∼10 µS above/below its conductance in dark conditions (idle). Next, we increase the optical power incrementally on the other, so-far unilluminated gate, using another light source. Figure 2**a** and **c** show the measurement configurations and applied powers, respectively. In Fig. 2**b** we show the simultaneously recorded conductance. Here we observe two traces with distinct step-like conductance modulations as the optical power is incrementally increased on either the n-gate (**i**) or the p-gate (**ii**). As either gate receives increasing optical power, the rate of charge carriers produced by the photodiode nanowire increases. These carriers recombine across the metal gate with the charge carriers (of opposite sign) being generated by the light incident on the other photodiode. Hence balancing the rates of the different carriers being generated, brings the device from its excited/inhibited state back to its idle state in a step-like manner. This result demonstrates the ability of the neuron device to sum two or more independent optical signals, a critical component enabling fanning in signals from other nodes.

Temporal dynamics and memory

Following, we explore the temporally-resolved dynamics of the nanowire neuron. In Fig. 3**a-c** we show conductance change recorded as a function of time and laser power. During these measurements light pulses of varying duration (1, 5 and 12 ms) and intensities are directed onto the n-gate resulting in inhibitory pulsing behavior. Similar measurements on the p-gate showing excitatory behavior are presented in Supplementary Note 4. In these traces we observe two different time dependent behaviors. For all pulse durations and intensities a fast decrease in conductance is observed within ~ 1 ms with a $\Delta G \sim -1$ µS. During pulses longer than 1 ms the conductance continues to decrease albeit at a slower rate before it saturates. This behavior is highlighted by the dashed lines in Fig. 3**b-c**. Comparing the slopes of the slower timescales (τ_2), we find

that as intensity increases the negative slope of τ_2 increases too. The performance and response of the device is not measurably affected by continuous and repeated pulsing (see Supplementary Note 5-6).

Next, we explore the timescales required for the neuron device to reset to its idle state (memory properties). In Fig. 3**d** we show a recording of the time extending after the 1 ms pulsing measurement from Fig. 3**a**. Here we observe a sharp decrease in conductance before conductance returns to baseline after about 0.8 s. In other measurements we find the reset time to be approximately 100 ms. This memory effect remains stable during continuous optical pulsing measurements performed over several days. In current device geometries the operation speeds of the neuron devices are biologically relevant with millisecond reaction speeds and memory timescales on the order of 100 milliseconds to several seconds.[23] We attribute the memory time of the neuron primarily to charge trapping at the HfO_2/InAs interface. Additional contributions, such as parasitic capacitance, surface states, and long channel lengths, are also known to govern the response/recovery dynamics of III–V transistors and can be engineered to realize targeted time constants and functionalities.[24] The seemingly intensity-independent initial conductance drop (τ_1) arises due to bandwidth limitations in the measurement readout. When operating the neuron at 20 pW (for a $\sim$ 1 µS conductance change) we estimate the energy use to approximately 200 fJ per operation (see Supplementary Note 2, for further details).

Tuning the activation function of nodes in a neural network is a crucial task. In Fig. 3**e** we show three different activation functions measured under different V_G applied across the two nanowire photodiodes. As V_G is tuned to larger negative values the magnitude of the non-linear response of the device becomes more pronounced. This is consistent with bringing the two InP-photodiodes deeper into reverse bias and increasing sensitivity due to widening of the intrinsic channel enhancing light absorption and limiting intrinsic carrier recombination. Focusing on the initial sigmoidal rise of the curves, we find that the slope increases by a factor of $\sim$2 when V_G is increased from 0 V to -1 V, and the same is true for the dynamic range. Additional information is presented in the Supplementary Note 7. Relying on this approach individual nodes can be switched ON and OFF while also tuning their activation functions dynamically. Lastly, we demonstrate how the neuron can receive optical input of different wavelengths and generate activation functions as long as the energy of the incident light is larger than the bandgap of the nanowire photodiode material. Here we observe similar non-linear activation functionality, all with sigmoidal-shapes, as shown in Fig. 1**d**. We show three examples using wavelengths of λ = 515 nm, 785 nm and 915 nm. In the Supplementary Note 8 we show how below-band gap optical pulses leave the neuron device unaffected. Hence selecting material compositions with desired energy bandgaps provides the neurons with tunable wavelength sensitivity enabling optical communication between only select nodes, or designing distinct excitatory/inhibitory neural pathways in the same nodes. In Supplementary Note 9, we provide an extended discussion on how to scale the nanowire neurons into networks, and realize wavelength and polarization-sensitivity.

Discussion

Substituting typical optical components such as waveguides, ring modulators and photodetectors (∼100 µm to 1 mm scale) with nanoscaled optoelectronic crystals is a promising route to significantly reducing circuit footprints for optical information processing. The active on-chip area of the nanowire-based neuron device ranges from 30-90 μm^2. Comparing to state-of-the-art optical activation function demonstrations[7] this provides a footprint reduction between two to eight orders of magnitude depending on the compared platform. See details on circuit footprints and comparisons to state-of-the-art in the Supplementary Note 10. In addition, our neuron can host more synaptic connections by integrating additional inhibiting/exciting wires of different material or polarization sensitivity, and can also naturally receive multiple signals from surrounding wires in a broadcasting scheme, even in 3D.[25]

Further footprint reduction and scalable production can be achieved by advanced nanowire placement techniques.[16] For large ensembles of in-plane neural nodes, the fibre-like morphology of nanowires, resembling biological axons, could emulate high-density connectivity, providing further miniaturization and recent work has shown direct on-chip optical communication between single nanowires providing synaptic capabilities.[26] Moving towards 3-dimensional interconnects between nanowire neurons relying on vertical nanowire arrays pioneered in the high-speed nanowire-based FET community[27] would enable further miniaturization. In neuromorphic systems, analog-to-digital conversion blocks put high demands on both power and area consumption. In this context, the modular nature of our nanowire neuron holds promise as the interface of analog-to-digital converters to other optical neural networks for read-out and digitization.

Most existing nanowire-based neural network approaches rely on randomly dispersed nanowires mostly using memristive dynamics.[28] Hence, in contrast this work provides a significantly different approach to nanowire-based neural networks, yielding a generalizable nodal architecture with highly optimized area efficiency while providing advantages of optical neural networks like speed and power consumption. Critically, the field of nanowire technology is highly mature and diverse, offering many routes for integration of desired functionality into novel nanowire-based neuromorphics while being compatible with CMOS technologies.[15–17]

Several future studies related to this work are important. (1) Using GaInP for the inhibitory photodiode could create a built-in spectral window: photons just above the InP band edge would activate the excitatory channel, whereas higher-energy photons above the larger GaInP edge would also engage inhibition and may be suppressed. Tuning the Ga fraction could set the upper cutoff, while the excitatory material fixes the lower. (2) Supplying controlled background illumination to the inhibitory input might let each pixel report local contrast rather than absolute intensity, enabling retina-like adaptation over a wide dynamic range without extra circuitry. (3) If each inhibitory input receives a weighted sum from neighboring pixels, via shared optics or simple interconnects, the array could implement center–surround filtering that enhances centers, suppresses backgrounds, and potentially sharpens edges and reduces noise before downstream processing. (4) Relying on a leaky, charge-based memory, the nanowire neuron is also suited for temporal coding. The floating metal gate stores a weighted

trace of recent excitatory and inhibitory spikes, so the output depends on their precise order and timing. When embedded in a larger network, assigning different effective weights and memory constants across neurons can support high-dimensional processing. (5) Integrating an optical-output[26] to the nanowire neuron establishes an O/E/O building block that, when integrated into interconnected arrays, supports all-optical neural computations.[11, 12] To achieve this, engineering tasks such as optimization of the FET geometry, threshold voltages and ON/OFF ratios, will be critical for the neuron device to control and power a nanowire-based LED optical output, as the neuron device in its current state provides a modulation of conductance of 5-12%. Based on modelling benchmarked via experiments, we note that an optimized O/E/O building block is projected to run at operation speeds in the 1 GHz regime, and use an estimated power consumption of 10 nW per node.[11] In the Supplementary Note 2 and 11, we provide details on the full energy budget of the nanowire neuron, device optimization and engineering strategies for GHz operation speeds.

We suggest several promising routes to engineer plasticity in the nanowire neurons. First, in-neuron memory can be realized by integrating floating-gate structures[29] into the InAs FET gate stack. Using a continuous floating metal or nano-floating gate layer embedded in a thin tunnel oxide allows charge programming by brief gate voltage pulses, with the tunnel oxide thickness setting the retention from non-volatile to leaky memory.[30–34] Related charge trapping at the InAs native oxide/gate dielectric interface can also be exploited for optical programming.[35–37, 37] Second, as we have previously demonstrated, synapse-to-synapse memory can be implemented by inserting light-sensitive molecular dyes in the optical path between neurons, where bleaching by repeated optical spikes and subsequent recovery define a volatile, intensity-dependent synaptic weight.[38]

In conclusion, we provide a nanowire-based and deterministic platform capable of drastically reducing the circuit footprint of all-optical neural networks and next-generation adaptive optical sensors. These are expected to be especially relevant for lightweight edge neural networks where direct coupling to optical inputs allow for on-device, AI-enhanced sensing.

Methods

InP nanowire growth. The InP nanowires were synthesized via metalorganic vapor phase epitaxy (MOVPE) on patterned substrates. Gold seed particles, defined by nanoimprint lithography into hexagonal arrays with a pitch of 0.50 µm, served as catalytic growth sites. Growth proceeded in a laminar flow MOVPE reactor (Aixtron 200/4), operating at 100 mbar total pressure using hydrogen (H_2) as carrier gas at a flow rate of 13 L/min. Prior to growth, substrates underwent a preanneal nucleation step at 280 °C, including TMIn precursors and PH3. This was followed by an annealing step at 550 °C under a phosphine (PH_3)/H_2 ambient to ensure pattern integrity.[39] Subsequently, the reactor temperature was lowered to the growth temperature of 440 °C. Growth was initiated by introducing trimethylindium (TMIn) and hydrogen chloride (HCl) into the gas stream. The doping profile consisted of a heavily controlled gradient: the bottom segment was uniformly n-doped using tetraethyltin (TESn) at

$_{\chi}$TESn = 4.3×10^{-5}. The middle segment was either nominally intrinsic or lightly p-doped, with DEZn concentrations ranging between $_{\chi}$DEZn = 0 and 2.1×10^{-7}. Finally, the top segment was p-doped, with molar fraction varied from $_{\chi}$DEZn = 0.09×10^{-5} to 8.24×10^{-5}. This recipe yields InP nanowires with a length of ∼ 2.6 µm, diameters from 230 to 260 nm and p-, i- and n-segments of 800, 1000 and 800 nm, respectively.

InAs nanowire growth. A molecular beam epitaxy (MBE) system is used to grow Au-seeded wurtzite InAs nanowires, along the [0001]B direction on InAs (111)B substrates using the vapour-liquid-solid mechanism. Arrays of Au catalyst particles are placed via standard EBL with particle radius r_{Au} = 20-120 nm and height h_{Au} = 10-50 nm. After substrate annealing at As overpressure at T = 500 °C for 5 min, predominantly vertical nanowire growth is initiated at growth temperatures ranging from T_{growth} = 445-450 °C. Axial nanowire growth is carried out for a duration of 10-120 min before a short break (5 min) is introduced and the As_4/As_2 ratio is increased. This recipe yields InAs nanowires with lengths ranging from 3 to 12 µm and diameters from 80 to 120 nm.

Device fabrication. All devices are fabricated on highly doped Si^{++} substrates covered by 200 nm of thermal oxide. Nanowires were picked up and placed semi-automatically using a tungsten-based micromanipulator needle under a 100x objective lens. Metallic leads were patterned using electron beam lithography, after which RF ion (Ar+) milling was performed in a metal deposition chamber, immediately followed by the e-beam deposition of Ti and Au (5 nm/300 nm) to create ohmic contacts to the nanowires. The bottom gates (5/30 nm) were defined similarly and covered by 20 nm of HfO_2 grown by atomic layer deposition at a growth temperature of 150°C using tetrakis(dimethylamino)-hafnium (TDMAH) as the precursor. The oxide thickness of 20 nm HfO_2 gate dielectric was based on a compromise between electrostatic control and process robustness.

Measurements. Optical-beam-induced current measurements were performed to spatially characterize the nanowire neuron devices. A continuous-wave laser diode emitting at 663 nm was focused near its diffraction limit (about 800 nm full width at half-maximum) onto the sample using a 100x objective lens. Precise spatial positioning of the spot relative to the nanowire device was achieved using a piezoelectric motor stage. As the laser beam was raster-scanned across the device, the generated photovoltage affecting the conductance of the InAs nanowire via the electrostatic gates was mapped (see details in Supplementary Note 1). Conductance $g{=}d\mathrm{I}/d\mathrm{V_{SD}}$ was measured across the InAs nanowire component using a.c.-lock-in techniques with an excitation voltage in the range 20 µV–5 mV and integration times of 10 µs. An iris-delimited LED was used in the signal summing measurement (Fig. 2) to provide a secondary optical probe. The laser intensity was measured with a photodiode *via* a fiber optic coupler. The LED intensity was determined from the applied driving voltage. The experimental setup is described in more detail in Supplementary Note 1.

Data availability

The raw measurement data presented in this study have been deposited in the ERDA database under accession code https://www.erda.dk/archives/d7f2686342816d7b228483ab4e4a6e04/published-archive.html.

Supplementary Information is available for this paper.

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Acknowledgements

This work was supported by the Swedish Research Council (A.M.), NanoLund, supported by Myfab (A.M.), Wallenberg Initiative Materials Science for Sustainability (WISE) and the Knut and Alice Wallenberg Foundation (M.T.B., A.M.), Danish National Research Foundation (DNRF101) (J.N.), the Olle Engkvist Foundation (M.T.B.), the Novo Nordisk Foundation project SolidQ and EPICAL (J.N.), and the European Union Horizon Europe project InsectNeuroNano (Grant 101046790) (M.T.B., J.N., A.M.).

Author contributions

Conceptualization, J.E.S., J.N. and A.M.; Device fabrication and recipe development, J.E.S., V.F., A.D., and R.D.S.; Material development, D.A., T.K., M.L., M.T.B. and J.N.; Measurements, T.K.J and J.E.S.; Writing, J.E.S. and T.K.J.; Supervision, M.T.B., J.N. and A.M.

Competing interests

The authors declare no competing interests.

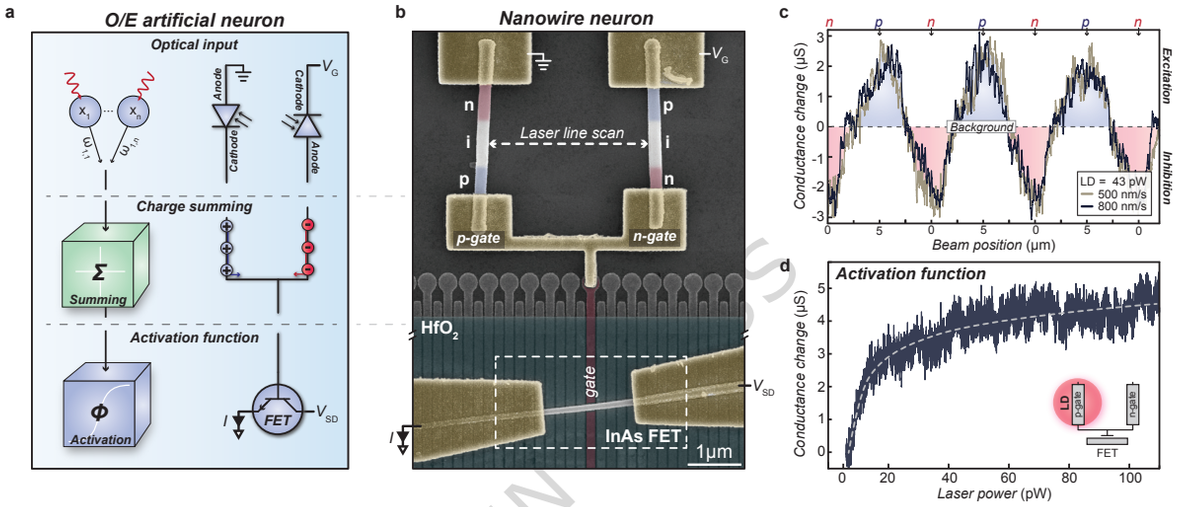


Fig. 1 Optoelectronic nanowire neuron. a, Conceptual artificial optical/electronic neuron and its circuit diagram. Optical inputs are converted to electrical charge carriers by two photodiodes. The carriers are summed and their total electrostatic signal is forwarded to a non-linear activation component (FET). **b**, False-coloured electron micrograph of the optoelectronic nanowire neuron device consisting of two InP pin-diode nanowires in opposing polarity connected electrostatically to an InAs nanowire-based field effect transistor. Yellow, Ti/Au contacts; Blue, p-doped region; Red, n-doped region; Grey, intrinsic InP or InAs; Dark red, Ti/Au gate; Light-blue, HfO_2. Electrical setup is composed of source-drain bias, V_{SD}, measured current, I, and applied voltage across the InP photodiode nanowires, V_G. Note: Image is cropped for illustrative purposes indicated by the two 'double slashes'. **c**, Conductance change as a function of laser spot position oscillating between the two photodiodes along the dashed line in **b**. Horizontal dashed line corresponds to the background conductance. **d**, Conductance change versus laser power indicating a sigmoid-like trace. The power meter at present setup calibrations does not detect linearly for power input <6 pW. Inset shows the stationary beam spot position and grey dashed line serves as a guide to to the eye.

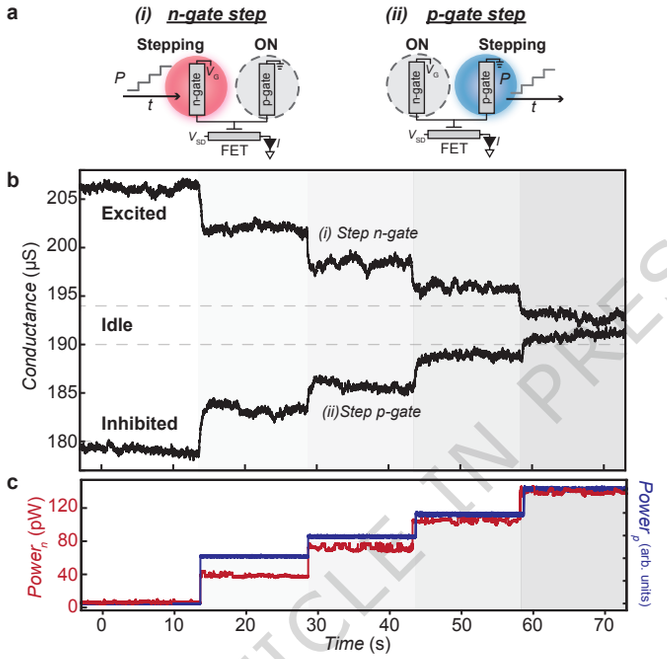


Fig. 2 Summing optical inputs. a, Measurement setup configuration where ***(i)*** denotes incident optical power stepped on the n-gate with constant light on the p-gate (ON) and ***(ii)*** shows the inverted configuration. **b**, Conductance across the FET plotted as a function of time. Traces are correlated with the two schematics shown in panel **a**. Idle state is defined as the background conductance (±2 μS) of the device under dark conditions, where $V_G = -3$ V. **c**, Power stepped of the light sources directed to the n-gate and p-gate in four increments as a function of time.

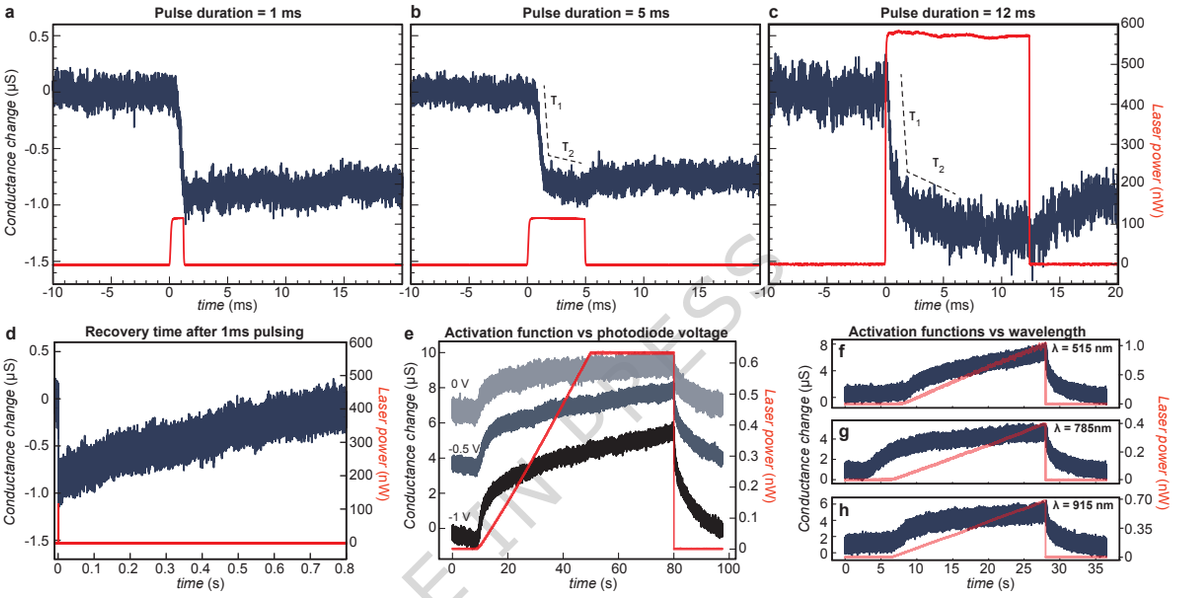
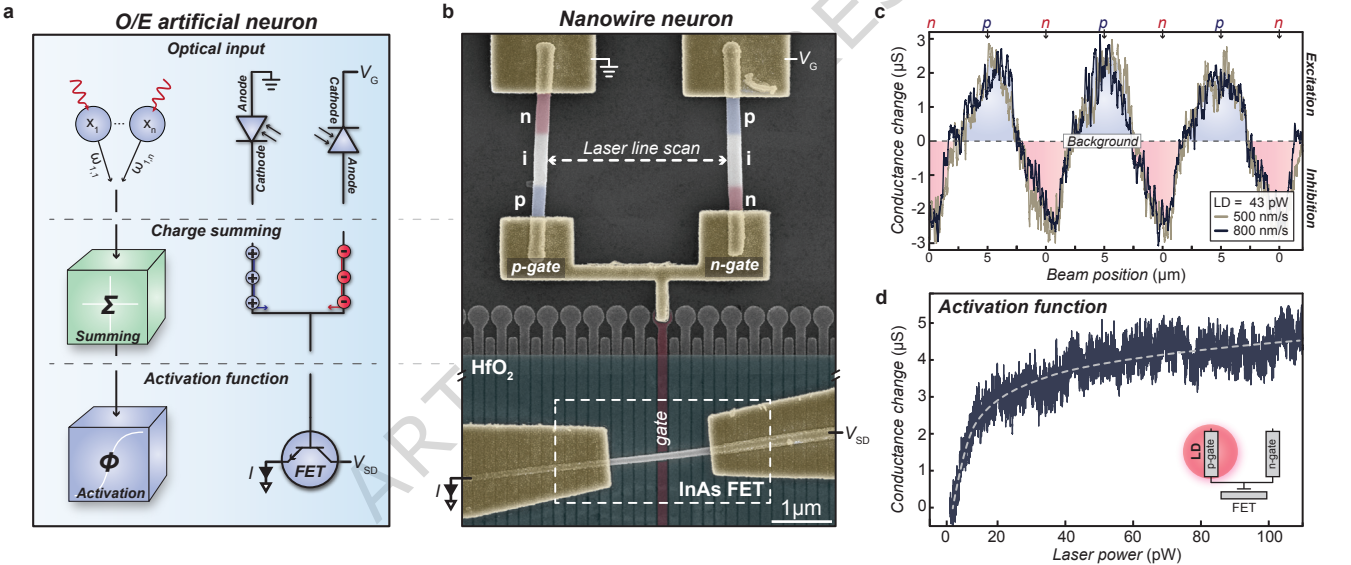


Fig. 3 Time dynamics, activation function tunability and wavelength sensitivity. a-c, Conductance change versus time recorded during three light pulse sequences of 1, 5 and 12 ms and different intensities. The light is directed onto the n-gate to generate 'inhibitory' behavior. Panels **a-c** show initial behavior during pulsing whereas **d** shows the time to recover to baseline conductance. During these measurements the p-gate is kept under constant selective illumination at power ranges of 10-20 mW. **e**, Conductance change recorded as a function of time and laser power for three different photodiode voltages, V_G = 0, -0.5 and -1 V. As V_G is tuned more negative the magnitude of the sigmoidal activation function shape becomes more pronounced. Traces are offset for clarity. **f-h**, Conductance change versus time and laser power recorded using three different wavelengths, λ = 515, 785 and 915 nm. All data are event-averaged.


a
O/E artificial neuron
Optical input
Anode
Cathode
Cathode
Anode
V_G
x_1
x_n
$\omega_{1,1}$
$\omega_{1,n}$
Charge summing
Σ
Summing
Activation function
Φ
Activation
FET
V_{SD}
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b
Nanowire neuron
V_G
n
i
p
Laser line scan
p
i
n
p-gate
n-gate
HfO_2
gate
V_{SD}
I
InAs FET
1μm
c
n
p
n
p
n
p
n
Excitation
Inhibition
Conductance change (μS)
Background
LD = 43 pW
500 nm/s
800 nm/s
Beam position (μm)
d
Activation function
Conductance change (μS)
LD
p-gate
n-gate
FET
Laser power (pW)