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Hybrid ferroelectric-ionic memristive hardware for high scalability in-memory computing

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Abstract

In-memory computing using two-terminal memristors offers a promising route to reduce the energy demands of data-intensive computing. However, current devices scale poorly due to sneak currents and materials that are incompatible with standard complementary metal-oxide-semiconductor and very large-scale integration processes. Here we demonstrate a self-rectifying memristor that unifies resistive switching and diode-like rectification in a single device, a hybrid ferroelectric–ionic tunnel diode fabricated using complementary metal-oxide-semiconductor compatible materials and processes. We harness the collective (ferroelectric-antiferroelectric polymorphism) and defective (ionic) switching behaviors of HfO_2-ZrO_2 to synergistically enhance both its electroresistance and rectifying behavior. Furthermore, conformal atomic layer deposition enables the integration of three-dimensional device structures, yielding high on/off (9.3×10^7) and rectifying (1.7×10^6) ratios with a storage capacity of 10 Gb. These results highlight the potential of this device as a hardware building block for scalable in-memory computing platforms.

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Introduction

The recent proliferation of artificial intelligence (AI) workloads, namely its need for enormous data throughput and off-chip memory, has overwhelmed conventional hardware, leading to rapidly increasing energy demands on modern computing systems[1,2]. A promising alternative, in-memory computing (IMC), co-locates data storage and processing to reduce data movement and power consumption[3–6]. In particular, two-terminal memristor-based crossbar arrays have attracted interest for their compact cell size and compatibility with analog computing tasks[3–5,7–11], as well as their three-dimensional (3D) integration potential with silicon complementary metal-oxide-semiconductor (CMOS)[12–15].

However, realizing large-scale memristor arrays is hindered by sneak path currents that degrade read/write accuracy and inflate power consumption[3]. Although adding selector devices (e.g., diodes or transistors) in one transistor–one resistor (1T-1R) or one diode–one resistor (1D-1R) configurations can mitigate sneak paths, these approaches cause challenges—including increased footprint area, matching issues between memristors and selectors, and complex peripheral circuitry requirements—that impede high-density integration[16,17]. Consequently, engineering intrinsic self-rectification in a single device has emerged as an attractive strategy[3]. Great progress has been made in maturing memristor technologies[18], e.g. resistive random access memory (RRAM)[8,19], phase change RAM (PCRAM)[20,21], and magnetic tunnel junction (MTJ)[22]; however, challenges in demonstrating robust self-rectifying behavior still remain unresolved[3]. Furthermore, these devices often exhibit limited compatibility with CMOS technology and very large-scale integration (VLSI) processes, thereby impeding their integration into modern microelectronics[23–27].

Fluorite-based ferroelectric devices—especially those employing HfO_2-ZrO_2 (HZO) thin films—have garnered significant interest due to their inherent functionality that can address these limitations of conventional memristors[28–30]. While alternative ferroelectric systems such as perovskite oxides[31], wurtzite nitrides[32], and van der Waals chalcogenides materials[33] demonstrate promising characteristics, their integration into modern microelectronics remains challenging. Notably, HZO can be synthesized using atomic layer deposition (ALD), a process already employed in the fabrication of modern logic transistors and DRAM capacitors[34,35]. This ensures that HZO-

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based devices are inherently compatible with CMOS and VLSI processes, enabling large-scale array integration with modern microelectronics[36–41].

Moreover, HZO exhibits polymorphism, including polar orthorhombic (o-), polar rhombohedral-[42], and antipolar phases, which coexist with nonpolar tetragonal or monoclinic phases, offering design flexibility to enhance device performance[43,44]. Alongside this rich structural polymorphism, the presence of ionic defects, namely oxygen vacancies (V_Os), provides an extra degree of freedom that can influence both ferroelectric polarization and ionic conduction under applied electric fields[45,46]. Whereas earlier studies concentrated on isolating intrinsic ferroelectric switching from defective ions, emerging evidence suggests that ion-mediated effects can synergistically improve ferroelectric switching in HZO[45,47–49]. Yet, harnessing these hybrid ferroelectric–ionic interactions in two-terminal memristors – to simultaneously achieve superior switching performance and robust rectifying behavior for large-scale, high-density arrays – remains an open challenge.

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Here, we demonstrate a CMOS-compatible and VLSI-scalable hybrid ferroelectric–ionic tunnel diode (HTD) that achieves both a giant on/off ratio and pronounced self-rectification. First, at the materials level, we exploit the rich polymorphism of HZO to harness its inherent ferroelectric properties while synergistically leveraging V_O to enhance both the switching dynamics and self-rectification. Second, at the device level, we capitalize on the conformal growth capability of ALD to integrate the HTD into a 3D structure. This 3D integration not only increases array density through vertical stacking but also improves electrostatic control and switching dynamics. This enables a remarkable enhancement in both the on/off ratio (9.3×10^7) and self-rectifying ratio (1.7×10^6)—values that exceed all previously reported benchmarks. Third, at the array level, the combined material and device optimizations enable a record-high Gb-level storage capacity, surpassing that of all other two-terminal memristor systems. Collectively, these results establish a robust, scalable, and energy-efficient memristor building block for next-generation IMC that seamlessly integrates with existing CMOS and VLSI processing.

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Results

Hybrid ferroelectric ionic switching Ferroelectric tunnel junctions (FTJs) and ferroelectric diodes (FeDiodes) represent established categories of two-terminal ferroelectric memristors (Supplementary Note 1). Here, we introduce a two-terminal memristive device exhibiting enhanced characteristics beyond traditional FTJ and FeDiode functionalities. The working principle of two-terminal memristors should be analyzed considering both barrier switching and carrier conduction mechanisms. When hafnia-based materials are used as the barrier switching layer, ferroelectric polarization and ionic migration can modulate the energy barrier (Fig. 1a)[50], thus generating a memory window (i.e. on/off ratio) defined by the current ratio between the high-resistance state (HRS) and the low-resistance state (LRS) (Fig. 1b)[4]. In this study, we introduce a novel two-terminal tunnel junction that achieves both giant on/off and rectifying ratios; which is essential to large-scale array demonstration based on two-terminal devices (Fig. 1c).

To understand the coexistence and hybrid ferroelectric-ionic switching behavior in HZO films, we fabricated three types of tunnel junctions, each demonstrating distinct switching behaviors: (i) an FTJ characterized by pure intrinsic ferroelectric polarization, (ii) an HTD featuring both intrinsic ferroelectric and defective ion switching, and (iii) an ionic memristor exhibiting defective ion switching without ferroelectric polarization (Fig. 1d). All tunnel junctions adopt ALD-grown-6 nm-HZO films with metal-ferroelectric-insulator-metal (MFIM) structures. To modulate the switching behavior of the tunnel junctions, we controlled the ferroelectricity and V_O concentration through the post-metal annealing (PMA) temperature and an oxygen scavenging layer (Ti) (Methods and Supplementary Figures 1-5).

All three devices exhibit counterclockwise hysteresis, yielding an HRS at the forward voltage sweep and an LRS at the backward sweep (Fig. 1e). Among the three devices, both the FTJ and the ionic memristor show an initial rise in on/off ratio but tend to saturate under higher bias. In contrast, only the HTD shows a continuous increase with increasing top electrode voltage (V_{TOP}). Notably, at around V_{TOP} = 4.4 V, the HTD undergoes a distinct transition, diverging from its earlier trend and further boosting the on/off ratio—suggesting that additional switching mechanisms come into play beyond intrinsic ferroelectric polarization. As a result, the HTD exhibits the largest

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on/off ratio owing to its mixed switching behavior, reaching an on/off ratio of 4.1×10^4 (Fig. 1f). Moreover, due to its large asymmetry in interface characteristics between the top and bottom electrodes in the HTD, results of the V_Os near the bottom electrode, the HTD exhibits the largest self-rectifying ratio of 9.1×10^3 (Supplementary Note 2). The different switching behaviors among tunnel junctions have been further verified by low-frequency noise (LFN) spectroscopy, pulsed program operation, retention characteristics, polarization properties, endurance cycling test, device-to-device (D2D) variation, negative voltage sweep characteristics, and by temperature-dependent transport that defines a practical bias map comprising low-bias trap-assisted tunneling, an intermediate polarization-controlled tunneling window, a V_O-assisted onset, and a high-bias ionic V_O-drift regime (Supplementary Figures 6-12 and Supplementary Notes 3-6).

We attribute the large on/off and rectifying ratios observed in the HTD to the coexistence of ferroelectric phases and V_Os in the HZO film, as confirmed by structural characterization. High-angle-annular dark-field (HAADF) and integrated differential phase contrast (iDPC) scanning transmission electron microscopy (STEM) images reveal an o-phase HZO region and localized polar ($Pbc2_1$) and antipolar ($Pbca$) phases, determined by tracking oxygen displacements (Figs. 2a,b)[49,51–54]. Electron energy-loss spectroscopy (EELS) and X-ray photoelectron spectroscopy (XPS) analyses reveal that V_Os mostly accumulate at the bottom interface (Fig. 2c and Supplementary Figure 13)[45,55]. Based on these observations, the hybrid switching mechanism can be illustrated via energy band diagrams for each switching phase under varying program voltage (V_{PGM}) (Figs. 2d-f). In the HRS, conduction is governed by direct tunneling, with the tunneling barrier width determined by the combined thicknesses of the ferroelectric and dielectric layers. The imprint field of the HZO, stemming from the asymmetric distribution of V_Os, contributes to the HTD's pronounced self-rectification (Fig. 2g and Supplementary Figure 14).

When a higher V_{PGM} is applied, ferroelectric switching reverses the energy band alignment in the HZO and dielectric (Al_2O_3), shifting the conduction mechanism to Fowler–Nordheim (FN) tunneling (Fig. 2e). During this stage, the polymorphic nature of HZO and its interaction with V_Os are critical for enhancing the ferroelectric switching. This involves (i) V_O-induced ferroelectric switching barrier lowering in the polar $Pbc2_1$ phase and (ii) V_O-assisted antipolar-to-polar transi-

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tion in the anti-polar $Pbca$ phase (Fig. 2h). First, the V_O-induced ferroelectric switching barrier lowering was verified by the nucleation-limited switching (NLS) model and density functional theory (DFT) calculations. It is revealed that V_O substantially decreases the nucleation energy and coercive field, enhancing switching speed (Supplementary Figure 15 and Supplementary Notes 7-8). DFT calculations further confirmed that introducing V_Os into the domain wall region dramatically reduces both the domain wall energy and the migration barrier. V_O alleviates electrostatic repulsion among oxygen ions, thereby accelerating domain nucleation and lowering the ferroelectric switching barrier (Methods, Supplementary Figures 16-20, and Supplementary Note 9). Concurrently, a volatile transition from the antipolar to the polar o-phase in the $Pbca$ phase can be induced under an external bias when a high concentration of V_Os is present[46]. This phase transition at the V_O-rich bottom electrode interface effectively increases the work function of HZO, bending the energy band downward and facilitating electron transport via FN tunneling in the LRS.

Further increases in V_{PGM} induce ionic switching via V_O migration, leading to space-charge limited conduction (SCLC) (Fig. 2i). In conventional FTJs, the ferroelectric polarization-induced barrier height modulation is limited due to the saturation of polarization beyond a certain V_{PGM}. However, in HTDs, even after polarization saturation, migration of positively charged V_O to the bottom dielectric layer can further lower the tunneling barrier and enhance the on-current. It is crucial to note that for the ionic component to effectively contribute to switching, the band of the dielectric layer must reverse toward the top electrode. In HTDs, this band reversal occurs at much lower voltages compared to FTJs (Fig. 2h), thereby maximizing the ionic component's contribution to the on-current.

Three dimensional device integration This hybrid switching can be further enhanced by 3D integration of the HTD. Here, four levels of 3D hole-type HTDs are fabricated leveraging the conformal growth nature of ALD (Fig. 3a, Supplementary Figure 21, and Methods). The structure of the 3D HTD is fundamentally similar to that of the two-dimensional (2D) HTD. As in the 2D structure, the polar phase ($Pbc2_1$) and antipolar phase ($Pbca$) are preserved in the 3D HTD (Fig. 3b and Supplementary Figures 22-23). Additionally, the V_O-rich characteristics at the bottom electrode, which play a crucial role in device operation, are also maintained (Fig. 3c and Supplementary Fig-

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ure 24), ensuring consistent switching behavior and self-rectifying properties. Note that the HZO exhibits a highly ordered ferroelectric crystalline structure in this 3D configuration.

The fabricated 3D HTDs exhibit the same switching behavior as the 2D structure, including distinct DC response, pulse-based program, and retention characteristics (Supplementary Figure 25). Notably, their switching dynamic demonstrates significant enhancement after 3D integration. First, in the 3D structure, the tensile stress introduced during the PMA is comparatively more oriented out-of-plane than in the 2D planar structures, facilitating the alignment of ferroelectric domains along the electric field axis and thereby enhancing its polarization response[56–58]. This enhancement originates from the conformal ALD process that uniformly coats the TiN dummy metal inside the vertical holes during PMA, resulting in homogeneous out-of-plane tensile stress distribution throughout the stacked structure. This effect is validated through TEM analysis, where, unlike the 2D device that exhibits a domain tilt of approximately 30°, regions of the 3D device can demonstrate perfectly out-of-plane aligned ferroelectric domains (Figs. 3d-e, Supplementary Figure 22, and Supplementary Note 10). Second, the 3D structures introduce electrostatic modifications that increase the electric field distribution across the ferroelectric layer (Fig. 3f). Therefore, the effective coercive voltage of HZO is reduced, further enhancing hybrid switching and enabling the higher on-current. Moreover, the voltage applied to the dielectric layer is lowered, effectively suppressing direct tunneling in the HRS, thereby achieving an ultra-low off-current (Fig. 3g, Supplementary Figures 26-27, and Supplementary Note 11). This synergistic enhancement leads to an on/off ratio of 9.3×10^7 and a rectifying ratio of 1.7×10^6, both of which are 10^3 larger than the 2D HTD (Fig. 3h,i). Note that these values are averages across multiple devices.

Notably, this improvement in switching dynamics enhances multi-level conductance behavior essential for IMC[7,59] (Methods, Supplementary Figures 28-29, and Supplementary Note 12). While conventional filamentary RRAM or FeDiode devices can achieve high on/off ratios, they typically exhibit abrupt, step-like transitions, limiting the realization of gradual multi-level conductance changes crucial for vector–matrix multiplication (VMM). In contrast, HTDs leverage a hybrid ferroelectric–ionic switching mechanism that provides both a large dynamic range and finely tunable conductance steps, enabling the gradual conductance modulation required for VMM

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operations[60,61].

Array scalability In both conventional memory and IMC applications, array scalability plays a key role. As aforementioned, the maximum practical array size is largely determined by the on/off and rectifying ratios of memristors. We benchmark the on/off and rectifying ratios across FTJs with various material systems, including both CMOS-compatible ALD HfO_2-based FTJs and less compatible ones, such as perovskite and epitaxial fluorite HfO_2-based FTJs (Fig. 4a). Perovskite-based FTJs, for instance, often require complex non-CMOS fabrication steps, while epitaxial fluorite-structure HfO_2-based FTJs, although promising, still pose challenges in process complexity and scalability[62]. Moreover, unlike conventional FTJs, which exhibit a trade-off between on/off and rectifying ratios, the HTD simultaneously achieves both superior on/off ratios and exceptional self-rectifying behavior. In typical FTJs, enhancing the on/off ratio often relies on reducing or homogenizing the tunneling barrier, both of which inadvertently lower the built-in asymmetry required for rectification. In contrast, the hybrid ferroelectric–ionic switching in HTD maintains pronounced conduction asymmetry, thus maintaining robust self-rectification even at the high on/off ratio. The HTD achieves an on/off ratio of 9.3×10^7 and a rectifying ratio of 1.7×10^6, both markedly higher than those of recently reported CMOS-compatible FTJs ($\approx 2 \times 10^4$ and 1.5×10^3)[63] and non-CMOS-compatible FeDiodes ($\approx 10^6$ and 2.5×10^3)[64]. This superior balance between switching contrast and self-rectification highlights the unique advantage of hybrid polarization-ionic modulation in maintaining asymmetric transport even at high conductance ratios.

Based on the on/off and rectifying ratio performance, we next evaluate the array scalability using a resistance model (Supplementary Figures 30-31 and Supplementary Note 13). In IMC systems, where numerous parameters necessitate large-scale VMM, it is essential to significantly scale the synaptic device array, each encoding multiple levels of conductance. Traditional two-terminal devices such as RRAM or FTJ, although capable of a high on/off ratio, typically lack sufficient rectification for large-scale integration, often requiring additional selectors to suppress sneak path currents. However, incorporating external selectors (1T-1R or 1D-1R) complicates device fabrication and reduces integration density. In contrast, by leveraging hybrid switching, HTDs achieve

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inherently self-rectifying behavior alongside a giant on/off ratio, enabling high-density arrays without additional selector elements. Extending beyond FTJs and FeDiodes, we compare HTDs against various two-terminal memristors, including RRAMs, PCRAMs, and MTJs, demonstrating that the HTD attains the highest array scalability among all two-terminal memristors, achieving array scalability up to the 10 Gb scale (Fig. 4b and Supplementary Figure 32).

Beyond benchmarking, we fabricated a 25×23 HTD array and confirmed negligible program/erase half-bias disturbance across all neighbor regions, evidencing robust array-level reliability (Supplementary Figure 33). Building on this result, we validated array-level VMM operation, observing reproducible weighted-sum outputs under repeated random inputs (Supplementary Figure 34). The program/erase pulse conditions were identical to those used for the single device switching-speed characterization (Supplementary Figure 6e), confirming that the HTD array operates reliably under the same operating regime. By combining a CMOS-compatible, 3D-integrable stack with intrinsic self-rectification (suppressing sneak paths), multi-level near-linear updates, and a large on/off window, the HTD removes the need for external selectors and sustains scalable, dense IMC arrays with robustness to measured device variability.

Another critical requirement for memristors is achieving a sufficiently high on-current.[65,66] Ferroelectric memristors based on tunneling currents, including FTJs and FeDiodes, typically suffer from reduced on-current as device dimensions scale down. While low on-currents can be advantageous in IMC for energy-efficient operation, excessively low currents may undermine device reliability and signal integrity. Crucially, our hybrid switching approach effectively addresses this limitation, simultaneously enabling device miniaturization and high on-current without compromising switching speed (Supplementary Figure 35 and Supplementary Note 14). Therefore, the HTD represents a compelling candidate for next-generation IMC architectures.

Discussion

Here, we demonstrate an HTD for memory and IMC that overcomes the intrinsic limitations of conventional two-terminal memristors, achieving a high on/off ratio, self-rectifying ratio, and array scalability. Building upon recent advancements in ferroelectric switching mechanisms—such as sliding ferroelectrics—that have significantly expanded memory functionalities, we introduce a

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hybrid switching paradigm uniquely enabled by the polymorphic nature of HZO intertwined with ionic dynamics. Furthermore, leveraging ALD-enabled 3D integration, we demonstrate the potential for ultra-high-density arrays capable of Gb-level scalability without selectors—representing the highest scalability reported to date among two-terminal memristors. Moving forward, the 3D HTD presents opportunities at multiple research levels: from exploring novel HZO polymorphs at the material level to developing advanced 3D device architectures, and ultimately enabling large-scale array integration. These advances collectively highlight the value of studying emergent phenomena within comparatively simple yet CMOS-compatible material systems—rather than relying on complex or non-integrable platforms—to realize next-generation electronics, such as energy-efficient IMC architectures. Future work should rigorously assess thermal stability and develop circuit-level compensation—deploying temperature-aware read/write schemes. Equally important is proving true BEOL integration by preserving device integrity and performance after BEOL-relevant thermal budgets. Finally, model-free validation through large-scale array prototypes is needed to quantify system-level behavior under realistic interconnect parasitics, considering IR drop, capacitive coupling, sneak-path interference; meeting these criteria will convert the promise of 3D HTDs into manufacturable, energy-efficient IMC.

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Methods

Fabrication process

Two dimensional devices: The fabrication process of FTJ, HTD, and ionic memristor is illustrated in Supplementary Figure 1. Tunnel junctions were fabricated on a highly doped p-type silicon substrate. First, the substrates were cleaned using SC-1 solution (NH_4OH : H_2O_2 : H_2O = 1:1:5), and the chemical oxide formed by the SC-1 solution was completely removed using buffered oxide etchant solution (NH_4F : HF = 6:1). Molybdenum (Mo) was sputtered as the bottom electrode for FTJ, HTD, and ion memristor. But titanium (Ti) was only sputtered for HTD and ionic memristor as the oxygen scavenging layer (OSL) on Mo. Al_2O_3 layer with trimethyl aluminum (TMA) precursor and HZO layer deposition with tetrakis (ethylmethylamino) hafnium (TEMAHf) and tetrakis (ethylmethylamino) zirconium (TEMAZr) precursors were sequentially conducted using thermal ALD (CN-1). Mo was sputtered as the dummy metal using DC sputter, and RTA was performed at 500 °C for FTJ and HTD to crystallize the HZO film, but performed at 400 °C for ion memristor to prevent crystallization. The dummy metal was removed using SC-1 solution, and then Mo was sputtered as the top electrode. Finally, it was patterned in a circular shape with an area of 1.25×10^{-4} cm^2 by an aligner and wet etching (SC-1 solution, NH_4OH : H_2O_2 : H_2O = 1:8:64).

Three dimensional devices: The fabrication process of 3D HTD is described in Supplementary Figure 21. First, oxide and metal layers were alternately deposited on cleaned p-type silicon by SC-1 solution (NH_4OH : H_2O_2 : H_2O = 1:1:5) and buffered oxide etchant solution (NH_4F : HF = 6:1). Each OMO stack was individually patterned to allow separate electrical contacts. Hole-pattern was etched to define vertical device geometry through the 4-layer OMO stack. During this etching process, the exposed TiN surface became more reactive, effectively serving as an oxygen-scavenging layer (OSL). The dielectric and ferroelectric layers were subsequently deposited using thermal ALD (CN-1). An Al_2O_3 layer was formed with trimethyl aluminum (TMA) precursor, acting as the dielectric layer, followed by deposition of an HZO layer using tetrakis (ethylmethylamino) hafnium (TEMAHf) and tetrakis (ethylmethylamino) zirconium (TEMAZr) precursors to form the ferroelectric layer. To ensure conformal coverage inside the etched structures, a TiN

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dummy metal was deposited by thermal ALD (CN-1). Post-metal annealing (PMA) was performed at 500 °C to induce ferroelectricity in the HZO film. The dummy metal layer was then selectively removed using SC-1 solution. After dummy removal, TiN was redeposited by thermal ALD to serve as the top electrode. Finally, an inter-layer dielectric (ILD) was deposited for device isolation, followed by the formation of contact pad metal to complete the device fabrication.

Electrical measurements

On/off & rectifying ratio: The on/off ratio and rectifying ratio were extracted from hysteretic DC double-sweep measurements. The on/off ratio was calculated as the current (or resistance) ratio between the low-resistance state (LRS, ON state) and the high-resistance state (HRS, OFF state) at the read voltage (V_{READ}). The rectifying ratio was determined as the current ratio between the forward and reverse biases at the same magnitude of V_{READ} in the LRS. The corresponding equations are expressed as follows:

$$\text{On/off ratio} = \frac{|I_{\text{LRS}}(V_{\text{READ}})|}{|I_{\text{HRS}}(V_{\text{READ}})|} \tag{1}$$

$$\text{Rectifying ratio} = \frac{|I_{\text{LRS}}(V_{\text{READ}})|}{|I_{\text{LRS}}(-V_{\text{READ}})|} \tag{2}$$

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Low-frequency noise: LFN measurements were performed by applying the device bias with a Keysight B1500A, capturing the resulting current and converting it to voltage with an SR570 low-noise current preamplifier, and analyzing the amplified output using a Keysight 35670A dynamic signal analyzer to obtain the power spectral density as a function of frequency ($S_{I_{\text{T}}}$ / I_{T}^2 versus f). Each spectrum covered 1 Hz to 1600 Hz with 20 averages to suppress random fluctuations. From the PSD, we extracted the noise magnitude and frequency exponent in both HRS and LRS, and we discuss the bias dependence and regime transitions in the manuscript.

Pulsed switching operation: Pulsed switching measurements were performed by applying program voltage pulses to the top electrode (TE), and the resulting resistance states were subsequently measured at a fixed read voltage (V_{READ}) using DC sampling mode. To evaluate the switching speed, the pulse width was progressively increased — 20 ns, 50 ns, 100 ns, 200 ns, and

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so on — under the same pulse amplitude. All measurements were carried out using a semiconductor parameter analyzer (Keysight B1500A). The pulse scheme used for the pulsed operation measurement is shown in the inset of Supplementary Figure 6f.

Retention: Retention measurements were conducted by applying program and erase voltage pulses to the TE, followed by monitoring the read current at a V_{READ} using DC sampling over time. After the initial program or erase pulse, the read current was measured at successive time intervals — 1 s, 5 s, 10 s, 20 s, and so on — to evaluate the temporal stability of the resistance states. All measurements were carried out using a semiconductor parameter analyzer (Keysight B1500A). The pulse scheme employed for the retention tests is illustrated in the inset of Supplementary Figure 6i.

Positive-up-negative-down method: The PUND measurement method was employed to distinguish the switching and non-switching components of the ferroelectric current. In this method, two consecutive voltage pulses with the same polarity are applied to the TE. The first pulse induces both switching and non-switching currents, whereas the second pulse, applied immediately afterward, measures only the non-switching current because the polarization state has already been reversed by the first pulse. The difference between these two current responses corresponds to the net switching current. Before the PUND sequence, a pre-poling pulse was applied to ensure complete polarization reversal. The measurements were performed using a semiconductor parameter analyzer (Keithley 4200A-SCS). The pulse scheme is illustrated in the inset of Supplementary Figure 7c.

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Endurance: Endurance cycling tests were performed by applying program and erase voltage pulses to the TE, followed by DC sampling at a (V_{READ}) to monitor the resistance states during repetitive program/erase pulse cycling. Initially, a single pulse was applied, and the corresponding read current was measured. The number of applied pulses was then progressively increased — 10^1, 10^2, and so on — while recording the read current after each set of cycles to evaluate the evolution of the resistance state. This iterative procedure enabled the assessment of switching stability and device endurance. All measurements were carried out using a semiconductor parameter analyzer (Keysight B1500A). The pulse scheme employed for the endurance tests is shown in the inset of

Supplementary Figure 9a.

Scanning transmission electron microscopy characterization Cross-sectional TEM samples of the device were prepared using a FEI Helios Nanolab 600 Dual Beam system. Protective layers of C, then Pt were deposited over the sample region using the electron beam. A cross-section was milled with Ga^+ ions, extracted with an Omniprobe nanomanipulator, and attached to a TEM copper half grid (manufacturer Ted Pella) using carbon deposited with the ion beam. The final thinning of the sample was then performed using Ga^+ ions to obtain a thickness of approximately 20 nm. Samples prepared in this way were imaged in an aberration-corrected Thermo Fisher Themis Z STEM operated at 200 kV. The probe convergence angle was 18.9 mrads, the beam current was ~50 pA, and the camera length was 285 mm. STEM-EELS measurements were conducted by a Cs-corrected (probe corrector) JEOL-ARM200CF microscope with a cold-field emission electron gun operated at an acceleration voltage of 200 kV. Model 965 GIF Quantum ER detector was used for STEM-EELS measurement. STEM-EELS quantification was conducted using Gatan Microscopy Suite software (GMS 3), based on the method inspired by the work of Verbeeck and Van Aert[67]. Oxygen K-edge signals from 532 eV to 592 eV were used, and the plural scattering effect was corrected for the quantification. TEM images were acquired and were drift corrected using the drift correction frame integration (DCFI) function of the Velox software to increase the signal-to-noise ratio for the HAADF images with a frame size of 1024 × 1024 pixels with a 500 ns/pixel dwell time. iDPC imaging was done to capture oxygen atoms with a frame size of 4096 × 4096 pixels and 2 μs/pixel dwell time.

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Density functional theory calculation DFT calculations are carried out using Vienna Ab-Initio Simulation Package (VASP) with the projector-augmented-wave pseudopotentials[68,69]. An energy cutoff of the plane wave basis is set to 500 eV. The PBEsol functional is employed to describe the exchange-correlation potential. The optimized lattice parameters of o-HfO_2 are a=5.20 Å, b=5.00 Å, and c=5.02 Å, which are in good agreement with experiments within 1% error[70]. A 2×2×2 supercell of o-HfO_2 is used to calculate direct polarization switching and formation energy of V_O in bulk. 1×8×1 and 2×8×2 supercells are employed to model the 180° DW with and without V_O^{2+},

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respectively. A transition state of polarization switching is explored by means of a climing image nudged elastic band (CINEB) method[71]. For the Brillouin-zone integration, 2×2×2, 4×1×4, and 2×1×2 k-point grids are used for 2×2×2, 1×8×1, and 2×8×2 supercells, respectively. The energy barriers for direct polarization switching of pristine bulk (0.347 eV) and the DW migration of the V_O-free model (0.237 eV) are consistent with previous calculations[72–75].

Electric field simulation To determine the HTD e-field, interfacial layer thickness (T_{ox}) of 2 nm, FE thickness of 6 nm, and body thickness (T_{body}) of 10 nm were selected. For the FE material, the HZO thickness (T_{FE}) was 6 nm with a dielectric constant of 25 between the interfacial layer (IL) and top metal. All FTJ e-field evaluations were performed using a commercial technology computer aided design(TCAD) tool (Synopsys Sentaurus™). To consider the e-field with polarization, we use Preisach model which is expressed as follows:

$$P_{aux} = c \cdot P_s \cdot tanh(w \cdot (E \pm E_c)) + P_{off} \tag{3}$$

$$w = \frac{1}{2E_C} ln \frac{P_s + P_r}{P_s - P_r} \tag{4}$$

where E is electric field, P_{aux} is auxiliary polarization and where P_{s} is saturation polarization, P_{r} is remanent polarization and E_{c} is coercive field. The schematics of planar and 3D HTD are shown in Supplementary Figure 27a,b with MFIM stacks. For various read voltages, the radius effect determines that hole type HTD has a lower e-field in DE and higher e-field in FE than a planar HTD. (Supplementary Figure 27c-f). In the TAT operating region of HTD, TAT is suppressed due to the lower e-field in the DE in the hole type, and switching is accelerated in the polarization switching region due to the higher FE e-field.

Neuromorphic simulation To assess the performance of the synaptic functionality of tunnel junctions, we simulated a nine-layer visual geometry group (VGG-9) network using the Canadian Institute for Advanced Research (CIFAR-10) dataset. This VGG-9 network architecture comprises six convolutional layers, three max-pooling layers, and two fully connected layers, with one max-pooling layer utilized for each pair of convolutional layers. All input images from the

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CIFAR-10 dataset were of size 32 × 32 × 3 pixels, and convolutional layers employed kernels with three weights. Upon processing CIFAR-10 images through the first and second convolutional layers, feature maps of dimensions 32 × 32 × 32 and 32 × 32 × 64 pixels were generated, respectively. Following operations of the third and fourth convolutional layers, feature maps of size 16 × 16 × 128 were obtained. Subsequently, the fifth and sixth convolutional layers produced feature maps sized 8 × 8 × 256. Finally, all feature maps were connected to the fully connected layers for further processing.

The long-term potentiation/depression LTP/LTD characteristics are compared on the base of linearity. The weight updates for LTP/LTD can be expressed as

$$W_{LTP} = g_{min} + \alpha(1 - e^{\beta x/N}) \tag{5}$$

$$W_{LTD} = g_{max} - g_{min} - \alpha(1 - e^{\beta x/N}) \tag{6}$$

$$\alpha = (g_{max} - g_{min})/(1 - e^{-\beta}) \tag{7}$$

where g_{max} and g_{min} are the maximum and minimum conductances, respectively, β is the non-linear factor, and N is the total number of pulses applied during the LTP (LTD). Supplementary Figure 28b,c show that the β is much lower in HTD, demonstrating superior synaptic characteristics over FTJ.

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Literature benchmarking In Fig. 4a,b, we utilized values reported directly in the cited papers[15,47,63–65,76–98]. For cases where the on/off ratio or rectifying ratio was not explicitly provided, we extracted these values from the I-V curves in the region showing the highest rectifying ratio and on/off ratio under the applied bias conditions. Based on these extracted values, we calculated array scalability using the $V/3$ scheme. It should be noted that this approach may lead to minor deviations from the actual figure of merit, as our extraction method approximates the reported device characteristics.

Data Availability The data supporting the findings of this study are available within the paper, the Supplementary Information, and the Source Data file. Source data are provided with this paper.

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Additional data is available from the corresponding author upon request.

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Author Contributions Statement J.-H.K., W.S., and R.-H.K. conceived the idea and experiments. J.Y. performed material synthesis and ferroic phase optimization. J.Y., D.Koh, and Y.C. performed dielectric characterization. J.-H.K., W.S., R.-H.K., and J.K. performed electrical measurements. R.-H.K. performed NLS modeling. R.-H.K. and J.I. performed IMC simulation. W.S., Y.H., and Q.X. performed LFN measurements. J.-H.K., J.Y., and H.-M.K. performed device fabrication. J.-H.K. performed 3D device fabrication. B.K. performed TCAD simulations. S.K., J.H., S.-Y.L., H.S., and D.-H.K. performed materials analyses. E.P., P.B., and D.-H.K. performed electron microscopy. Y.K. performed first-principles calculations. F.A.D. performed 3D array scalability modeling. H.J., W.J., K.L., and D.H. advised on 3D device fabrication. J.-H.K., W.S., E.P., D.-H.K., S.S.C., and D.Kwon wrote the manuscript. W.S., S.-Y.L., J.-H.L., F.M.R., S.S.C., and D.Kwon supervised the research. All authors contributed to discussions and manuscript preparations.

Competing Interests Statement The authors declare no competing interests.

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Fig. 1 | Hybrid ferroelectric-ionic switching. **(a)** Schematic of the device structure and switching characteristics of tunnel junctions. Ferroelectric polarization and ionic migration can modulate the energy barrier in hafnia-based switching devices. **(b)** Carrier conduction mechanism of the junctions depending on the HRS and LRS. **(c)** Memory performance of tunnel junctions, including on/off and rectifying ratios. **(d)** Method to leverage the synergistic ferroelectric-ionic switching in HZO. **(e)** DC hysteretic switching behavior. **(f)** On/off and rectifying ratios of FTJ, HTD, and ionic memristor, respectively. The HTD exhibits the largest on/off ratio (4.1×10^4) and rectifying ratio (1.2×10^4).

Fig. 2 | Microscopic origin of ferroelectric-ionic switching and synergistic enhancement. **(a)** Cross-sectional HAADF-STEM image through the HZO thickness. The image was taken at a location where o-phase HZO is present with an orientation suitable for imaging its polarity. Scale bar: 2 nm **(b)** iDPC image of the HZO region showing the two polarization directions, up and down, highlighted in purple and blue, respectively. Magnified antipolar and polar o-phases are shown in the purple and blue outlined insets, respectively. Scale bar: 2 nm **(c)** Oxygen vacancy distribution analysis using EELS and XPS, suggesting a higher oxygen vacancy concentration at the HZO/insulator interface compared to the HZO/top electrode interface. The absence of interfacial stress effects was further confirmed by GPA strain mapping shown in Supplementary Figure 13. Energy band diagram and I-V characteristic evolution under applied electric field. **(d)** HRS with self-rectifying behavior with direct tunneling as a conduction mechanism, **(e)** LRS with FN tunneling, and **(f)** LRS with hybrid switching with SCLC. **(g)** EELS analysis for the oxygen vacancy distribution mapping using the p_1/p_2 ratio. **(h)** Polarization switching enhancement in polar o-phase ($Pbc2_1$) and antipolar to polar phase transition in antipolar phase ($Pbca$) with the presence of oxygen vacancies. **(i)** Pulsed program behavior of the HTD and comparison with FTJ and ionic memristor. The hybrid switching provides HTDs with significantly improved switching characteristics compared to conventional FTJs and ionic memristors.

Fig. 3 | Array scalability enhancement by 3D integration. **(a)** TEM image of 3D integrated HTD using conformal growth of ALD-based HZO. The 4 levels of the HTDs are vertically stacked in a single trench. Scale bar: 200 nm **(b)** Oxygen image of HZO, exhibiting polar o-phase ($Pbc2_1$) and antipolar phase ($Pbca$). **(c)** Oxygen distribution of the 3D HTD by EELS analysis, showing an increase in oxygen vacancies near the bottom electrode. The absence of interfacial stress effects was further confirmed by thickness mapping

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analysis in Supplementary Figure 24. **(d)** Schematic image of the 3D HTD with 4 levels. Enhanced electrostatic in 3D HTD. Field enhancement can be achieved in some regions of HZO in 3D HTD due to **(e)** the out-of-plane domain alignment and **(f)** increased/decreased electric field at ferroelectric/dielectric layers in the 3D HTD compared to that of planar structures. **(g)** Current density versus voltage curve of the 2D and 3D HTDs. Comparison of **(h)** on/off ratio and **(i)** rectifying ratio (RR) of the 2D and 3D HTDs.

Fig. 4 | Benchmark and array scalability. **(a)** Benchmark of on/off ratio and rectifying ratio of FTJs with different material systems, including CMOS-compatible ALD HfO_2-based FTJs[63,82,83] and less compatible alternatives such as perovskite oxide[77–79,97], van der Waals[47,64,80,81,98], Wurtzite nitride[15,76], and epitaxial fluorite HfO_2-based FTJs[84,85]. **(b)** Comparison of array scalability between HTDs and other two-terminal nonvolatile memories, including RRAM[86–88,93–95], MTJ[96], PCRAM[91], FeDiode[64,65,92], and FTJ[63,89,90]. The crystal structure of FTJ was visualized using VESTA[99].

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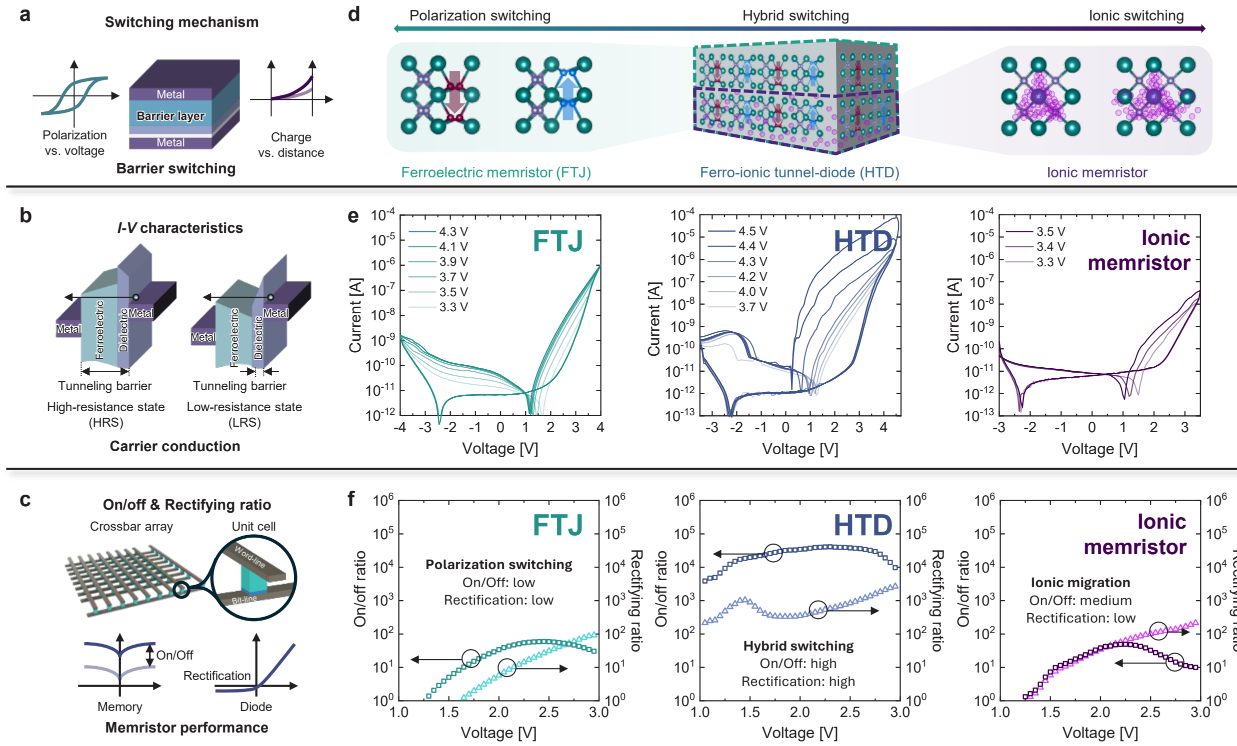

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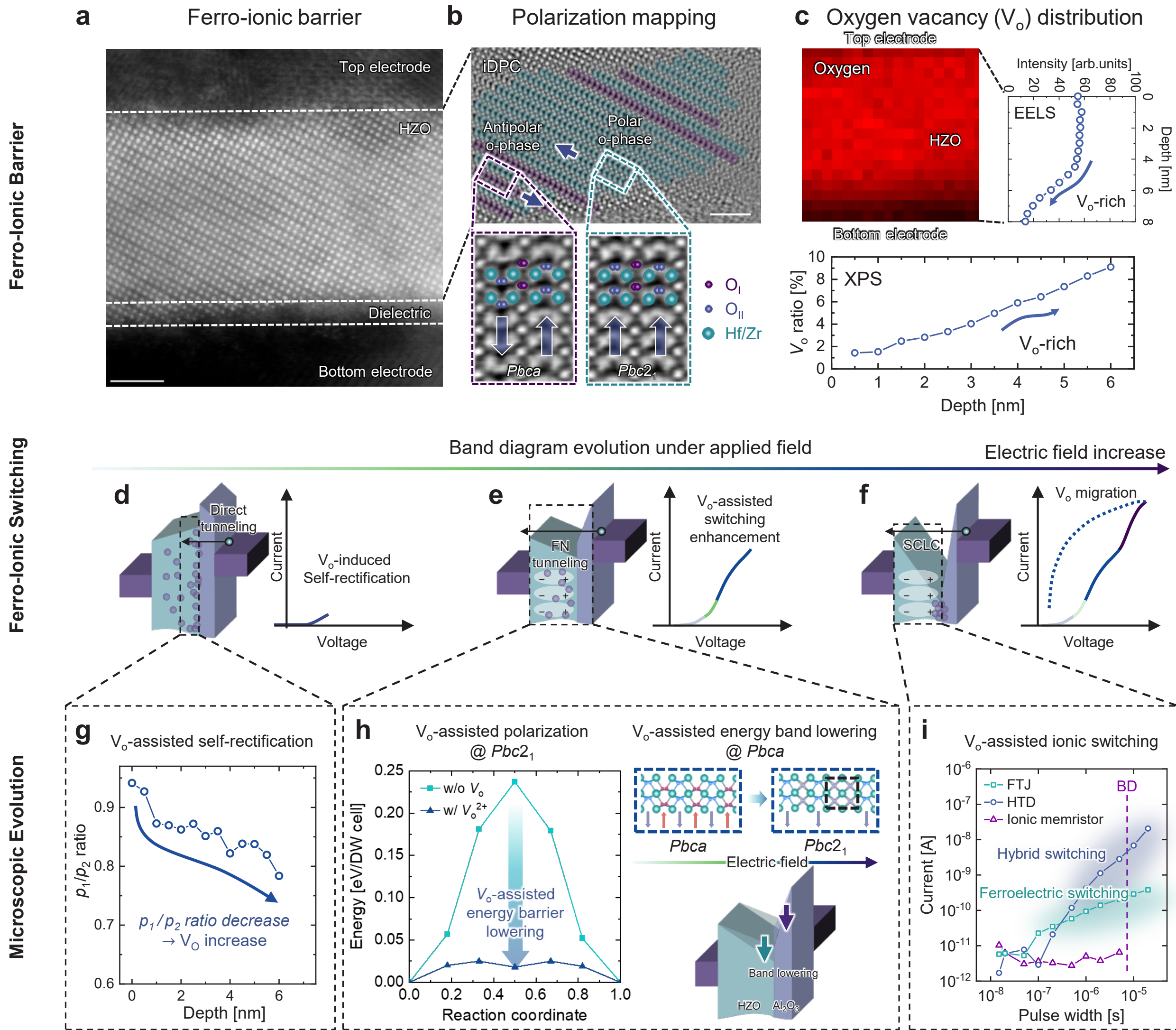
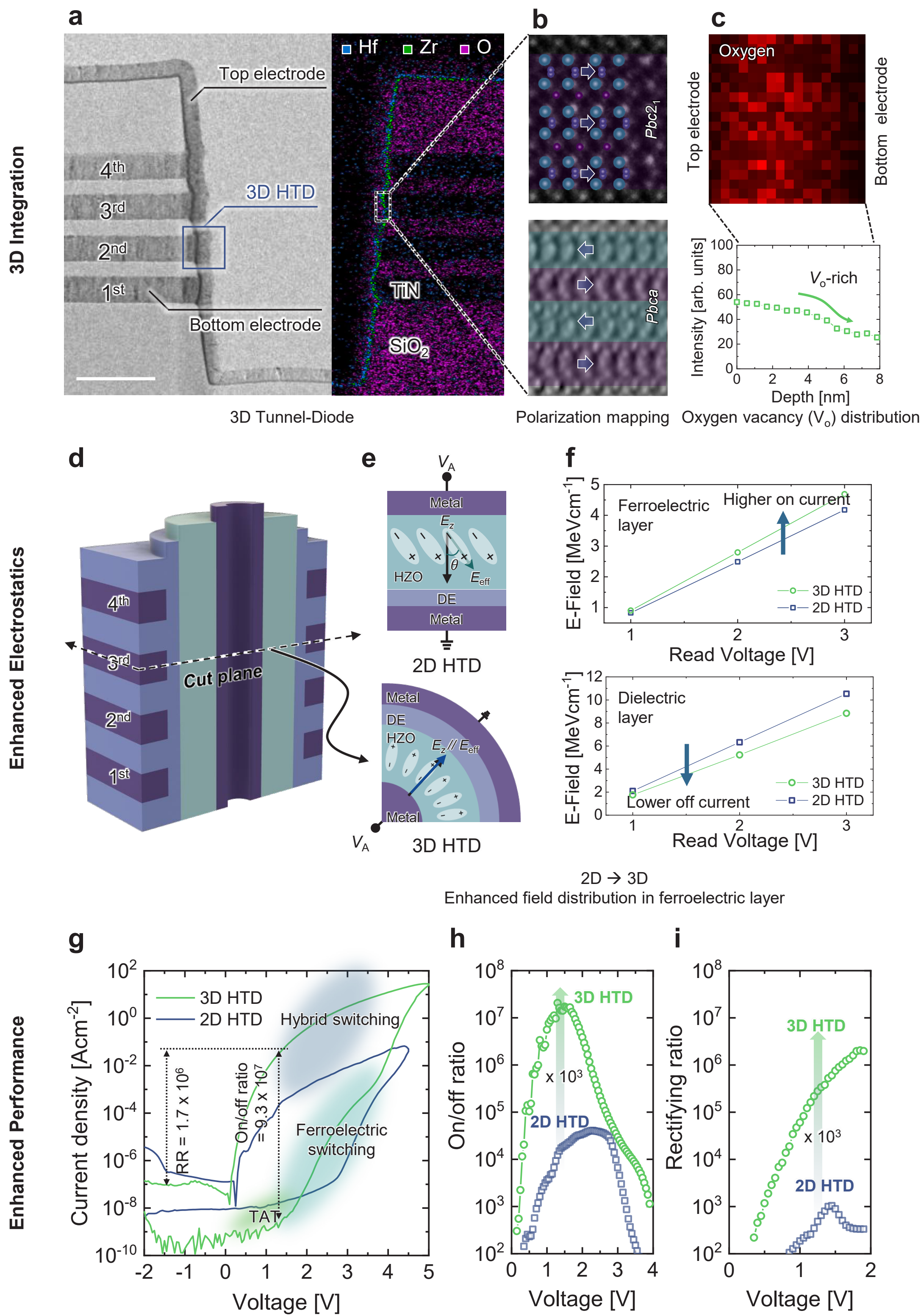
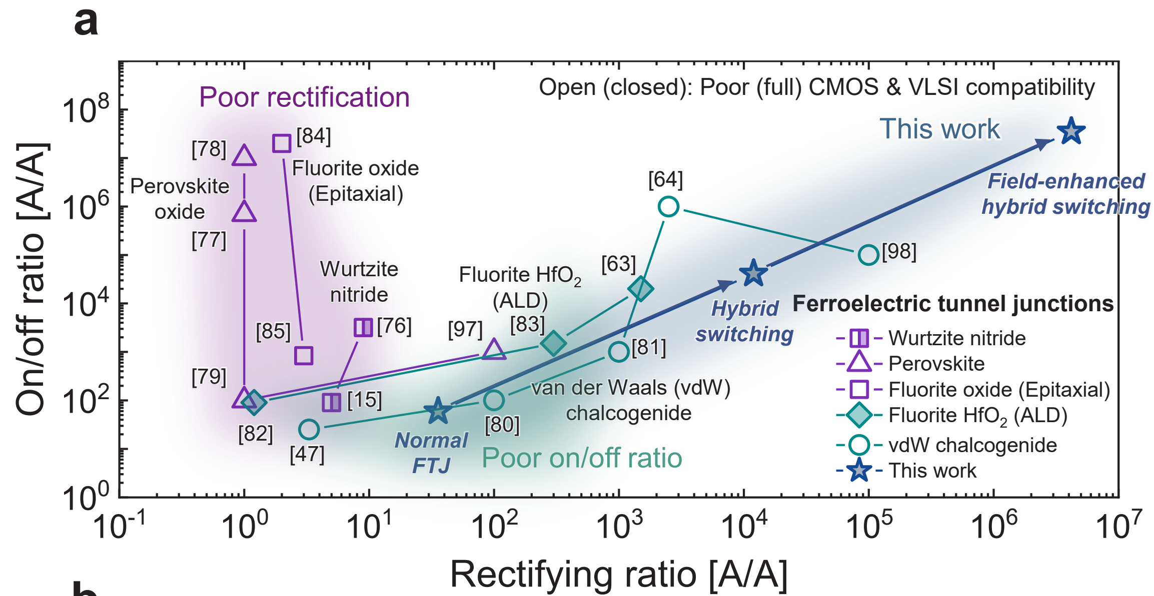
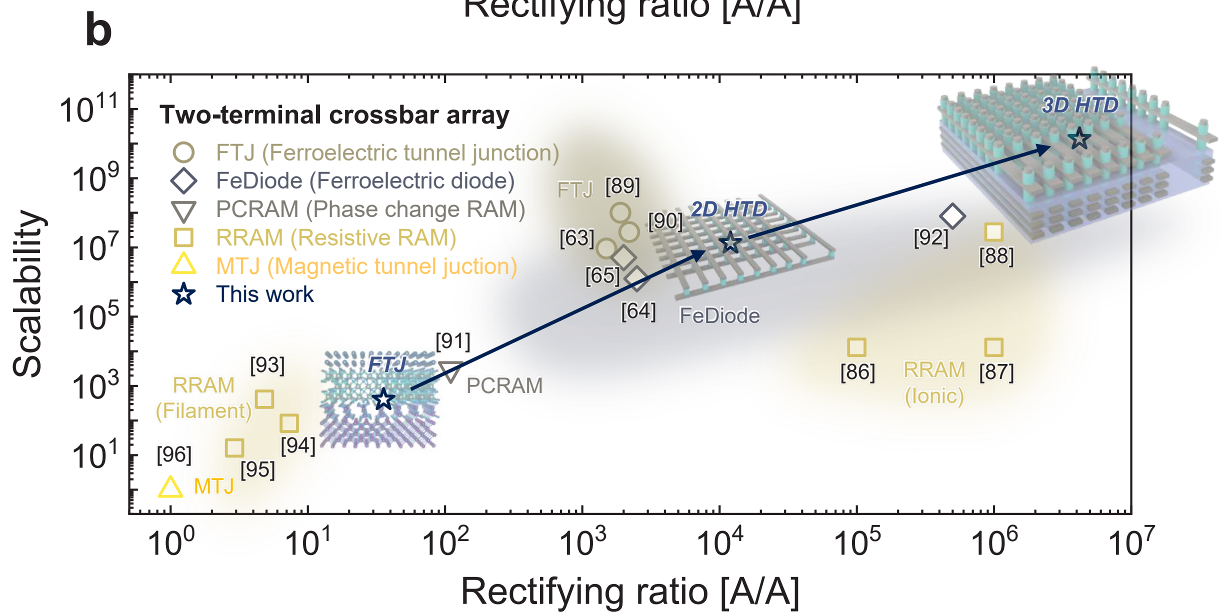


a
Ferro-ionic barrier
Top electrode
HZO
Dielectric
Bottom electrode
b
Polarization mapping
iDPC
Antipolar o-phase
Polar o-phase
Pbca
Pbc2$_1$
O$_I$
O$_{II}$
Hf/Zr
c
Oxygen vacancy (V$_o$) distribution
Top electrode
Oxygen
HZO
Bottom electrode
Intensity [arb.units]
EELS
V$_o$-rich
Depth [nm]
XPS
V$_o$ ratio [%]
Depth [nm]
Ferro-Ionic Barrier
Band diagram evolution under applied field
Electric field increase
Ferro-Ionic Switching
d
Direct tunneling
V$_o$-induced Self-rectification
Current
Voltage
e
FN tunneling
V$_o$-assisted switching enhancement
f
SCLC
V$_o$ migration
Microscopic Evolution
g
V$_o$-assisted self-rectification
p_1/p_2 ratio
p_1/p_2 ratio decrease → V$_O$ increase
Depth [nm]
h
V$_o$-assisted polarization @ Pbc2$_1$
w/o V$_o$
w/ V$_o^{2+}$
V$_o$-assisted energy barrier lowering
Energy [eV/DW cell]
Reaction coordinate
V$_o$-assisted energy band lowering @ Pbca
Pbca
Pbc2$_1$
Electric field
Band lowering
HZO
Al$_2$O$_3$
i
V$_o$-assisted ionic switching
FTJ
HTD
Ionic memristor
BD
Hybrid switching
Ferroelectric switching
Current [A]
Pulse width [s]



a
b
c
3D Integration
Top electrode
4th
3rd
2nd
1st
3D HTD
Bottom electrode
Hf
Zr
O
TiN
SiO2
Pbc21
Pbca
Oxygen
Top electrode
Bottom electrode
Intensity [arb. units]
Vo-rich
Depth [nm]
3D Tunnel-Diode
Polarization mapping
Oxygen vacancy (Vo) distribution
d
e
f
Enhanced Electrostatics
Cut plane
VA
Metal
Ez
HZO
θ
Eeff
DE
2D HTD
Ez // Eeff
3D HTD
E-Field [MeVcm-1]
Ferroelectric layer
Higher on current
Read Voltage [V]
Dielectric layer
Lower off current
2D → 3D
Enhanced field distribution in ferroelectric layer
g
h
i
Enhanced Performance
Current density [Acm-2]
Hybrid switching
RR = 1.7 x 10^6
On/off ratio = 9.3 x 10^7
Ferroelectric switching
TAT
Voltage [V]
On/off ratio
x 10^3
Rectifying ratio


a
Poor rectification
Open (closed): Poor (full) CMOS & VLSI compatibility
This work
Field-enhanced hybrid switching
Hybrid switching
Normal FTJ
Poor on/off ratio
Perovskite oxide
Fluorite oxide (Epitaxial)
Wurtzite nitride
Fluorite HfO2 (ALD)
van der Waals (vdW) chalcogenide
Ferroelectric tunnel junctions
Wurtzite nitride
Perovskite
Fluorite oxide (Epitaxial)
Fluorite HfO2 (ALD)
vdW chalcogenide
This work
On/off ratio [A/A]
Rectifying ratio [A/A]


b
Two-terminal crossbar array
FTJ (Ferroelectric tunnel junction)
FeDiode (Ferroelectric diode)
PCRAM (Phase change RAM)
RRAM (Resistive RAM)
MTJ (Magnetic tunnel juction)
This work
3D HTD
2D HTD
FTJ
FeDiode
PCRAM
RRAM (Filament)
RRAM (Ionic)
MTJ
Scalability
Rectifying ratio [A/A]