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Review

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Model representation in amorphous metal oxide thin-film transistors: a critical review

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This review examines modeling methodologies for amorphous metal oxide thin-film transistors (a-MO TFTs). It covers underlying device physics, charge transport mechanisms including multiple trapping and release, surface potential, mobility, drain current, and capacitance models, alongside bias, temperature, and mechanical stress effects. Comparisons of compact models highlight trade-offs in accuracy, parameter extraction, and circuit-level validation. Future directions emphasize machine learning integration, unified multi-material frameworks, and strain-aware simulations.

Metal oxide thin-film transistors are a pivotal innovation in the development of flexible displays, transparent electronics, and large-area electronic applications[1–3]. The capacity to manufacture these transistors at reduced temperatures facilitates their integration onto flexible and unconventional substrates. Comprehending these devices, particularly using advanced modeling techniques, is crucial for precisely delineating their complex operational physics and enabling device tuning for improved performance.

These devices possess distinctive characteristics, including high carrier mobility, optical transparency, and remarkable reliability in diverse environmental conditions. These features are most effectively harnessed when accurate models are used to forecast device performance and guide experimental initiative[4,5]. The advancement of diverse modeling methodologies, such as sophisticated numerical simulations that incorporate the physics of amorphous MO TFTs, has profoundly impacted device performance and reliability. These simulations consider defect state distributions, carrier transport mechanisms, band tail states, and gate dielectric interface phenomena, enabling precise optimization of electrical characteristics, including threshold voltage stability, subthreshold swing, field-effect mobility, and bias stress-induced instability[6,7]. This advancement rendered modeling an essential instrument in creating MO TFTs by broadening the scope of electronic device design and functionality.

Conventionally, device modeling requires the setup of the semiconductor model describing carrier transport and electronic states from fundamental device physics[8,9]. It incorporates material constants and structural parameters to accurately replicate the device's electrical characteristics. In Si devices, well-established carrier transport and electronic states are the major determinants of electrical characteristics[10–13]. In contrast, MO TFTs, such as a-IGZO and a-ITZO TFTs, rely on proper understanding of the carrier transport and electronic states of the channel material, while mobility and density of states (DOS) of sub-gap states are needed to incorporate into the device model to make an appropriate prediction of device performance[14].

In TFT development, the semiconductor device model acts as a vital bridge between manufacturing processes and circuit design optimization. While the integrated circuit designer uses simulation tools like Cadence, SPICE, and PHILIPAC, the foundations of these simulation tools depend upon the accurate models of each separate device[15–20]. Since ICs are composed of millions of transistors, running a complete transistor model for each device would lead to very expensive computational demand and also risk system-level divergence. In return, for balancing computational efficiency against accuracy, the device model must capture the physics of the device reliably with reasonable computational feasibility[21]. An accurate compact model helps in this regard with a simple yet precise representation of device behavior. In addition, it enables the efficient simulation of circuits and systems, provides a facility for parameter extraction, and supports designs for future technology nodes[22,23].

In the context of compact modeling, several approaches have been suggested for understanding physical characteristics of Si-based TFTs, including a semiempirical approach, effective medium approach (EMA), charge sheet model, surface-potential-based model, and generation–recombination model[24–28]. New compact modeling frameworks employing these approaches have been formulated for MO TFTs[29–32]. Most existing compact models can broadly be divided into charge-oriented and surface potential-driven formulations[33,34]. Between the two modeling approaches, surface-potential-based models provide a more precise description of the transistor operation without recourse to smooth functions[35]. They are indeed more accurate, have a sounder physical basis, and can easily be simplified to either a charge-based or threshold voltage model[36].

Accurate compact models based on physical characteristics are needed to simulate MO TFTs in digital and analog circuits. To precisely capture the

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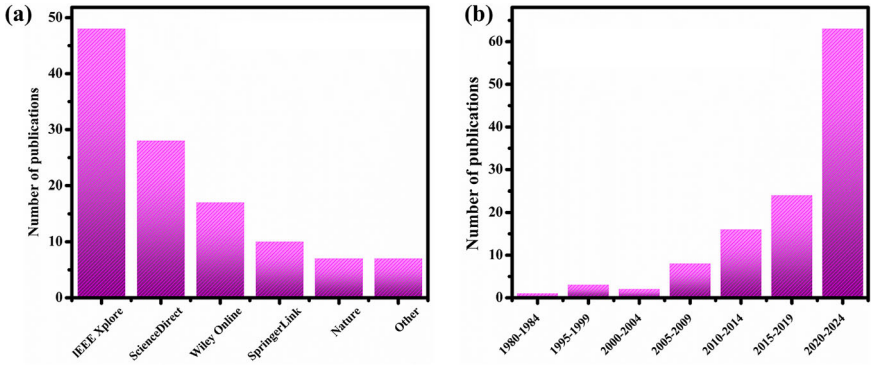

Fig. 1 | Publication trends in academic research. **a** Distribution of publications across different data bases. **b** Number of publications over the years, grouped by 5-year intervals. Bars represent the number of publications.

device behavior, the model should provide a consistent and symmetrical representation of the TFT structure and remain fully analytical, and be analytical, with no complex integrals or differentials. In addition, it has to be as simple as possible, derivable, and parameterizable with easy-to-characterize parameters. Moreover, it needs to be flexible enough to accommodate physical changes in device parameters, physically justified, and coherent with other MO TFT models. Besides, it must be tunable to fit the measured data, even in the presence of uncertainties[36].

Recently, machine learning (ML) techniques have been found to be a useful addition to traditional physics-based methods. Artificial neural networks (ANNs) have been used to automate the extraction of important parameters like field-effect mobility and threshold voltage from transfer characteristics. Recent research by Xie et al. illustrates a Bayesian-optimized artificial neural network integrated with genetic algorithms for the compact modeling of MO TFTs[37]. This method yields reliable predictions of drain current by incorporation of small-signal parameters through derivative-enhanced loss functions. Likewise, for a-IGZO TFTs, ML interatomic potentials have yielded atomistic insights into defect dynamics for reliability simulations[38]. These data-driven strategies pave the way for ML-enhanced frameworks in multiscale modeling. However, further investigations are required for the consistency of ML approaches with physical models and their integration with established tools like Verilog-A.

Furthermore, as TFTs with the semiconductor channel composed of multiple distinct metal oxide materials are becoming more common, researchers are facing new challenges with uneven compositions and dynamic interface behavior. Improvement is required for existing models so that these models can make predictions for all these varying systems. Improved multiscale reliability simulations could link atomic-level defect analysis to the whole device, giving us a clearer picture of bias-induced failures. And for flexible electronics, mechanical-electrical coupling models are crucial to analyze strain effects on mobility. Developing strain-aware models can reduce degradation in deformable devices.

Ultimately, the utility of compact models for emerging applications depends on carefully balancing simulation accuracy with computational cost. A balance between accuracy and computational efficiency will ensure faster simulations without sacrificing reliability, physical relevance, or scalability across different technologies. In addition, advancements in display and electronics applications impose a stringent requirement for precise and efficient compact TFT models. Therefore, advanced techniques are required to capture MO TFT behavior for different present and future applications.

This extensive review aims to elucidate the key mechanisms that govern the operation of amorphous MO TFTs, while concurrently highlighting prospective directions for future studies and applications in this critical area. Motivated by recent achievements, the present manuscript presents a detailed analysis concerning modeling methodologies relevant to amorphous MO TFTs. Figure 1a presents the distribution of published research articles, sourced from databases such as IEEE Xplore, Nature, ScienceDirect, and so on, and used to support this review. Figure 1b shows relevant publications output to date in the field of amorphous MO TFTs modeling for the last forty years.

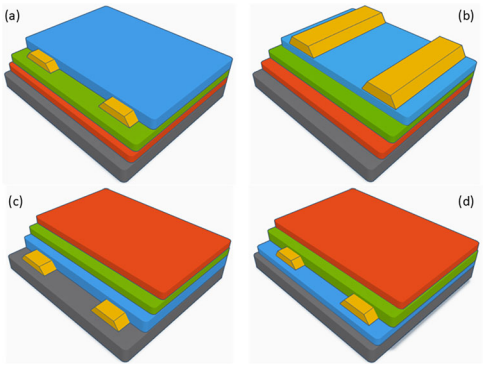

Fig. 2 | 3D cross-sectional schematics of common thin-film transistor (TFT) configurations. **a** Bottom-Gate Bottom-Contact, **b** Bottom-Gate Top-Contact, **c** Top-Gate Bottom-Contact, and **d** Top-Gate Top-Contact. Each structure highlights key layers, including the substrate, gate dielectric, semiconductor, gate electrode, and source/drain electrodes. The colors to the transistor components as follows: gray for Substrate, green for Gate Dielectric, blue for Semiconductor, red for Gate Electrode, and yellow for Source/Drain Electrode.

In this review, "Underlying physics of metal oxide TFT operation" discusses device physics of the amorphous MO TFTs, focusing on their unique electronic architecture and how several challenges arise because of its intrinsic disorder. In "Modeling of metal oxide TFTs," it concerns charge-transport mechanisms with an emphasis on the influence of traps, percolation pathways, and the amorphous material nature on carrier mobility. "Comparison of compact models for metal oxide TFTs" describes the modeling of the surface potential, mobility, and drain current, jointly with charge and capacitance modeling; an in-depth review of the strong and weak aspects of the different models is also provided. "Modeling of stress-induced effects: bias and mechanical influences on device reliability" models the bias and temperature-induced stress, focusing on the implications on device reliability. The most important conclusions of this overview are summarized in "Models including temperature effects," together with the directions for further research toward better stability and efficiency of a-MO TFTs.

Underlying physics of metal oxide TFT operation

Metal oxide TFTs demonstrate distinctive electronic characteristics owing to their wide band gaps and ability to facilitate efficient electron mobility when suitably doped. The typical architecture of MO TFTs comprises a semiconductor layer sandwiched between source/drain electrodes and a gate dielectric layer, as illustrated in Fig. 2.

The operating principles of these TFTs are quite similar to conventional MOSFETs. Transfer characteristics show the off-state, threshold, and saturation regions according to the controlling variable, the gate voltage (V_G). When gate voltage is less than threshold voltage (V_{th}) i.e., $V_G < V_{th}$, the device is not conductive; once $V_G > V_{th}$, electron accumulation at the

semiconductor-dielectric interface allows the conduction channel to be formed and improves the current. The device reaches saturation, which results in a stabilized drain current (I_D) at elevated V_G values.

Electron mobility in MO TFTs is generally superior to that in amorphous silicon TFTs, owing to the more ordered atomic structure in metal oxides, which facilitates smoother potential energy settings for carrier transport[39,40]. Nonetheless, effective mobility can still fluctuate significantly, affected by the film's deposition conditions, the ambient oxygen concentration during sintering, and the post-processing temperature[41,42]. These characteristics can cause alterations in the stoichiometry and microstructural arrangement of the oxide layer, therefore, influencing the magnitude and depth of the potential wells created by the trap states.

Carrier transport mechanisms in metal oxide TFTs are considerably influenced by defects in the oxide semiconductor layer. These defects frequently present as trap states that can entrap free carriers, significantly impacting carrier mobility and, subsequently, device performance. The density and distribution of these traps depend on the crystalline quality of the material and the manufacturing procedures, such as deposition methods and post-deposition annealing[43–47]. IGZO TFTs generally display fewer trap states in the bandgap relative to solely zinc oxide or tin oxide-based TFTs, owing to their composite material structure, which enhances orbital overlap and diminishes the density of localized states that impede carrier mobility[39,48,49].

Furthermore, the performance parameters of metal oxide TFTs, including mobility (μ), on/off ratio, threshold voltage (V_{th}), and subthreshold swing (SS), are essential for evaluating their appropriateness for particular applications. For high-speed electronic equipment, high mobility is essential, while a high on/off ratio guarantees power efficiency and signal integrity[50,51]. The stability of the threshold voltage is critical for reliable device performance, highlighting the necessity of comprehending and managing the previously described trap dynamics and material interfaces[52]. To provide a clearer comparison of typical performance benchmarks across different metal oxide TFT technologies, Table 1 summarizes the key electrical characteristics reported for various device structures, further illustrating how material and process choices impact the fundamental figures of merit.

Charge transport in amorphous metal oxide thin-film transistors (TFTs)

Charge transport in amorphous metal oxide TFTs is a complex phenomenon, since it depends both on the disordered structures of the materials and on the localized states within the bandgap. The electronic structure of the amorphous metal oxides differs markedly from that of their crystalline counterparts. In amorphous materials, without long-range order, energy states are continuously distributed instead of discrete bands. In these oxides, electrical conduction is enabled mainly by the overlap of metal cation s-orbitals, which are delocalized and exhibit minimal sensitivity to structural disorder. Such characteristics allow for relatively high electron mobility even in the amorphous state by allowing electrons to delocalize over these orbitals[39].

In amorphous metal oxides, the DOS exhibits exponential band tails that extend into the bandgap from both the conduction and valence bands, a consequence of structural disorder-induced variations in bond lengths and angles. These tail states play a very important role in charge transport, acting as trap states for charge carriers[53].

Charge transport in amorphous metal oxide TFTs involves several mechanisms that can operate simultaneously due to the absence of crystalline periodicity in the material. In the extended state, conduction occurs by means of charge carriers in extended states above the mobility edge and therefore suffers minimal effects of localization. In field-effect devices, carrier mobility within extended energy states is influenced by dynamic scattering mechanisms, particularly phonon-induced perturbations. As temperature increases, the amplitude of the phonon vibrations becomes larger; as a result, scattering increases, and mobility decreases. This temperature variation is a characteristic of band-like conduction, but can be modified because of disorder[54].

$$\mu(T) = \mu_0 T^{(-n)} \tag{1}$$

μ_0 is a pre-exponential factor, and n is the scattering exponent.

Below the mobility edge energy, the carriers are in localized states, and their motion is possible by hopping through localized states. The hopping conduction is a thermally activated process, wherein carriers gain enough thermal energy to jump to the next neighboring sites. Mott's variable range hopping model accounts for the conductivity variation with temperature in such disordered systems. In such a process, the hopping probability of a carrier is determined by the spatial separation as well as the energy offset between initial and final localized states[55].

$$\mu(T) = \mu_0 exp[-(T_0/T)^{(1/4)}] \tag{2}$$

where, σ_0 is a constant and T_0 is the characteristic Mott temperature.

Another critical mechanism is the multiple trapping and release (MTR) model, where charge carriers become trapped in localized states before being thermally activated into extended states, enabling their participation in conduction. The effective mobility here becomes a balance between the time carriers spend in extended states compared with the time spent trapped. A high density of states for traps can significantly lower mobility through an increase in the trapping probability[56].

$$\mu_{eff} = \mu_{band} \frac{n_c}{n_c + n_t} \tag{3}$$

where μ_{band} is the band mobility, n_c is the concentration of carriers in extended states, and n_t is the concentration of trapped carriers.

In TFTs, the effective field-induced mobility (μ_{FE}) represents a principal metric, indicating how effectively the gate voltage controls the channel conductance. The presence of trap states affects μ_{FE} due to the capture of carriers that reduces their number available for conduction. During the increase of the gate voltage, more trap states start occupying, and the free carrier concentration with mobility increases effectively. This dependence of

Table 1 | Electrical performance comparison of representative metal oxide semiconductors used in TFTs

Metal Oxide	μ_{FE} (cm²/Vs)	V_{th} (V)	On/Off Ratio	SS (mV/dec)	Band Gap (eV)	Proc. T (°C)	Stability
IGZO[139,140]	10–30	0.5–1.5	10^6–10^8	150–300	3.2–3.5	300–350	Good
ITZO[141–143]	20–60	−5 to 5	10^6–10^7	220–300	3.6–3.9	300–400	Moderate
IZO[144,145]	20–80	−15 to 10	10^6–10^7	100–500	3.2–3.8	300–350	Moderate
In_2O_3[5,146,147]	10–150	−10 to 0	10^5–10^6	80–300	3.0–3.75	200–350	Moderate
SnO_2[148,149]	0.5–150	1.5–2.5	10^4–10^7	70–350	3.6–4.0	200–400	Poor
ZnSnO[150–152]	0.5–20	−1 to 3	10^5–10^7	50–300	3.4–3.9	300–400	Moderate
ZnO[153,154]	1–30	−1 to 3	10^4–10^9	80–350	3.1–3.4	150–350	Poor

Values are based on commonly reported ranges in the literature.

gate voltage and temperature underlines the interplay between charge transport and occupation of trap states[57]. In TFTs, μ_{FE} is typically derived from the transfer characteristics by analyzing the relationship between gate voltage and drain current in the linear or saturation regime. In the linear regime:

$$I_D = \frac{W}{L}\mu_{FE}C_i\left(V_G - V_T - \frac{V_D}{2}\right)V_D \tag{4}$$

In the saturation regime:

$$I_D = \frac{W}{2L}\mu_{FE}C_i(V_G - V_{th}) \tag{5}$$

where I_D denotes the drain current, W and L represent the width and length of the transistor channel, C_i is the areal capacitance of the gate dielectric, V_G is the applied gate voltage, V_{th} is the threshold voltage, V_D is the voltage applied at the drain terminal.

The field-effect mobility is influenced by gate voltage and temperature, reflecting the occupancy of trap states:

$$\mu_{FE}(V_G, T) = \mu_o \exp\left(\frac{-E_a}{k_B T}\right) \times \left[1 - \exp(-\beta(V_G - V_{th}))\right] \tag{6}$$

where E_a is the activation energy, β is the fitting parameter for trap distribution, k_B is the Boltzmann constant, and T is the temperature.

Trap states within the bandgap as a result of structural defects, impurities, or compositional fluctuations contribute immensely to the charge transport by capturing the carriers and impeding their movement. These states can be modeled by exponential and Gaussian functions with a view to represent the tail and deep states, respectively. Knowledge of sub-gap DOS is essential for device characteristic modeling and prediction. Some techniques employed to probe these states are capacitance–voltage measurements and photothermal deflection spectroscopy[58]. The total carrier concentration (n) is obtained by integrating the product of the Fermi-Dirac distribution $f(E)$ and DOS:

$$n = \int_{-\infty}^{\infty} g(E)f(E)dE \tag{7}$$

Figure 3 depicts the visual representation of charge conduction in doped semiconductor materials in general. Almost all amorphous metal oxides have exhibited temperature-dependent conductivity displaying an Arrhenius-type behavior indicative of a thermally activated process. The associated activation energy decreases with higher gate voltage as the Fermi level shifts toward the conduction band edge, lowering the energy barrier for charge carrier excitation. This phenomenon thereby infers that overcoming

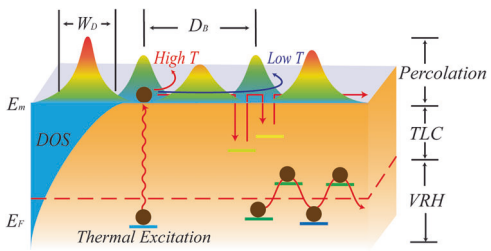

Fig. 3 | The diagram depicts the conduction mechanisms in doped semiconductors, i.e. The electron transport pathways in a doped semiconductor material, highlighting the transition between different conduction mechanisms based on temperature and energy levels. It shows percolation when the Fermi level (E_F) is above the mobility edge (E_m), thermal-limited conduction (TLC) at high temperatures when E_F is below E_m, and variable-range hopping (VRH) at lower temperatures when E_F remains below E_m.

of the trap barrier by thermal energy is essential in charge transport[59]. The temperature dependence of conductivity (σ) often shows Arrhenius behavior due to thermal activation over trap barriers:

$$\sigma(T) = \sigma_o \exp\left(-\frac{E_a}{k_T}\right) \tag{8}$$

The percolation theory provides a framework for viewing the transition from localized to extended conduction with increased carrier concentration. A critical carrier concentration, the percolation threshold, exists in a disordered system. For carrier concentrations below the threshold, the carriers are confined to isolated clusters, and transport occurs by hopping. For concentrations above the threshold, a continuous path opens up through the material, allowing extended state conduction. It serves to explain the nonlinear mobility dependence on carrier concentration and conductivity abrupt changes near the threshold[60].

Polar optical phonon scattering primarily impacts high-energy carriers by facilitating energy exchange with phonons, which reduces carrier velocity and effective mobility. This effect becomes more pronounced at higher temperatures, where increased phonon activity leads to stronger scattering and thus greater mobility degradation[61]. On the other hand, carrier velocity in TFTs, particularly under high electric fields, saturates due to optical phonon emission. Saturation velocity is affected by trap density and the distribution of carriers between trapped and extended states[62].

$$v = \frac{P_{MTR}P_{TRF}\mu_o E}{\left[1 + \left(\frac{\mu_o E}{v_{sato}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{9}$$

where v is the carrier velocity, P_{MTR} is the MTR factor, P_{TRF} is the transport reduction factor, μ_0 corresponds to the mobility under low electric fields, E is the electric field, v_{sato} denotes the carrier saturation velocity, whereas β is an empirical fitting parameter that is typically set to ≈2 for electron transport.

In more sophisticated models, incorporating transport theories on percolation conduction, thermally activated hopping conduction, and variable range hopping in a-IGZO TFTs yields more accurate modeling for various conditions. Such modeling enhances the capability to account for many interacting mechanisms, such as the interplay of charge carrier dynamics, disorder, and energy landscape toward comprehensiveness in understanding device performance[63].

Furthermore, recent studies have concentrated on the formulation of cohesive charge transport models that effectively incorporate various conduction mechanisms. These models account for the spatial and energetic distribution of localized states, the influence of electric field and temperature on carrier hopping, and the percolation thresholds. Utilizing these complete models enables the precise simulation of device features[61].

In the case of operational stability in amorphous metal oxide TFTs, it has been affected by various phenomena, including bias stress-induced threshold voltage shift. Long duration of gate bias can result in charge trapping either in the dielectric or at the semiconductor/dielectric interface, leading to progressive shifts in device characteristics. These shifts often involve models containing logarithmic functions or stretched exponentials that capture the kinetics of the filling and emptying of traps. Knowledge of such time-dependent behaviors is vital for the enhancement of reliability and lifespan in devices[64]. The time-dependent shift in threshold voltage (ΔV_{th}) can be described using a basic model as follows:

$$\Delta V_{th}(t) = A \ln\left(1 + \frac{t}{\tau}\right) \tag{10}$$

where A is a constant related to trap density, τ is a characteristic time constant.

Alternatively, a stretched exponential function captures dispersive kinetics:

$$\Delta V_{th}(t) = \Delta V_{th_o}\left[1 - \exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right)\right] \tag{11}$$

where β ($0 < \beta < 1$) indicates the degree of dispersion.

Among the most typical kinds of defects in metal oxide semiconductors, oxygen vacancies act like donor states due to the introduction of extra electrons in the vicinity of the conduction band. Electrical properties may be drastically altered by the substantial change in carrier concentration and mobility as a result of changes in the concentration of oxygen vacancies. Increased conductivity can take place at a moderate amount of oxygen vacancies; excess vacancies increase scattering and decrease mobility. Hence, for desired electrical properties, control over oxygen stoichiometry is highly crucial during material synthesis[65].

ML offers a transformative complement to conventional charge-transport models in a-MO TFTs. This is especially true for capturing the arbitrary nature of traps and percolation in disordered systems. By training on large datasets from ab initio simulations or experimental *I–V* curves, ML can predict defect distributions and carrier hopping dynamics at a lower computational cost than methods that only rely on physics[66]. Recent research has employed ML interatomic potentials to clarify hydrogen diffusion in a-IGZO[38]. This approach demonstrates the impact of defect migration on trap states and mobility under bias stress. These advancements deal with key problems in scalability and interpretability. However, integrating ML with existing transport theories is still an open area for research, which could accelerate the process of designing stable and high-mobility devices.

Modeling of metal oxide TFTs

General modeling efforts are usually the preliminary steps in attempts to understand the dynamics in improving metal oxide thin-film transistor performance. Efforts like these are essential in simulating the behavior of TFTs under various operational conditions, thus availing proper insights necessary to guide device optimization and application. While such modeling is perhaps not as essential as direct experimental methods that deal with the discontinuity and anomalies in real-world material, it is a basic framework that conditions further improvement. Now the review proceeds to go into the specifics of surface potential-based modeling, which has provided more detailed examination of electrostatics in the device structure.

Surface potential model

For amorphous oxide semiconductors like a-IGZO, the overall carrier density $n(z)$ is governed by the sum of carrier concentration in extended and localized states[67,68].

$$n(z) = \int_{-\infty}^{\infty} \frac{g(E)}{1 + \exp\left(\frac{E - E_F(z)}{k_B T}\right)} dE \tag{12}$$

$$g(E) = \begin{cases} g_c\sqrt{E + \left(\frac{N_t}{k_B T_0 g_c}\right)^2} & E > 0 \\ \frac{N_t}{k_B T_0}\exp\left(\frac{E}{k_B T_0}\right) & E < 0 \end{cases} \tag{13}$$

where N_t represents the overall density of localized trap states, g_c is reported as 1.4×10^{21} cm^{-3} $eV^{-3/2}$ (for a-IGZO), T_0 is the characteristic slope temperature describing the exponential tail of the density of states and E_F (z) indicates the position-dependent quasi-Fermi energy level.

A state-of-the-art methodology[69] has been able to simplify the modeling of carrier behavior without necessarily having to resort to usual iterative solutions[70–72] whenever there is a change in electrical conditions. This advancement leverages the latest computational techniques or an enhanced understanding of the material properties that make those predictions of carrier dynamics increasingly effective.

Besides, the important role of the Poisson equation in understanding the electrostatic potentials of the semiconductor was addressed by the separation of variables. The result combines the effects of extended and localized states through a modified Schroder series, correcting for unrepresented extended state contributions. The series refines the solution, which previously[73] only included one type of carrier, carrying nuances not accessible within the realm of the standard modeling approaches:

$$\alpha^2 = k_{1(2)}^2 q_{1(2)}^2 - A_0 e^{x_{1(2)} - x_n} - B_0 e^{t(x_{1(2)} - x_n)} \tag{14}$$

$$\alpha^2 = t_{IGZO}^2\left(\frac{\partial x}{\partial z}\right)^2 - A_0 e^{(x - x_n)} - B_0 e^{t(x - x_n)} \tag{15}$$

Equation (14) defines the normalized coupling charge (α_2), which integrates both structural (k_1), dynamic (B_0) parameters and extended state contribution (A_0). Equation (15) links this to the vertical electric field gradient $\partial x/\partial z$, while Eqs. (16)–(18) provide iterative corrections for the surface potentials φ_{s1} and φ_{s2}[63].

$$x_{11} = x_1 - \frac{F(x_1)}{F'(x_1) - \frac{F(x_1)}{F\prime(x_1)}\frac{F''(x_1)}{2}} \tag{16}$$

$$\varphi_{s1} = \phi_{T0}\left(x_{11} - \frac{F(x_{11})}{F\prime(x_{11}) - \frac{F(x_{11})}{F\prime(x_{11})}\frac{F''(x_{11})}{2}}\right) \tag{17}$$

$$\varphi_{s2} = \phi_{T0}(x_{g2} - q_2) \tag{18}$$

Figure 4 shows the comparison of the analytical solution for this model with the numerical results for potentials on the bottom surfaces, exhibiting a percentage error less than 0.01% constantly. Figure 4 also shows the distribution of the electrostatic potential along the vertical direction of the semiconducting channel for various TG biases and active layer thicknesses.

Mobility model

In the amorphous phase of IGZO, these sub-gap localized states are given by the fluctuations of the conduction band; hence, potential barriers arise above the conduction band minima (E_m). As represented in Fig. 3 in the previous

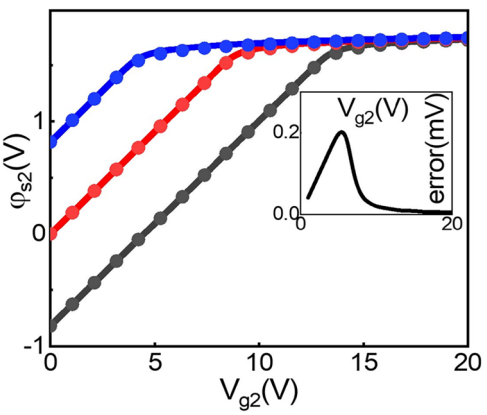

Fig. 4 | Comparison of analytical solutions and numerical results for the surface potential (ϕ_s) across varying top-gate voltages (V_{g2}). The data is presented for three conditions of the back-gate voltage (V_{g1}): −1V (red), 0 V (grey), and 1 V (blue). The inset graph displays the error analysis, emphasizing the precision of the model at different V_{g2} values[63]. Points represent numerical results; lines represent analytical model solutions. Gray: $V_{g1} = -1$ V; red: $V_{g1} = 0$ V; blue: $V_{g1} = 1$ V. Inset: Error (mV) versus V_{g2} (V).

section, at low gate voltages, the Fermi level (E_F) lies in the localized tail states, causing electrons to become trapped. The electrons might get thermally excited and set mobile. As a result, TCL is dominant for a wider temperature range, while VRH dominates at lower temperatures because of reduced carrier activation. In the case of high gate voltage, E_F enters the conduction band, and hence conduction occurs via percolation. At high temperatures, electrons prefer to hop through the shorter path with a higher barrier due to their higher thermal energy and occupation of the localized states. It means that they like to take longer paths with low barriers at low temperatures, as shown in Fig. 3. Thus, the carrier transport in IGZO involves both the trapped carriers in the localized states and free electrons in the extended states.

The temperature-dependent mobility model for amorphous metal oxide TFTs can be described by three dominant transport mechanisms, namely VH, percolation conduction, and TLC, which operate under different gate voltage regimes and temperature conditions[74].

$$\mu_{TLC} = \mu_b^* A^* (V_{g1} - V_{FB1} + V_{g2} - V_{FB2})^{2(T_0/T-1)} \quad (19)$$

$$\mu_{PERC} = \mu_b^* B^* (V_{g1} - V_{P1} + V_{g2} - V_{P2})^{4[(D_B - W_B)/D_B]} \quad (20)$$

$$\mu_{VRH} = \mu_o C^* exp\left(\left(\frac{T_1}{T}\right)^{1/4}\right)(V_{g1} - V_{T1} + V_{g2} - V_{T2})^{\gamma} \quad (21)$$

Trap density (N_t) and reference temperature (T_0) are functions of the coefficients A^*, B^*, and C^*. In this case, μ_b^* is the band mobility, normalized by the percolation factor according to the potential barrier height and its variance, and μ_0 is the reference mobility for hopping conduction. The $V_{P1(2)}$ is the specific gate voltage at which the transitions between percolation and trap-limited conduction regimes takes place, and it occurs when the Fermi level (E_F) coincides with the mobility edge (E_m). Furthermore, in the above equations, T_1 is the characteristic temperature, and while the ratio of spatial coherence of potential barriers is calculated from the formula $(D_B–W_B)/D_B$. Further, the exponent γ is related with the density of tail states. In all cases, the carrier mobility exhibits a universal power-law dependence on the gate voltage.

Drain current model

Foundational drift-diffusion equations specifically designed to describe transport in disordered amorphous materials ruled by trap states gave rise to early physical models of drain current in TFTs[75,76]. Using exponential DOS distributions to explain localized tail states, Shur and Hack's pioneering 1980s work laid the foundation by characterizing mobility via several trap-and-release (MTR) processes[8]. Building on this framework, subsequent research presented improved models including more realistic DOS profiles, such as the combined exponential-Gaussian distributions suggested by Germs et al., which offered a deeper understanding of how localized states affected conduction[77,78]. Hernández-Barrios et al. created analytical expressions explicitly linking gate-voltage-dependent mobility and effective carrier densities to overcome limitations connected to the naive assumptions of early models, so accurately capturing carrier dynamics in a-IGZO channels[79,80]. Estrada et al.'s additional improvements correctly described velocity saturation effects at high electric fields in MO TFTs by combining percolation conduction and polar optical phonon scattering influences[81]. These physics-based analytical developments taken together greatly increased the knowledge of charge transport phenomena in amorphous oxide semiconductors, therefore improving the accuracy of drain current modelling.

By introducing empirical modifications designed particularly for oxide semiconductor channels, early compact drain current models for metal oxide TFTs adapted classical MOSFET equations, including the alpha-power law and fundamental charge-based approximations[82]. Initial attempts, represented by the Rensselaer Polytechnic Institute (RPI) model, concentrated on simplifying the mobility term using gate-voltage-dependent parameterization to effectively capture conduction properties[83]. Building on RPI's method, a more advanced model increased computational efficiency and broadened practical utility by a unified charge-based formulation relevant over several operating regimes, therefore simplifying drain current equations[84]. Later, modifications explicitly parameterizing mobility and threshold voltage empirically using compact equations greatly simplified model extraction and guaranteed consistency across several device geometries, therefore improving adaptability for circuit simulation[85–88]. These small modelling innovations collectively provided important tools allowing reliable and efficient integration of metal oxide TFTs into complicated circuit designs.

Rios et al. (2021) made a significant progress by solving the complete vertical one-dimensional Poisson equation without approximations, therefore addressing shortcomings of previous methods and producing a physically based compact drain current model for IGZO TFTs[89]. This captures the impact of asymmetric gate structures and semiconductor doping. Beginning with electrostatic analysis, the model derives the channel charge using gate, back-gate, and body contributions under constant mobility assuming lateral drift-dominated transport. The first long-channel drain current formula is

$$I'_{ds} = \frac{\mu W C_{OX}}{L}\left[V_g - V_o - \frac{1}{2}(\phi_{fd} + \phi_{fs})\right]\Delta\phi \quad (22)$$

where $\Delta\phi = \phi_{fd} - \phi_{fs}$ and V_0 encapsulates back-gate influence, body charge, and doping effects. Figure 5 demonstrates a strong correlation between the experimental data and the modeling results.

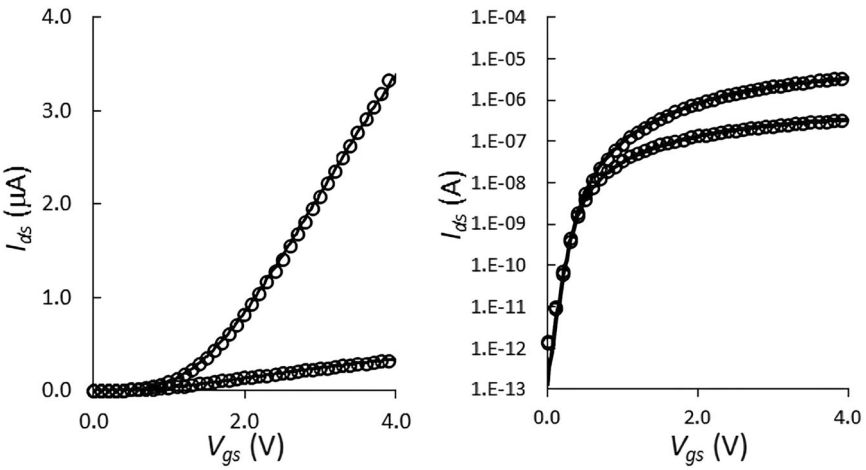

Fig. 5 | Comparison of measured and modeled transfer characteristics under low and high Vds (linear and log scale)[89]. Solid lines: Measured data; open circles: Model. Left panel: Linear scale I_{ds} (μA) vs V_{gs} (V) at V_{ds} = 0.1 V (lower curve) and 1.2 V (upper curve). Right panel: Logarithmic scale I_{ds} (A) vs V_{gs} (V) at V_{ds} = 0.1 V (lower curve) and 1.2 V (upper curve). Device dimensions: L/W = 367/63 nm.

To account for short-channel phenomena, the model introduces empirical corrections for velocity saturation and DIBL, and the final corrected drain current is given by

$$I_{ds} = I'_{ds} / (1 + (V_d - V_{dx}) / V_e) \quad (23)$$

where V_{dx} is the effective drain bias defined by a smoothing function and is an early voltage parameter controlling output conductance modulation. This formulation accurately reflects saturation behavior in nanoscale devices and preserves continuity across all bias regimes.

Among the main benefits are the model's relevance to doped and asymmetric structures, the lowering of grid complexity using a seven-point nonuniform discretization approach, and its integration readiness for circuit-level simulation. Unlike previous compact models that depend on threshold-voltage-based smoothing or symmetric assumptions, this work offers a completely electrostatics-consistent formulation flexible to current IGZO TFT architectures.

Charge and capacitance model

Charge and capacitance models developed for TFTs have greatly improved the accuracy of device simulation. Early models, which were based on DC characteristics, gave a fundamental understanding of AOS and enabled predictions for static conditions[23,90]. These have then been extended to advanced models, including a variety of gate configurations and operation regimes, and such improvements enhance predictive capability and reliability in circuit simulation[29,91,92]. Recent progress has come with models considering effective densities of charge carriers, accounting for both free and localized state contributions, that were able to predict behavior in all regimes of operation appropriately[90,93]. Capacitance models, instead, consider separately the presence of trapped charges as a function of frequency and further increase the accuracy of dynamic simulations in a wide frequency and temperature range[94]. Analytical expressions now also include structural factors like overlap capacitance in staggered bottom-gate TFTs and allow for the accurate dynamic circuit simulations with a good agreement in experiment[79].

Unified charge and capacitance models in amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) enable a smooth transition between subthreshold and above-threshold operations, which extends their applicability in circuit design[95,96]. These quantitative models are extremely useful in the development of technology related to TFTs, allowing for the simulation of circuits with high precision by accurately representing the charge distribution and capacitance effects within the devices[97,98]. In this way, integrating continuous charge-based models and their empirical verification approaches the realization of optimized electronic devices, enhancing performance and efficiency in advanced electronic systems.

Charge and capacitance models for metal oxide TFTs in compact modeling frameworks provide an accurate description of the electrostatics, bridging the theoretical modeling with practical applications. Zong et al. presented an analytical methodology utilizing multi-trapping/detrapping theories, which correlates channel charge behavior and gate capacitance for the purpose of ensuring consistent predictions in DC/AC characteristics of amorphous-IGZO TFTs[30].

The compact models developed for RFID applications focus on the needs of low power and high stability, optimized regarding charge and capacitance to reach the performance of the circuits[29]. These models succeeded in incorporating physical effects like charge trapping at interfaces and nonlinear capacitance behavior by means of charge control to manage the surface potential and define the capacitive response under different gate biases[29,91]. The connection between charge accumulation, mobility modulation, and capacitance changes provides valuable insights into applications such as RFID, display technologies, and low-power memory devices. These compact models are able to capture the subtlety of charge dynamics, thus allowing better device performance, reliability, and efficiency in integration for modern electronic systems[29].

Rios et al. developed a physically based compact model for IGZO transistors, capturing variations in charge distribution through a numerical solution of the Poisson equation, which is vital for accurate capacitance predictions under diverse conditions[89]. Similarly, Guo et al. focused on the finite-size corrections for charge transport regarding nanoscale devices by accounting for charge localization and quantum confinement effects with the aim of refining capacitance modeling in high-retention DRAM applications[99]. Compact models proposed by Zong et al. implement both transient and static charge dynamics through surface-potential calculations to ensure full coverage of capacitance variation over operational states[30].

A charge and capacitance model based on the drain current model discussed above introduced a model for the dual-gate a-IGZO TFTs using surface potential-based calculations, which is a precise description of charge distribution and has influences on channel charge modulation and capacitance behavior in different regimes, as shown in Fig. 6[63].

Q_g is derived while taking care of the effects caused by the charges accumulated in the semiconductor. Conventionally, models have problems when the potentials in the source and drain are equal because denominators become zero. In this regard, L'Hopital's rule is used to give meaningful results that capture how charges will distribute under balanced potential conditions.

$$Q_{g(V_{DS}=0)} = WL\left(\frac{G_{11} + G_{22}}{3C_{ox1}(A+B) + 3C_{ox2}(C+D)}\right) \quad (24)$$

$$G_{11} = 2C_{ox1}^2(A^2 + AB + B^2) + 3C_{ox1}C_{ox2}(A^*C + B^*D) \quad (25)$$

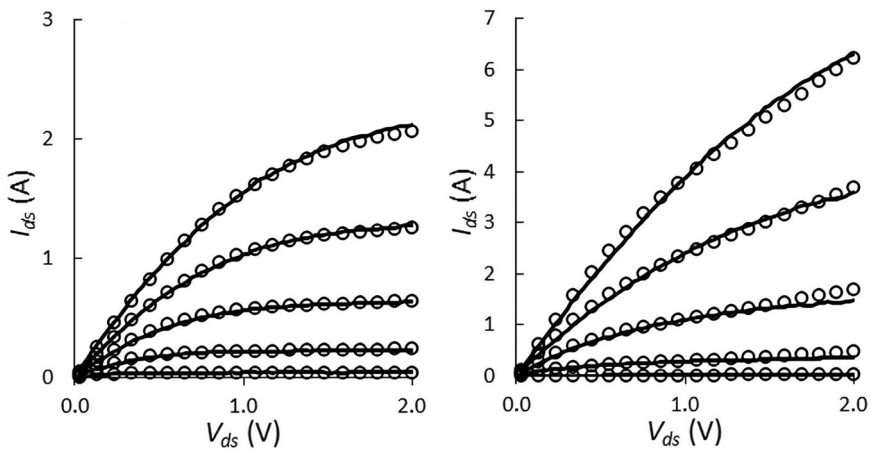

Fig. 6 | Comparison of drain current (I_{ds}) versus drain-source voltage (V_{ds}) for two metal oxide thin-film transistor devices: a longer channel ($L/W = 367/63$ nm, left) and a shorter channel ($L/W = 86/62$ nm, right). Solid lines denote experimental measurements, while symbols represent simulated model responses. The shorter-channel device exhibits a gradual transition into saturation, accurately captured by the model using a low early voltage ($V_e = 2$ V). Gate-source voltages (V_{gs}) were swept from 0.92 to 2.92 V (left) and 0.7–2.7 V (right) in 0.5 V increments[89]. Left panel: I_{ds} (A) vs V_{ds} (V) for L/W = 367/63 nm; curves from bottom to top: $V_{gs} = 0.92, 1.42, 1.92, 2.42, 2.92$ V (0.5 V steps). Right panel: I_{ds} (A) vs V_{ds} (V) for $L/W = 86/62$ nm; curves from bottom to top: $V_{gs} = 0.7, 1.2, 1.7, 2.2, 2.7$ V (0.5 V steps). Solid lines: Measured; open circles: Model.

$$G_{22} = 2C_{ox2}^2(C^2 + CD + D^2) + 3C_{ox1}C_{ox2}(A^*C + B^*D) \quad (26)$$

Charges at drain Q_d and source Q_s terminals are computed by means of the Ward's charge-partitioning scheme in order to guarantee that the device total charge is conserved. The model removes the singularities of the conventional approach by splitting the charge contributions into three parts: D_1, D_2, D_3 each related to different power terms of the voltages at the gates and further increases the accuracy of charge distribution predictions in a large biasing range.

$$Q_d = WL\left(\frac{2(D_1 + D_2 + D_3)}{(C_{ox1}(A^2 - B^2) + C_{ox2}(C^2 - D^2))^2}\right) \quad (27)$$

$$D_1 = \frac{1}{5}C_{ox1}^3(A^5 - B^5) + \frac{1}{5}C_{ox2}^3(C^5 - D^5) \quad (28)$$

$$D_2 = \frac{1}{12}C_{ox1}^2C_{ox2}(3A^5C - 3B^4D + 10A^3C^2 - 10B^3D^2) \quad (29)$$

$$D_3 = \frac{1}{12}C_{ox1}C_{ox2}^2(3AC^4 - 3BD^4 + 10A^2C^3 - 10B^2D^3) \quad (30)$$

$$Q_S = -Q_D - Q_G \quad (31)$$

The capacitance between any two terminals, to be represented as $C_{i,j}$, is obtained by the differentiation of the charge in one terminal with respect to the voltage on another.

$$C_{i,j} = \pm\frac{\partial Q_i}{\partial V_j} \quad (32)$$

This differential approach allows catching dynamic changes in capacitance due to voltage variations—an important issue while designing responsive IDG circuits. This model introduces the overlap capacitance, C_{total_G1S}, considering the physical overlap in device layout caused by the fabrication process. It is a very relevant point for a more realistic simulation of the gate capacitance in realistic geometries of devices.

$$C_{total\_G1S} = C_{G1S} + C_{G1So} \quad (33)$$

Figure 6 shows good agreement of experimental results with modeled capacitance at various channel lengths. In the Fig. 6, points show the experimental results while solid lines show the fitting results of the capacitance model.

ML-based modeling

In the future, device modeling for MO TFTs will use ML extensively to improve accuracy and efficiency. Particularly, ML can help with surface-potential calculations and mobility predictions that are affected by sub-gap states. Neural networks can automate the process of fitting compact models to experimental data[100]. ML can also consider nonlinear effects from traps and interfaces that can be a challenge for traditional analytical methods. A possible direction is the application of physics-informed neural networks for α-IGZO TFTs, facilitating neuromorphic applications by accurately simulating drain current and capacitance while accommodating variability in amorphous structures. Integrated AI-physics frameworks can enhance this capability to multiscale modeling, encompassing atomistic defect analysis to circuit-level optimization. These methods may speed up iterations in SPICE-compatible simulations, but it is still challenging to make sure that the results are physically understandable and can be applied to different materials. This shows that hybrid approaches are needed to make TFT designs more reliable.

Comparison of compact models for metal oxide TFTs

Comparisons between compact models for metal oxide TFTs should be done to enable a better design and optimization of electronic circuits, which will allow choosing the most accurate model of a particular application. Such a comparison enables the engineer to understand the trade-offs between computational efficiency and accuracy so that better performance of electronic devices could be ensured. Moreover, the comparison between the different models will drive innovation in model development and push the envelope on what is currently possible as regards electronic designs and fabrication techniques. Table 2 shows the comparison between various compact models for amorphous metal oxide TFTs.

Model accuracy

The compact model by Guo et al.[63] includes the Schroder method in order to calculate the surface potential and, therefore, has greater accuracy over a large operating regime range, considering percolation conduction, TLC, and VRH. In this model, the IDG a-IGZO TFT behavior is simulated through a unique approach whereby one equation for front and back surface potential is used with high precision, as mentioned in all regimes of operation. Experimental verification also verified this.

Modeling approach by Rios et al.[89] stands out for its prudent numerical discretization using a highly non-uniform grid of only seven points across the channel thickness. When benchmarked against exact solutions from grids with more than 100 nodes, the authors achieved errors below ~1%, a margin much tighter than typical compact-model tolerances and thus exemplary in balancing speed and accuracy. By carefully comparing their simulations to measured C–V and I–V data from fabricated CAAC-IGZO MOSFETs operating under linear, saturation, and subthreshold conditions with top- and back-gate biases varied independently, they validate this accuracy. The close overlap of simulation and experiment across all regimes

Table 2 | Comparison of compact models developed for amorphous metal oxide TFTs

Method	Accuracy	Validation	Param.	Strengths	Weaknesses	Ref.
Surface potential	Medium	Experimental	12	CAD-compatible	Limited	30
UMEM, semi-empirical	Medium	Experimental	15	Direct extraction	Heavy computation	31
Surface potential	High	Both	20	Physics-based	Narrow scope	101
Semi-empirical	Low	Both	13	User-friendly	Low accuracy	102
Charge-based surface	High	Both	25	CAD-compatible	DC-specific	84
Numerical-empirical	High	Experimental	23	Asymmetry-ready	Heavy computation	89
Surface potential	Very High	Both	14	Accurate	Needs extension	63
UMEM, TLC	High	Both	8	Oxide-centric	Narrow scope	81
Empirical	High	Both	12	Broad accuracy	Narrow scope	103

The models are evaluated based on accuracy, validation method, and parameter complexity. Key strengths and limitations are noted.

demonstrates the resilience of the model in capturing core electrostatics. The work introduces practical empirical corrections to extend fidelity to short-channel devices, including DIBL, ideality-factor shifts, carrier-velocity saturation, and Early-voltage effects. These corrections are parameter-based rather than purely physical, but they significantly improve agreement with short-channel characteristics and are openly discussed with their limitations. Lastly, a self-consistent computation of terminal charges enhances the usefulness of the model for high-performance circuit simulation and optimization by naturally incorporating coupling between the asymmetric gates and the semiconductor channel, which provides accurate capacitance prediction, which is essential for analog and RF design.

On the other hand, Yu et al.[84] and Zhao et al.[101] use less effective methods for compact modeling. Yu et al. developed a closed-form model that was used for discussing the influence of trapped charges for amorphous oxide semiconductor TFTs, combining solutions for surface potential with charge density calculations. However, the focus of the current model is more on the device reliability based on the interface trapped charges, something that was not specifically given in the model by Guo et al. A general compact model applicable for a-Si, AOS, and organic semiconductors for TFTs is presented by Zhao et al.[101]. The objective of this model is to be very general rather than highly specific and therefore might lose some accuracy for certain applications of AOS TFTs but is much more generally useful.

Parameter comparison and extraction

Among all the works related to parameter comparison and extraction, the work of Guo et al.[63], stands out because of its sophisticated handling of dual-gate configurations and its comprehensive approach to parameter extraction, which is deeply rooted in the physics of the device. It explicitly takes into consideration both the front and back surface potentials within one framework, something quite crucial in simulating the real, complex behavior of dual-gate TFTs under a variety of operating conditions.

Furthermore, the study by Rios et al.[89] separates physical parameters—fixed from fabrication and literature data, such as CAAC-IGZO film thickness, oxide EOTs, doping density, electron affinity, and band-gap—from empirical terms added to capture mobility roll-off and short-channel behavior. Extraction proceeds hierarchically: first lock the physical set; next fit mobility coefficients to low-V_D I–V data with a field-dependent expression tailored to IGZO; finally tune ideality factor (N_f), DIBL parameter (δ), carrier saturation velocity (υ_{sat}), and early voltage parameter (V_e) using devices that show DIBL and velocity saturation until simulated and measured I–V curves align. Validation on both long and short-channel TFTs, in addition to back-gate sweeps, shows tight agreement in C–V and I–V characteristics without geometry-specific retuning, proving the robustness of the extraction and yielding a compact model ready for reliable IGZO TFT circuit simulation.

Contrary to this, the rest of the models tend to focus on some specific aspects or conditions of behavior peculiar to TFT. For example, in the Sharma et al. model[102], much emphasis is placed on temperature-dependent characteristics that also employ fewer empirical parameters. This may render the model less sophisticated compared to that given by Guo et al. The one from Iñiguez et al[81]. covers everything from organic to amorphous oxide semiconductors, targeting the integration of these models in EDA. That might be very useful in practice but lacks specific parameter extraction for complex structures of a-IGZO TFTs. Also, the nature of validation adopted in the model of Guo et al. through comprehensive comparisons with experimental data is highly accurate and reliable. This aspect is quite important in TFTs applications, especially when the interaction between the two gates plays a significant role in device performance. Through the use of a model that can capture these interactions accurately, with thorough parameter extraction for validation, more reliable device simulations are realized, coupled with effective design for designers and researchers.

Evaluation criteria and consistency testing of compact models

The work by Guo et al.[63] demonstrates excellence in the criterion and continuous test of compact models, because there is a fitting verification and validation approach, inclusive of numerical simulations and experimental data across a variety of operational states, testifying to its great effectiveness in dual-gate configurations (as shown in Fig. 8). This model is rigorously tested to properly predict device behavior under real-world conditions, which is a critical factor in ensuring the reliable design and simulation of advanced electronic devices.

Compact model by Rios et al.[89] has been thoroughly examined and shown to be very consistent in a number of ways. It accurately replicates measured I–V and C–V curves, scales consistently across various device geometries, accounts for double-gate structure asymmetry, and reports runtime cost and numerical error. Especially noteworthy is the seven-point discretization of the vertical Poisson equation, which secures excellent numerical accuracy with minimal computational overhead. The authors also implement charge conservation analytically by explicitly integrating terminal charges, reinforcing the physical credibility of the model. Even so, the work omits several advanced consistency checks that are routine in industrial validation. It does not include derivative-based continuity metrics (such as higher-order transconductance), capacitance-reciprocity residue tests, Gummel-symmetry analyses, or comprehensive smoothness evaluations of derivatives. Incorporating these formal tests would markedly improve the readiness of the model for inclusion in Process Design Kits and high-fidelity circuit-simulation environments.

On the contrary, even though other compact models also reflect very important successes within their particular areas, they often deal with very restricted aspects or conditions of their thin-film transistor behavior. For instance, the Sharma et al.'s model is particularly pointed out for its temperature-dependent features and has been validated by circuit simulation, which justifies its practical usability within a wide temperature range[102]. Though it is not as specific to the challenges of complex TFT device configurations as the model from Guo et al.[63]. Similar limitations can be seen for surface-potential-based compact model by Yu et al.[103]. Also, the model by Iñiguez et al.[81], while broad in its applicability and integration to EDA tools, do not have the same depth of validation on complex configurations as that found in Guo et al. The compact models by Zong et al.[29]. and Moldovan et al.[31]. are validated against device measurements to ensure practical applicability but may lack the broader operational testing found in Guo et al.'s[63] approach.

Compact model validation at the circuit level

For verification at circuit level, compact models are coded in hardware description languages such as Verilog-A and added to electronic design automation (EDA) tools like Cadence, SPICE, or SmartSpice. Circuit simulations with multiple transistors verify computational efficiency, convergence stability, and predictive fidelity of these compact models under different bias, temperature, and scaling conditions.

Dynamic performance and power consumption evaluation is generally made with circuit level applicability of compact models on inverters and ring oscillators. The analytical surface-potential based model for a-IGZO TFTs is implemented in Verilog-A and utilized to simulate an inverter circuit[30]. The validation is done with voltage transfer curves (V_{in}-V_{out}) for different width-to-length ratios of the driver transistor. Furthermore, a five-stage ring oscillator is also simulated for further validation, and the oscillation frequency was plotted against the supply voltage for different driver geometries. However, this work lacks direct comparisons to experimental data from fabricated circuits.

On the other hand, some other works show more thorough validations that use real-world benchmarks. The universal compact DC model for TFTs was tested using SPICE simulations of a diode-load inverter with organic TFT parameters as a stand-in ref. 101. This model can be used with amorphous oxide semiconductors (AOS) and other technologies. The simulated voltage transfer characteristics (V_{TC}) matched up perfectly with measurements from real circuits, which showed that the model was reliable and that there were no problems with convergence. Similarly, a surface potential-based model for independent dual-gate (IDG) a-IGZO TFTs is

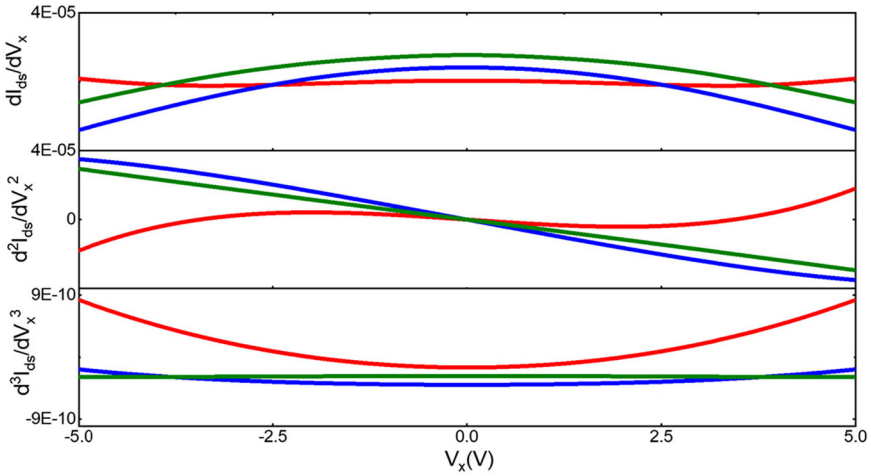

Fig. 7 | Gummel symmetry test showing the first, second, and third-order derivatives of the drain current (Id) with respect to the gate voltage (Vx) for different gate voltages ($V_{g1} = V_{g2} = 12$ V, 16 V, 20 V)[63]. Top panel: First-order dI_{ds}/dV_x (A/V). Middle panel: Second-order d^2I_{ds}/dV_x2 (A/V²). Bottom panel: Third-order d^3I_{ds}/dV_x3 (A/V³). Red: $V_{g1} = V_{g2} = 12$ V; blue: $V_{g1} = V_{g2} = 16$ V; green: $V_{g1} = V_{g2} = 20$ V.

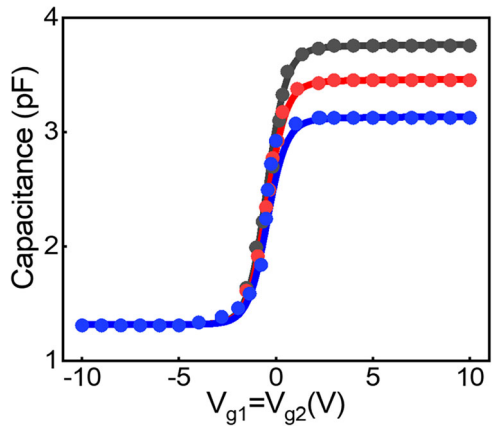

Fig. 8 | Total gate capacitance of the a-IGZO TFT as a function of gate voltage (Vg1 = Vg2) for different channel lengths ($L = 7$ µm, 8 µm, and 9 µm), with experimental data and model predictions shown for comparison[63]. Gray: $L = 9$ µm; red: $L = 8$ µm; blue: $L = 7$ µm. Points: Experimental (Expt.); solid lines: Model.

presented[63]. This model is written in Verilog-A and has been tested in a CAD environment. Simulations of a basic inverter (with one TFT acting as load and another as driver, and varying back-gate voltage) that matched experimental V_{TC} from manufactured devices under different bias conditions showed that the model could capture threshold compensation effects in circuit contexts.

Regarding temperature dependent models, an 11-stage ring oscillator was simulated utilizing Verilog-A and a compact model for a-IGZO TFTs, incorporating power-law mobility and Arrhenius-based temperature parameters[102]. Comparisons with measured oscillation frequencies from fabricated circuits over a 25 °C to 85 °C range showed that the predictive accuracy is good across operational regimes (cutoff, linear, saturation) and thermal variations. The results were within 8% of each other.

Analog validations provide supplementary evidence of the model's versatility beyond basic digital circuits. A review of compact solutions for AOS TFTs looked at Verilog-A implementations tested in a differential amplifier built on flexible substrates using MO systems[81]. The quasi-static AC model demonstrated its efficacy for printed electronics design by accurately replicating magnitude and phase responses up to 10 kHz, aligning well with experimental measurements.

Nonetheless, the robust demonstration of agreement at the device level, coupled with the absence of circuit-level validations for the compact models indicates potential avenues for future research[31,84,89,103]. To move this field forward, we need standardized benchmarks to connect modeling and real-world implementation.

Adaptations for short-channel effects in scaled a-MO TFTs

When channel lengths are less than 2 µm, short-channel effects (SCE) become very critical. A modeling approach has been explained earlier in this section. Empirical corrections were incorporated in Eq. 23 for velocity saturation and DIBL to address SCE. To get gradual saturation in nanoscale regimes, the ideal current is divided by a term that includes effective drain bias (V_{dx}) and early voltage (V_e). This is confirmed by experimental data as shown in Fig. 7, where SCE showed up as V_T roll-off, increased off-leakage, and higher mobility due to quasi-ballistic transport and less scattering[89,104].

Additional advancements include 2D analytical models that employ Green's function to analyze electrostatics in thin-film architectures[105]. These models effectively reduce SCE in TFTs that are compatible with back-end-of-line (BEOL) processes. In oxide TFTs, effective mobility increases with a decrease in channel length[106]. This is shown by TCAD simulations that take into account high-field effects and increase up to 36 cm²/V s in sub 2 µm channels. In self-aligned IGZO structures, degradation that depends on channel length intensifies below 2 µm. This stems from electrons diffusion from n^+ regions and the elevated trap density (N_{OT}). This causes ΔV_T to rise to 1.2 V (compared to 0.6 V in long channels)[107]. TCAD-based adjustments use lateral diffusion factors (≥0.15) and composition tuning, such as higher Ga content to suppress oxygen vacancies and decrease transient overshoot currents (ΔI_{OS}) by 0.4 V in $L = 0.5$ µm devices[108]. In $L = 50$ nm IGZO, low-frequency noise also changes from mobility fluctuations (1/µ) to carrier number fluctuations (1/n). This is fixed by improving the dielectric and optimizing the cation.

To reduce edge trapping, practical solutions include structural changes like lightly doped drain (LDD) (10^{18} cm^{-3} doping) or repositioning electrodes[107]. These changes are incorporated into hybrid TCAD-SPICE frameworks that manage scalable DOS distributions and ensure convergence in sub-micron regimes. Recent multiscale simulations have established a connection between defects such as oxygen vacancies and PBS in elevated-metal IGZO TFTs, integrating atomic-level insights with device-level SCE[109]. These changes make high-density applications possible, but there are still problems with experimental validation for extreme scales and maintaining symmetry under various bias conditions, so ongoing research is important.

Modeling of stress-induced effects: bias and mechanical influences on device reliability

When metal-based thin-film transistors (TFTs) are put under stress, their reliability suffers. The problem lies in the way they react to different types of stress. There are several key stress mechanisms at play, including positive gate bias stress (PBS), where the gate is subjected to a positive voltage,

potentially exacerbated by temperature[110,111]. Negative gate bias stress (NBS) and negative gate bias illumination stress (NBIS) also occur, with temperature effects in play, particularly in amorphous oxide semiconductor (AOS) TFTs[112,113]. Self-heating stress occurs when the gate and drain are subjected to high positive voltages, causing the TFT to overheat, while hot carrier stress is caused by high positive drain voltages[114,115]. In AOS TFTs, these stresses can cause two main effects: a threshold voltage shift, resulting in a parallel displacement of the transfer curve, and a distortion in the subthreshold slope, reflecting changes in the interface or bulk trap states.

Negative bias illumination stress (NBIS), negative bias temperature stress (NBTS), and negative bias stress (NBS) substantially influence the performance of metal oxide thin-film transistors (TFTs). The degradation mechanisms under these stresses principally involve the generation and trapping of defects in various regions of the TFT.

Both NBIS and NBTS induce threshold voltage alterations in a-IGZO TFTs. Under NBIS, light exposure facilitates the production of supplementary carriers (holes) that may be sequestered within the device architecture, particularly at the interface or inside the channel's bulk region, resulting in a negative shift in threshold voltage. For NBTS, similar effects arise from elevated temperature and electric field stresses, resulting in increased carrier generation and trapping, hence intensifying instability issues. Both stresses exhibit a correlation with the proliferation of defect states, including interface and bulk states, which substantially affect the electrical characteristics and reliability of the device[116,117]. Following equation is derived based on the generation, transport, and trapping of photo-generated holes under negative bias illumination stress (NBIS) conditions.

$$\Delta V_{on} = \frac{qP_S}{C_{ox}} = \underbrace{\frac{J_f}{C_{ox}}}_{\Delta V_\infty} \tau_S \left(1 - e^{-\frac{t}{\tau_S}}\right) \tag{34}$$

where ΔV_{on} is the shift in the turn-on voltage, P_S is the trapped hole concentration, C_{ox} is the gate insulator capacitance, J_f is the drift current density of holes, τ_S is the time constant of trapping at the interface, t is the stress duration.

The NBS conditions primarily involve the application of a negative gate bias in the absence of light or thermal stress. Like NBIS and NBTS, NBS affects the threshold voltage shift via defect formation and charge trapping. Depending upon the duration and intensity of the applied stress, various degradation behaviors can occur, including an early positive shift in threshold voltage, which may subsequently be followed by a more significant negative shift. The two-stage degradation process under NBS and NBIS indicates an inherent connection between the degradation mechanisms under various stress types[118,119].

The proposed unified model can be described by the two-stage degradation process during NBS (Negative Bias Stress), and NBIS in TFTs

$$\Delta V_{th} = \frac{2q\Delta N_{it}}{C_{ox}} \tag{35}$$

where ΔV_{th} is the threshold voltage shift, ΔN_{it} is the change in interface trap density and C_{ox} refers to the areal capacitance of the gate dielectric.

The degradation model for a-IGZO TFTs under NBS and NBIS indicates that the initial phase involves a slight positive shift resulting from shallow trap filling, but the subsequent, more significant phase entails negative shifts induced by the filling or formation of deeper trap states due to extended stress. This model demonstrates the intricate interactions between charge carriers and trap states under various bias and environmental conditions[118].

Both PBS and PBTS result in positive V_{th} shifts due to the carrier localization, typically electrons, in the gate insulation layer close to the channel/insulator interface. This trapping effect creates an additional electric field that opposes input voltage at the gate, thus requiring a higher threshold voltage to turn on the transistor. High gate voltage stress leads to a distinct trapping dynamic, where electrons from the channel are driven into the gate dielectric[116,117,120]. This impacts the immediate and long-term performance of the device.

Illumination introduces additional complexity to the stress dynamics. Under PBTIS, light exposure can contribute to the de-trapping of carriers or modify the charge trapping dynamics by photogeneration of carriers. This typically results in a more pronounced V_{th} shift under illumination as compared to PBS without light. Light can either exacerbate or mitigate the effects of bias stress, depending on the specific device and operational conditions[121]. Temperature plays a significant role in the kinetics of charge trapping and de-trapping. Higher temperatures typically accelerate these processes. It leads to a more rapid onset of stress effects but also faster recovery once the stress is removed. The following equation models the degradation of EMMO TFTs under Positive Bias Stress (PBS) and Positive Bias Illumination Stress (PBIS) and explains how threshold voltage shifts as a result of stress conditions

$$-\Delta V_{th} \propto t^n \exp\left(-\frac{E_a}{k_B T}\right) \exp\left(\frac{V_G}{V_o}\right) \tag{36}$$

where t is the stress time, E_a is the activation energy, V_0 is the characteristic voltage, n is the time exponent.

Quantitative models and simulations have been developed to focus on the distribution and dynamics of trapped charges within the gate dielectric and the impacts of these trapped charges on the electrical characteristics of the TFTs[120]. The threshold voltage shift model is given as follows

$$\Delta V_{th}(t) = \int_{x_2}^{x_1} \frac{qn_{tr}}{\varepsilon_o \varepsilon_{SiO_2} / (t_{ox} - x)} dx = \frac{qn_{tr}}{\varepsilon_o \varepsilon_{SiO_2}} (x_1 - x_2)\left(t_{ox} - \frac{x_1 + x_o}{2}\right) \tag{37}$$

where n_{tr} is the concentration of trapped electrons, ε_o is the permittivity of free space, ε_{SiO2} is the relative permittivity of the silicon dioxide layer, x_1 and x_2 are spatial boundaries of the region where the electrons are trapped and t_{ox} is the total thickness of the oxide layer. Figure 9 depicts the fitting of experimental results with the extracted values by using the above model. Implementing such advanced models can provide better device designs and operational strategies to enhance the stability and performance of amorphous metal oxide TFTs under various operational stresses.

The parallel shift in the transfer curve of AOS TFTs shows a positive V_{th} shift under PB(T)S and a negative V_{th} shift under NB(T)S and NBI(T)S[122–124]. Threshold voltage shifts are attributed primarily to carrier capture into sub-gap states at either the channel interface, AOS interface, or gate insulator interface. During the conditions of PB(T)S, electrons are captured, while the capture of photo-excited holes dominates for NBI(T)S[116,118,125]. The DOS model assumes such sub-gap states located at very shallow levels, about 0.2 eV from the conduction band, and/or deep levels at about 0.8 eV from the conduction band.

All of the other ions in the AOS may also contribute to such shifts; however, the mobility of hydrogen and oxygen ions in the AOS at room temperature is poor, and hence their effect can almost be neglected[126–128]. For NB(T)S, because there is no hole generation, the negative shift is caused by the ionized molecules[117]. The shifts may further be related to changes in the shape of the transfer curve through a rise in subthreshold slope S and an I_D hump[129]. These are accentuated in the case of self-heating stress, which likely acts as an accelerator of the change in DOS and related electrical properties[130].

Multi-channel MO TFTs[42] that mix materials like amorphous InGaZnSnO with thin InZnO layers have led to hybrid models that simulate charge transfer at the interface. It resulted in getting high mobilities while also making sure that stacked structures are reliable[131]. To demonstrate their reliability, a threshold voltage shift model has been proposed as follows

$$\Delta V_{th} = \left(1 - \exp(-[v \cdot t]^{-\beta}) \exp[\beta(E_{Th})/k_B T]\right) \tag{38}$$

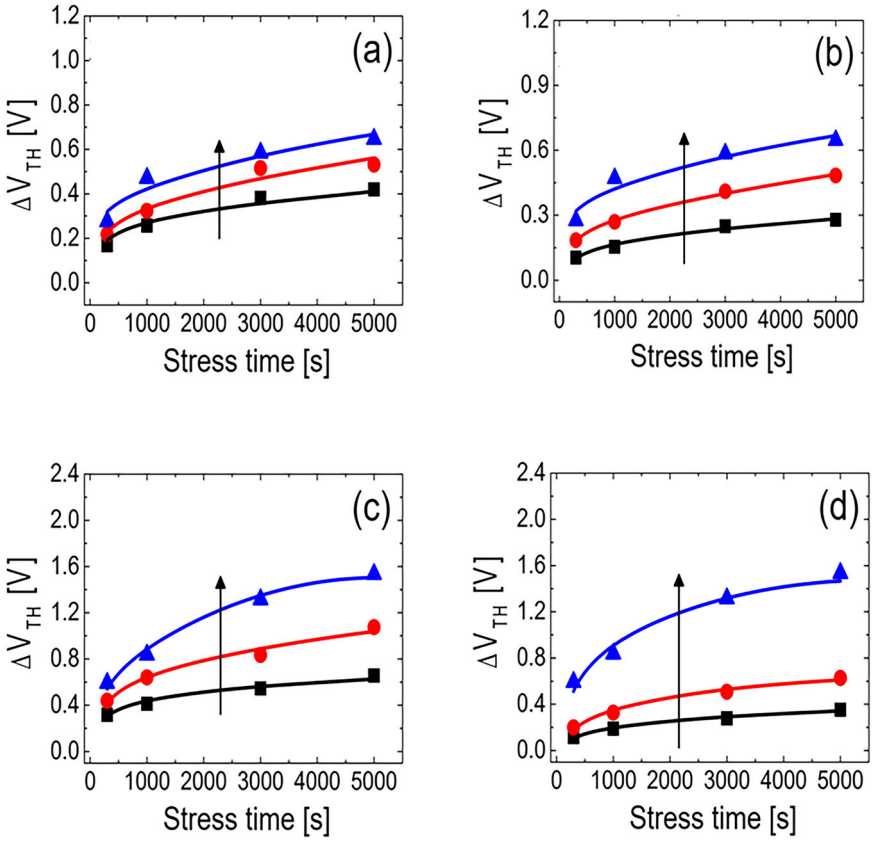

Fig. 9 | Positive bias temperature stress (PBTS) induced threshold voltage shifts in a-IGZO TFTs. **a**, **b** Dependence of threshold voltage shift (ΔV_{th}) on temperature (T) and gate-source voltage (V_{GS}) for electrons trapped in shallow trap states under PBTS at V_{GS} = 40 V, V_{DS} = 0 V, and 80 °C. **c**, **d** Dependence of ΔV_{th} on temperature and V_{GS} for electrons trapped in deep trap states under PBTS at V_{GS} = 40 V, V_{DS} = 0 V, and 80 °C[120]. **a** Shallow trap, V_{gs} = 40 V, V_{ds} = 0 V: blue (80 °C), red (60 °C), black (40 °C). **b** Shallow trap, V_{ds} = 0 V, 80 °C: blue (V_{gs} = 40 V), red (30 V), black (20 V). **c** Deep trap, V_{gs} = 40 V, V_{ds} = 0 V: blue (80 °C), red (60 °C), black (40 °C). **d** Deep trap, V_{ds} = 0 V, 80 °C: blue (V_{gs} = 40 V), red (30 V), black (20 V). Lines: Model; symbols: Extracted data.

In this equation, the symbols υ, β, k_B, E_{Th}, t, and T correspond to the frequency of attempt-to-escape, the coefficient for stretched exponential fitting time, the Boltzmann constant, the activation energy for reaching thermal equilibrium, time, and the absolute temperature expressed in Kelvin, respectively. Modeling reliability is a huge milestone in multi-material TFTs, as stability is one of the major outcomes of devices with such configurations. However, there are still challenges with scalability and parameter extraction for alloyed TFT systems. Future endeavors should emphasize physically substantiated extensions to surface-potential-based models.

New possibilities in multiscale reliability simulation for MO TFTs solve the problems with traditional models by connecting atomic-scale phenomena like defect migration and trap formation to the degradation of devices on a larger scale when they are under stress from temperature and bias. For instance, recent density functional theory (DFT) integrated with TCAD simulations has clarified the function of oxygen vacancies in elevated-metal metal-oxide (EMMO) IGZO TFTs under positive bias stress, demonstrating how defect accumulation at interfaces results in threshold voltage shifts and mobility degradation[109]. ML potentials also make it possible to quickly model hydrogen states in a-IGZO at the atomic level[38]. This links diffusion kinetics to bias instability and helps with reliability metrics. Hybrid physics-informed ML and deep learning frameworks take this a step further by making predictions at the circuit level, which makes it easier to evaluate lifetime and failure modes on a larger scale[66]. These methods improve accuracy for flexible and high-stress applications. However, there are still problems with computational efficiency and validation against experimental data. For TFT enhanced stability, more refined hybrid approaches are required.

Future research in mechanical-strain-aware modeling for flexible a-MO TFTs focuses on the incorporation of mechanical-electrical coupling to mitigate performance fluctuations during bending or stretching. Mechanical stress on TFTs can cause reliability issues. Strain can lead to trap formation, mobility alterations, and threshold voltage instabilities. Recent research has utilized finite element modeling (FEM) to simulate stress distributions in IGZO TFTs, demonstrating that compressive mechanical stress (~0.9 GPa) induces reversible positive threshold shifts through conduction band modulation and increased electron trapping at gate oxide interfaces, especially under combined bias conditions[132]. Deformation-aware SPICE models that have been calibrated for IGZO devices under tensile or compressive strain also make active compensation circuits possible, which greatly reduce changes in current[133]. These methods show that strain effects in amorphous oxides are not the same in all directions. However, it is still hard to include real-time substrate deformation and long-term fatigue in compact models. To make sure that flexible displays and sensors are physically accurate even amid material uncertainties, it will be important to improve hybrid simulations that combine mechanical FEM with electrical TCAD.

Models including temperature effects

Temperature can affect device stability through changes in threshold voltage, charge carrier mobility, and subthreshold swing[74,134–136]. These phenomena are both due to the change of DOS in the semiconductor layer and to the modification of the charge carrier mobility[56]. Temperature variation influences both trap-state dynamics and band structure of the material[137].

An analytical current–voltage and capacitance model for a-IGZO TFTs, considering temperature characteristics, integrates the numerical Pao–Sah model for describing the temperature-dependent behavior of deep and tail trap states. The compact model offers a unified analytical description of validated against experimental data from 253 K to 393 K by connecting subthreshold and above-threshold regimes with a smooth function[96]. Additionally, another compact model for a-IGZO TFTs has been validated at device and circuit levels. It provides a prediction about temperature-dependent behavior and also shows a very close matching between the simulated and measured results of an 11-stage ring oscillator circuit[102].

The relationship between temperature effects and the ferroelectric properties of some MO materials has also been studied in an effort to

improve device performance. For example, a model for such temperature-dependent effects on the ferroelectric switching, trapping dynamics, and intrinsic characteristics of metal oxide FeTFTs was developed based on theories such as Preisach, disorder physics, and Newton correction[138].

$$\begin{cases} n_e = N_t \nu_0 \tau_0 \exp\left((q\varphi_s + E_{F0})/K_0 T\right) \\ n_l = (\pi T/T_A)/\sin(\pi T/T_A) \cdot N_t \exp\left((q\varphi_s + E_{F0})/K_0 T_A\right) \\ Q_S(\varphi_s) = \varepsilon_s E_s(0) = \sqrt{2q\varepsilon_s \cdot (\varnothing_T n_e + \varnothing_{TA} n_l)} \end{cases} \quad (39)$$

where *ne, nl*: Free and localized carrier density, respectively, Q_S: Channel charge concentration, K_0: Boltzmann's constant, T, T_A: Temperature and characteristic temperature of exponential DOS, N_t: Total concentration of localized states, ν_0, τ_0: Attempt-to-escape frequency and carrier lifetime, ε_s: Dielectric constant of the semiconductor. While ferroelectric polarization and charge convergence represented by the following equation

$$\begin{cases} P_{FE}(E_{FE}) = \eta \cdot C_{ox} V_{ox} = \eta \cdot Q_S(\varphi_S) \\ Q_S(\varphi_S) = C_{ox}(V_{GS} - V_{FB} - V_{FE} - \varphi_S) \end{cases} \quad (40)$$

where C_{ox}: Gate insulator capacitance per unit area, V_{GS}, V_{FB}, V_{FE}: Gate-source voltage, flat-band voltage, and ferroelectric voltage, respectively, φ_S: Surface potential

Mobility and drain current are represented as following

$$\begin{cases} \mu_p = u_b A_p (V_{GS} - V_{FB} - t_{FE}E_{FE} - V_p)^{4(1-W/D)} \\ \mu_v = u_0 A_v \cdot \exp\left(-(T_0/T)^{\beta}\right)(V_{GS} - V_{FB} - t_{FE}E_{FE})^{\alpha} \\ \mu_{eff} = 1/(1/\mu_p + 1/\mu_v) \end{cases} \quad (41)$$

$$I_D = \frac{W \cdot \mu_{eff} \cdot C_{ox}}{L}(\varphi_{S,D} - \varphi_{S,S}) \times \left(2\varnothing_T + V_{GS} - V_{FB} - \left(\frac{F_S + F_D}{2}\right)\right) \quad (42)$$

where μ_p, μ_v: mobilities for percolation and hopping conduction, respectively, F_S, F_D: Contributions from source and drain terminal respectively, $\varphi_{s,D}$, $\varphi_{s,S}$: Surface potential at drain and source and $_T$: A thermal voltage constant, related to the temperature and Boltzmann's constant. Figure 10 shows agreement between experimental results and the drain current model.

Conclusion and future outlook

This review examines modeling methodologies for metal oxide thin-film transistors, which support advancements in flexible displays and transparent electronics. Further, we have also underlined how the compact models evolve to balance computational efficiency with precision, ideally united for reliable device simulation and effective circuit optimization. The discussion also showed that a full charge and capacitance model would help in a better understanding of the dynamic charge behavior with improvements in circuit design based on several operating conditions. We also pointed out that the modeling needed to be performed with considerations for reliability under environmental stress and temperature variation, ensuring stability and performance for devices with TFTs. In other words, we contribute to further advances in modeling TFTs in view of the dynamic needs due to new applications in electronics. This review relies on published literature without new experimental validation and focuses primarily on a-IGZO with limited coverage of other materials. We critically need models that can be easily incorporated into commercially available simulation tools, hence furthering future technological advancement and innovation in the field.

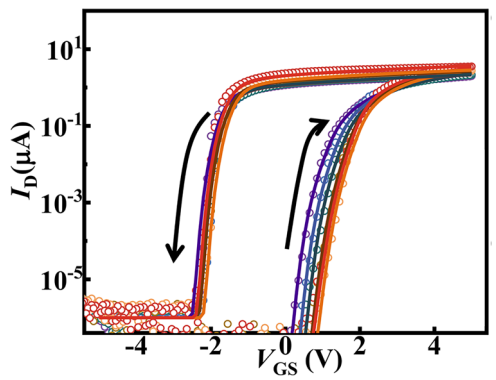

Fig. 10 | Comparison of modeled and measured transfer curves across a temperature range of 0 °C to 100 °C[138]. Points: FeTFT 5 μm experimental; solid lines: Model. At V_{DS} = 0.1 V. Curves from right to left (shifting towards negative V_{GS}): T = 0 °C (violet), 20 °C (cyan), 40 °C (dark blue), 60 °C (brown), 80 °C (orange), 100 °C (red). Arrow indicates increasing temperature direction.

Looking ahead with compact modeling in metal oxide thin-film transistors, a few important tasks stand out as being promising and leading towards the future. First, there is compact modeling with the use of machine learning algorithms; this indeed constitutes a fast-emerging trend with potential for enhancement of predictive accuracy, besides simulation speeds. Optimal compact model parameters can be deduced with the aid of machine learning using large data sets generated from experiment and simulation studies. This may enable new insight into metal oxide TFT operation under a variety of conditions. Such approaches remain conceptual in some discussions without deeper quantitative comparisons.

Other promising directions involve the development of unified compact models that should handle different metal oxide materials smoothly. Such a model would provide a more general way of simulating TFTs, and this is required in multi-material device design. This may mean integrating the physical insight of various metal oxide systems into one flexible and wider applicable model framework.

Besides this, the compact model is also becoming very important in simulating flexible electronics. As metal oxide TFTs will be one of the key contributors to flexible displays and sensors, developing such a model that can predict the performance variation with incoming mechanical stresses and strains with much higher accuracy is needed. Mechanical aspect enhancement of these compact models is an important consideration for reliable design in next-generation flexible and wearable electronics.

It is particularly important to highlight that modeling methodologies addressing the effects of mechanical flexibility and stress on metal oxide TFT performance remain relatively underexplored. Developing advanced mathematical and compact models capable of accurately capturing the mechanical-electrical coupling could enhance our ability to design robust, flexible electronics. Models incorporating mechanical deformation, strain-dependent electronic transport parameters, and long-term reliability under repeated bending cycles will serve as tools in enabling the transition of metal oxide TFT technologies from laboratory demonstrations to real-world flexible and wearable applications. This addresses gaps in real-world variability and long-term reliability testing.

There is also a growing demand to incorporate more environmental factors into compact models. Humidity, temperature, and exposure to various light spectrums will impact the performance of metal oxide TFTs. An advanced model can simulate those environmental impacts in real time and can turn out to be an important tool for the realization of robust devices, both for outdoor and automotive applications.

Conclusively, in the race towards greener electronic solutions, compact model developments that can contribute to the design of energy-efficient metal oxide TFTs will be important. Such models would have to be developed with a view not only towards efficiency during operation but also for reduced environmental impact during fabrication and at the stage of device disposal. The future of compact modeling for metal oxide TFTs holds potential, with opportunities remaining for advancements aimed at improving electronic design. In the future, it will be quite significant that these models evolve further with consistency in keeping with technological advancement and emerging fresh needs from the industry.

Data availability

No datasets were generated or analyzed during the current study.

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Author contributions

H.U.H. conceived the idea and wrote the paper. S.T.H. provided valuable suggestions. M.Z. supervised and coordinated the study. All the authors discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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