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Demonstrating a universal logical gate set in error-detecting surface codes on a superconducting quantum processor

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Fault-tolerant quantum computing (FTQC) is essential for achieving large-scale practical quantum computation. Implementing arbitrary FTQC requires the execution of a universal gate set on logical qubits, which is highly challenging. Particularly, in the superconducting system, two-qubit gates on surface code logical qubits have not been realized. Here, we experimentally implement a logical CNOT gate along with arbitrary single-qubit rotation gates on distance-2 surface codes using the superconducting quantum processor *Wukong*, thereby demonstrating a universal logical gate set. In the experiment, we demonstrate the transversal CNOT gate on a two-dimensional topological processor based on a tailored encoding circuit, at the cost of removing the ancilla qubits required for stabilizer measurements. Furthermore, we fault-tolerantly prepare logical Bell states and observe a violation of CHSH inequality, confirming the entanglement between logical qubits. Using the logical CNOT gate and an ancilla logical state, arbitrary single-qubit rotation gates are realized through gate teleportation. All logical gates are characterized on a complete state set and their fidelities are evaluated by logical Pauli transfer matrices. The demonstration of a universal logical gate set and the entangled logical states highlights significant aspects of FTQC on superconducting quantum processors.

Quantum computing holds the promise to accelerate classical computing in various applications such as large number factorization[1], quantum simulation[2], and machine learning[3]. However, physical qubits are typically very fragile and are easily disturbed by environmental noise. To address the noise issues in large-scale quantum computing, quantum error correction techniques have been proposed, which introduce redundant information and encode quantum states onto logical qubits to ensure fault tolerance[4–6].

In recent years, multiple experiments across various quantum computing platforms have demonstrated the memory of quantum information on logical qubits. These experiments are based on hardware systems encompassing superconducting[7–15], ion trap[16,17], neutral atom[18], and other systems[19–23]. Particularly in experiments using bosonic codes, it has been demonstrated that the quality of logical qubits can exceed the so-called break-even point[21,22], validating the effectiveness of quantum error correction techniques in suppressing quantum noise.

Furthermore, to achieve fault-tolerant quantum computing (FTQC), a set of logical gates needs to be implemented. The simplest approach to implement logical gates is transversally, where all physical qubits have interacted with at most one physical qubit from each logical block, therefore naturally ensuring fault-tolerance. However, a well-known theorem states that no quantum code can simultaneously promise a transversal and universal logical gate set[24–26]. For instance, in the surface code, the CNOT gate is transversal. While some single-qubit rotation gates, such as the S gate and T gate, typically need to be implemented indirectly using gate teleportation circuits with ancilla logical states[27,28].

Currently, more and more experimental works are focusing on demonstrations of logical gates of various quantum error correction codes[12,14,18,29–37]. For instance, in neutral atom systems, demonstrations of the CNOT, CZ, and CCZ gates have been achieved on the [8,3,2] color code[18]. In ion trap systems, the H, S, T, and CNOT gates have been demonstrated on the Steane code[30], forming a universal gate set. In superconducting systems,

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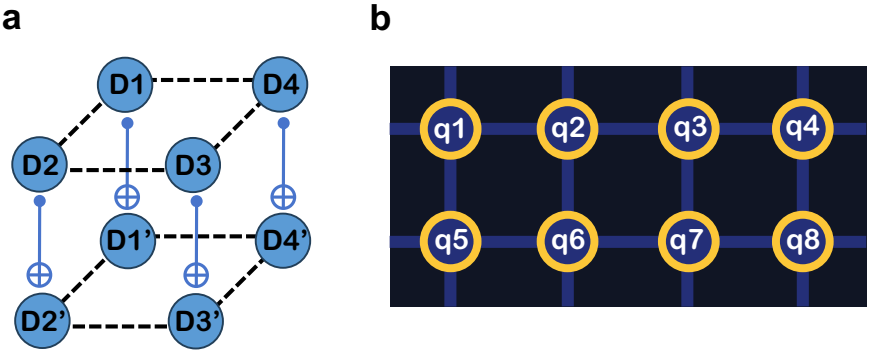

Fig. 1 | Distance-2 surface code and qubit layout in the experiment. a Two logical qubits of the distance-2 surface code and transversal CNOT gate. Each logical qubit is encoded by four data qubits and the logical CNOT gate between two logical qubits corresponds to the four physical CNOT gates between the corresponding data qubits. **b** The experiment uses eight physical qubits arranged in a 2×4 rectangular region on the superconducting quantum processor *Wukong*. The deep blue lines represent the topology of the processor, indicating the allowed two-qubit gates between physical qubits.

experimental demonstrations of logical gates remain limited, particularly for the surface code, which is the most promising encoding scheme due to its high theoretical threshold and practical nearest-neighbor connectivity requirements[28,38]. Ref. 31 demonstrated a universal set of single-qubit gates on the distance-2 surface code in superconducting systems, showing the potential of using surface code logical qubits for FTQC in the superconducting quantum processor. The main limitation of their work is the lack of two-qubit logical operations, thus not constituting a complete universal gate set. Additionally, the ancilla quantum states used in gate teleportation are physical states rather than logical states, which is inconsistent with the requirements in FTQC. To the best of our knowledge, no work has yet implemented a complete universal set of logical gates in either the superconducting system or the surface code encoding.

In our work, we use the error-detecting surface code with distance 2 (Fig. 1a) to implement a complete set of universal logical gates, including arbitrary single-qubit rotations around the Z or X axis and the CNOT gate, filling the gap in current literature. In the experiment, we encode two logical qubits in a 2×4 qubit region of the superconducting quantum processor *Wukong* (see Fig. 1b and Supplementary Note 1). The logical CNOT gate is implemented transversally, i.e., by performing four CNOT gates between the corresponding physical qubits. Additionally, single-qubit rotation gates are implemented by preparing the ancilla logical states and applying gate teleportation circuit, which consists of a logical CNOT gate and logical X or Z measurement on the ancilla qubit. To implement transversal CNOT gates on a two-dimensional topology, our design has to simplify the encoding of two logical qubits by removing the measurement qubits required for stabilizer measurements. The error detection in our experiment is achieved through measurement and post-selection at the end of the circuit. While no stabilizer measurements are performed after logical operations, any single error can still be detected in fault-tolerant circuits by reconstructing the stabilizers from the terminal measurement results.

The logical Pauli transfer matrices (LPTMs) of these logical gates are characterized on a complete set of states, according to which the gate fidelities are evaluated and listed in Table 1. Using fault-tolerant logical state encoding circuits and transversal CNOT gates, four logical Bell states are also prepared. By verifying the violation of the CHSH inequality with these Bell states, we have confirmed the presence of quantum entanglement between two logical qubits. In the experiment, all fault-tolerantly prepared logical states, including single-qubit states and Bell states, exhibit higher fidelity than the results on the corresponding physical qubits (see Table 2).

Note that the fidelity referred to here is the overall fidelity of the preparation and characterization process, therefore, it does not indicate that a logical state beyond the break-even point has been achieved. However, as hardware improves, the logical error rate of error detection codes could exceed the breakeven point, as indicated by some theoretical and experimental work using error detection codes in the context of early fault-tolerant computing[39,40].

Moreover, in the long term, the demonstration of transversal CNOT gates on surface codes could support more efficient FTQC. Theoretical works suggest that combining transversal CNOT gates with two-dimensional (2-D) operations has the potential to reduce the space-time overhead of FTQC on surface codes[41,42]. However, we recognize that this may be a rather distant goal for superconducting systems, as the transversal CNOT gate for surface codes typically requires a multi-layer architecture or a 2-D architecture with long-distance couplings[43–46]. Nonetheless, our experiment provides an early exploration for these intriguing applications.

Results

Logical state preparation and measurement

The logical qubit of distance-2 surface code is encoded on four data qubits and is capable of detecting any single-qubit errors. Its code space is the $+1$ eigenspace of the following stabilizer group:

$$\mathcal{S} = \langle X_1X_2X_3X_4, Z_1Z_2, Z_3Z_4 \rangle. \tag{1}$$

Then the logical Pauli operators are defined as:

$$Z_L = Z_1Z_3, \quad X_L = X_3X_4. \tag{2}$$

Accordingly, the explicit form of the logical state can be written as:

$$\begin{aligned} |0_L\rangle &= \tfrac{1}{\sqrt{2}}(|0000\rangle + |1111\rangle), \\ |1_L\rangle &= \tfrac{1}{\sqrt{2}}(|0011\rangle + |1100\rangle), \end{aligned} \tag{3}$$

and

$$|\pm_L\rangle = \frac{1}{\sqrt{2}}(|0_L\rangle \pm |1_L\rangle). \tag{4}$$

Here, we designed circuits for preparing the logical states $|0_L\rangle$, $|1_L\rangle$, $|+_L\rangle$ and $|-_L\rangle$ fault-tolerantly (see Fig. 1), whose fault tolerance is proven in the Methods. In this error-detection context, an operation is fault-tolerant if any single error produces a non-trivial syndrome and can therefore be post-selected out. In order to simultaneously ensure fault-tolerant state preparation and transversal CNOT gate implementation between $|\pm_L\rangle$ and $|0/1_L\rangle$ states, we adopt the qubit allocation scheme depicted in Fig. 2a and b. The key is that we exploit the property that $|\pm_L\rangle$ can be decomposed into product states ($|\pm_L\rangle = \frac{1}{2}(|00\rangle \pm |11\rangle)^{\otimes 2}$), and encode $|\pm_L\rangle$ on the leftmost two (q1 and q5) and the rightmost two physical qubits (q4 and q8) in the hardware. Moreover, we also provide a circuit for preparing arbitrary logical state $|\psi_L\rangle$ in Fig. 2c. Generally, such a circuit for encoding arbitrary logical state is not fault-tolerant, nor is this circuit. In this way, a logical state can be encoded on a chain of four physical qubits (q1-q4) with only nearest-neighbor coupling.

After preparing the logical states, logical X, Y, or Z measurements are performed to characterize these states. Their measurement results are determined by the product of the corresponding Pauli operator

measurement result on each data qubits. The logical X and Z measurements are fault-tolerant and correspond to measurements in the X and Z bases on all data qubits, respectively. Post-selection is carried out based on the conditions provided by the three generators of the stabilizer group, discarding results that violate these conditions. Specifically, assuming the X or Z measurement result on the ith data qubit is m_i^x or $m_i^z \in \{+1, -1\}$ the post-selection conditions are $m_1^x m_2^x m_3^x m_4^x = +1$, and $m_1^z m_2^z = +1, m_3^z m_4^z = +1$

Table 1 | Summary of the fidelities of logical gates (including characterization) in the experiment

Logical gate	Fidelity	Logical gate	Fidelity
$R_Z(0)$	94.4(5)%	$R_X(0)$	92.1(6)%
$R_Z(\frac{\pi}{4})$	90.0(7)%	$R_X(\frac{\pi}{4})$	90.7(7)%
$R_Z(\frac{\pi}{2})$	87.4(7)%	$R_X(\frac{\pi}{2})$	89.6(7)%
$R_Z(\pi)$	93.9(5)%	$R_X(\pi)$	92.4(6)%
CNOT	88.9(5)%		

Table 2 | Comparison of the fidelities between fault-tolerant prepared logical states and physical states (including preparation and characterization) in the experiment

State	Logical state fidelity	Physical state fidelity
$\|0_L\rangle/\|0\rangle$	97.9(2)%	96.9(3)%
$\|1_L\rangle/\|1\rangle$	98.0(2)%	90.8(6)%
$\|+_L\rangle/\|+\rangle$	97.7(2)%	94.8(4)%
$\|-_L\rangle/\|-\rangle$	97.8(2)%	93.6(5)%
Four Bell states	79.5(5)%	74.4(9)%
	79.5(5)%	74.2(9)%
	79.4(5)%	74.5(9)%
	79.4(5)%	74.2(9)%

for logical X and Z measurements, respectively. On the other hand, measurement of the logical Y operator $Y_L = Z_1 Y_3 X_4$ is not fault-tolerant. It requires Z measurements on data qubits D1 and D2, a Y measurement on D3, and an X measurement on D4. The corresponding post-selection condition is $m_1^z m_2^z = +1$. In this case, post-selection cannot eliminate all single-qubit error cases but can suppress some of them. Define the probability of successfully passing the post-selection condition as the post-selection rate. Since the post-selection conditions vary under different measurement bases, the post-selection rate is significantly influenced by the measurement basis.

Here, we conduct experimental demonstrations and characterizations on the fault-tolerantly prepared $|0/1_L\rangle$, $|\pm_L\rangle$ states, and non-fault-tolerantly prepared $|0/1_L\rangle$ states. Through logical quantum state tomography, we constructed the density matrix ρ_L in the code space, as shown in Fig. 2d–f. Furthermore, we computed the fidelity of the logical state:

$$F_L = \langle\psi_L|\rho_L|\psi_L\rangle, \tag{5}$$

where $|\psi_L\rangle$ is the ideal logical quantum state. The fidelities of the fault-tolerantly prepared states $|0_L\rangle, |1_L\rangle$ and $|+_L\rangle, |-_L\rangle$, as well as the non-fault-tolerantly prepared states $|0_L\rangle$ and $|1_L\rangle$, are 97.9(2)%, 98.0(2)%, 97.7(2)%, 97.8(2)%, 89.2(3)%, and 88.9(3)%, respectively. We also computed the fidelities of the $|0\rangle, |1\rangle$ and $|+\rangle, |-\rangle$ states prepared on the eight physical qubits in the experiment using physical state tomography. For a fair comparison, we did not use readout error mitigation techniques[47] during the physical state tomography. The highest values among eight physical qubits are 96.9(3)% for $|0\rangle$ in q2, 94.8(4)% for $|+\rangle$ in q2, 93.6(5)% for $|-\rangle$ in q2 and 90.8(6)% for $|1\rangle$ in q3. All these values are lower than the fidelities of the fault-tolerantly prepared logical states, demonstrating the noise-suppressing effect in the overall process of the preparation and characterization. However, we remind readers that the fidelities of logical or physical states also affected by noise in the tomography protocol. Due to the difficulty in distinguishing noise in characterization from noise in state preparation, these results do not imply that the fidelity of logical state preparation exceeds that of the physical state. Especially given the significant

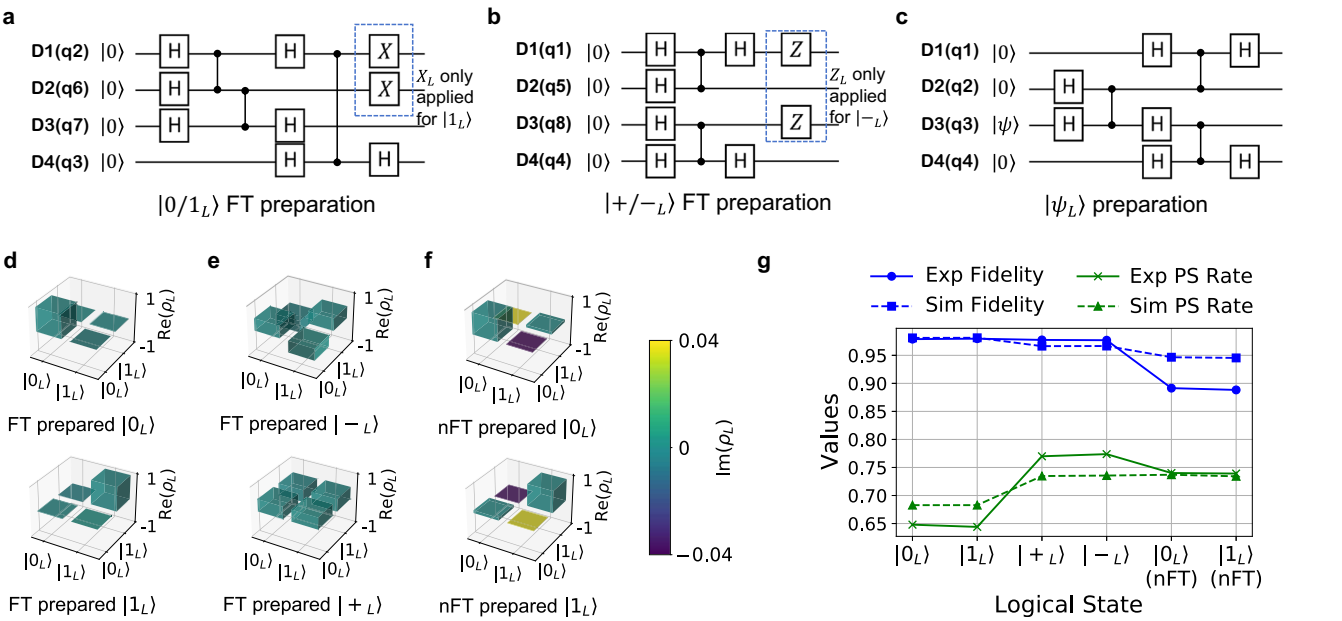

Fig. 2 | Logical state preparation circuits and characterization. a, b Circuits for fault-tolerant (FT) preparation of $|0/1_L\rangle$ and $|\pm_L\rangle$ states. The $|1_L\rangle$ (or $|-_L\rangle$) state are obtained by applying X_L (or Z_L) gate after preparing the $|0_L\rangle$ (or $|+_L\rangle$) state. **c** Circuits for non-fault-tolerant (nFT) preparation of arbitrary logical state $|\psi_L\rangle$. **d–f** Density matrices and fidelities of the six single logical states prepared in the experiment. All logical state density matrices are obtained through logical state tomography. **g** Comparison of fidelity and post-selection (PS) rates between experiments and simulations. The figure shows the fidelity of six logical states and the post-selection rates when measuring their eigenoperators (Z_L or X_L).

readout noise on our superconducting processor, the contribution of error detection to the improvement in readout fidelity is likely more substantial.

In addition, we provide information on the post-selection rates when measuring the logical state eigenoperators in Fig. 2e (see Supplementary Note 3 for complete data on the post-selection rate). We also present simulation results for comparison, which are based on the Pauli depolarizing noise model, a commonly used error model in quantum error correction research (see details in Supplementary Note 4). However, we also remark that this model does not fully capture the real noise, leading to discrepancies between experimental and simulated data.

Logical CNOT gate and Bell states

Next, our experiment demonstrates a transversal CNOT gate between two surface code logical qubits (see Fig. 3a and b). Initially, two logical states $|\psi_L\rangle$ and $|\varphi_L\rangle$, are prepared on two chains of the quantum processor (q1-q4 and q5-q8), where $|\psi_L\rangle$ and $|\varphi_L\rangle$ are from a complete state set $\{|+_L\rangle, |-_L\rangle, |0_L\rangle, |i_L\rangle\}$. Here $|i_L\rangle = (|0_L\rangle + i|1_L\rangle)/\sqrt{2}$ is the $+1$ eigenstate of the logical operator Y_L. This step is realized by the preparation circuit for arbitrary logical states described in the previous section. Since the fidelity of states $|+_L\rangle$ and $|-_L\rangle$ in our experiment is higher, we prioritize selecting these two states to form the complete state set. The density matrices of the initial logical states are characterized by logical state tomography. Subsequently, a transversal CNOT gate is applied to the initial logical states, and the output states are characterized using logical state tomography. Based on the expectation values of two-qubit Pauli operators of the initial and output states, we extract the LPTMs using the method presented in ref. 31. The fidelity of the logical CNOT gate, as computed from the LPTM, is found to be $F_L^G = 88.9(5)\%$. Details concerning the LPTM and fidelity calculation are presented in Supplementary Note 2. Due to the noise in the characterization, this result is actually a conservative estimate of the logical gate fidelity.

Then we use the logical CNOT gate to prepare four Bell states on logical qubits, which are important entangled resources in quantum information. Following the above initialization method, the control and target logical qubits can be initialized to $|\pm_L\rangle$ and $|0/1_L\rangle$ states, respectively. Then they can be acted by a logical CNOT gate to generate a Bell state. However, under such qubit allocation, the prepared $|0/1_L\rangle$ state is not fault-tolerant. Therefore, we adopt the qubit allocation scheme from the previous section to simultaneously fault-tolerantly prepare the $|0/1_L\rangle$ and $|\pm_L\rangle$ states (see Fig. 3c). This circuit can be viewed as a special planarization of a two-layer architecture. In this layout, all physical CZ gates required in both the logical state preparation and the transversal CNOT gate implementation are 2-D hardware-neighbor. We reconstruct the density matrix of the logical Bell states in Fig. 3d. The overall fidelities in the preparation and characterization for the four logical Bell states are 79.5(5)%, 79.5(5)%, 79.4(5)%, and 79.4(5)%, respectively. We also report the post-selection rates for Bell states under $X \otimes X$, $X \otimes X$, $Z \otimes Z$ measurements along with a comparison between simulated and experimental data in Fig. 3e. Correspondingly, we prepare four physical Bell states by physical CNOT gate on qubits q6 and q7. The fidelity of the CNOT gate between q6 and q7 is the highest among all physical CNOT gates in the experiment. The fidelities for the four physical Bell states are 74.4(9)%, 74.2(9)%, 74.5(9)%, and 74.2(9)%, respectively, all of which are lower than the fidelity of the fault-tolerantly prepared logical Bell states.

To confirm entanglement between the two surface code logical qubits, we verify a variant of the CHSH inequality[48]. For a two-qubit density matrix ρ, define the matrix T_ρ with elements $(T_\rho)_{ij} = \mathrm{Tr}(\rho P_i \otimes P_j)$, where $P_i \in \{X, Y, Z\}$. A necessary and sufficient condition for violating the CHSH

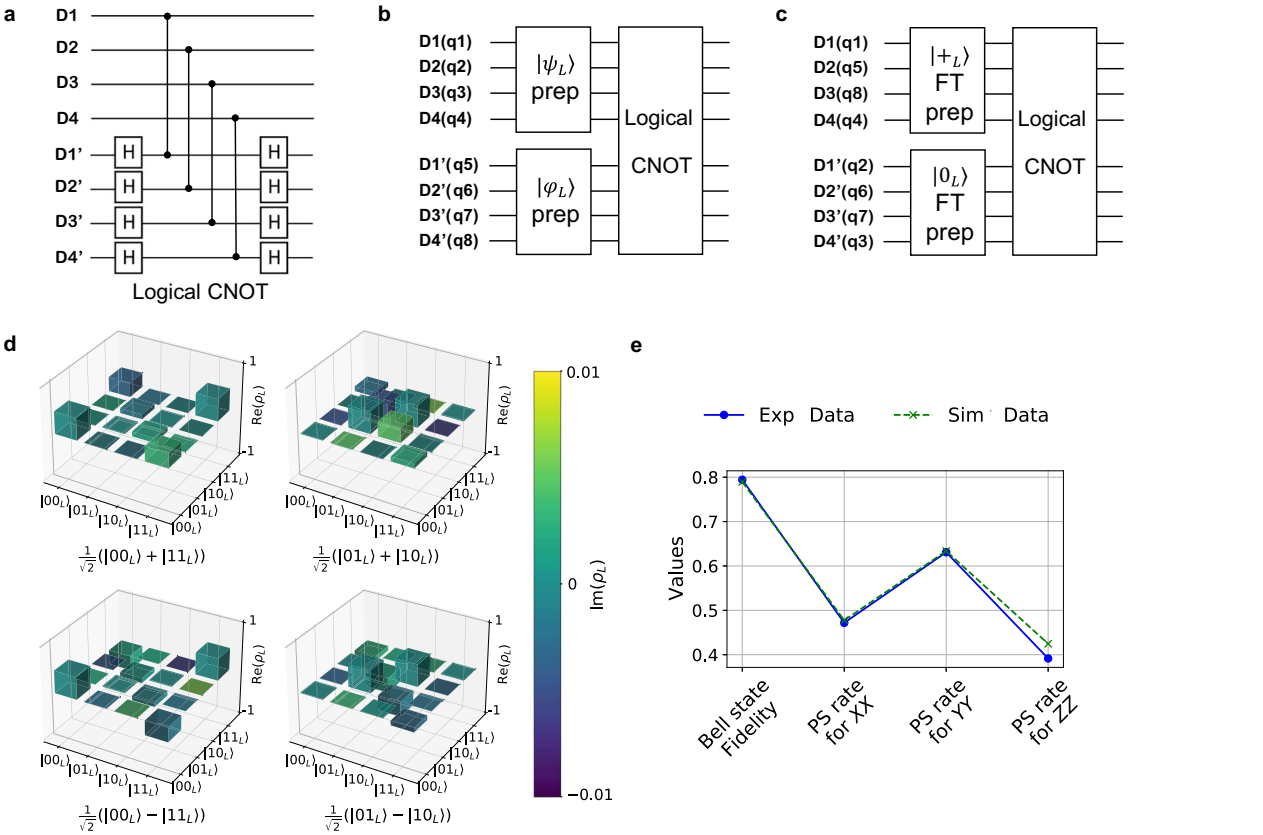

Fig. 3 | Logical CNOT gate and Bell state characterization. a Circuit of the logical CNOT gate implemented transversally. **b**, **c** Circuit for applying a logical CNOT gate on arbitrary logical states $|\psi_L\rangle$ and $|\varphi_L\rangle$, and the circuit for fault-tolerant preparation of Bell states, respectively. The blocks represent logical state preparation circuits and the logical CNOT gate. The upper half of the logical CNOT block corresponds to the control logical qubit, while the lower half corresponds to the target logical qubit. **d** Density matrices and fidelities of the four logical Bell states prepared fault-tolerantly in the experiment. **e** Average fidelity and post-selection (PS) rates of four logical Bell states when measuring $X_L \otimes X_L$, $Y_L \otimes Y_L$ and $Z_L \otimes Z_L$ in experiments and simulations.

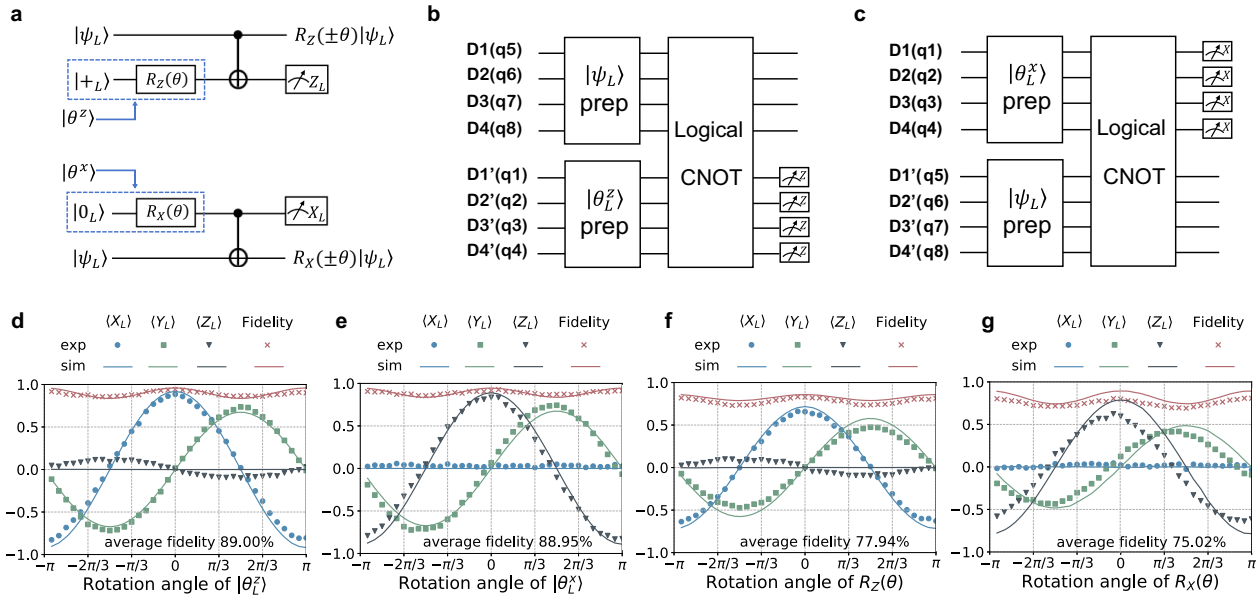

Fig. 4 | Logical single-qubit rotations and characterization. a Gate teleportation circuits that implement single-qubit rotation operations on logical qubits. The ± sign of the rotation angle depends on the measurement results of the ancilla logical states. **b**, **c** Circuits for applying single-qubit rotations $R_Z(\theta)$ and $R_X(\theta)$ on the logical state $|\psi_L\rangle$ based on gate teleportation, respectively. **d**, **e** Average values of Pauli operators and fidelity of the ancilla logical states $|\theta_L^z\rangle$ and $|\theta_L^x\rangle$ with rotation angles $\theta \in (-\pi, \pi]$, respectively. Scatter points and solid lines are used to distinguish experimental and simulated data. **f**, **g** Average values of Pauli operators and fidelity of the output states $R_Z(\theta)|+_L\rangle$ or $R_X(\theta)|0_L\rangle$ with rotation angles $\theta \in (-\pi, \pi]$, respectively.

inequality is $u_1 + u_2 > 1$, where u_1 and u_2 are the two largest eigenvalues of the matrix $T_\rho^T T_\rho$. In our experiment, the values of $u_1 + u_2$ for the four logical Bell states are 1.55, 1.55, 1.54, and 1.54, respectively. This result confirms the presence of quantum entanglement between the two surface code logical qubits.

Logical single-qubit rotation

Finally, we demonstrated logical single-qubit rotations around the Z or X axis based on gate teleportation circuit (Fig. 4a). More specifically, these rotation operations are

$$R_Z(\theta) = e^{-i\theta Z_L/2}, \quad R_X(\theta) = e^{-i\theta X_L/2}, \tag{6}$$

where θ is the rotation angle. The gate teleportation circuit consists of three parts. First, preparing the ancilla states

$$\begin{aligned} |\theta_L^z\rangle &= \tfrac{1}{\sqrt{2}}(|0_L\rangle + e^{i\theta}|1_L\rangle), \\ |\theta_L^x\rangle &= \cos\tfrac{\theta}{2}|0_L\rangle - i\sin\tfrac{\theta}{2}|1_L\rangle. \end{aligned} \tag{7}$$

Then the logical CNOT gate is applied, and finally, ancilla state is measured in logical Z or X basis. The $R_Z(\theta)$ or $R_X(\theta)$ gate is successfully executed only when the logical Z or X measurement results in $+1$; otherwise, operation $R_Z(2\theta)$ or $R_X(2\theta)$ needs to be applied as a compensation. Here, we simply use the post-selection strategy, that is, only retaining the cases where the measurement result is $+1$. Note that the ancilla states can be viewed as the result of applying $R_Z(\theta)$ or $R_X(\theta)$ gates to $|+_L\rangle$ or $|0_L\rangle$, respectively, that is why we refer to this circuit as gate teleportation circuit.

In the experiment, we first prepare the required ancilla logical states $|\theta_L^z\rangle$ and $|\theta_L^x\rangle$ with $\theta \in (-\pi, \pi]$ on a chain of the quantum processor (q1-q4). Then these input states are measured in X_L, Y_L or Z_L basis to obtain the expectation values of the logical Pauli operators. Subsequently, we execute the circuits in Fig. 4b, c, demonstrating the single-qubit rotation gates around the Z or X axis on the state $|\psi_L\rangle = |+_L\rangle$ or $|0_L\rangle$, respectively. The expectation values of the logical Pauli operators for the input and output states are shown in Fig. 4d–g. Using the expectation values $\langle X\rangle$, $\langle Y\rangle$, $\langle Z\rangle$, we reconstructed the density matrices, thereby calculating the fidelity of each state. The average fidelities of input states $|\theta_L^z\rangle$ and $|\theta_L^x\rangle$ are evaluated to be 89.0(3)%. Correspondingly, the average fidelities of the output states are 78.0(9)% and 75.0(9)%, respectively.

To characterize the fidelity of the single-qubit logical gates, it is required to construct the LPTMs of these gates. Here, we test the LPTMs of $R_Z(\theta)$ and $R_X(\theta)$ with $\theta \in \{0, \pi/4, \pi/2, \pi\}$ as examples. The input states are encoded as the logical states from the set $\{|+_L\rangle, |-_L\rangle, |0_L\rangle, |i_L\rangle\}$, and the above logical gates are applied separately. We measure the expectation values of the Pauli operators for the input and output states and construct the LPTMs for these eight logical gates accordingly (see Supplementary Note 2). The fidelities F_L^G of these eight logical gates are estimated to be 94.4(5)%, 90.0(7)%, 87.4(7)%, 93.9(5)%, 92.1(6)%, 90.7(7)%, 89.6(7)%, 92.4(6)%, respectively.

Discussion

This work experimentally demonstrates a complete universal set of logical gates on distance-2 surface code in a superconducting processor. Particularly, logical Bell states that violates CHSH inequality have been fault-tolerantly prepared using the transversal CNOT gate. Based on the logical CNOT gate, the gate teleportation process is experimentally demonstrated to implement single-qubit rotation operations. These results reveal several significant aspects of FTQC based on the surface code in superconducting hardware.

The fidelity of logical operations are in the experiment is affected by a variety of factors. The dominant noise of our superconducting processor is the readout noise and two-qubit gate noise. Through numerical simulations, we found that the performance of logical circuits in our experiment is more sensitive to readout errors compared to gate errors. The Supplementary Note 4 presents the results of these numerical simulations and discusses the mechanisms underlying various types of noise as well as potential approaches for improvement. In addition, in the implementation of single-qubit rotation gates, the fidelity of the logical gates largely depends on the quality of the ancilla logical states in the gate teleportation circuit. In our experiment, the ancilla logical states are generated by non-fault-tolerant preparation circuits, resulting in a relatively high error rate. In a complete FTQC framework, high-fidelity ancilla logical states are typically obtained through state distillation[27,49–51]. A particularly challenging future task is to experimentally demonstrate these distillation protocols.

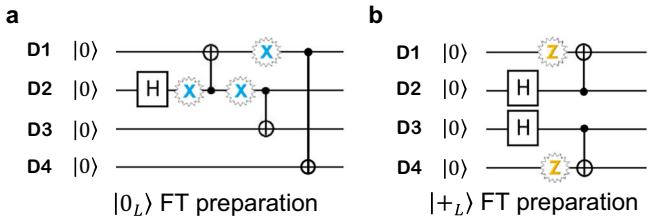

Fig. 5 | Equivalent logical state fault-tolerant preparation circuit. The circuits are simplified to a composition of CNOT and H gates, with fault tolerance equivalent to the original circuits. The possible X (blue) or Z (yellow) errors that could propagate are shown. **a** Fault-tolerant (FT) preparation circuit for $|0\rangle$. **b** Fault-tolerant (FT) preparation circuit for $|+\rangle$.

In our experiment, logical qubits are confined to a one-dimensional structure without measurement qubits. A natural extension is to incorporate the repeated stabilizer measurement process into our work. Achieving both the stabilizer measurement process and transversal CNOT gate typically requires a multi-layer structure or long-range entangling gates (see Supplementary Note 6). For superconducting platforms, this is regarded as a challenging long-term goal. However, we are also excited to see that they are increasingly gaining attention due to the requirements in FTQC[52–54]. Meanwhile, some prototypes of these technologies have been demonstrated recently[43–46,55], indicating that they are not beyond reach.

In conclusion, our experiment enriches the possibilities for research in FTQC. First, from a near-term perspective, our work demonstrates the role of error detection codes or small-distance error-correction codes in the early FTQC era. Notably, the performance of some logical circuits in the experiment surpassed that of physical circuits. Numerical simulations further indicate that the pseudo-threshold of the experimental circuits can significantly exceed the fault-tolerant threshold (approximately 1%, see Supplementary Note 4). Second, on superconducting platforms with planar nearest-neighbor connectivity, lattice surgery is the mainstream method for logical operations[56–58]. Demonstrating transversal CNOT gates supports a hybrid scheme combining them with lattice surgery, potentially reducing the significant overhead of FTQC[41,42]. We have elaborated on the feasibility and benefits of this architecture in the Supplementary Note 6. Achieving this requires extending the experimental qubit layout to a multi-layer structure, which remains a long-term goal for superconducting platforms.

Methods

Fault-tolerant logical state preparation

Here, we prove that the circuits in the first two parts of Fig. 2a and b are fault-tolerant, meaning that a single-qubit error occurring at any position in the circuit can be detected without leading to a logical error. To clarify this, we note that there are two types of errors to consider: those that remain localized in a single qubit and are thus detectable by the stabilizers, and those that might affect the final state of more than one qubit. We focus on the latter type of errors, ensuring that they do not spread to become logical errors. For ease of discussion, we combine the H gates and CZ gates in the circuit into CNOT gates, focusing on the preparation of the $|0_L\rangle$ and $|+_L\rangle$ states, resulting in the circuit shown in Fig. 5. This simplification does not affect the fault-tolerance of the original circuits.

For the $|0_L\rangle$ state preparation circuit, we only need to consider the Pauli X errors in the circuit, as any logical Z_L error produced is trivial for the $|0/1_L\rangle$ state up to a global phase. We mark the locations of all possible single-qubit Pauli X errors (shown as blue X in Fig. 5a). The leftmost X error affects qubits 1 through 4 as $X_1X_2X_3X_4$, which is a stabilizer. The second and third X errors affect qubits 2 and 3 as X_2X_3 and qubits 1 and 4 as X_1X_4, respectively. These errors anti-commute with the stabilizers Z_1Z_2 and Z_3Z_4, and thus they will be detected by the stabilizer measurements. This proves that no single-qubit Pauli X error at any position in the circuit can spread to become a logical X_L error.

Similarly, in the $|+_L\rangle$ state preparation circuit, we consider the possible Pauli Z errors. The two possible spreading Pauli Z errors (yellow Z in Fig. 5b) affect qubits 1 and 2 as Z_1Z_2 and qubits 3 and 4 as Z_3Z_4, which are the two stabilizers of this code. Since all these errors can be detected or lead to a stabilizer operator, we have demonstrated the fault-tolerance of these two encoding circuits.

Logical Pauli transfer matrix (LPTM)

The Pauli transfer matrix (PTM) describes a quantum process on the components of the density matrix represented in the basis of Pauli operators[6,59–61]. For a d-dimensional Hilbert space, a PTM $\mathcal{R}$ is a linear transformation matrix from the expectation values $p_i = \langle P_i\rangle$ of the Pauli operators P_i in the input state to the expectation values p_j' in the output state:

$$p_j' = \sum_i \mathcal{R}_{ij} p_i. \tag{8}$$

In our experiment, P_i belongs to $\{I_L, X_L, Y_L, Z_L\}^{\otimes 2}$ and $\{I_L, X_L, Y_L, Z_L\}$ for the cases $d = 4$ and $d = 2$, respectively. To construct the LPTMs of the logical quantum gates in the main text, we use input states from the complete set $\{|+_L\rangle, |-_L\rangle, |0_L\rangle, |i_L\rangle\}^{\otimes 2}$ (for the logical CNOT gate) or $\{|+_L\rangle, |-_L\rangle, |0_L\rangle, |i_L\rangle\}$ (for the logical single-qubit gates). The density matrices of the input and output states are obtained through logical state tomography, and the expectation values p_i and p_j' are then calculated. The inverse of the expectation value matrix yields the raw result $\mathcal{R}^{\text{raw}}$. However, $\mathcal{R}^{\text{raw}}$ may not satisfy the conditions of a physical channel, i.e., being completely positive and trace-preserving[6]. Therefore, using the techniques in ref. 31, $\mathcal{R}^{\text{raw}}$ is transformed into the Choi state representation:

$$\rho_{\text{choi}} = \frac{1}{d^2}\sum_{ij} \mathcal{R}_{ij}^{\text{raw}} P_j^T \otimes P_i. \tag{9}$$

We then optimize ρ under the following objective function and constraints:

$$\begin{aligned} &\text{minimize} && \sum_{i,j} |\text{Tr}(\rho P_j^T \otimes P_i) - \mathcal{R}_{ij}^{\text{raw}}|^2, \\ &\text{subject to} && \rho \geq 0, \text{Tr}(\rho) = 1, \text{Tr}_1(\rho) = \tfrac{1}{2}\mathbb{1}, \end{aligned} \tag{10}$$

where Tr_1 is the partial trace over the left half subsystem. Using the convex optimization package *cvxpy*, we obtain the optimal result ρ_{opt}. The corresponding LPTM $\mathcal{R}$ is

$$\mathcal{R}_{ij} = \text{Tr}(\rho_{\text{opt}} P_j^T \otimes P_i) \tag{11}$$

and the fidelity of the logical gate is

$$F_L^G = \frac{\text{Tr}(\mathcal{R}^\dagger \mathcal{R}_{\text{ideal}}) + d}{d^2 + d}, \tag{12}$$

where $\mathcal{R}_{\text{ideal}}$ is the ideal LPTM of the logical gate?. In our experiment, we constructed the LPTMs for the logical CNOT gate and eight logical single-qubit gates. The specific details of these LPTMs can be found in the Supplementary Note 2.

Quantum state tomography

Quantum state tomography[62–64] reconstructs the density matrix of an unknown quantum state by measuring some observables. In our experiment, we measure $4^n - 1$ Pauli operators of the logical qubits, where n is the number of logical qubits. Assuming the expectation values of these Pauli operators are $p_i = \langle P_i\rangle$, where $P_i \in \{I_L, X_L, Y_L, Z_L\}^{\otimes n}/\{I_L^{\otimes n}\}$, the density

matrix is reconstructed as:

$$\rho_{L,0} = \sum_{i=0}^{4^n-1} \frac{p_i P_i}{2^n},$$

with $p_0 = 1$ and $P_0 = I_L^{\otimes n}$. Such a density matrix $\rho_{L,0}$ may not satisfy the physicality characteristics of a quantum state. Therefore, we use maximum likelihood estimation[65,66] to construct the logical density matrix ρ_L. Specifically, the objective function to minimize is

$$\sum_i |\mathrm{Tr}(\rho_L P_i) - p_i|^2, \tag{13}$$

subject to $\mathrm{Tr}(\rho_L) = 1$, and $\rho_L \geq 0$. This process is implemented also using the convex optimization package *cvxpy*. Likewise, we also apply state tomography to physical states for constructing the density operators of states $|0\rangle$, $|1\rangle$, $|+\rangle$, $|-\rangle$ and four Bell states, which is done for comparison with the logical state density matrices. These results are shown in the Supplementary Note 2.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

Jiaxuan Zhang conceived and designed the project. Peng Duan, Yu-Chun Wu, and Guo-Ping Guo provide overall supervision throughout the research. Jiaxuan Zhang, Zhao-Yun Chen, Bin-Han Lu and Hai-Feng Zhang performed the majority of the experiments. Jiaxuan Zhang and Yun-Jie Wang contributed to data analysis. Jiaxuan Zhang drafted the initial manuscript. All authors discussed the results and reviewed the final version of the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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