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Optimized DC–DC converter based on new interleaved switched inductor capacitor for verifying high voltage gain in renewable energy applications

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This paper introduces an optimized DC–DC converter that employs a modified switched inductor-capacitor technique to achieve ultra-high voltage gain for renewable energy systems. The development is based on adding one cell of modified switched inductor (MSL1) with series diodes interleaved with the main switch in the proposed DC–DC converter. The (MSL1) with capacitor operates in resonant mode to reduce current stress across the main switch when the charge in capacitor becomes zero. This approach also reduces voltage stress across the main switch, all inductors, and diodes. Furthermore, modified switched inductors (MSL2) with an auxiliary switch and a coupled capacitor are incorporated to provide double boosting voltage and to achieve high voltage gain. Additionally, a main and auxiliary switch are integrated with modified switched capacitors (MSC) to provide ultra-high voltage gain and to reduce voltage stress across auxiliary switch. Moreover, the proposed converter exhibits a continuous input current with zero pulsating, even at very low duty cycles. The advantages of the proposed converter are high efficiency, low voltage stress, and low values of inductors and capacitors when utilizing a high switching frequency. A mathematical model for the proposed converter is developed for both continuous conduction mode and discontinuous conduction mode. In addition, the PCB design for the proposed converter is presented, and experimental tests are conducted to verify the simulation and laboratory results. The proposed converter aims to boost the voltage from 20 to 40 V to a variable output voltage between 200 and 400 V, delivering 400 watts of power with an efficiency of 96.2%.

Over the past few decades, attention has been drawn to the pressing issues of climate change and global warming due to greenhouse gas emissions. As a result, the necessity of reducing carbon emissions from fossil fuels has been recognized[1–8]. Sustainable energy resources, such as photovoltaic cells, FC fuel cells, and wind energy, are being utilized for electricity generation. However, these sources are characterized by a lower output voltage when compared to the voltage of the main grid connection. To increase the output voltage of photovoltaic cells, they can be connected in series. Nevertheless, a high and stable output voltage is not achieved through this method due to the shadow effect[8–29]. A suitable solution to this problem is the application of a DC–DC converter. By employing power electronic DC–DC converters with high voltage gain, the output voltage of PV panels can be enhanced[12]. However, many challenges are faced by researchers in the modification and development of new DC–DC power converters for renewable energy applications. Several conventional DC–DC converters, such as Boost, SEPIC, CUK, ZETA, and Buck Boost converters, are employed to increase low voltage to high voltage gain for various applications like Uninterruptible Power Supply, street LED lights, and medical devices. Nevertheless, these converters come with their own set of problems when utilized for achieving boosted high-voltage gain, as previously mentioned. For instance, a conventional boost converter can operate and boost low voltage up to 10 times the voltage gain[6]. However, the efficiency of traditional boost converters diminishes after high extreme duty ratios are employed. Additionally, the limited counts of inductors and capacitors render traditional converters unsuitable

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for ultra-high voltage gain. Furthermore, power MOSFET devices experience high voltage stress and high current stress when the converter operates at a high extreme duty ratio. Moreover, when the converter operates at high voltage with a very high duty ratio, MOSFET conduction and switching power losses significantly increase, along with the issue of reverse recovery due to diodes[5]. These converters, as mentioned earlier, have attracted the interest of many researchers aiming to achieve high voltage gains. Various topologies have been developed using coupled and non-coupled inductors, isolated and non-isolated transformers to boost voltage gain. Concerning the converters developed using coupled inductors and transformers, a dual boosting stage with a common ground coupled inductor and switched capacitor for RES was proposed in[1], while[11] combined two conventional CUK and SEPIC converters with coupled inductors for the same purpose. Another development is presented in[22], which introduces a Y-source step-up converter based on three coupled inductors for boosting applications. Additionally, Nafari and Beiranvand[31] presents an improved Z-source (ZS) converter using a coupled inductor with one core. In[32], a modification to a DC–DC converter is proposed using a single-switch SEPIC converter with an isolated transformer and supporting Voltage Doppler (VD) cell, without using a clamped circuit. In[27], a modified Z-source (ZS) converter with a unique ground between the energy source and load is discussed, utilizing coupled inductors and a voltage multiplier (VM) for RES applications as non-isolated. Siwakoti et al.[25] presents a modified SEPIC converter with a coupled inductor for piezoelectric drive systems, while[28] developed a SEPIC converter using a coupled inductor with a passive clamp circuit for high step-up gain converters. Additionally, Kushwaha et al.[24] presents a combined conventional Cuk and SEPIC converter developed as a single stage for electric vehicle battery chargers with coupled inductors. These developed converters have been demonstrated to achieve high voltage gain but at the cost of utilizing a high number of inductors and capacitors. Moreover, coupled inductors can result in leakage inductance, leading to a very high spike voltage across the MOSFET during the off-time. This can result in the converter becoming bulky, heavy, and costly. Furthermore, using a higher number of MOSFETs and diodes leads to a significant decrease in converter efficiency, as conduction and switching losses increase. Additionally, increasing the number of turns ratio of the coupled inductor to enhance the voltage gain results in higher internal resistance, which can impair the system's efficiency and performance.

Numerous advancements have been made in non-isolated DC–DC converters to achieve high voltage transfer ratios. In[2], a modification to the non-isolated Luo converter is proposed, employing a single switch with a hybrid switched capacitor (SC) technique. In[3], a modified Z-source network with a double input DC–DC converter is presented to achieve a high voltage transfer gain. Additionally, Bhaskar et al.[4] introduces an Improved Boost Converter as a multistage Switched Inductor that utilizes a polarized capacitor, while[5] presents a single switch with a single inductor based on a new hybrid boosting converter (HBC) that employs a bipolar voltage multiplier (BVM) to enhance the voltage conversion ratio. The SEPIC structure has been enhanced by integrating it with a conventional boost using active switched capacitors (ASC) and switched inductors (ASL), as described in[10–18], resulting in modifications in[9–34]. Furthermore, Sedaghati et al.[8] proposed the use of two interleaved KY converters, and[16] combined a KY converter interleaved with a conventional buck converter to form a buck-boost converter for stepping up the output voltage. While high voltage gain can be achieved by these converters, they face limitations when operating at low switching frequencies. Larger inductors and capacitors are necessitated by low switching frequencies, increasing the internal resistance of MOSFETs, leading to higher power losses and reduced efficiency. Additionally, conduction and switching losses can be elevated by a high number of diodes and MOSFETs, further reducing efficiency. The impact on voltage gain values is also exacerbated by the use of diodes with a high forward voltage, contributing to converter performance issues. Other topologies, such as the conventional ZS impedance network converter with (SC) proposed in[7], and the modified traditional buck-boost converter with an additional switch in[14], have also been suggested. In[15], a traditional boost converter was developed by adding a switched network with two conventional four-quadrant switches, while in[19], a SC with a diode was added. In[17–30], a traditional SEPIC converter is combined with a conventional boost converter and with (n) number of voltage multipliers in[26], and an active (SL) combined with passive inductors in[12], to achieve high step-up voltage gain. Two traditional SEPIC converters are combined in[20,21], a converter with a dual-switch and (SC) is proposed to attain a high voltage gain. Maalandish et al.[23] presents two modified three-phase interleaved boost converters, each with two (SC) in every phase, while[33] describes a conventional SEPIC converter with a combination of inductors, capacitors, and diodes. These non-isolated converters, designed for use in photovoltaic (PV) applications, have the potential to achieve high conversion ratios. However, as mentioned earlier, lower voltage gain is exhibited by these converters with pulsating input current at low duty cycles. Additionally, complex control circuits are required for the power MOSFETs, and the input current can follow more than one path during the on and off states. Moreover, power MOSFETs and diodes are subjected to high voltage and current stresses during the on and off states. Furthermore, high conduction and switching losses are incurred by these converters at high extreme duty cycles in achieving high voltage gain. Additionally, a high number of switches is required to achieve high voltage gain.

This paper optimized a DC–DC converter that utilizes a modified (MSLSC) technique to achieve ultra-high voltage gain for renewable energy sources (RES). The development is based on adding one cell of (MSL1) (L_2 and C_1) with series diodes interleaved with the main switch in the proposed DC–DC converter, as shown in Fig. 1b. This MSL1 with capacitor operates in resonant mode to reduce current stress across the main switch when charge in capacitor C1 becomes zero. In addition, this approach also reduces voltage stress across the main, auxiliary switches and diodes (D_1, D_2, and D_3). Furthermore, (MSL2) with an auxiliary switch and a coupled capacitor are incorporated to provide double boosting voltage and achieve high voltage gain. Additionally, main and auxiliary switches are integrated with (MSC) to provide ultra-high voltage gain. Moreover, the proposed converter exhibits a continuous input current with zero pulsating at a very low duty cycle. In addition, D_2 and D_3 operate in zero voltage switching (ZVS), as shown in Fig. 3c, at minimum input voltage and at high load current. The proposed DC DC converter operate at DCM and CCM with zero pulsating input current at low duty cycle. In addition, the proposed DC–DC converter can supply variable high-output voltage between 200 and 400 V, making it more

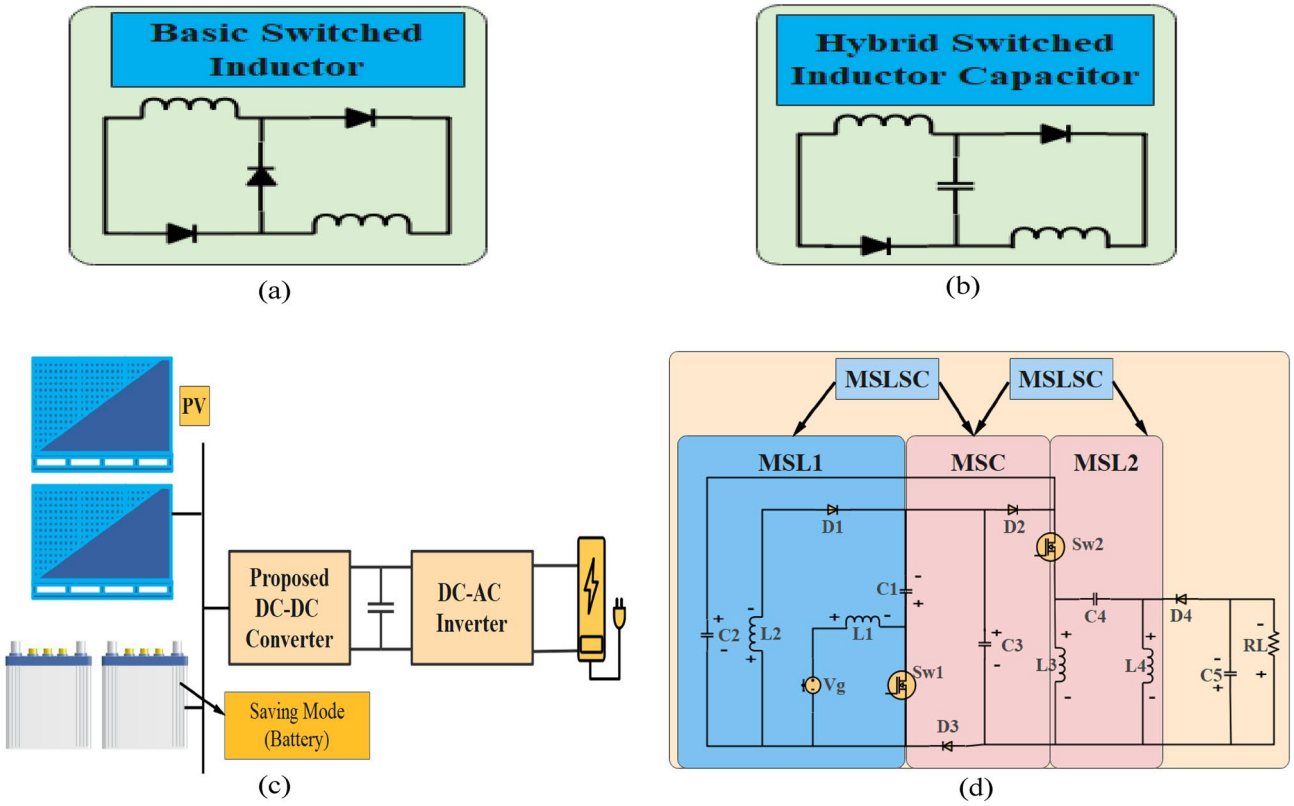


Figure 1. (**a**) Connection of a basic switched inductor, (**b**) a hybrid connection both a switched inductor and a capacitor (**c**), the proposed converter connects with PV Panels and Batteries, designed for Energy Saving Mode Applications (**d**). The structure of proposed DC–DC converter.

suitable for a wide range of applications. Furthermore, a dual PI controller is designed for the proposed converter to maintain a fixed output voltage under variable load and input voltage conditions.

Structure and operation principle of the proposed converter

The structure of the proposed converter consists of four main low-value inductors, five capacitors, four diodes, and two power MOSFET switches (main and auxiliary) as shown in Fig. 1d. Where the main switch is Sw_1 and auxiliary switch is Sw_2. The proposed DC–DC converter has been modified to incorporate a basic switched inductor and a hybrid switched inductor-capacitor, as illustrated in Fig. 1a,b. The interconnection between the suggested converter, photovoltaic panels, and a battery, specifically for applications related to energy-saving modes is shown in Fig. 1c. The proposed DC–DC converter has been developed to achieve an ultra-high voltage gain, capable of boosting a low input voltage range of 20–40 V to a variable output voltage between 200 and 400 V under a 400 W load, making the system more suitable for a wide range of applications. The proposed DC–DC converter offers several advantages over previous converters. Firstly, it eliminates the need for isolated coupled inductors and transformers to step up the voltage, resulting in reduced values of inductors and capacitors at high switching frequencies. This enhances the efficiency of the proposed converter. Moreover, the structure of the converter is simple and easy to implement. The proposed converter is also highly reliable for renewable energy system (RES) applications as it ensures no pulsating input current at low duty cycle. In addition, L_2 and C_1 operate at resonant mode, which reduces the current stress through Sw_1 when the charge in capacitor C_1 becomes zero at (D-2m), as shown in Fig. 11b,f. In addition, D_2 and D_3 operate in (ZVS) as shown in Fig. 13c at minimum input voltage and at high load current. Furthermore, the MOSFET switches and diodes experience very low voltage stress. Moreover, the voltage stress across inductors is also reduced when L_2 and C_1 operate at resonant mode. Additionally, the proposed converter achieves a higher voltage gain at high switching frequency than previous DC–DC converters. It can accommodate a wide range of duty cycles for high-power applications and boost low input voltage to high output voltage at very low duty cycles without the use of coupled inductors and transformers. The PWM generator of the MOSFET switches is simple, and both MOSFET devices turn on and off at the same time. The converter is characterized by its small size, low cost, and high efficiency, achieved by using capacitors and inductors with very small values.

Operation of the proposed converter

The proposed converter is illustrated in Fig. 1d and is capable of operating in two modes. The first mode, known as DCM, has two conditions: DCMC1 and DCMC2. DCMC1 occurs at the maximum input voltage with four states of operation during one cycle at very low duty ratios. DCMC2 occurs when the converter operates at the

minimum input voltage with a duty ratio of approximately 33%, as shown in Fig. 4a,b. The proposed converter can also function in CCM at high load currents when duty ratio is above 70%.

The proposed converter operation at DCMC1

The proposed converter can operate in DCMC1 with five modes of operation, as illustrated in Fig. 3a, which presents the waveform of the proposed converter in DCMC1. This mode appears in light load applications with a duty cycle below 30%, as shown in Fig. 4a, b. In this mode, the input current remains in (CCM) at both low and high duty ratios. Conversely, the current through L3 and L4 operates in (DCM).

Mode 1 [0–t0] Both MOSFETs S_{w1} and Sw_2 are simultaneously switched on, causing diodes D_2, D_3, and D_4 to be turned off. Energy is linearly charged from the input source Vg by L_1 since it is in series with it. L_2 is charged from C_1 through Sw_1. In this mode, D_1 is switched on, and capacitors C_2 and C_3 are connected in series. They are employed to charge L_3 through Sw_2, while L_4 is charged from C_4. Energy is provided to the load by C_5. The converter for this mode is illustrated in Fig. 2a. Below are the voltage and current equations for the various components in this mode:

$$\left.\begin{aligned} VL_1 &= V_g \\ VL_2 &= Vc_1 \\ VL_3 &= Vc_1 + Vc_2 + Vc_3 \\ VL_4 &= Vc_1 + Vc_2 + Vc_3 - Vc_4 \\ Vc_5 &= V_o \end{aligned}\right\} \tag{1}$$

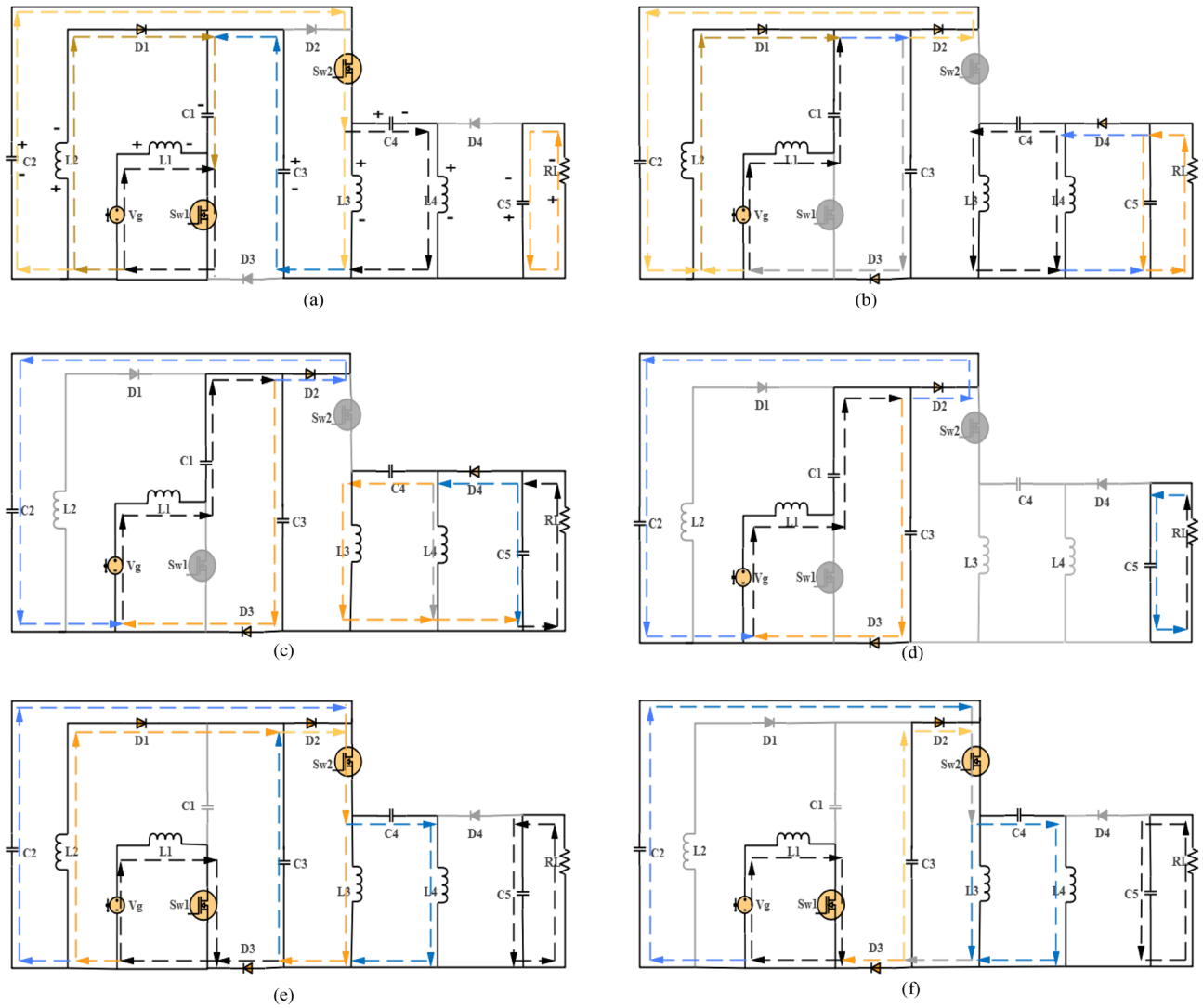


Figure 2. (**a**) Mode 1 DCMC1, Mode 1 DCMC2, (**b**) Mode 2 DCMC1, (**c**) Mode 3 DCMC1, Mode 4 DCMC2, Mode 4 CCM, (**d**) Mode 4 DCMC1, Mode 5 DCMC2, Mode 3 DCMC1, (**e**) Mode 1 DCMC2, Mode 2 DCMC2, Mode 2 CCM , (**f**) Mode 3 DCMC2,Mode 2 DCMC2, Mode 2 CCM, Mode 3 CCM.

$$iL_1 + iL_2 = Isw_1 \tag{2}$$

$$\left.\begin{aligned} Ic_2 = Ic_3 = Isw_2 = iL_3 \\ iL_4 = Ic_4 \end{aligned}\right\} \tag{3}$$

$$ID_1 = iL_2 = IC_1 \tag{4}$$

$$IC_5 = I_o \tag{5}$$

$$\left.\begin{aligned} iL_1 &= \frac{V_g}{L_1} \\ iL_2 &= \frac{Vc_1}{L_2} \\ iL_3 &= \frac{Vc_2 + Vc_3 + Vc_1}{L_3} \\ iL_4 &= \frac{Vc_2 + Vc_3 + Vc_1 - Vc_4}{L_4} \\ I_o &= \frac{V_o}{RL} \end{aligned}\right\} \tag{6}$$

where VL is the voltage across the inductor, iL is the current through the inductor, Ic is the current through the capacitor, Io is the output current, ID is the diode current, Vg is the input voltage source, Vo is the output voltage of the proposed converter, Vc is the voltage across the capacitor, and RL is the resistive load.

Mode 2 [t0–t1] the power MOSFETs are in the off state as zero gate voltage is provided to them by the Pulse generator to keep them off. Both diodes D_2 and D_3 are in the on state, and D_4 is also in the on state during this mode. L_1 will discharge its energy to C_1 while charging of C_2 and C_3 occurs in a nonlinear manner. L_2 will begin to discharge its power to C_2 and C_3. D_1 remains in the on state in this mode due to the discharging current of L_2 through it. C_2 and C_3 will start storing a significant amount of energy from L_1 and L_2. C_5 will receive a large amount of energy from L_3 and L_4 during the discharging time, allowing high power to be supplied to the load. The proposed converter for this mode is depicted in Fig. 2b. Here are the voltage and current equations for the various components in this state:

$$\left.\begin{aligned} VL_1 &= V_g - Vc_1 - Vc_2 \\ VL_2 &= -Vc_2 \\ VL_3 &= Vc_4 + VL_4 \\ VL_4 &= -Vc_5 \\ Vc_5 &= V_o \end{aligned}\right\} \tag{7}$$

$$\left.\begin{aligned} iL_1 &= \left(\frac{Vg}{L_1} - \frac{Vc_1}{L_1} - \frac{Vc_2}{L_1}\right) \\ iL_2 &= \frac{-Vc_2}{L_2} \\ iL_3 &= \frac{Vc_4 + VL_4}{L_3} \\ iL_4 &= \frac{-V_o}{L_4} \\ I_o &= \frac{V_o}{RL} \end{aligned}\right\} \tag{8}$$

$$iL_1 + iL_2 = ID_2 + ID_3 = Ic_2 + Ic_3 \tag{9}$$

$$iL_3 + iL_4 = ID_4 \tag{10}$$

$$ID_1 = iL_2 \tag{11}$$

$$iL_1 = Ic_1 \tag{12}$$

Mode 3 [t1–t2]: The power MOSFETs are still in the off state, and diodes D_2 and D_3 remain in the on state. The energy of L_1 is discharged nonlinearly due to resonance with C_1, resulting in energy transfer to C_1 to minimize input current ripple and to charge C_2 and C_3. During the time (D + m1), L_2 is not charged and reaches zero, resulting in ID_1 being zero. Energy is continued to be received by C_2 and C_3 only from L_1. Energy continues to be supplied to C_5 from L_3 and L_4 during the discharging period, while high power is still received by the load

from C_5. The proposed converter for this mode is shown in Fig. 2c. The voltage equations remain the same as in the previous mode, and the current equations for this state are as follows:

$$Ic_5 = Io = iL_3 + iL_4 \tag{13}$$

$$iL_1 = ID_2 + ID_3 \tag{14}$$

$$ID_1 = iL_2 = 0 \tag{15}$$

$$Ic_2 + Ic_3 = iL_1 \tag{16}$$

Mode 4 [t2–t3]: The power MOSFETs are still in the off state, and only D_2 and D_3 remain on. In this mode, D_4 is turned off, while D_1 remains off. The energy stored in L_1 is discharged through C_1 to charge C_2 and C_3, which store a large amount of energy for the next gate pulse to supply a substantial amount of energy to the load. L_4 will have the same current values as L_3 but in opposite directions ($iL_3 = -iL_4$). C_5 supplies high power to the load. The proposed converter for this mode is shown in Fig. 2d. The waveforms for these four operational modes are illustrated in Fig. 3a.

Operation of the proposed converter in DCMC2

When Vg is decreased to its minimum value, the proposed converter can operate in DCMC2 with five modes of operation, as illustrated in Fig. 3b, which presents the waveform of the proposed converter in DCMC2. In this mode, the input current remains in CCM at both low and high duty ratios, while C_1 operates in a resonant mode with L_2. Conversely, the current through L_3 and L_4 operates in DCM. This approach effectively reduces the voltage stress across the auxiliary switch, thereby decreasing the losses in the proposed converter.

Mode 1 [0–t0]: Both Sw_1 and Sw_2 are simultaneously switched on, resulting in the switching off of diodes D_2, D_3, and D_4. L_1 accumulates energy linearly from the input source Vg. L_2 accumulates energy from C_1 through Sw_1 until (D-2m), at which point the charge in C_1 becomes zero. D_1 is switched on, and the capacitors currents C_2 and C_3 are utilized to charge L_3 through Sw_2, while L_4 charges from C_4. C_5 supplies energy to the load. The proposed converter for this mode is illustrated in Fig. 2a,e.

Mode 2 [t0–t1]: The power MOSFETs remain in the on state. Both diodes, D_2 and D_3, turn on during this state because the charge in C_1 becomes zero at (D-2 m), as shown in Fig. 3b. Consequently, L_2 begins to discharge energy through D_2 and D_3 to charge L_3 and L_4. This reduces the current stress through Sw_1, as depicted in Fig. 11b. The current through Sw_1 is solely sourced from L_1. D_4 remains off, and L_1 continues to accumulate energy from the input voltage source. In this mode, D_1 experiences very low voltage stress, implying that L_2 acts as an open circuit during the time (D-m). Furthermore, in this mode, D_2 and D_3 experience (ZVS) across them from ((D-2m) < t < (D-m)). After this time, both of them work as a path to pass the current from L_2. L_3 and L_4 continue to charge from C_2, C_3 and L_2. L_2's charge becomes zero at (D-m). C_5 still supplies power to the load. The proposed converter for this mode is shown in Fig. 2e,f. The current equations for this state are provided below.

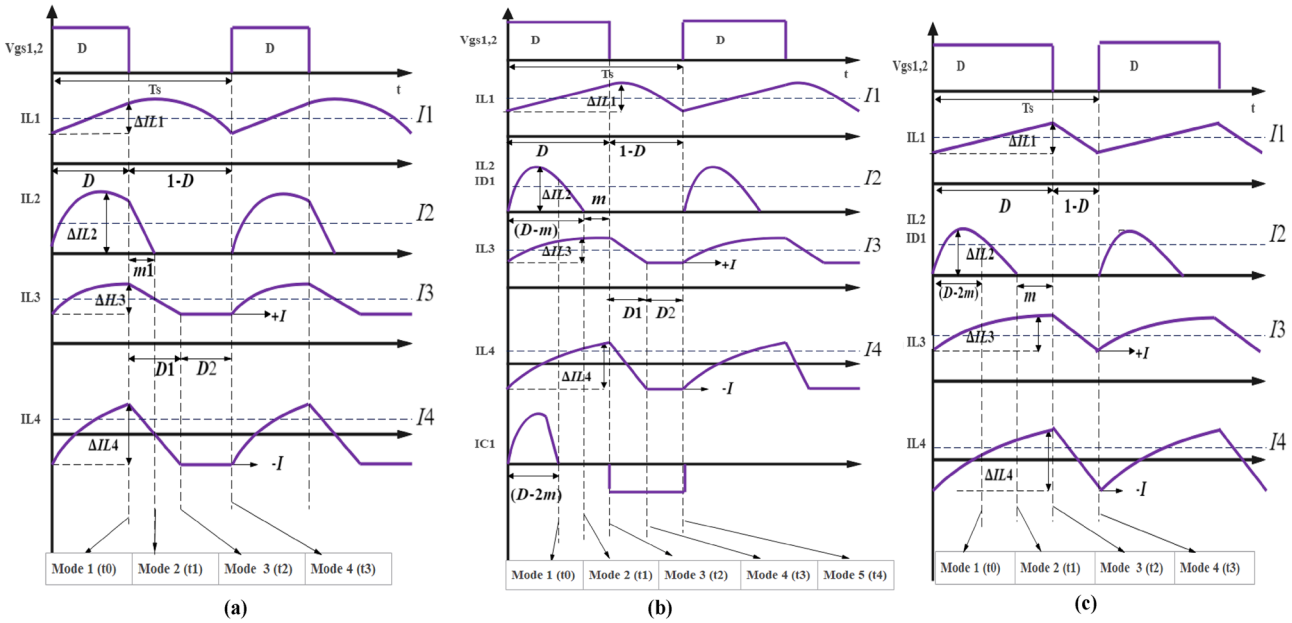


Figure 3. (**a**) Time-domain waveforms for the proposed DC–DC converter operating in DCMC1. (**b**) Time domain waveforms for the proposed DC–DC converter operating in DCMC 2. (**c**) Time domain waveforms for the proposed DC–DC converter operating in CCM.

$$\left.\begin{aligned} iL_2 &= \frac{Vc_1}{L_2}(D-2m) \\ iL_2 &= \frac{(-Vc_2)}{L_2}\ from\ (D-2m) < t < (D-m) \\ iL_3 &= \frac{Vc_2 + Vc_3}{L_3},\ from\ \ D < t < (D-2m) \\ iL_3 &= \frac{Vc_3}{L_3},\ from\ \ (D-2m) < t < D \end{aligned}\right\} \tag{17}$$

$$\left.\begin{aligned} Isw_1 &= iL_1 + iL_2,\ from\ 0 < t < (D-2m) \\ Isw_1 &= iL_1(only)\ from\ (D-2m) < t < D \\ Isw_2 &= Ic_2 = Ic_3,\ from\ 0 < t < (D-2m) \\ Isw_2 &= Ic_2 + Ic_3,\ from\ (D-2m) < t < D \end{aligned}\right\} \tag{18}$$

Mode 3 [t1–t2] The Power MOSFETs remain in the "on" state, and both diodes D_2 and D_3 are still turned on. L_2 is treated as an open circuit, with D_1 is switched off. L_1 continues to charge from the input source, and L_3 and L_4 will continue to accumulate current from C_2 and C_3 through Sw_2. C_5 will begin accumulating a larger amount of energy from L_3 and L_4 through D_4, and this energy will be used to supply power to the load. The proposed converter for this mode is depicted in Fig. 2f. The current equations for this mode are presented in Eq. (18).

Mode 4 [t2–t3] The Power MOSFETs are both turned off, and D_2 and D_3 remain in the "on" state, while D_4 is switched on. L_2 is treated as an open circuit in this mode, and L_1 is discharging energy to charge C_1, C_2, and C_3 while storing a significant amount of energy to supply to the load. C_5 continues to receive energy from L_3 and L_4 during the discharging period (D1), while the load continues to receive high power from C_5. The proposed converter for this mode is illustrated in Fig. 2c.

Mode 5 [t3–t4]: Both MOSFETs remain in the off state, and D_2 and D_3 are still on. D_4 is now turned off. During this period (D2), L_3 will carry the same current as L_4 but in opposite directions: $iL_3 = -iL_4$. The load will receive a high amount of energy from C_5. The proposed converter for this mode is depicted in Fig. 2d.

Operation of the proposed converter in CCM

This mode is activated when the load current surpasses a 70% duty cycle, as depicted in Fig. 4, and when the load factor (k) exceeds the critical value of K (Kcrit). In this mode, the proposed converter maintains the input current in CCM, with L_2 still operating in resonance mode with C_1, and the current through L_3 and L_4 also remains in CCM. Furthermore, the voltage transfer ratio in this mode experiences a significant increase. When the proposed converter operates in CCM, it exhibits four distinct modes of operation. The time-domain waveforms for the proposed DC–DC converter operating in CCM are also illustrated in Fig. 3c.

Mode 1 [0–t0]: same as for Mode 1 of DCMC2

Mode 2 [t0–t1]: same as for Mode 2 of DCMC2

Mode 3 [t0–t1]: same as for Mode 3 of DCMC2

Mode 4 [t2–t3]: Both MOSFETs Sw_1 and Sw_2 are in the off state, D_2 and D_3 remain on. L_1 will discharge energy linearly due to the short discharging time required to charge C_1, C_2, and C_3 with a large amount of power. L_2 is an open circuit with no current, and D_1 remains off. Both capacitors C_2 and C_3 accumulate a significant amount of energy from L_1, while C_4 starts to store a large amount of energy from L_3 and L_4. The current waveform of L_3 and L_4 will be the same but in opposite directions, without a constant current (I), and the load receives a substantial power supply from C_5 through D_4. The proposed converter for this mode is shown in Fig. 2c.

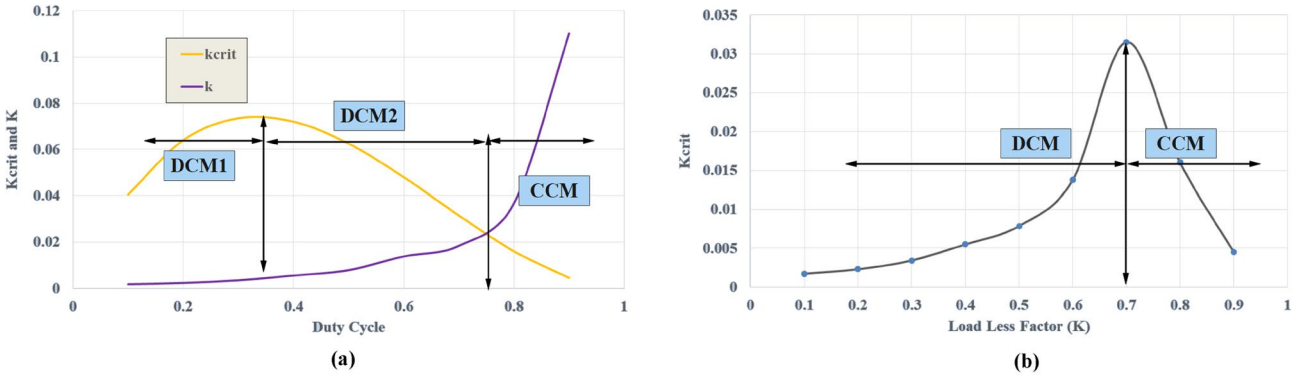


Figure 4. Dynamic response of the proposed converter (**a**) Kcrit and K versus duty cycle, (**b**) load less factor (K) versus (Kcrit).

Voltage transfer gain calculation

The voltage transfer gain of the proposed converter is calculated under two conditions when the converter operates in DCM and CCM.

Voltage transfer gain calculation at DCMC1

To derive the voltage gain equation for the proposed converter operating in DCMC1, the volt-second balance equation is applied to L_1, L_2, L_3, and L_4 using Eqs. (1) and (7). This process yields Eqs. (19) and (20), which can be solved to obtain Eqs. (22) and (24). Additionally, during the steady state in DCMC1 at low duty cycle, the average voltage across C_1 can be determined using Eq. (21). Equation (22) establishes the relationship between C_2 and the input voltage source. In this context, (m1) represents the discharging time of L_2, and its values can be obtained from Eq. (23), which is a function of (D, Vg, Vc_2, and Vc_3). (D1) denotes the discharging time of L_3 and L_4, and it can be calculated using Eq. (24).

$$\frac{1}{Ts}\left(\int_0^{DTs}(V_g+Vc_1)dt+\int_D^{Ts}(V_g-Vc_1-Vc_2)dt+\int_{DTs}^{m1Ts}(-Vc_2)dt\right)=0 \tag{19}$$

$$\frac{1}{Ts}\left(\int_0^{DTs}2(Vc_2+Vc_3+Vc_1)-Vc_4dt+\int_D^{D1Ts}(-2Vo)dt\right)=0 \tag{20}$$

$$Vc_1=\frac{Vg}{(1-D)}-Vc_2 \tag{21}$$

$$Vc_2=\frac{V_gD}{(1-D)(D+m1)} \tag{22}$$

$$m1=\frac{V_gD}{Vc_2(1-D)}-D \tag{23}$$

$$D1=\frac{D(Vc_2+Vc_3+Vc_1)}{V_o} \tag{24}$$

$$\left.\begin{aligned}<I1>&=\frac{V_g}{2L_1}DTs\\ <I2>&=\frac{V_gD^2(V_g-(1-D)Vc_2)}{2fsL_2(1-D)^2Vc_2}\end{aligned}\right\} \tag{25}$$

$$\left.\begin{aligned}iL_1peak&=\frac{V_gDTs}{L_1}\\ iL_{2Peak}&=\frac{(V_g-(1-D)Vc_2)DTs}{L_2(1-D)}\end{aligned}\right\} \tag{26}$$

Equations (25) and (26) represent the average and peak current through inductors L_1 and L_2, respectively. Equation (27) provides the average inductor current in L_3 and L_4. Meanwhile, Eqs. (28) and (29) deal with the peak inductor current in L_3 and L_4, respectively. To find the output current, we can calculate it by adding the currents from Eqs. (27), as demonstrated in Eq. (30). In this context, (LE) represents the equivalent inductors of L_3 and L_4, as shown in Eq. (31).

$$\left.\begin{aligned}<I3>&=\frac{(Vc_2+Vc_3+Vc_1)}{2L_3}DTs(D+D1)+I\\ <I4>&=\frac{(Vc_2+Vc_3+Vc_1-Vc_4)}{2L_4}DTs(D+D1)-I\end{aligned}\right\} \tag{27}$$

$$iL_{3peak}=\frac{(Vc_2+Vc_3+Vc_1)}{L_3}DTs \tag{28}$$

$$iL_{4peak}=\frac{(Vc_2+Vc_3+Vc_1-Vc_4)}{L_4}DTs \tag{29}$$

$$I_o=\frac{(Vc_2+Vc_3+Vc_1)DD1}{FsLE} \tag{30}$$

$$LE = \frac{L_3 L_4}{L_3 + L_4} \tag{31}$$

$$Vo = \frac{(Vc_2 + Vc_3)^2 D^2}{LEIoFs} \tag{32}$$

Equation (32) represents the output voltage of the proposed converter. The voltage gain equation for the proposed converter in DCMC1 can be obtained through Eq. (33), and solving this equation helps determine the load factor (K). Consequently, the voltage gain equation for the proposed converter as a function of K can be derived in Eq. (34). To find the critical load factor (Kcrit), we can use Eq. (35). The boundary condition of the proposed converter between CCM and DCM at Kcrit is shown in Eq. (36).

$$VG(DCMC1) = \frac{2VgD^4 TsRL}{LEV_o(1-D)^2(D+m1)^2} \tag{33}$$

$$\left.\begin{aligned} VG(DCMC1) &= \frac{D^2}{(1-D)(D+m1)}\sqrt{\frac{2}{k}} \\ K &= \frac{2LE}{TsR_L} \end{aligned}\right\} \tag{34}$$

$$k_{crit} = \frac{(1-D)^2 D}{2} \tag{35}$$

$$K_{crit} = \begin{cases} \text{if Kcrit} > \text{K Proposed Converter work In DCM} \\ \text{if Kcrit} < K \text{ Proposed Converter work In CCM} \end{cases} \tag{36}$$

Voltage transfer gain calculation at DCMC2

To derive the voltage gain equation for the proposed converter when it operates in DCMC2, volt-second balance equations are applied to L_1, L_2, L_3, and L_4 using Eqs. (17) and (7), which results in Eq. (37). Solving this equation leads to the results shown in Eqs. (38).

$$\left.\begin{aligned} &\frac{1}{Ts}\left(\int_0^{DTs}(V_g)dt + \int_{(D-2m)T}^{(D-m)Ts}(-Vc_2)dt\right) \\ &+\int_0^{(D-2m)Ts}(Vc_1)dt + \int_D^{Ts}(V_g - Vc_1 - Vc_2)dt) \\ &+\frac{1}{Ts}(\int_0^{(D-2m)Ts} 2(Vc_2 + Vc_3)dt + \int_{(D-2m)}^{(D-m)Ts} 2(Vc_3)dt \\ &+\int_D^{D1Ts}(-2Vo)dt = 0 \end{aligned}\right\} \tag{37}$$

$$\left.\begin{aligned} &D(V_g) - m(Vc_2) + (1-D)(V_g - Vc_1 - Vc_2) + (D-2m)(Vc_1) \\ &2(D-2m)(Vc_2 + Vc_3) + 4mVc_3 - 2D1Vo = 0 \end{aligned}\right\} \tag{38}$$

$$m = D - \frac{\sqrt{L_2 C_1}}{Ts} \tag{39}$$

$$Vc_2 = \frac{Vg}{(1-D)} \tag{40}$$

$$D1 = \frac{D(Vc_2 + Vc_3)}{V_o} \tag{41}$$

$$VG(DCMC2) = \frac{2VgD^2 TsRL}{LEV_o(1-D)^2} \tag{42}$$

The value of (m) can be determined using Eq. (39), which depends on the values of L_2 and C_1. This approach reduces the current stress across the main switch as the load current increases. Additionally, it lowers the voltage stress across both the main and auxiliary switches, resulting in a reduction in voltage stress on all switched inductors, and diodes. When the charge in C_1 reaches zero at (D-2m), the two diodes D_2 and D_3 will operate

at ZVS, as shown in Fig. 13c. Equation (40) describes the voltage across C_2. The discharging time of L_3 and L_4, denoted as (D1), can be determined from Eq. (41) after solving Eq. (38). Finally, the voltage gain equation of the proposed converter in DCMC2 is provided in Eq. (42).

Voltage transfer gain calculation at CCM

By applying the volt-second balance equation to L_1, L_2, L_3, and L_4 in Eq. (43) at different times, the results can be found in (44) and (45) by substituting the value of Vc_1 from Eq. (21) into Eq. (44). The voltage transfer gain of the proposed DC–DC converter when operating in CCM is given by Eq. (46). It can be observed that the voltage gain ratio equations of the proposed converter in DCM and CCM exhibit higher voltage gain ratios than those of previous DC–DC converters, as shown in Table 2.

$$\frac{1}{Ts}\left(\int_0^{DTs}(V_g)dt+\int_D^{Ts}(V_g-Vc_1-Vc_2)dt\right)=0 \tag{43}$$

$$D(V_g)+(1-D)(V_g-Vc_1-Vc_2-Vc_3)=0 \tag{44}$$

$$D(Vc_2+Vc_3)=(1-D)V_o \tag{45}$$

$$VGCCM=\frac{V_o}{V_g}=\frac{2D}{(1-D)^2} \tag{46}$$

Voltage stress across power MOSFETs and diodes

In this section, the voltage stresses across the four power diodes and the voltage stresses across the power MOSFETs main and auxiliary are calculated both in DCM and CCM.

Voltage across power MOSFETs and diodes in DCM

From Eq. (47), it can be determined that the voltage across D_1 depends on the average voltage across C_2, which is a very small value. Additionally, Eq. (48) provides information about the voltage across diodes D_2 and D_3 when the converter is operated in DCM, which is also very small and depends on the input voltage. Equation (49) allows us to calculate the voltage across MOSFET Sw_1, which is equal to the input voltage as an average voltage. Equations (50) and (51) enable us to calculate the voltage across power MOSFET Sw_2 and the voltage across D_4, respectively. It can be seen that the voltage stress across diodes and switches is significantly reduced when the proposed converter is operated in DCMC1.

$$VD_1=\sqrt{\frac{LEV_o^2}{RLD^2Ts}} \tag{47}$$

$$VD_2=\frac{V_g}{(1-D)}=VD_3 \tag{48}$$

$$Vs_1=V_g\ \ average\ \ voltage\ \ across\ \ \mathrm{Sw_1} \tag{49}$$

$$Vs_2=\sqrt{\frac{LEV_o^2}{RLD^2Ts}} \tag{50}$$

$$VD_4=V_o \tag{51}$$

Voltage across power MOSFETs and diodes in CCM

Equation (52) allows us to determine the voltage across D_1 in CCM. During the time period (D-m), the voltage across D_1 is reduced due to the resonant mode between L_2 and C_1. Additionally, inductor L_2 remains uncharged and functions as an open circuit during this period. By utilizing Eq. (53), the voltage stress across Sw_1 can be determined, and Eq. (54) can be used to find the voltage across diodes D_2 and D_3 in CCM. The voltage stress on power MOSFETs and power diodes is significantly reduced, resulting in decreased losses for the proposed DC–DC converter.

$$VD_1=\frac{V_g}{2(1-D)} \tag{52}$$

$$VD_2=\frac{(1-D)V_o}{D}=VD_3 \tag{53}$$

$$Vs_1 = \frac{V_g}{(1-D)} \tag{54}$$

$$Vs_2 = \frac{V_o(1-D)}{2D} \tag{55}$$

$$VD_4 = \frac{2V_gD}{(1-D)^2} \tag{56}$$

Furthermore, the voltage stress across D_2 and D_3 decreases, as both diodes operate with (ZVS) across them when one cell switched capacitor charge in C1 becomes zero from (D-2m < t < D), as shown in Fig. 11f. At the time (D-2m), the inductor current L_2 flows through diodes D_2 and D_3, as depicted in Fig. 11c. Upon observing Fig. 4a,b, it becomes evident that the proposed converter operates in DCMC1 when the duty cycle is below 30%, provided that Kcrit (a critical factor) is lower than the load factor K. When the input voltage decreases to its minimum value, the converter operates in DCMC2 with a duty cycle above 30%. However, as the load increases and K exceeds Kcrit, the suggested converter can operate in CCM, as shown in Fig. 4, with a duty ratio exceeding 70%.

Proposed converter design: component selection strategies

In this section, components for a 400 W prototype of the proposed DC–DC converter have been designed to validate the experimental results. The suggested converter comprises four inductors with very small values, five capacitors with low values, two power MOSFETs with low on-state resistance (Ron), and a simple gate drive circuit, along with four power diodes. The components have been designed to achieve a high voltage transfer gain, and their specifications for the 400 W model can be found in Table 1. To design the capacitors and inductors of the converter, Eq. (57) can be utilized to calculate the value of L_1 with low ripple input current. Ripple of input current (ΔiL_1) can be found in Eq. (57). The resonant mode between C_1 and L_2 can be employed to find the value of L_2 from Eq. (58). The values of inductors L_3 and L_4 can be obtained from Eq. (59), where L_3 and L_4 are in parallel connection. The values of C_2 and C_3 with very low ripple voltage can be derived from Eq. (60), and the value of C_4 can be determined using Eq. (61). Finally, the value of C_5 can be computed from Eq. (62) to achieve very low output voltage ripple.

$$\left.\begin{aligned} L_1 &= \frac{V_gD}{Fs\Delta iL_1} \\ \Delta iL_1 &= (10\%to25\%)\frac{Vo}{Vg}Io_{\max} \end{aligned}\right\} \tag{57}$$

$$\left.\begin{aligned} L_2 &= \frac{\Delta VRL(1-D)^2}{8VoD^2\pi^2fS} \\ C_1 &= \frac{2V_{out}D^2}{\Delta VR_LFs(1-D)^2} \end{aligned}\right\} \tag{58}$$

$$\left.\begin{aligned} L_3 &\geq \frac{V_g(1-D)R_L}{2V_oFs} \\ L_4 &\geq \frac{V_gDR_L}{V_o(1-D)Fs} \end{aligned}\right\} \tag{59}$$

$$C_2 = \frac{V_{out}D}{\Delta VR_LFs(1-D)} = C_3 \tag{60}$$

$$C_4 = \frac{VoD}{\Delta Vc_4.FsRL} \tag{61}$$

$$C_5 = \frac{V_oD}{\Delta V_oFsRL} \tag{62}$$

Table 1 indicates that the utilization of a high switching frequency can decrease the size of inductors and capacitors in the proposed converter, leading to a lightweight and compact prototype with reduced costs. The specifications for the inductors include the use of flat wire with minimal internal resistance, effectively lowering losses in the proposed converter. Moreover, the power MOSFETs employed feature extremely low on-state resistance, thereby increasing voltage transfer gain and decreasing conduction power losses. In order to.

SiC MOSFET	**650 *v*, *Ron* = 57 mΩ (IMZA65R057M1H)**
SiC Schottcky	1200 V 40 A,Vf = 1.1 IDWD40G120C5
*L*1, *L*2 *L*3 *and L*4	100 µH, 2.9 mΩ, 2.2 µH, 1.3 mΩ 100 µH, 2.9 mΩ *and* 15 µH, 1.9 mΩ (flat wire with very small size)
*C*1, *C*2=*C*3 *C*4, *and*C5	2 µF 100 V, 200 µF 100 V 10 µF 500 V *and*, 100 µF 500 V
V_g	20 − 40 V
Vo	200 − 400 V
Power	200 W, 400 W
RL	200 Ω, 400 Ω
Duty Cycle	0.27 at 200 w at 40 V 0.33 *at* 400 w at 40 V
Frequency	150 kHZ
Ic drive	1EDI60N12AF
Inductor size (L1,L3 and L4) L2 size	(L/2.5 cm*W/2.25 cm*H/1.78 cm) (L/1.5 cm*W/1.2*H/1.5 cm)
Input current ripple percentage	(10–25%)

Table 1. Design of prototype components for proposed converter.

Comparison of the proposed converter with other high boosting converters

To validate the superior performance of the proposed converter in achieving a high voltage gain and low voltage stress across power devices, a comparison is conducted in this section between the proposed converter and previous DC–DC converters. The previous DC–DC converters were simulated using Matlab Simulink under the same conditions. Figure 5 shows that a higher voltage transfer gain is exhibited by the proposed converter compared to the previous converters. Additionally, the high gain of the proposed converter at a low duty cycle indicates several benefits, including higher efficiency, lower switching losses, low voltage stress across power devices, lower conduction losses with rms value current, and fewer capacitors and inductors required to achieve high voltage gain. The voltage gain of the proposed converter, approximately 13.5, can be calculated using Eq. (42) when the converter operates in DCM2.When looking at Fig. 6a, it can be seen that the voltage across the MOSFET device in the proposed converter is lower than that in the previous converters when compared to the gain ratio. In Fig. 6b, it can be observed that the voltage across the diode to the voltage source in the proposed DC–DC converter is lower than that in the previously used boosting converters.

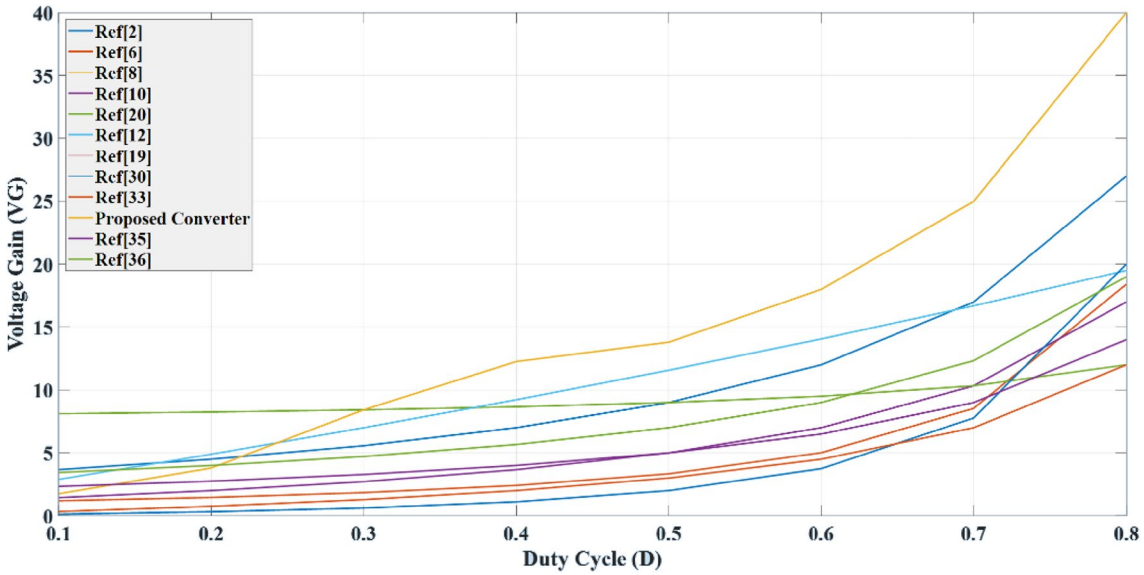


Figure 5. Comparison of voltage transfer gain of converters.

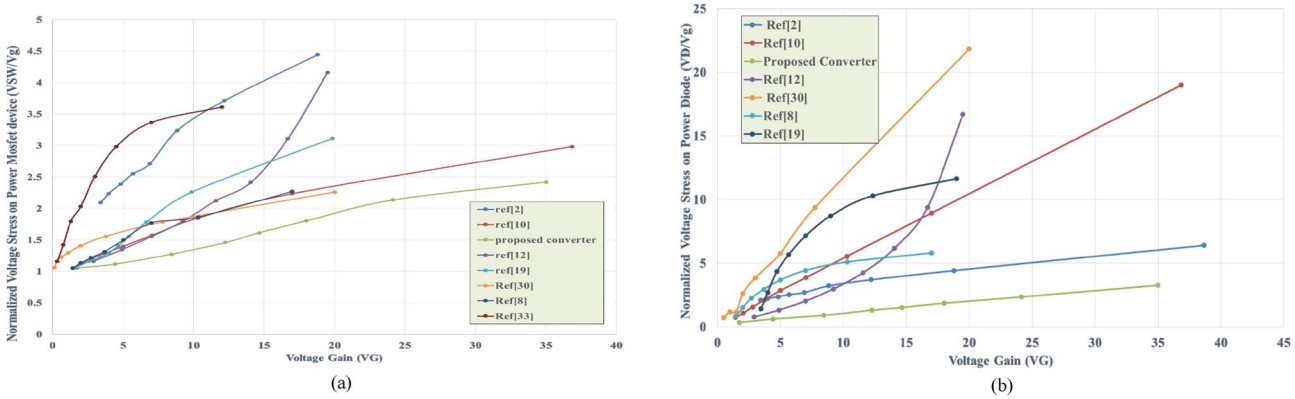


Figure 6. (**a**) Voltage stress across power MOSFET versus voltage gain, (**b**) voltage stress across power diode versus voltage gain.

Items	Proposed converter	Reference[2]	Reference[6]	Reference[8]	Reference[10]	Reference[20]	Reference[12]	Reference[19]	Reference[30]	Reference[33]	Reference[35]	Reference[36]
F_S (KHZ)	150	100	30	30	50	100	1	24	24	30	50	50
Vg	20–40v	10v	60v	29v	40v	40v	24v	20v	20v	25v	25v	48v
Vo	200v 400v	120v	300v	325v	260v	364v	221v	300v	172.2v	110v	200v	408v
L	4	3	5	4	3	4	4	2	3	4	2	2
C	5	6	5	6	3	7	2	4	3	6	5	3
Diodes D	4	6	0	4	2	3	8	4	3	3	4	3
Switches SW	2	1	7	2	2	2	2	1	1	1	1	2
Duty cycle	33%	73.5%	70%	73%	72%	71%	42%	77%	70%	60%	72%	60%
Power	400w	50 w	200w	220w	200w	265w	200w	250w	100w	110w	200w	250w
Input current	No pulsating	Pulsating	Pulsating	No pulsating	Pulsating	No pulsating	Pulsating	No pulsating	No pulsating	Pulsating	No pulsating	Pulsating at low D
Efficiency %	96.3	88	93	95.5	96	94.5	92	91.5	91.4	92	93	91
VG at D = 0.75	24	21	12.4	13	13	11	17.2	13.5	12	9	11	15
$VG = \frac{Vo}{Vg}$	$\frac{2D}{(1-D)^2}$	$\frac{3(1+D)}{(1-D)}$	$\frac{(1-\frac{1}{3}D)}{(1-D)^2}$	$\frac{(1+3D)}{(1-D)}$	$\frac{(1+3D)}{(1-D)}$	$\frac{(8-7D)}{(1-D)}$	$\frac{(1+18.25D)}{(1-0.25D)}$	$\frac{(3+D)}{2(1-D)}$	$\frac{(D)}{(1-D)^2}$	$\frac{(3D)}{(1-D)}$	$\frac{(2+D)}{(1-D)}$	$\frac{(3+D)}{(1-D)}$

Table 2. A comparative analysis of the proposed converters and previous high-boosting converters.

Table 2 presents a comparison between the proposed DC–DC converter and previous converters. The comparison focuses on the number of inductors, capacitors, diodes, switching frequency, input current, duty cycle percentage, and MOSFETs utilized in both the proposed and previous boosting converters. The results indicate that the previous boosting DC–DC converters are operated at a lower switching frequency than the proposed converter, resulting in higher inductor and capacitor values, as well as higher parasitic resistance. Additionally, the MOSFET's internal resistance at low switching frequency is high, leading to high conduction and switching losses. Moreover, the values of inductors and capacitors used in previous converters are larger, resulting in a larger, more costly, and heavier system. The previous boosting DC–DC converters can boost low voltage with a high voltage transfer ratio, but at an extremely high duty ratio. In contrast, the proposed converter can boost low voltage sources to a variable output voltage between 200 and 400 V at a lower duty ratio than previous boosting converters. The input current in the proposed converter is non-pulsating at both low and high duty cycles, whereas the converters in References[2, 6, 10, 12] exhibit pulsating currents at low duty cycles. Finally, the proposed converter has a higher voltage gain compared to previous boosting DC–DC converters, making it more suitable for renewable energy systems that require variable and fixed high output voltage with a wider range in the duty ratio.

Control strategy of the proposed converter

The proposed converter controller, as depicted in Fig. 7, employs double PI controllers. The first controller serves as the inner loop controller and is designed to regulate the load current, while the second controller functions as the outer loop controller and is responsible for regulating the output voltage. The PI voltage controller takes the error between the reference voltage and the output voltage as its input, and its output is the reference current, which is restricted to prevent excessive current draw from the converter. The error between the reference current

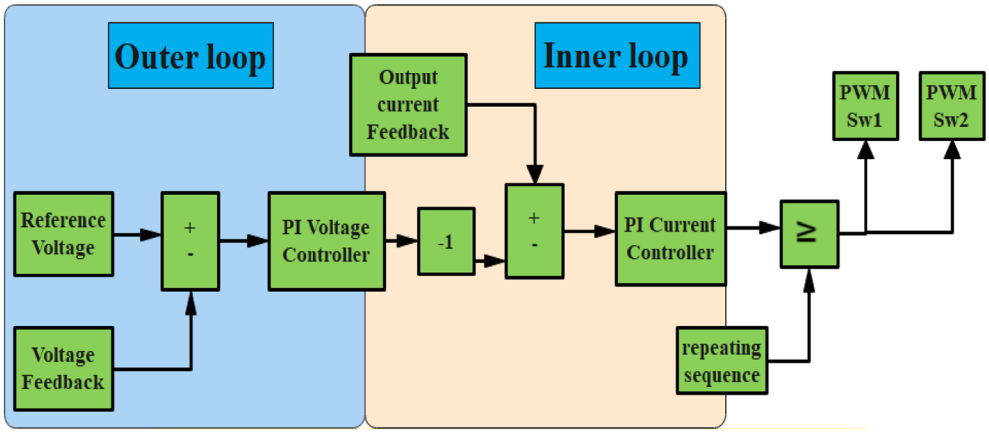


Figure 7. Voltage and current controller of proposed converter.

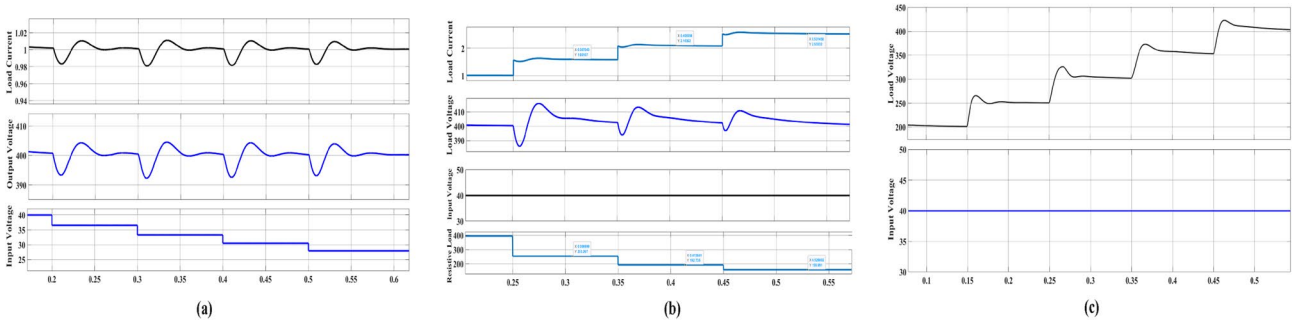


Figure 8. (**a**) Output of proposed converter at variable input voltage, (**b**) variable load current at fixed output and input voltage of the proposed converter, (**c**) variable load voltage 200–400 V at fixed input voltage.

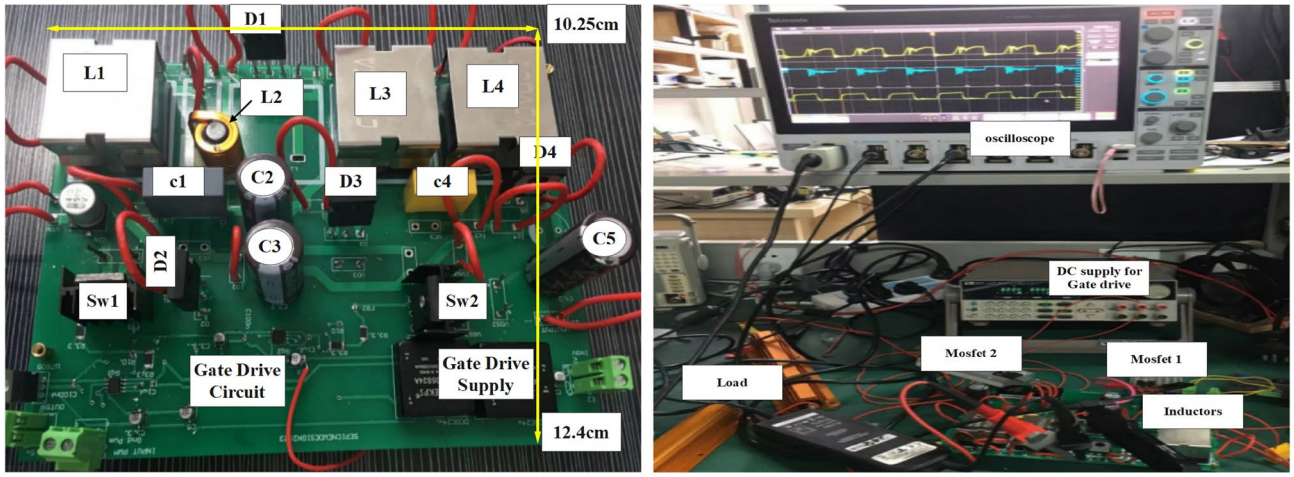
and the output current is then fed into the PI current controller. The controller design process involves utilizing an equation that describes a PI controller with proportional and integral action control parameters KP and Ki. In Fig. 8(a), the proposed converter can maintain a constant output voltage of 400 V, regardless of input voltage changes from 40 to 30 V. This exemplary performance highlights the stability of the proposed converter and its capacity to deliver a consistent output voltage despite varying input voltage levels. In Fig. 8(b), the proposed converter can validate a constant output voltage at a fixed input voltage with variable load current. In Fig. 8(c), it can be observed that the proposed converter can verify variable output voltage ranging from 200 to 400 V at a fixed input voltage. This makes the proposed converter more suitable for a wide range of applications.

The dual PI controller of the proposed converter demonstrates enhanced robustness and reliability, facilitating a quicker attainment of steady state. Furthermore, the proposed converter, equipped with current and voltage controllers, can achieve a wide range of duty ratios to supply high load current.

Results and discussions of proposed converter: simulation and experiment

In this section, a prototype of the 400 W converter design was constructed to confirm the accuracy of the simulation and experimental outcomes, as depicted in Fig. 9a. The converter was subjected to experimental evaluation in the laboratory, as shown in Fig. 9b. Furthermore, the laboratory results were verified using MATLAB software under various conditions. It should be noted that non-ideal inductors and capacitors were used, and all parasitic resistances were accounted for in the proposed DC–DC converter.

In Fig. 10a depicts a PWM generator producing a 33% duty ratio with an output voltage of 413 V. The voltage source is 40 V, and the voltage across capacitors C_2 is 60 V at a load current of 1 A. Figure 10b displays the current flowing through inductors L_1, L_2, L_3, and L_4. It is evident that iL_1 experiences no pulsation at the low duty cycle of 33% with very low ripple input current. Current L_2 discharges to C_2 and C_3 during period (m1), while the currents through L_3 and L_4 have the same shape but in reverse directions. Figure 10c shows the voltage across inductors. It is noticeable that the voltage across L_2 is Vc_2 during the off state of period (m1), and it is zero from ($D + m1 < t < Ts$). Figure 10d shows the current through capacitors, while Fig. 10e displays the voltage across power MOSFETs and diodes of the proposed converter. The voltage stress across S_{W1} is significantly reduced, and the average voltage is equal to the input voltage. The voltage across Sw_2 is equal to the output voltage during the very short period ($D < t < D1$) and Vc_3 voltage during the very long time ($D1 < t < Ts$). Moreover, the voltage across D_1, D_2, and D_3 is equal to Vc_3. Figure 10f illustrates the current through MOSFETs and power diodes. It



(a) (b)

Figure 9. (**a**) PCB design of the prototype proposed converter, (**b**) experimental prototype test of the proposed converter.

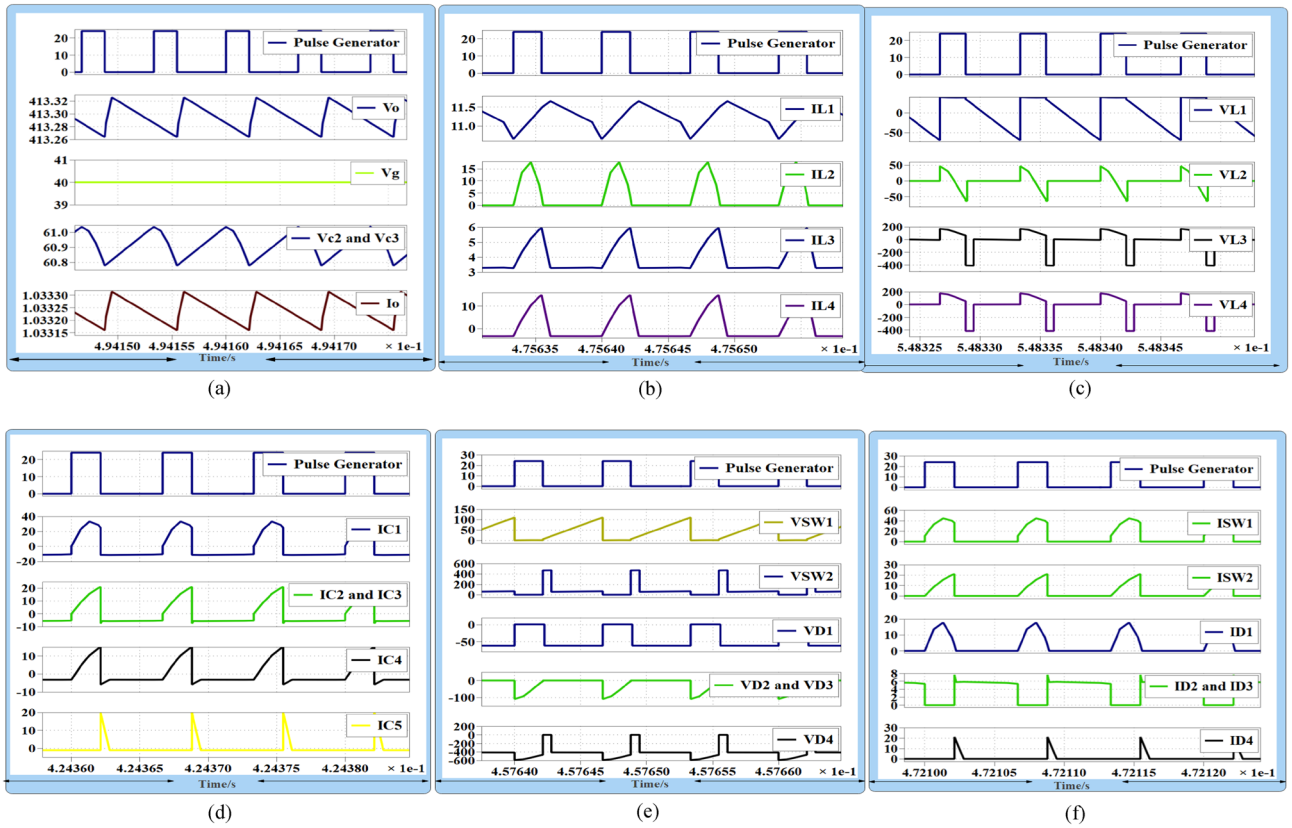


Figure 10. Proposed converter operation at DCMC1 (**a**) gate source voltage at D = 0.33, Vo = 413 V, Vc_2 = 60 V, Vg = 40 V and load current Io = 1 A, (**b**) iL_1, iL_2, iL_3 and iL_4, in DCMC1, (**c**) VL_1, VL_2, VL_3 and VL_4, (**d**) capacitors Current Ic_1, Ic_2, Ic_3, Ic_4 and Ic_5, (**e**) voltage stress, Vsw_1, Vsw_2 and VD_1, VD_2, VD_3 and VD_4, (**f**) Isw_1, Isw_2 I_{D1}, I_{D2}, I_{D3} and I_{D4}.

can be observed that IS_{W1} equals iL_1 and iL_2, while the current through IS_{W2} is equal to capacitor current C_2. Furthermore, the current through D_2 and D_3 equals L_1 and L_2 current during the off state.

During this experiment, the voltage transfer gain equals 10 at a duty cycle of 0.33. The proposed converter exhibits zero pulsating input current at very low duty ratios. Additionally, the voltage across power MOSFETs and diodes is significantly reduced, indicating very small values. Hence, the proposed DC–DC converter is more suitable for renewable energy sources (RES) applications. After incorporating all parasitic components, the simulations show that the proposed converter operates in DCMC2. At an input voltage of 20 V, Fig. 11a demonstrates

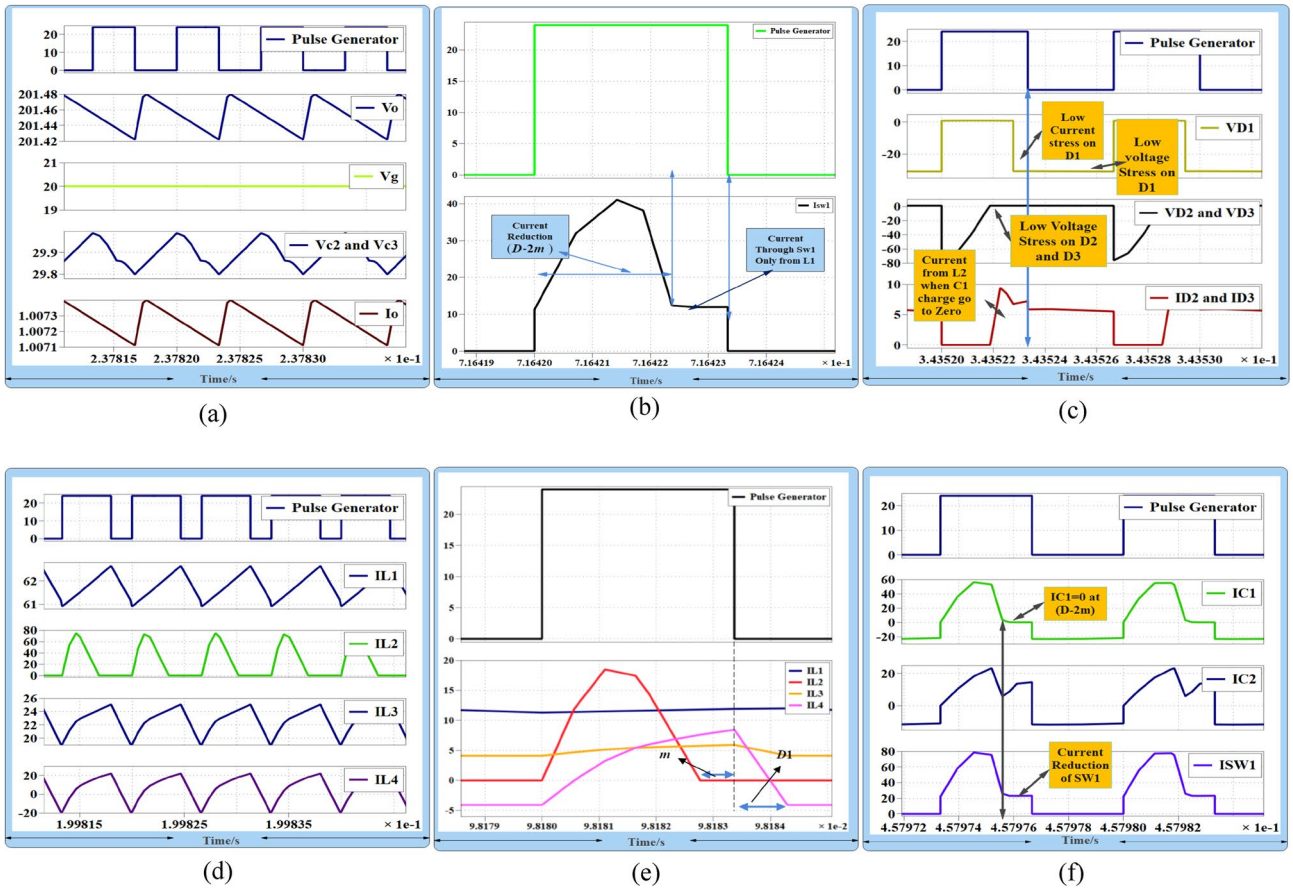


Figure 11. (**a**) Gate source voltage at D = 0.5, Vo = 200 V, Vc_2 = 29 V, and Vg = 20 V, (**b**) Isw_1, at zero charge of C1 and show the current reduction of Sw1 after (D-2m), (**c**) V_{SW1},V_{SW2} and V_{D1},V_{D2},V_{D3} and V_{D4}, (**d**) current through inductors iL_1,iL_2,iL_3 and iL_4, at CCM, (**e**) current through inductors at DCMC2, (**f**) current through capacitors IC_1 and IC_2 and current through S_{w1}.

that the converter produces an output voltage of 200 V, and the voltage across capacitor Vc_3 is approximately 29 V at a load current of 1 A. Figure 11b displays the current through power switch S_{W1}, revealing that the stress current through S_{W1} is reduced because charge in C_1 becomes zero at (D-2m) and L_2's charge makes D_2 and D_3 turn on to charge L_3 and L_4. Figure 11c shows the voltage across D_2 and D_3. It can be seen that the voltage across D_2 and D_3 is totally reduced when L_2 and C_1 work in resonant mode. So, both of them opearte in ZVS during this time (D-2m) as shown in Fig. 13c. Meanwhile, L_2 will pass current through them at (D-2m) < t < Ts and will work as ring to charge L_3 and L_4 through S_{w2}. Figure 11d shows inductor current when the converter operates in CCM, and Fig. 11e shows inductor current in DCMC2.

Figure 11f shows that the current through capacitors Ic_1 and Ic_2, as well as the current through S_{w1}, reduce when the charge in capacitor C_1 becomes zero at (D-2m). In terms of experimental test results, Fig. 12a illustrates the current through inductors L_1 and L_2 when the converter operates in DCMC1. Figure 12b illustrates the current through inductors L_2 and L_3 when the converter operates in DCMC1. Figure 12c shows the MOSFETs current IS_{W1} and IS_{W2}. Figure 12d,e show the voltage across switches Vs_{w1} and Vs_{w2}. In Fig. 12f, the current through D_2 and D_3 can be observed when L_2 discharges current through them due to the charge in capacitor C_1 becoming zero at (D-2 m). It shows that D_1 operates with low current stress, and during this time, inductor L_2 works as an open circuit. The voltage across D_1 is equal to Vc_3. Figure 13a displays the inductor current when the converter operates in DCMC2. In Fig. 13b, the voltage across D_4 is shown.

Figure 13c demonstrates the voltage across D_2 and D_3, revealing that they experience ZVS during the on state from (D-2m) when charge in C_1 becomes zero during (D-2m). During this time, L_2 discharges current to charge L_3 and L_4 through S_{w2}, reducing the voltage across the power MOSFET and diodes. This method enhances the efficiency and performance of the converter. Furthermore, the open circuit state of inductor L_2 minimizes losses from the converter's passive components. Figure 13d shows the currents through capacitors IC_1 and IC_2. Figure 13e displays the output voltage of the proposed converter, Vo = 200 V, at a load current of 1 A, with D = 50%. Figure 13f shows the load voltage Vo = 400 V at D = 33%. In Fig. 13g, the voltage across C_1, equal to 25 V, is depicted, while Fig. 13h shows the voltage across C_2 at a low duty cycle, which is equal to 54 V. The dynamic response of the proposed converter at load changing from 280 to 200 w is shown in Fig. 13i.

As a result, when the input voltage reaches its minimum value, the proposed converter can operate with high efficiency. It utilizes D_1 power diode, which operates with low current stress and low voltage stress, and diodes D_2 and D_3, which work at low voltage stress during the on state, thus reducing the number of passive components.

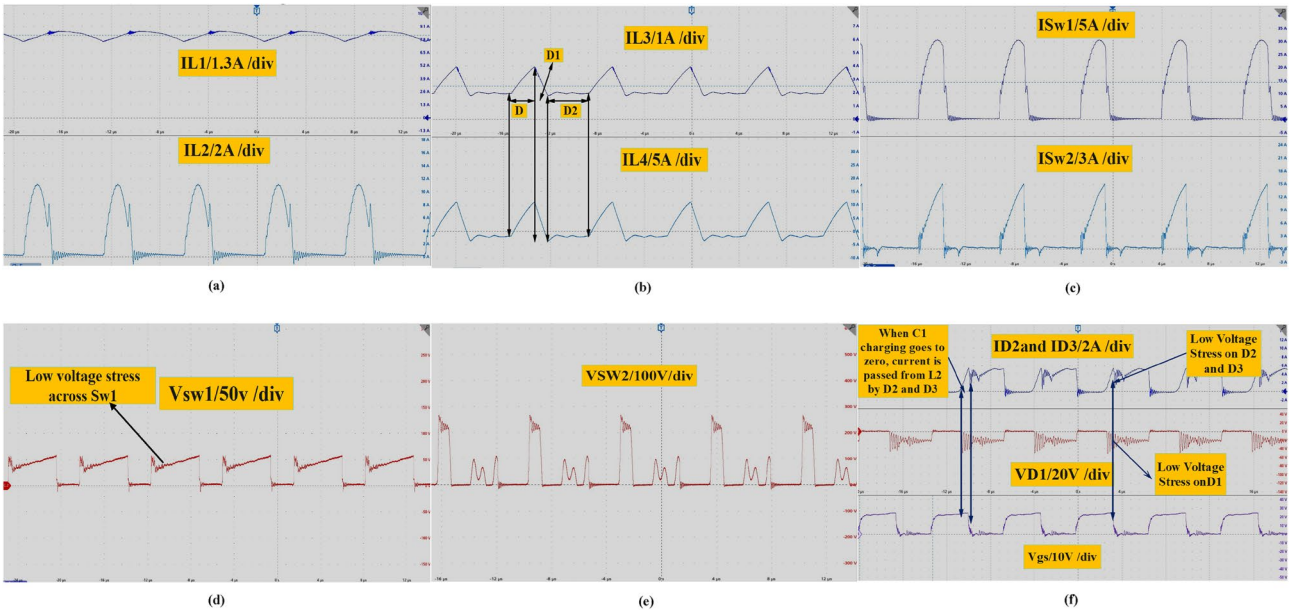


Figure 12. (**a**) Inductors currents iL_1, iL_2 at DCMC1, (**b**) inductors currents iL_3 and iL_4, at DCMC1, (**c**) power MOSFETs current Is_{w1}, Is_{w2}, (**d, e**) voltage across power MOSFET Vs_{w1} and Vs_{w2}, (**f**) current through D_2,D_3 and Voltage across D_1.

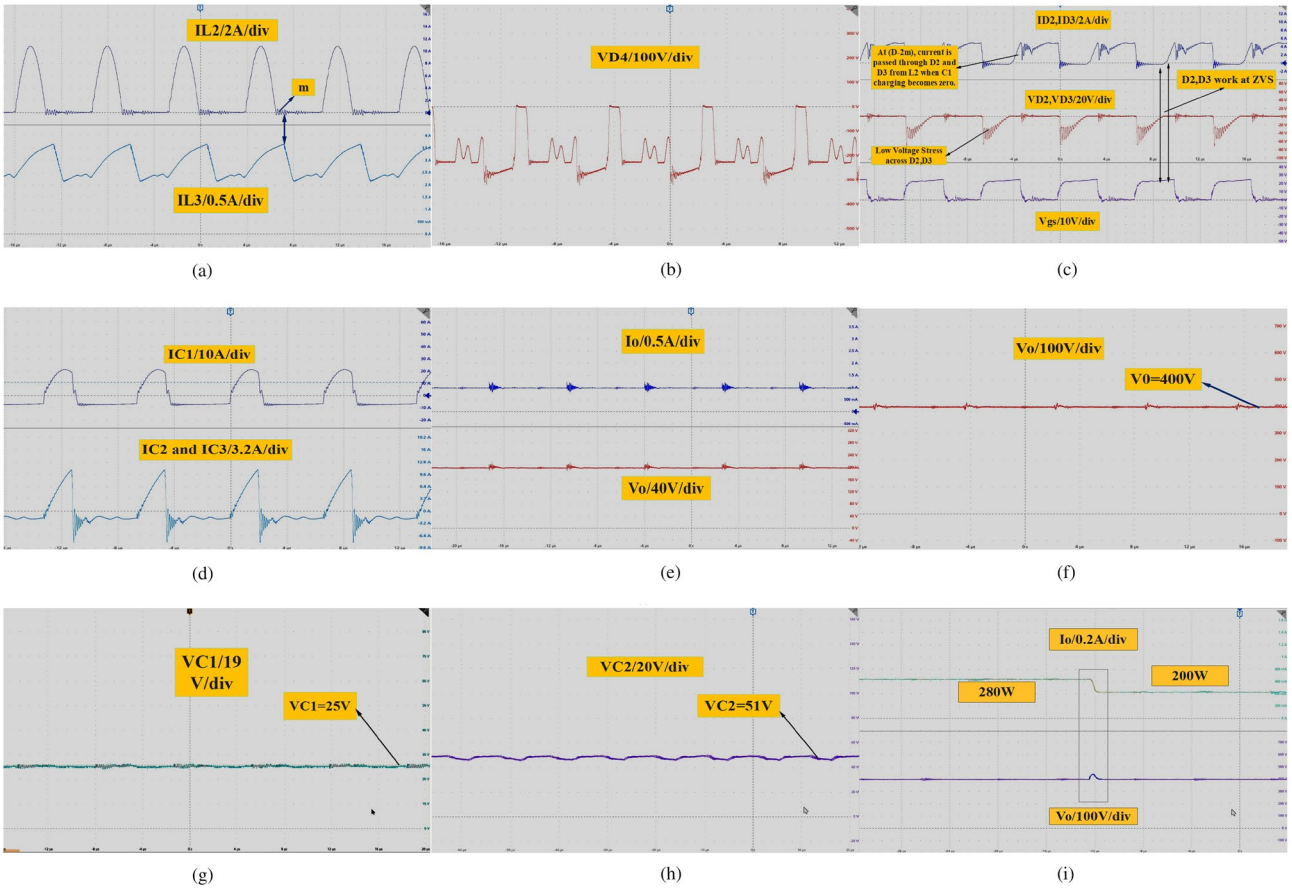


Figure 13. (**a**) Inductors currents iL_1,iL_2 at DCMC2, (**b**) VD_4, (**c**) current through D_2, D_3 and voltage across D_2 and D_3, (**d**) current through capacitors C_1 and C_2,C_3, (**e**) Vo = 200 V at load current 1 A, (**f**) load voltage V_O = 400 V. (**g**) Vc1, (**h**) Vc2 and Vc3, (**i**) dynamic response of the proposed converter at load change from 280 to 200 w.

Additionally, this design enhances the efficiency and reliability of the proposed converter for renewable energy systems that require high output fixed and variable DC voltages. Furthermore, the voltage stress across S_{w1} and S_{w2} is significantly reduced when the proposed converter operates in DCMC2 at 400 W. Moreover, the current and voltage stress of all power diodes are significantly reduced, resulting in a significant reduction in total power losses. Additionally, the current of S_{w1} is significantly reduced when a single cell of switched inductor capacitors is added and operates in the resonant mode.

Analyzing power loss and efficiency of the proposed converter

The proposed converter comprises five capacitors, four inductors, two power switches, and four diodes. However, it should be noted that these components are not ideal, meaning that each component has its internal resistance that affects its performance. For instance, the internal resistance of an inductor increases as the value of the inductor increases. The internal resistance of each inductor is denoted as rl1, rl2, rl3, and rl4, while the equivalent series resistances of capacitors are rc1, rc2, rc3, rc4, and rc5. Additionally, the power diode has two power losses: one due to its internal resistance rd and the other due to its forward voltage Vf. Other power losses occur due to conduction and switching losses of the power MOSFET devices. Therefore, all of these losses should be taken into account when considering the proposed converter. The internal resistances of all the inductors, capacitors, power diode, and MOSFETs can be seen in Fig. 14.

$$Irms = \sqrt{\frac{1}{Ts}\int_{0}^{Ts}(I)^2 dt} \tag{63}$$

$$Isw_{1rms} = \sqrt{\frac{1}{Ts}\int_{0}^{(D-2m)Ts}(iL_1 + iL_2)^2 dt + \int_{(D-2m)T}^{DTs}(iL_1)^2 dt +} \tag{64}$$

$$Isw_{2rms} = \sqrt{\frac{1}{Ts}\int_{0}^{(D-2m)}(Ic2)^2 + \int_{(D-2m)}^{(D-m)}(Ic2 + Ic3)^2 dt} \tag{65}$$

$$ID_{1rms} = \sqrt{\frac{1}{Ts}\int_{0}^{(D-m)Ts}(iL2)^2 dt} = iL2rms \tag{66}$$

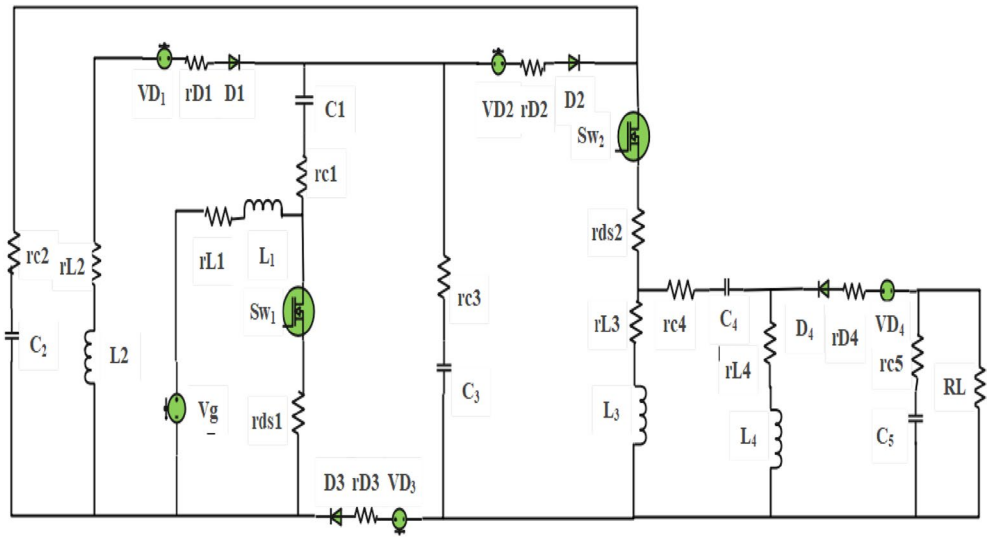


Figure 14. The proposed converter with internal resistance in passive and active components.

$$ID_{2rms} = ID_{3rms} = \sqrt{\frac{1}{Ts}\int_{(D-2m)}^{DTs}(iL_2)^2dt + \int_{DTs}^{Ts}(iL_1)^2dt} \tag{67}$$

$$ID_{4rms} = \sqrt{\frac{1}{Ts}\int_{D}^{Ts}(iL_3 + iL_4)^2dt} \tag{68}$$

$$Ic_{1rms} = \sqrt{\frac{1}{Ts}\left[\int_{0}^{(D-2m)Ts}(iL2)^2dt + \int_{D}^{Ts}(iL1)^2dt\right]} \tag{69}$$

$$Ic_{2rms} = Ic_{3rms} = \sqrt{\frac{1}{Ts}\left[\int_{0}^{DTs}(iL3 + iL4)^2dt + \int_{D}^{Ts}(iL1)^2dt\right]} \tag{70}$$

$$Ic_{4rms} = \sqrt{\frac{1}{Ts}\left[\int_{0}^{DTs}(iL4)^2dt + \int_{D}^{Ts}(iL3)^2dt\right]} \tag{71}$$

$$Ic_{5rms} = \sqrt{\frac{1}{Ts}\left[\int_{0}^{DTs}(I_o)^2dt + \int_{D}^{Ts}(iL3 + iL4)^2dt\right]} \tag{72}$$

To determine the total power losses of the proposed converter, it is necessary to calculate the RMS current for the inductors, capacitors, power MOSFET, and diodes in both on and off states. Equation (63) represents the general equation for RMS current. Equations (64) and (65) can be utilized to obtain the RMS current through S_{W1} and S_{W2} during the on state. During the on state, the RMS current through D1, which is equal to the RMS current through inductor L_2 during the period (0 < t < D-m), can be calculated using Eq. (66). Equation (67) provide the RMS current for D_2 and D_3 and, Eq. (68) provide the RMS current for D4, and Eqs. (69), (70), (71),and (72) can be employed to determine the RMS currents for capacitors C_1, C_2, C_3, C_4 and C_5, respectively.

$$Isw_{1rms} = \frac{2Io\sqrt{4D - 6m}}{(1 - D)^2} \tag{73}$$

$$Isw_{2rms} = \frac{2DIo\sqrt{D + m}}{(1 - D)^2} \tag{74}$$

$$ID_{1rms} = \frac{2IoD\sqrt{D - m}}{(1 - D)^2} = iL_{2rms} \tag{75}$$

$$ID_{2rms} = ID_{3rms} = \frac{IoD}{(1 - D)^2}\sqrt{2m + 1 - D} \tag{76}$$

$$ID_{4rms} = \frac{Io(1 + D)}{\sqrt{(1 - D)}} \tag{77}$$

$$iL_1rms = \frac{2IoD}{(1 - D)^2} \tag{78}$$

$$iL_{3rms} = \frac{2DIo}{(1 - D)} \tag{79}$$

$$iL_{4rms} = \frac{DIo}{(1 - D)} \tag{80}$$

$$Ic_1 rms = \frac{IoD\sqrt{1+2m}}{(1-D)^2} \tag{81}$$

$$Ic_{2rms} = Ic_{3rms} = \frac{IoD}{(1-D)^2}\sqrt{2m+1-D} \tag{82}$$

$$Ic_{4rms} = Io\sqrt{D}\sqrt{\frac{1+3D}{1-D}} \tag{83}$$

$$Ic_{5rms} = \frac{Io(1+D)}{\sqrt{(1-D)}} \tag{84}$$

Equations (73) and (74) describe the RMS current flowing through the MOSFETs. To calculate the RMS currents flowing through the power diodes, you can use Eqs. (75), (76), and (77). Equations (78), (79), and (80) provide the RMS current flowing through inductors L_1, L_3, and L_4 respectively. Finally, we can determine the RMS current through capacitors C_1, C_2, C_3, C_4, and C_5 using Eqs. (81), (82), (83), and (84), respectively.

Conduction and switching losses calculation of power MOSFETs

To determine the conduction losses of the power MOSFET in the proposed converter, (RMS) current is multiplied by the value of the on state resistance of the MOSFET.

$$Pcd1 = \frac{4Po(4D-6m)}{R_L(1-D)^4} rds1 \tag{85}$$

$$Pcd2 = \frac{4P_oD^2(D+m)}{RL(1-D)^4} rds2 \tag{86}$$

$$PSW = \frac{1}{2} Vsw^2 FsCo \tag{87}$$

$$P_{SWL1} = \frac{1}{2} V_g^2 FsCo \tag{88}$$

$$P_{SWL2} = \frac{V_o^2(1-D)^2}{8D^2} FsCo \tag{89}$$

$$T_{PLCS1,2} = \frac{4Po(4D-6m)}{R_L(1-D)^4} rds1 + \frac{4P_oD^2(D+m)}{RL(1-D)^4} rds2 + \frac{1}{2} V_g^2 FsCo + \frac{V_o^2(1-D)^2}{8D^2} FsCo \tag{90}$$

The power conduction losses of MOSFETs Sw_1 and Sw_2, Pcd1 and Pcd2, can be obtained from Eqs. (85) and (86). Equation (82) provides a means to calculate the power switching losses, P_{SWL1} and P_{SWL2}, of MOSFETs Sw_1 and Sw_2. These losses can be obtained using the output capacitor of the MOSFET, Co, and the switching frequency, Fs. The total power losses of MOSFETs P_{SWL1} and P_{SWL2} can be obtained by adding Eqs. (85), (86), (88), and (89) as a result, resulting in Eq. (90).

Power losses calculation in all diodes

In order to accurately calculate the power losses incurred by the four diodes in the converter, it is important to take both types of losses into consideration. To determine the power losses due to Vf, one can use Eq. (91) to calculate the average current flowing through diodes, and then multiply this result by Vf and the power losses (Pvf) caused by the forward voltage. On the other hand, Eq. (92) can be used to calculate the diode power losses due to rd, while Eq. (93) is used to determine the power losses due to Vf. Finally, to obtain the total power losses (T_{PDL1}, T_{PDL2}, T_{PDL3}, T_{PDL4}) across all four diodes, Eq. (94) can be used to add up all losses in the power diode.

$$\left.\begin{aligned} I_{D1ave} &= \frac{2IoD(D-m)}{(1-D)^2} \\ I_{D2ave} &= \frac{2I_o(-D+m+1)}{(1-D)^2} \\ I_{D3ave} &= \frac{2I_o(-D+m+1)}{(1-D)^2} \\ I_{D4ave} &= I_o(1+D) \end{aligned}\right\} \tag{91}$$

$$\left.\begin{aligned} P_{Dr} &= IDrmsrd \\ P_{Dr1} &= \frac{4P_oD^2(D-m)}{RL(1-D)^4}rd1 \\ P_{Dr2} &= \frac{PoD(2m+1-D)}{R_L(1-D)^4}rd2 \\ P_{Dr3} &= \frac{PoD(2m+1-D)}{R_L(1-D)^4}rd3 \\ P_{Dr4} &= \frac{P_o(1+D)^2}{R_L(1-D)}rd4 \end{aligned}\right\} \tag{92}$$

$$\left.\begin{aligned} P_{Vf} &= I_{Dav}Vf \\ P_{Vf1} &= Vf_1\frac{2P_oD(D-m)}{RL(1-D)^2} \\ P_{Vf2} &= Vf_2\frac{2P_o(-D+1+m)}{RL(1-D)^2} \\ P_{Vf3} &= Vf_3\frac{2p_o(-D+1+m)}{RL(1-D)^2} \\ P_{Vf4} &= Vf_4\frac{P_o}{RL}(1+D) \end{aligned}\right\} \tag{93}$$

$$T_{PDL} = P_{Dr1,2,3,4} + P_{Vf1,2,3,4} \tag{94}$$

Total power losses in inductor and capacitors

$$\left.\begin{aligned} P_L &= iLrms^2rl \\ P_{L1} &= \frac{4P_oD^2}{RL(1-D)4}rl1 \\ P_{L2} &= \frac{2P_oD^2(D-m)}{RL(1-D)^4}rl2 \\ P_{L3} &= \frac{4D^2P_o}{RL(1-D)^2}rl3 \\ P_{L4} &= \frac{D^2P_o}{RL(1-D)^2}rl4 \end{aligned}\right\} \tag{95}$$

$$\left.\begin{aligned} P_C &= Icrms^2rc1 \\ P_{C1} &= \frac{P_oD^2(1+2m)}{RL(1-D)^4}rc1 \\ P_{C2} &= \frac{PoD^2(2m+1-D)}{R_L(1-D)^4}rc2 \\ P_{C3} &= \frac{PoD^2(2m+1-D)}{R_L(1-D)^4}rc3 \\ P_{C4} &= \frac{P_oD(1+3D)}{RL(1-D)}rc4 \\ P_{C5} &= \frac{P_o(1+D)^2}{RL(1-D)}rc5 \end{aligned}\right\} \tag{96}$$

Total power losses in proposed converter (T_{PLPC})

By utilizing Eqs. (95) and (96), it is possible to determine the power losses (PL) and (PC) in the inductors and capacitors, respectively. The losses associated with the proposed converter can be categorized into four types: MOSFET losses, diode losses, inductor losses, and capacitor losses. Equation (97) can be employed to calculate the total power loss (T_{PLPC}) of the converter by adding the power losses of the power MOSFETs ($T_{PLCS1,2}$), the total power losses of the diodes ($T_{PDL1,2,3,4}$), and the losses in the inductors and capacitors ($T_{PL1,2,3,4}$ and $T_{PC1,2,3,4,5}$) respectively. The efficiency of the proposed converter can be determined by Eq. (98). Clearly, SiC MOSFETs with very low on-state resistance are the optimal choice for minimizing conduction losses. Additionally, utilizing

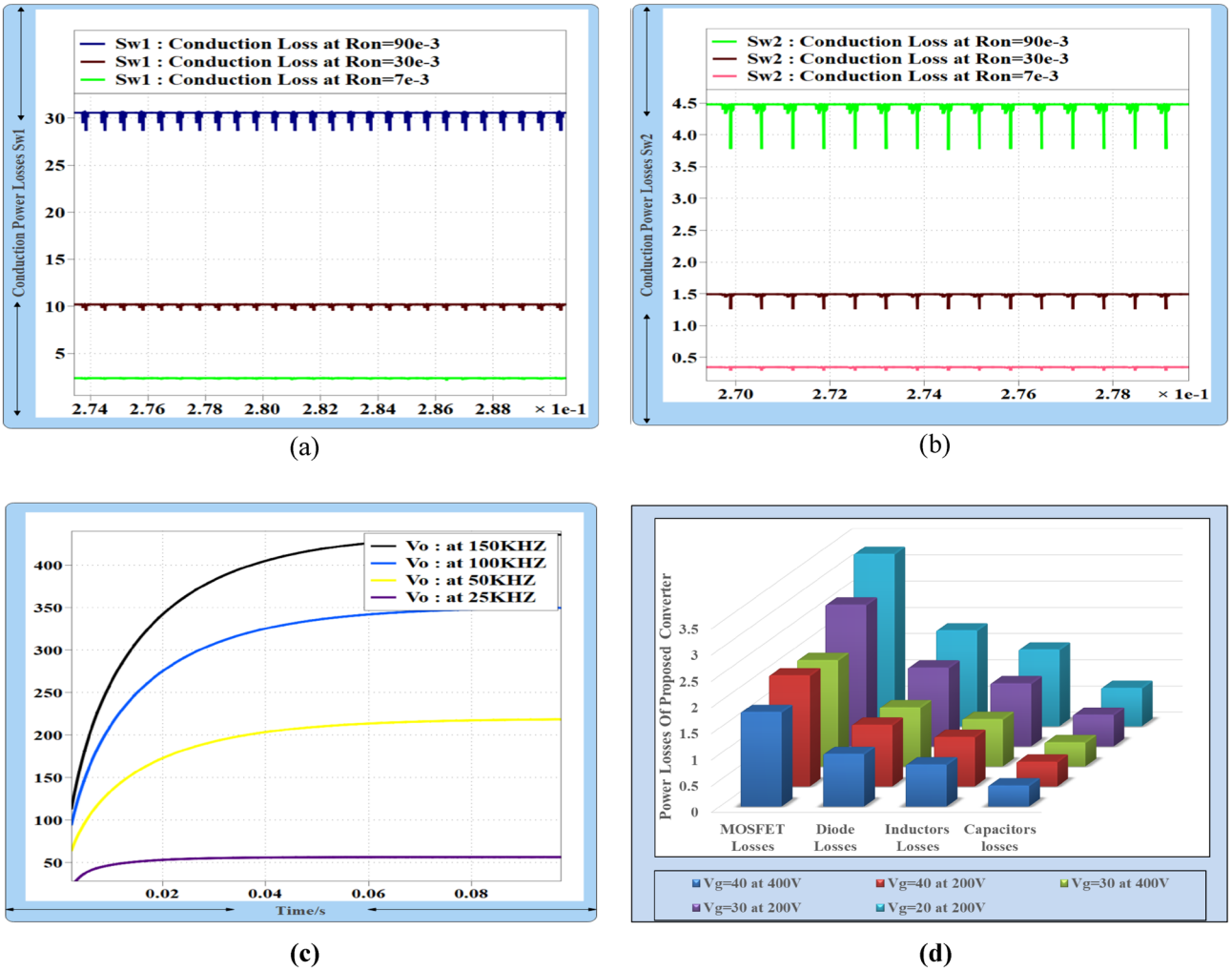


Figure 15. (**a, b**) Conduction power losses of MOSFET Sw1 and Sw2at variable input and output voltage, (**c**) output voltage of the proposed converter at different switching frequency at D = 33%, (**d**) total power losses in proposed converter.

inductors with low internal resistance values will further improve the performance and efficiency of the proposed converter.

$$T_{PLPC} = T_{PLCS1,2} + T_{PDL1,2,3,4} + T_{PL1,2,3,4} + T_{PC1,2,3,4,5} \tag{97}$$

$$\eta = \frac{P_o}{P_o + T_{PLPC}} 100\% \tag{98}$$

Figure 15a,b illustrate the conduction power losses of MOSFETs across different input and output voltages. It showed that, the conduction power losses of both MOSFET with a small value of internal resistance are decreased.

Therefore, the proposed converter utilizing SiC MOSFET with Ron 7 m demonstrated minimal power conduction losses even with varying duty cycles, resulting in higher efficiency than previous DC–DC converters. The implementation of WBG MOSFETs is expected to further reduce both conduction and switching losses, leading to a substantial increase in the efficiency of the proposed converter.

In Fig. 15c, it can be seen that the proposed converter's output voltage varies with different switching frequencies. The new design of the proposed converter enables high output voltage at high switching frequencies with very low values of inductors and capacitors. However, the load voltage of the proposed converter significantly reduces when the switching frequency is reduced to 25 kHz. This means that the proposed converter can supply 400 V to a 400 W load at a duty cycle of 33% by utilizing high switching frequency, resulting in a small size and low cost of the proposed converter. Figure 15d displays the overall power losses of the proposed converter, taking into account various input and output voltages. One significant observation is that the converter experiences a loss of 4% at 400 W when the input voltage is around 40 V. The proposed converter demonstrates remarkable efficiency when supplying high load current at a low duty cycle within the input voltage range of 20–40 V.

In Fig. 16a,b, the proposed converter's efficiency is shown under variable input voltage at an output voltage 200 V. The results indicate an efficiency of around 96% at 40 V input voltage. In Fig. 16c,d, the efficiency of the

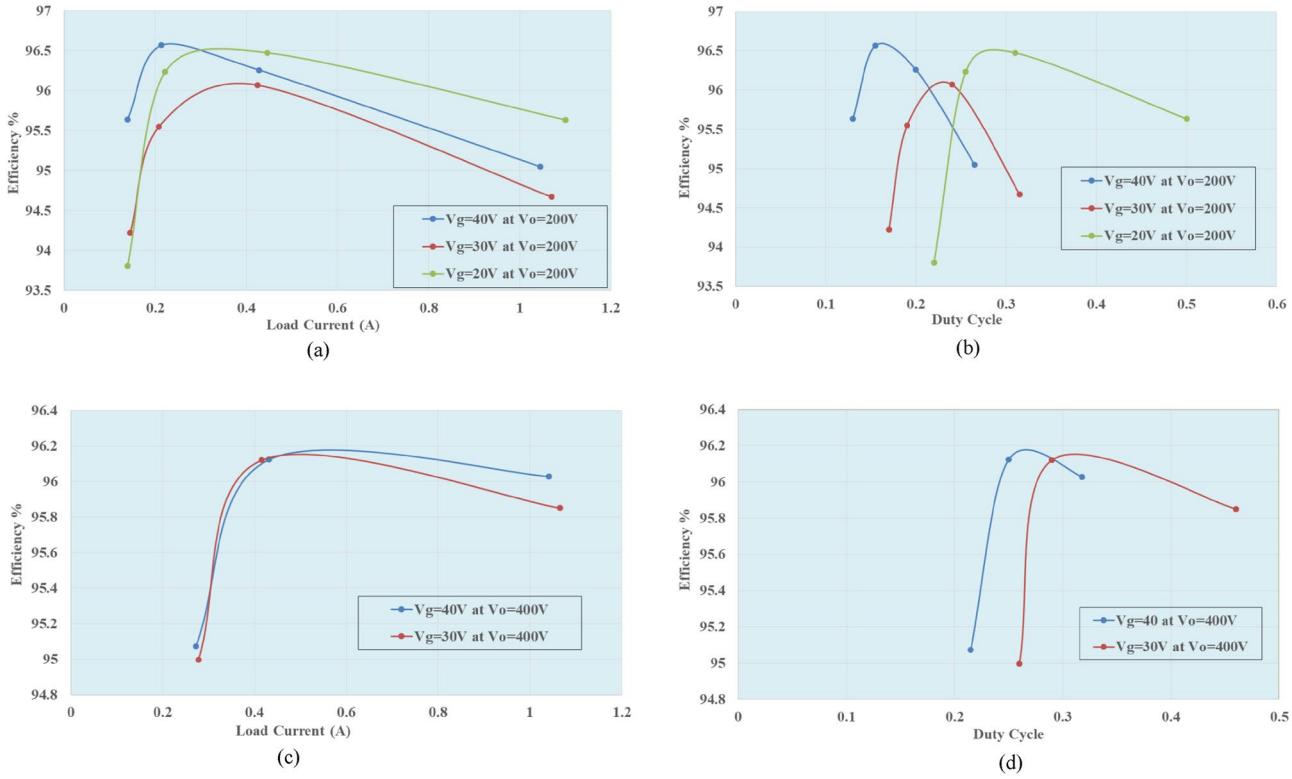


Figure 16. (**a**–**d**) Efficiency of the proposed converter at variable input and output voltage versus load current and duty cycle respectively.

proposed converter is shown for variable input voltage at an output voltage of 400 V. The results indicate an efficiency of approximately 96% at 40 V input voltage.

Therefore, the suggested converter is capable of increasing a low input voltage to a high output voltage while providing a high load current at variable input voltage without any input current pulsation at a low duty cycle with high power density efficiency. In addition, the proposed DC–DC converter can supply variable high-output voltage between 200 and 400 V, making it more suitable for a wide range of applications.

Conclusion

In conclusion, this paper has introduced a highly optimized DC–DC converter employing the innovative modified switched inductor-capacitor (MSLSC) technique, which represents a significant advancement in the field of (RES). The MSLSC-based converter offers several remarkable advantages that make it a promising solution for various applications. One of the key contributions of this research is the introduction of the modified switched inductor (MSL1) and capacitor in series with diodes, which operate in a resonant mode. This design effectively reduces current stress across the main switch, diodes, and inductors, thereby enhancing the overall reliability of the converter. Additionally, the integration of modified switched inductors (MSL2) and capacitors with auxiliary switches further boosts voltage gain and reduces voltage stress on critical components. In addition, the proposed DC–DC converter can supply variable high-output voltage between 200 and 400 V, making it more suitable for a wide range of applications.

The experimental results, including the construction of a 400 W printed circuit board (PCB), validate the simulation findings, demonstrating a remarkable efficiency of approximately 96.2% at 400 W with a 40 V input voltage. This level of efficiency is a significant achievement, especially for RES applications, where converting low input voltages to high output voltages is crucial. Furthermore, the elimination of pulsating input current and reduced voltage stress on power devices highlight the practicality and reliability of the proposed converter. By leveraging SiC MOSFETs and high switching frequencies, this converter minimizes switching losses, component values, and circuit size while maximizing efficiency and performance.

In summary, the optimized DC–DC converter based on the MSLSC technique represents a groundbreaking development in RES. Its exceptional efficiency, voltage stress reduction, and adaptability to various duty cycles make it a promising candidate for enhancing the efficiency and reliability of RES applications. This innovation holds great potential for contributing to the advancement of sustainable energy solutions.

Data availability

All data is available upon request.

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Author contributions

A.A.: Formal analysis, Investigation, Methodology, Writing – original draft, Writing – review & editing. X.W.: Conceptualization, Supervision. M.F.: Proofreading and figures.

Competing interests

The authors declare no competing interests.

Additional information

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