



## OPEN Novel design and implementation of 3d packaged wideband bandpass filters

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This study presents an innovative method for designing a 3D packaged wideband bandpass filter (BPF) by vertically integrating a high-pass filter (HPF) and a low-pass filter (LPF) using an air cavity and vertical interconnect accesses (VIAs). This integration enhances performance while significantly reducing system size. The fabricated BPF, constructed on multilayer substrates, achieves a passband from 2.175 to 4.2 GHz with less than 2.5 dB insertion loss and a return loss exceeding 10 dB. The design utilizes a partial substrate integrated suspended line (SISL) structure, enabling precise control over the equivalent dielectric constant and characteristic impedance to optimize insertion loss. The height of the air cavity, determined through theoretical analysis and S-parameter inversion, is critical for achieving optimal filter performance. The methodology allows for independent circuit designs on each layer, resulting in a 3D assembly. This refined approach makes it easier to produce compact bandpass and multi-band filters, simplifying circuit development and enabling scalable fabrication. This design is versatile across different frequency ranges, demonstrating significant practical and theoretical benefits.

In the rapidly evolving landscape of wireless communication systems, radio frequency (RF) filters are indispensable components that select desired frequency bands while suppressing out-of-band noise. As these systems advance in performance and integration, there is an increasing demand for RF filters that are not only small and cost-effective but also deliver high performance<sup>1–3</sup>. This necessity has driven the development of various techniques for wideband bandpass filters (BPFs), each with its own set of challenges and limitations.

Traditional approaches to achieving wide bandwidth in BPFs involve cascading multiple filters, a method that, while effective, is marred by drawbacks such as increased size, complex design, high cost, and suboptimal system performance<sup>4–6</sup>. Furthermore, this approach is not scalable for arbitrary frequency bands or an infinite number of bands. An alternative is the multi-resonance structure, which offers compact and low-loss designs but suffers from the complexity and non-repetitiveness of the layouts<sup>7–11</sup>. Another method involves connecting a high-pass filter (HPF) in series with a low-pass filter (LPF), which provides design flexibility but still faces size challenges<sup>12–14</sup>.

Currently, driven by the technology of miniaturization of electronic devices, three-dimensional (3D) integration across different substrates and heterogeneous structures is a burgeoning field in the realm of microelectronic device miniaturization<sup>15,16</sup>. Utilizing vertical through-hole technology, this method integrates various circuit-laden substrates in a predefined sequence, transforming the conventional two-dimensional (2D) cascade circuit into a compact 3D vertical interconnect architecture. This innovative approach significantly diminishes the spatial footprint and retains full functionality.

In the realm of 3D integrated circuit design, the conventional approach to isolating circuit layers employs a blank substrate. However, to enhance system performance and mitigate electromagnetic interference, this substrate is replaced by an air cavity in a substrate integrated suspended line (SISL) configuration<sup>17–19</sup>. The cavity is surrounded by vertical interconnect accesses (VIAs) that connect all substrate grounds, drawing inspiration from the shielded suspended substrate microstrip line<sup>20–23</sup>.

Although the SISL structure is an ideal solution for wideband filters<sup>24–26</sup>, as it can combine multiple filters to form a wider bandwidth without increasing the circuit size. However, it necessitates the use of air cavities above and below each circuit layer. This requirement can significantly increase the system's overall thickness, as the stacking of multiple circuit layers, each with its own pair of air cavities, somewhat reduces the size advantages achieved by transitioning from two-dimensional to three-dimensional integration.

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This study introduces a wideband BPF constructed by vertically interconnecting an HPF with a defective ground structure (DGS) and an LPF through VIAs. A substrate with an integrated air cavity isolates the filters, housing the HPF circuit within the cavity and connecting all substrate grounds via densely distributed VIAs around the cavity. The LPF circuit and the DGS of the HPF are strategically positioned at the bottom and top layers, respectively. This configuration enhances the HPF's in-band insertion loss and ingeniously uses the LPF's ground as a cover for the air cavity. Through meticulous impedance matching, a compact and high-performance BPF is achieved. Compared to traditional SISL structures, this design conserves three air cavities, significantly enhancing compactness by placing air cavities only where necessary.

## Design and modeling

### Design processes

The proposed design incorporates both an LPF and an HPF to form a wide BPF. The LPF section features a conventional L-C ladder topology, complemented by open-circuited stubs, as depicted in Fig. 1 (a).

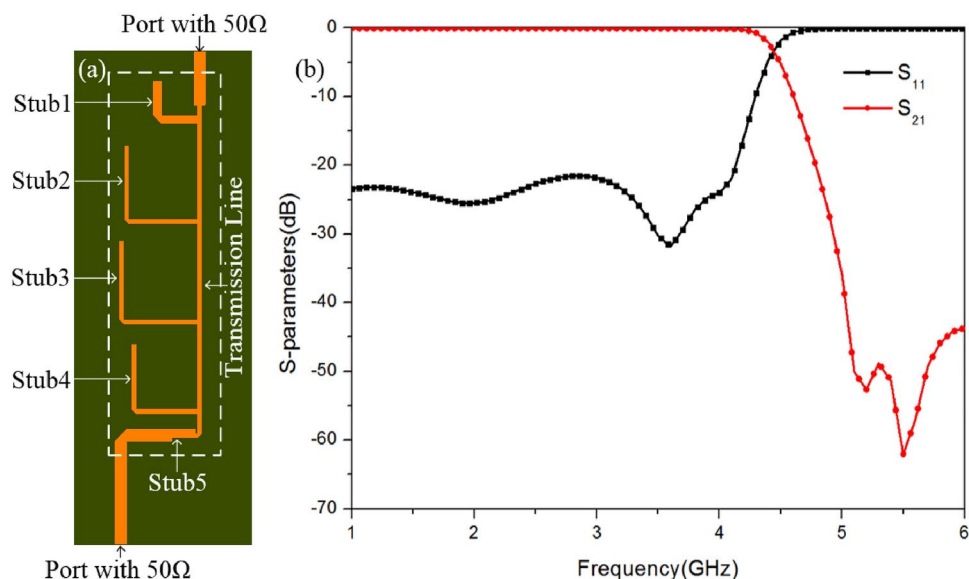
There are five stubs, named Stub1, Stub2, Stub3, Stub4, and Stub5, from top to bottom. Stub1 has a size of long is 2.9 mm and wide of 0.29 mm, located 0.4 mm from the upper port with  $50\ \Omega$ . Stub2 is positioned 3.6 mm away from Stub1 with dimensions of 5.5 mm by 0.14 mm. Stub3, placed at the same distance as that between Stub1 and Stub2, has dimensions of 5.9 mm in length and 0.13 mm in width. Stub4, positioned 3.2 mm from Stub3, measures 4.9 mm in length and 0.17 mm in width. Stub5, connected to the lower port with  $50\ \Omega$ , is 1.8 mm long and 0.31 mm wide. To enable miniaturization, all stubs, except for the shorter Stub5, are bent. Stub1 bends at 1.58 mm from the transmission line, while Stubs 2 to 4 bend at their midpoints. Additionally, to connect with the HPF, the transmission line bends 0.75 mm from Stub4.

The corresponding simulated S-parameters are displayed in Fig. 1 (b). From Fig. 1 (b), it can be observed that the LPF has a cutoff frequency of 4.4 GHz, demonstrating superior performance with a 40 dB out-of-band rejection at 5 GHz. Within the passband, ranging from DC to 4.2 GHz, the insertion loss remains under 0.2 dB, while the return loss is greater than 20 dB.

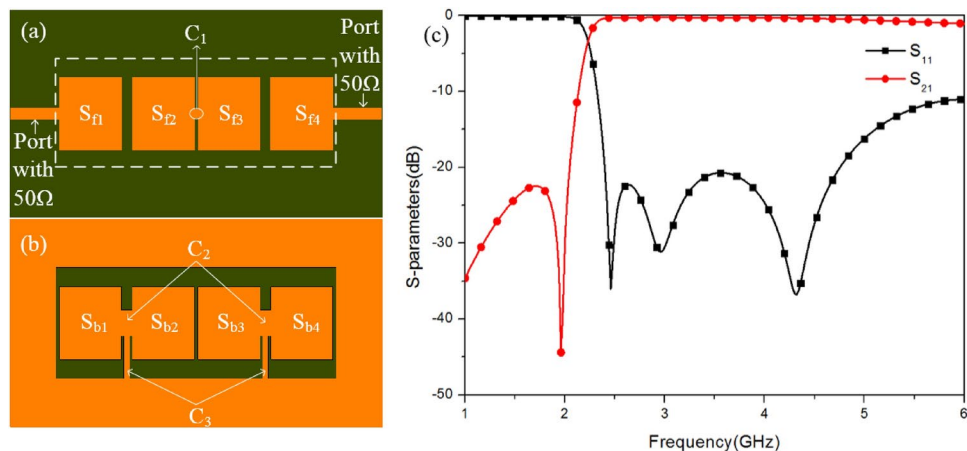
Significantly, we have introduced strategic bends in the open-circuited stub and the adjacent  $50\ \Omega$  transmission line. These modifications have resulted in a compacted primary circuit section of  $13 \times 4\ \text{mm}^2$ , as indicated by the white dashed box in Fig. 1 (a), achieving a 33.3% reduction in circuit area compared to the original unbent design.

The HPF, depicted in Fig. 2 (a) and (b), incorporates a defective ground structure (DGS), enhancing its performance. The DGS component consists of four identical rectangular microstrips, labeled  $S_{f1}$  through  $S_{f4}$  from left to right, each measuring 2.8 mm by 2.5 mm. The microstrips are positioned with a 0.45 mm gap between  $S_{f1}$  and  $S_{f2}$ , and between  $S_{f3}$  and  $S_{f4}$ . In addition,  $S_{f2}$  and  $S_{f3}$  are connected by a rectangular connector,  $C_1$ , with dimensions of 0.3 mm by 0.15 mm. As shown in Fig. 2(b), the backside of the DGS structure also contains four rectangular microstrips, labeled  $S_{b1}$  through  $S_{b4}$  from left to right, matching the dimensions of  $S_{f1}$  to  $S_{f4}$ . These microstrips are linked together by a rectangular connector,  $C_2$ , with a width of 1 mm. A central microstrip rectangle,  $C_3$ , with a width of 0.225 mm, extends from  $C_2$  to the ground plane. The vertical distance from the ground plane to microstrips  $S_{b1}$ ,  $S_{b2}$ ,  $S_{b3}$ , and  $S_{b4}$  is 0.75 mm, and the horizontal distance next to these components is 0.15 mm.

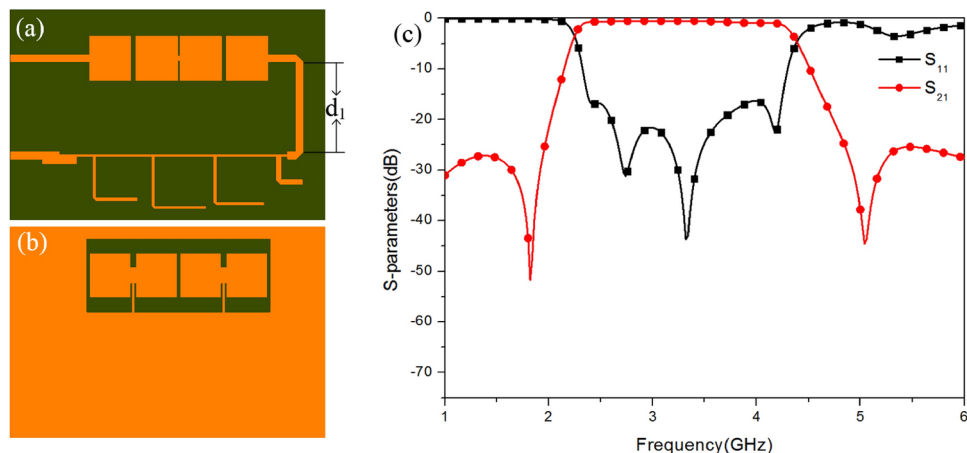
The simulated S-parameters, shown in Fig. 2 (c), reveal a cutoff frequency of 2.22 GHz, with 40 dB rejection at 1.9 GHz. The HPF exhibits an insertion loss of less than 0.6 dB and a return loss above 20 dB within the



**Fig. 1.** The circuit configuration and S-parameters of the bent LPF. (a) Configuration, (b) S-parameters.



**Fig. 2.** The circuit configuration and S-parameters of the HPF. (a) Top view, (b) Back view, (c) S-parameters.



**Fig. 3.** The circuit configuration and S-parameters of the BPF. (a) Top view, (b) Back view, (c) S-parameters.

passbands ranging from 2.3 to 4.8 GHz. The primary circuit section of the HPF is  $11.4 \times 4.3 \text{ mm}^2$ , which is delineated by the white dashed box in Fig. 2 (a).

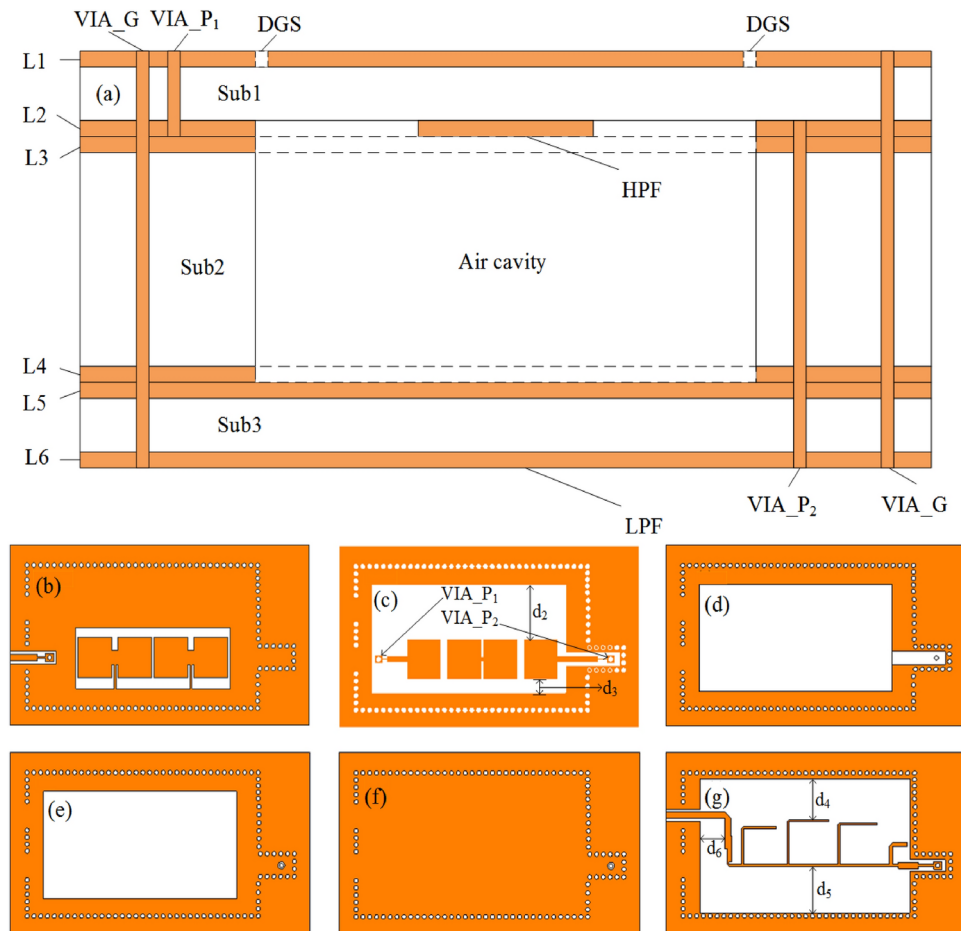
The aforementioned filters are designed on a Rogers6010 substrate, characterized by a thickness of  $h=0.508 \text{ mm}$ , a relative permittivity  $\epsilon_r = 10.2$ , and a loss tangent  $\tan \delta = 0.0023$ .

The LPF and HPF, as detailed in Fig. 1 and Fig. 2, are connected in series on a common substrate to form the wideband BPF. To mitigate the impact of the HPF's DGS on the LPF, a specific minimum spacing has been maintained between them, and it is defined as  $d_1 = 5.55 \text{ mm}$ . The resulting optimized BPF configuration is depicted in Fig. 3 (a) and (b), with the corresponding S-parameters displayed in Fig. 3 (c). These parameters indicate a passband ranging from 2.25 to 4.34 GHz, featuring an insertion loss of less than 1.3 dB and a return loss exceeding 15.6 dB within the passband. The overall dimensions of the BPF are  $20.3 \times 12 \text{ mm}^2$ .

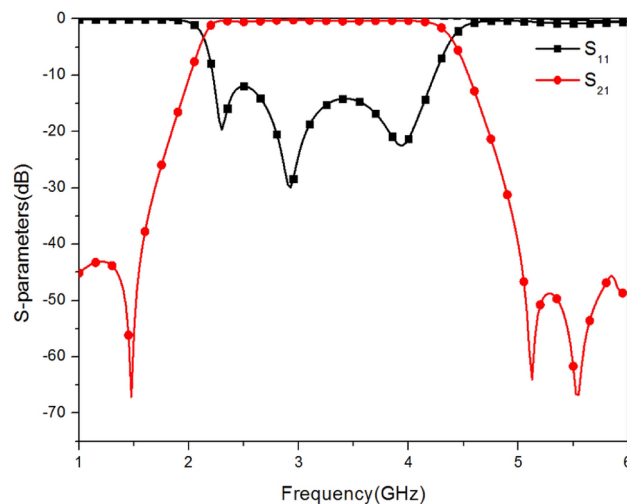
It is worth noting that the output port configuration of the LPF in Fig. 3 (a) differs from that in Fig. 1 (a). In Fig. 3 (a), a section of the input port has been folded to align the input and output ports on the same side, facilitating easier integration with other devices.

To improve miniaturization, the original 2D cascade-connected structure shown in Fig. 3 has been rearranged into a more compact 3D vertical interconnection layout, as depicted in Fig. 4 (a). Fig. 4 (a) shows the entire circuit that consists of three substrates Sub1 through Sub3. The HPF and LPF are designed on Sub1 and Sub3 respectively. The substrate two (Sub2) contains an integrated air cavity that separates the filters. This cavity houses the HPF circuit and connects all substrate grounds via densely distributed VIAs (labeled as VIA\_G) around the cavity. All substrates are topped with a series of metal layers, labeled L1 to L6. Specifically, Fig. 4 (b) to (g) illustrates the role of each layer: L1 serves as the backside DGS layer for the HPF, L2 contains the front circuit of the HPF (as shown in Fig. 4 (c)), and L3 and L4 are the upper and lower layers, respectively, surrounding the air cavity.

To reduce costs associated with this cavity, an FR4 substrate with a relative permittivity of  $\epsilon_r = 4.4$ , and a loss tangent  $\tan \delta = 0.02$  is utilized. The center of the substrate is excavated to create an air cavity, which provides an



**Fig. 4.** Showing the modeling configuration of multilayers of the proposed BPF: (a) illustrating the cross-sectional view of the proposed BPF that demonstrates the multilayers from layer one to layer 7, the vias that connect the top layer (L1) to the bottom layer seven (L7), and the air cavity. (b) demonstrating the backside DGS layer for the HPF (L1), (c) showing the front circuit of the HPF (L2), (d) showing the top layer (L3), (e) showing the bottom layer (L4), (f) showing the ground layer (L5), and (g) illustrating the LPF circuit situated (L6).



**Fig. 5.** Simulation result showing S-parameters of the proposed BPF.

isolated environment for the two filters. Layer five (L5) acts as the ground layer for the LPF and plays a crucial role in shielding the upper ground layer. Additionally, L6 is the layer where the LPF circuit is located.

As illustrated in Figs. 4 (b) and (g), the signal is fed from the HPF input port through the VIA ports (labeled as VIA\_P<sub>1</sub>) to the HPF circuit on layer L2. It then traverses layers L3, L4, and L5 before arriving at the LPF circuit layer. The signal subsequently exits through the LPF's output port (labeled as VIA\_P<sub>2</sub>). The alignment of the LPF's output port with the HPF's input port on the same side facilitates integration with external circuits and contributes to a compact design.

All VIA\_G has a size of radius of 0.15 mm and a spacing of 0.18 mm as shown in Fig. 4. In Fig. 4 (c), VIA\_P<sub>1</sub> is positioned 2.75 mm from the left substrate edge, and VIA\_P<sub>2</sub> is 1.95 mm from the right edge. Both are 4.54 mm from the lower substrate edge, with a radius of 0.15 mm. The distances d<sub>2</sub> and d<sub>3</sub> of the HPF circuit from the upper and lower grounds are 3.7 mm and 0.9 mm, respectively. The air cavity openings in Figs. 4 (d) and (e) measure 14.2 mm by 7.4 mm, with distances of 2.4 mm and 2.45 mm from the lower and left substrate edges. In Fig. 4 (g), the distances of the LPF circuit from the substrate's upper, lower, and left edges, labeled as d<sub>4</sub>, d<sub>5</sub>, and d<sub>6</sub>, are 2.87 mm, 3.22 mm, and 1.83 mm, respectively. The right Stub<sub>5</sub> is 0.17 mm from the right substrate edge.

The simulation outcomes, depicted in Fig. 5, reveal a passband range of 2.2 to 4.37 GHz. Within this range, the insertion loss remains below 0.6 dB, and the in-band return loss consistently exceeds 12 dB. These performance metrics are comparable to those of the series-connection approach illustrated in Fig. 3 (c). Notably, the redesigned circuit's footprint has been minimized to  $18 \times 8 \text{ mm}^2$ , representing a 40% reduction in area compared to the series-connection method, thus demonstrating the significant potential for miniaturization.

### Measurement results

The fabricated prototype is presented, with each layer from L1 to L6 illustrated in Fig. 6. The physical depictions of the layers following the packaged prototype are displayed on the right-hand side of the same figure.

After completing the welding of the filter and the coaxial SMA cable, the proposed design is measured utilizing the R & S<sup>®</sup> ZNB 8 vector network analyzer (VNA). The experimental configuration is illustrated in Fig. 7 (a). A comparison between the measured and simulated results, as shown in Fig. 7 (b), demonstrates that the passband remains largely consistent, with a frequency range of 2.175 to 4.2 GHz. Within this passband, the insertion loss is below 2.5 dB, indicating effective signal transmission. Additionally, the out-of-band suppression is commendable, and the overall return loss across the band exceeds 10 dB, signifying a well-matched system.

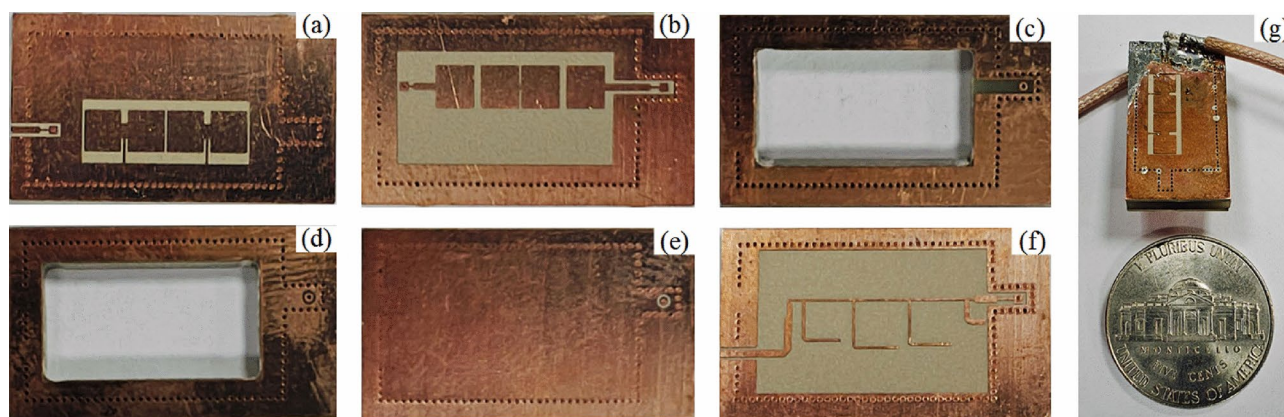
A comparative analysis focuses on Passband (GHz), Fractional Bandwidth (FBW (%)), Insertion Loss (IL (dB)), Return Loss (RL (dB)), Size ( $\lambda_g$  at the central frequency), Size (mm) and Height (mm) with prior studies is provided in Tab. 1. This analysis indicates that the current design's passband IL is competitive with other filters within similar frequency bands, with a notable advantage in compactness<sup>27–32</sup>.

### Methods

#### Influence of air cavity height

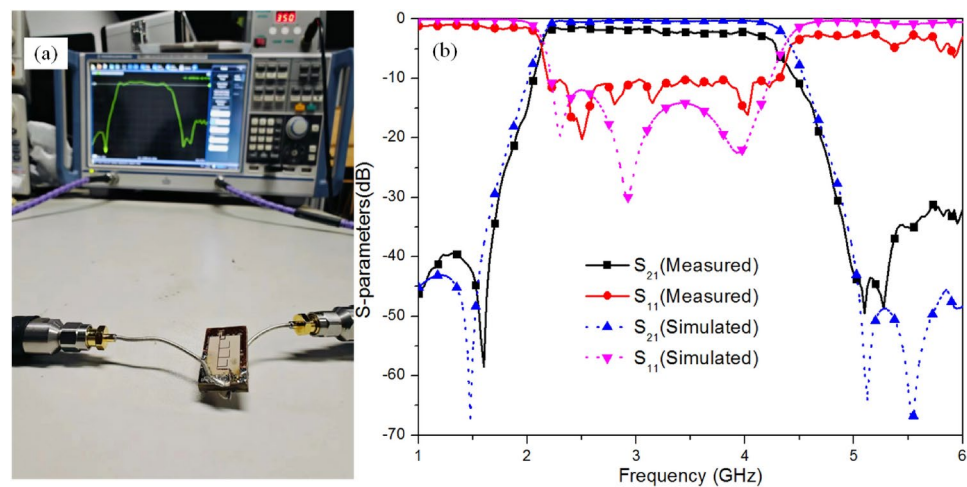
In the proposed design, an air cavity is strategically positioned between the LPF and the HPF, serving as a separator. Along the cavity's periphery, VIAs are meticulously integrated, forming a SISL with a packaging-like structure. This design deviates from traditional SISL configurations, which necessitate two air cavities: one positioned above and one below each component. Consequently, our design requires an initial configuration comprising four air cavities to ensure optimal performance.

During the design process, it is observed that the high-frequency performance of the HPF directly influences the insertion loss of the synthesized BPF within its passband, whereas the LPF exerts minimal impact on the BPF's overall performance. Consequently, only the HPF is packaged. Given its special structure with a DGS (packaging of which would alter the HPF's performance), only the front side of its circuit was packaged within an air cavity, with the DGS layer positioned at the top layer. Additionally, the front side of the LPF's circuit layer was placed at the bottom layer of the entire structure, utilizing its ground as an isolation for the air cavity, thus



**Fig. 6.** Each layer and photo of the prototype. (a) L1, (b) L2, (c) L3, (d) L4, (e) L5, (f) L6, (g) Photo of the packaged prototype.





**Fig. 7.** Measurement results of the BPF. **(a)** Setup of the measurement, **(b)** Comparison between measured and simulated results.

Ref.	Passband (GHz)	IL (dB)	RL (dB)	FBW (%)	Size ( $\lambda_g$ )	Size (mm)	Height (mm)
27	1.4–5.95	4.5	15	124	$0.34 \times 0.27$	$27.4 \times 22$	0.8
28	1.9–6.3	0.5 (simulated)	14 (simulated)	125	$1.09 \times 0.676$	$56.5 \times 35.2$	0.8
29	4.24–7.81	2.2	9	59.25	$2.69 \times 0.42$	$115 \times 30$	0.508
30	1.03–3	2.4	12	98.5	$0.61 \times 0.88$	$76.2 \times 68$	1.5
31	2.32–2.47	1.2	15	12.1	$0.25 \times 0.148$	$19.1 \times 11.2$	0.508
32	2.2–3.6	0.4	11	48	$0.32 \times 0.089$	$24.4 \times 6.6$	0.7874
This work	2.175–4.2	2.5	10	63.5	$0.489 \times 0.218$	$18 \times 8$	3.016

**Table 1.** Analysis of the performance of the proposed BPF in this study compared to several related previous works.

forming a structure with a single air cavity as depicted in Fig. 4 (a). This design merely adopts the packaging method of the SISL, deviating from the typical SISL structure, and can be referred to as a partial SISL, where air cavities are set only where necessary.

Packaging will change the equivalent impedance of the circuit and thus its performance. The characteristic impedance after packaging is mainly determined by the size of the microstrip line, cavity width, and height of the packaged circuit. In this design, the circuit microstrip line size is already determined by the high-pass filter performance, and the air cavity size is also determined by the HPF size, only the air cavity height can be adjusted. Therefore, the air cavity height significantly affects the overall performance of the packaged HPF.

The results of the simulation show that the return loss, as shown in Fig. 8 (a), improves with an increase in the height of the air cavity. However, this improvement necessitates consideration of the trade-offs involved. Specifically, an increased air cavity height leads to a lengthened aperture, essential for the interconnection of the HPF and LPF through VIAs. The extended apertures introduce additional parasitic inductance, which can potentially compromise impedance matching and impact the BPF’s overall performance. Furthermore, increasing the air cavity height results in a proportional expansion of the structure’s dimensions, which counters the objective of miniaturization. Following a thorough evaluation of these factors, we have selected a 2 mm air cavity height.

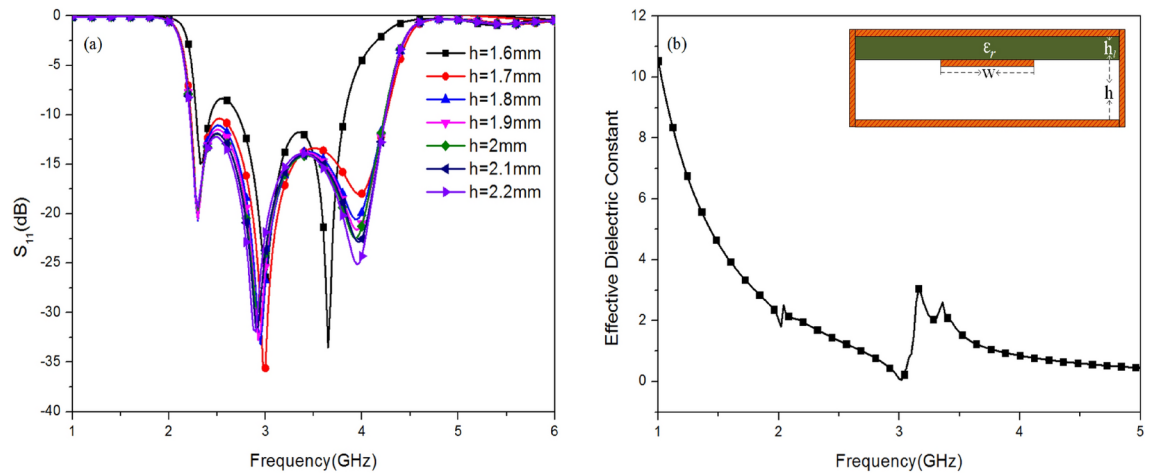
Within the SISL structure, the calculation of characteristic impedance is based on the properties of a shielded suspended substrate microstrip line. The impedance  $Z$  is derived using the following methodology<sup>33</sup>:

$$Z = \frac{Z_0}{\sqrt{\epsilon_{\text{eff}}}}, \tag{1}$$

where  $Z_0$  is the impedance of an identical air-filled line, is again defined as

$$Z_0 = 60 \ln \left[ \frac{f(u)}{u} + \sqrt{1 + \frac{4}{u^2}} \right], \tag{2}$$

with



**Fig. 8.** Influence of air cavity height. (a)  $S_{11}$  parameter as a function of air cavity height, (b) Relative dielectric constant as a function of frequency.

$$f(u) = 6 + (2\pi - 6)e^{-(30.666/u)^{0.7528}}, \quad (3)$$

and

$$u = \frac{\frac{w}{h_l}}{1 + \frac{h}{h_l}}, \quad (4)$$

The effective dielectric constant of the suspended microstrip is given by

$$\epsilon_{\text{eff}} = (1 + f_1 f_2)^2, \quad (5)$$

where

$$f_1 = \sqrt{\epsilon_r} - 1, \quad (6)$$

and

$$f_2 = \frac{1}{\sum_{i=0}^3 c_i \left(\frac{w}{h_l}\right)^i}. \quad (7)$$

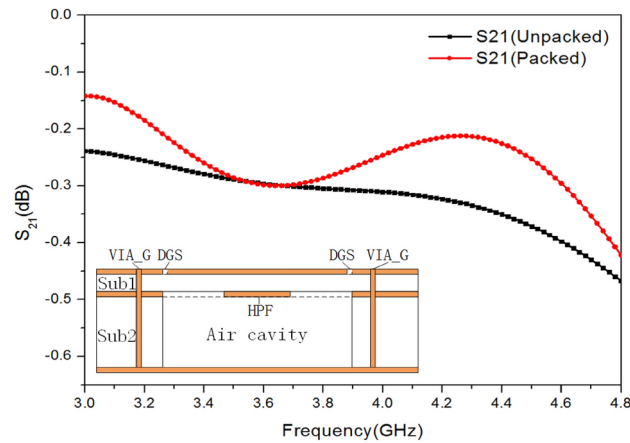
The functions  $c_i$  in Eq. 7, as well as the subsequent formulas, can also be found in Ref. 33.

In this design, upon setting the air cavity height to 2 mm and employing the aforementioned formulas, the calculated characteristic impedance of the packaged structure is determined to be 17.43  $\Omega$ . This value does not align with the desired 50  $\Omega$  port impedance, resulting in a significant discrepancy when compared to the simulation results.

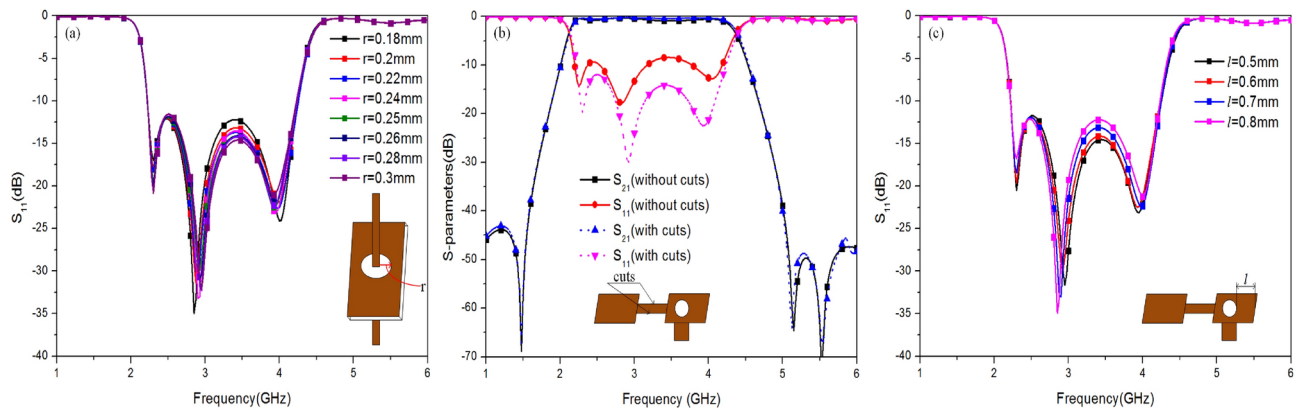
Within this configuration, the HPF circuit, which is packaged in the air cavity, alters the original dielectric constant of the substrate. Direct application of the substrate's nominal relative dielectric constant 10.2 in the formulae yields unreliable results due to this alteration. By employing the S-parameter inversion method detailed in Ref. 34, and further elaborated in Ref. 35 and 36, the actual equivalent dielectric constant post-encapsulation can be accurately determined<sup>34–36</sup>. As illustrated in Fig. 8 (b), at our central frequency of 3.3 GHz, the equivalent dielectric constant is calculated with the air cavity height fixed at 2 mm, resulting in a value of 2.05. By using this value in the formulae, we can calculate a characteristic impedance of 47.34  $\Omega$  for the packaged structure, which is close to the desired 50  $\Omega$  matching condition.

### Influence of package

A comparison between Fig. 5 and Fig. 3 (c) reveals that the BPF with the final encapsulated structure exhibits an in-band insertion loss of less than 0.5 dB within the passband of 3.5 to 4.2 GHz. This performance is superior to the direct series connection depicted in Fig. 3 (a) and (b), where the insertion loss is 0.66 dB at 3.5 GHz and increases to 1.28 dB at 4.2 GHz. As previously discussed, the packaging structure effectively reduces the equivalent dielectric constant of the packaged circuits. According to the attenuation parameter calculation method presented in Eq. 8, a reduction in the equivalent dielectric constant leads to a decrease in the attenuation parameter. Since only the HPF circuit is packaged within the air cavity, we will now proceed to compare the



**Fig. 9.** Changes in  $S_{21}$  after packaged of the HPF.



**Fig 10.** Matching processes. (a)  $S_{11}$  parameter as a function of  $r$ , (b)  $S$  parameter as a comparison with and without cuts, (c)  $S_{11}$  parameter as a function of  $l$ .

insertion losses before and after the packaging of the HPF. This comparison will elucidate the impact of packaging on the filter's performance<sup>37</sup>.

$$a_d = \pi \sqrt{\varepsilon_e q_e} \frac{tg\delta}{\lambda_0} = \frac{\beta \tan \delta}{2} q_e \quad (8)$$

Where  $a_d$  is the attenuation parameter,  $\varepsilon_e$  is the equivalent dielectric constant,  $q_e$  is the filling factor, which is described in detail in Ref. 37,  $\tan \delta$  is the loss tangent,  $\lambda_0$  is the free-space wavelength, and  $\beta$  is the phase constant.

Figure 9 illustrates the simulation results, which clearly indicate that the implementation of air cavity packaging significantly enhances the performance of the BPF by reducing the insertion loss of the HPF.

### Impedance matching

As depicted in Fig. 4 (a), VIA\_Gs interconnect all substrate grounds, while VIA\_Ps link the LPF and HPF ports, necessitating isolation from grounds L2 and L4, named as the isolation ring. This ring significantly influences overall performance. A parametric analysis, varying the isolation ring's radius (labeled as 'r'), is presented in Fig. 10 (a), showcasing its impact.

Impedance mismatches frequently arise at microstrip-to-VIA\_P junctions, mandating impedance matching strategies. Additionally, the VIA\_Ps, traversing multilayer substrates, induce parasitic inductance that must be offset through impedance matching.

Standard practice involves integrating matching cuts in the microstrip line leading to the VIA\_Ps, which are vital for impedance alignment. However, achieving precise impedance matching requires more than adjusting the isolation ring's radius and the cut sizes; an open stub is also incorporated. As Fig. 10 (b) and (c) show, parametric optimizations for the cuts' presence and the open stub's length ( $l$ ) were conducted. After thorough analysis, a configuration of 0.6 mm for the stub length was selected.



## Conclusion

This study introduces a method for constructing wideband BPFs through the vertical three-dimensional interconnection of HPFs and LPFs. The design strategically integrates air cavities and VIAs, packaging the HPF within an air cavity that enhances overall performance while reducing system size and is critical for optimizing insertion loss and the equivalent dielectric constant. Determining the optimal air cavity height through theoretical analysis of the shielded suspended substrate microstrip line and S-parameter inversion is essential for maximizing the filter's performance. The proposed design achieves a wideband frequency range of 2.175 to 4.2 GHz, with an IL of less than 2.5 dB and an RL of more than 10 dB, indicating its acceptable performance.

This design simplifies the structure by placing air cavities only where necessary, providing a streamlined approach to constructing bandpass and multi-band filters with significant reference values. This design, facilitated by a multilayer substrate process, allows for the independent design of each circuit layer, with impedance matching specifically tailored at the connections with feeding VIAs. The layers are then precisely aligned and integrated through a unified sintering process, resulting in a monolithic structure that is well-suited for mass production. This innovative methodology not only enhances fault tolerance and simplifies debugging but also underscores the promising engineering value and theoretical applicability of the design across various frequency bands. The final product is a high-performance, compact bandpass filter that advances the state-of-the-art in microwave component design.

## Data availability

All data generated or analyzed during this study are included in this published article [and its supplementary information files].

Received: 24 July 2024; Accepted: 27 September 2024

Published online: 09 October 2024

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## Acknowledgements

This work was supported by the Southwest Minzu University Research Startup Funds(RQD2024009). Also, this study is supported via funding from Prince sattam bin Abdulaziz University project number (PSAU/2024/R/1446)

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Conceptualization, T.Tang; methodology, M. Aldhaeabi, and T. S. Almoneef; experimental, X. Zhang; data curation, T. Tang; writing—original draft preparation, X. Zhang, and M. Aldhaeabi; writing—review and editing, M. Aldhaeabi and T. S. Almoneef. All authors have read and agreed to the published version of the manuscript.

## Declarations

## Conflicts of interest

The authors declare that there is no conflict of interest regarding the publication of this article.

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