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Performance analysis of DC-DC Buck converter with innovative multi-stage PIDn(1+PD) controller using GEO algorithm

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Power electronic converters are widely used in various fields of electrical equipment. Due to their fast dynamics and non-linear nature, controlling them requires dealing with various complexities. Therefore, having a well-designed, high-speed, and robust controller is critical to ensure the effective operation of these devices. In a DC-DC converter, steady-state performance with minimum error and fast dynamic response relies on controller design. This paper presents the design of a multi-stage PID controller with an N-filter combined with a one plus proportional derivative (1+PD) controller. This controller illustrates fast tracking reference voltage; additionally, it shows incredible results when the DC-DC converter operates in different modes. The parameters of the proposed controller are effectively determined using the golden eagle optimization (GEO) algorithm. Furthermore, a comprehensive comparison between the proposed controller, proportional–integral–derivative (PID), and fractional order PID (FOPID) controllers, as well as different metaheuristic optimization methods in various conditions, has been conducted to demonstrate the effectiveness of the proposed controller. The behavior of the closed-loop system under different conditions has been thoroughly investigated. The superior time and frequency domain characteristics of the closed-loop system with the PIDn(1+PD) controller highlight its superiority over other controllers. The demonstrated enhancements in settling time, voltage regulation accuracy, and transient response emphasize the potential applicability of the proposed control strategy in real-world power electronics systems, particularly in scenarios requiring high efficiency, stability, and dynamic performance.

Keywords Multi-stage controller, DC-DC buck converter, GEO optimization method, Robustness analysis, Transient response, Output voltage control

Abbreviations

DC	Direct current
GEO	Golden eagle optimization
EV	Electric vehicle
RES	Renewable energy systems
PID	Proportional–integral–derivative
$FOPID$	Fractional order PID
IoT	Internet of thing
TID	Tilt-integral-derivative
AO	Aquila optimizer
$AVOA$	African vulture's optimization algorithm

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HGS	Hunger games search
$FDBRUN$	Fitness-distance balance based Runge Kutta
$ITAE$	Integral of time-weighted absolute error
IAE	Integral of absolute error
$ITSE$	Integral of time-weighted square error
ISE	Integral of square error
GWO	Grey wolf optimization
$AEONM$	Artificial ecosystem-based optimization integrated with the Nelder-Mead method
$WOASAT$	Whale optimization algorithm and simulated annealing
$IGJO$	Improved grasshopper jaya optimization
AC	Alternating current
D	Duty cycle
F_S	Switching frequency
POA	Pelican optimization algorithm
CF	Cost function
Δv	Voltage error between reference and actual angular voltage
K_P	Proportional gains of multi-stage controller
K_D	Derivative gains of multi-stage controller
PI	Proportional-Integral
PD	Proportional derivative
MOA	Mayfly optimization algorithm
$OCSANM$	Opposition-based cooperation search algorithm with Nelder- Mead
AEO	Artificial ecosystem optimization
NM	Nelder-Mead
AOA	Archimedes optimization algorithm
GA	Genetic algorithm
SCA	Sine cosine algorithm
EO	Equilibrium optimizer
PSO	Particle swarm optimization
$ISCA$	Improved sine cosine algorithm
PWM	Pulse-width modulation
T_s	Switching time
T_{on}	The duration of the switch is open
T_{off}	The duration of the switch is close
SFG	Switching flow-graph
i_L	Inductor current
i_C	Capacitor current
i_R	Resistance current
V_G	Input voltage
V_O	Output voltage
V_{ref}	Referenced voltage
$E(s)$	Error signal between reference voltage and actual voltage
HO	Hippopotamus optimization
$e(t)$	Error value between reference voltage and actual voltage
V_{dist}	Disturbance voltage
K_I	Integral gains of multi-stage controller
N	Low-pass filter gain

Power electronic converters, such as DC-DC converters, are integral components in a wide array of electrical equipment, ranging from consumer electronics to industrial machinery[1,2]. Buck converters are utilized in renewable energy systems (RES) and DC microgrids[3,4], electrical vehicles (EVs)[5,6], electrical motors[7,8], fast and wireless charging equipment's[5,9–11], electronics and internet of things (IoTs) applications[12–14]. These converters play a critical role in regulating voltage levels, ensuring efficient power transfer, and maintaining the stability of electrical systems. However, the fast dynamics and non-linear nature of DC-DC converters pose significant challenges for control design[15,16]. To achieve optimal performance, it is essential to develop controllers that not only respond swiftly to dynamic changes but also maintain robust performance across various operating conditions[17].

The design and performance of controllers in DC-DC buck converters have been extensively studied, with various controllers proposed to enhance performance[18]. Traditional PID controllers are commonly used due to their simplicity and effectiveness[19,20]. However, more advanced controllers like the FOPID and tilt integral derivative (TID) controllers have been introduced to improve performance further[21,22]. In recent studies, PID, FOPID, TID and self-adaptive Fuzzy-PID controllers have been utilized to control buck converters and power quality enhancement[23–26], demonstrating different advantages. The FOPID controller, for instance, has shown superior performance in handling the non-linear behavior of converters and electrical machines[27,28], while the TID controller offers robust stability and improved dynamic response[29]. This sets the stage for the exploration of optimization algorithms to further enhance these controllers' effectiveness.

To optimize the parameters of these controllers, various metaheuristic optimization algorithms have been employed. Algorithms such as the aquila optimizer (AO)[30,31], African vultures optimization algorithm (AVOA)[32,33], hunger games search (HGS)[34], and fitness-distance balance based Runge-Kutta (FDBRUN)[35]

have been used to fine-tune controller coefficients, resulting in enhanced performance metrics like integral absolute error (IAE), integral square error (ISE), integral time absolute error (ITAE), and integral time squared error (ITSE)[36–38]. The integration of metaheuristic algorithms like grey wolf optimization (GWO) has shown promising results in improving the stability and disturbance rejection behavior of controllers for power converters[23,39,40]. Additionally, hybrid approaches[41–43], such as the artificial ecosystem-based optimization integrated with the Nelder-Mead method (AEONM), have been proposed to combine global search capabilities with local optimization for more precise tuning[42]. These optimization techniques have been critical in improving the steady-state and dynamic responses of buck converters, making them more robust and efficient[44]. However, despite these advancements, there remains a need for controllers that can provide even faster tracking and better performance across various modes of operation.

Hekimoğlu and Ekinci[21] employs a novel approach for tuning PID controller parameters in a DC-DC buck converter. The study introduces the WOASAT algorithm, a hybrid of the whale optimization algorithm and simulated annealing, enhanced with a tournament selection mechanism. Sangeetha, et al.[45] proposes an improved golden jackal optimization (IGJO) algorithm to optimally tune a FOPID controller for a DC-DC buck converter. Based on this, the IGJO algorithm combines the golden jackal optimization algorithm with the capuchin search algorithm to enhance its ability to explore and exploit for finding the best FOPID parameters. In another study, Shayeghi et al.[46] proposed a multi-stage PD(1 + PI) controller for a DC-DC buck converter. This controller cascades a proportional-derivative (PD) stage with a one-plus-proportional-integral (1 + PI) stage. The parameters of the PD(1 + PI) controller are optimized using the mayfly optimization algorithm (MOA) to minimize the ITAE. Similarly, Isen[35], utilizes a novel approach for optimizing the parameters of PID, FOPID, and TID controllers for DC-DC buck converters using a hybrid metaheuristic algorithm called FDBRUN. The proposed FDBRUN algorithm effectively optimizes the parameters of FOPID controllers, leading to improved transient response, robustness, and overall performance enhancement for DC-DC buck converter systems compared to traditional tuning methods.

Izci et al.[42] introduced a new hybrid optimization algorithm called AEONM, which combines the artificial ecosystem optimization (AEO) algorithm with the Nelder-Mead (NM) method. This AEONM algorithm showed improved optimization capabilities and effectiveness in designing PID controllers for buck converter systems. Fong et al.[47] explores the application of the Archimedes optimization algorithm (AOA) for tuning PID controllers in DC-DC buck converters. The AOA is a metaheuristic method inspired by Archimedes' principle, which has shown superior performance in various benchmark tests compared to other optimization algorithms like particle swarm optimizer (PSO), genetic algorithm (GA), sine cosine algorithm (SCA), and equilibrium optimizer (EO). Ersali and Hekimoğlu[48] introduced a new hybrid metaheuristic algorithm called opposition-based cooperation search algorithm with Nelder-Mead (OCSANM) to tune the parameters of a FOPID controller for a DC-DC buck converter system. This controller provides a fast, high-performance solution by combining proportional, derivative, and integral actions in a multi-stage architecture optimized by the MOA. Nanyan et al.[49] introduced the improved sine cosine algorithm (ISCA), an upgraded version of the SCA, to optimize PID controller parameters for a DC-DC buck converter. The ISCA-PID controller demonstrated superior performance in terms of transient response, frequency response, integral error metrics, disturbance rejection, and robustness to parameter variations. Table 1 summarizes the key features and optimization methods used in these studies for tuning DC-DC buck converter controllers.

In the field of power electronics, DC-DC buck converters are crucial for regulating voltage in various applications. Despite progress in controller design, achieving fast and accurate voltage tracking remains a challenge, especially during changing conditions. This study aims to tackle this issue by proposing a new controller, PIDn(1+PD), optimized with the GEO algorithm. Existing research highlights the need for better converter performance across different modes, requiring new control methods. By combining advanced control techniques with optimization algorithms, this research aims to improve transient response and frequency characteristics. Through experiments, we aim to show how the PIDn(1+PD) controller surpasses traditional ones like PID and FOPID. Ultimately, this work seeks to advance power electronics by introducing a new control approach that enhances converter performance and paves the way for future developments.

The primary contributions of this paper are as follows:

(a) **Innovative controller design**: This paper introduces a novel multi-stage controller. The advanced design enables fast tracking of reference voltages, delivering robust performance across different operational modes. By integrating the N-filter and the (1+PD) component, the proposed controller minimizes overshoot and enhances stability, setting a new benchmark in control design.
(b) **Optimization method**: The proposed controller employs the GEO algorithm for precise tuning of its parameters. The GEO algorithm's ability to explore a broad solution space and converge on optimal settings enhances the controller's performance significantly. This optimization ensures that the controller maintains high efficiency and reliability, even in complex and dynamic environments.
(c) **Comprehensive comparison**: This paper conducts extensive comparative analyses between the proposed PIDn(1+PD) controller and conventional PID and FOPID controllers. By evaluating a range of performance metrics, such as rise time, settling time, overshoot, and steady-state error, under different operating conditions, the paper demonstrates the superior performance and versatility of the proposed controller.
(d) **Performance evaluation**: A detailed evaluation of the closed-loop system's behavior is conducted in both time and frequency domains. The results showcase the proposed controller's ability to achieve minimal steady-state error, rapid dynamic response, and robust performance. This comprehensive analysis confirms the controller's effectiveness in maintaining high performance under a wide range of operations.
(e) **Robustness and stability**: The robustness and stability of the proposed controller are rigorously tested against various disturbances and parameter variations. The results highlight the controller's capacity to

Article Ref.	Controllers and optimizations type	Approaches	Findings
[43]	FOPID controllers for buck converters	Effective FOPID tuning via metaheuristic algorithms	FOPID controllers optimized by metaheuristics for buck converters
	Parameters optimized using IGJO, PSO, ABC, SA, GA	Improved performance over conventional PID controller	Outperform FOPID based on IAE, ISE, ITAE, ITSE
	Performance evaluated via IAE, ISE, ITAE, ITSE		Metaheuristics like IGJO, PSO, PSO, ABC, SA, GA are used
[44]	Multi-stage PD(1 + PI) controller	Enhanced dynamics and response over conventional controllers	Proposes multi-stage PD(1 + PI) controller for buck converters
	MOA for parameter optimization	MOA optimization improves time/frequency characteristics	Cascaded PD and 1 + PI structure improves response speed
	Comparisons show efficiency over PID/FOPID	Outperforms PID and FOPID controllers	Parameters optimized via Mayfly Optimization Algorithm (MOA
[19]	PID for DC-DC buck converter	Effective PID optimization via WOASAT	Proposes hybrid whale optimization with simulated annealing (WOASAT) for PID tuning
	WOASAT for parameter tuning	Improved transient, disturbance rejection, time/frequency metrics	WOASAT algorithm with simulated annealing for PID tuning
	WOASAT combines WOA, SA, tournament selection	Superior to standalone SA-PID, WOA-PID	WOASAT combines WOA, SA, and tournament selection
	Demonstrates superiority over SA-PID, WOA-PID		WOASAT-PID outperforms SA-PID and WOA-PID controllers
[45]	PID for closed-loop buck converter	Effective AOA-based PID optimization	AOA for PID tuning in buck converter
	AOA optimizes P, I, D gains	Faster recovery, minimal overshoot, enhanced response	Optimizes P, I, D gains based on load
	Compared to AEONM, AEO, DE, PSO-tuned PIDs AOA-PID demonstrates superiority	Outperforms AEONM, AEO, DE, PSO tuning	Superior voltage recovery, response, regulation
[33]	FOPID, PID, TID controllers for buck converter	Metaheuristics effectively tune FOPID, PID, TID parameters	Investigates FOPID, PID, TID controllers for buck converter
	Parameters optimized using AO, AVOA, HGS, FDBRUN	FOPID with metaheuristic optimization shows superior performance	Parameters optimized via AO, AVOA, HGS, FDBRUN algorithms
	Performance evaluated via IAE, ISE, ITAE, ITSE metrics	Highlights benefits of metaheuristics for controller optimization	FOPID optimized by metaheuristics outperforms PID, TID based on IAE, ISE, ITAE, ITSE
[40]	PID controller for buck converter	Effective PID optimization via hybrid AEONM	Proposes hybrid AEONM algorithm for PID tuning in buck converter
	AEONM tunes PID parameters	Faster response, lower overshoot, better robustness	AEONM = AEO + NM simplex method
	AEONM combines AEO and NM	Outperforms AEO, PSO, DE algorithms	Superior to AEO, PSO, DE-based PID controllers
	Comparisons with AEO, PSO, DE-PID	Effective PID optimization via ISCA, avoids local optima	Proposes Improved Sine Cosine Algorithm (ISCA) for PID tuning
[47]	PID controller for DC-DC buck converter	Outperforms other algorithm-based PID controllers	ISCA overcomes SCA limitations, balances exploration/exploitation
	Parameters optimized using proposed ISCA	Exceptional transient response for buck converter	ISCA-PID shows superior transient response, disturbance rejection, robustness
	ISCA modifies SCA for improved optimization		
	Comparisons with other algorithm-based PID controllers		

Table 1. Overview of utilizing controller and optimization method for DC-DC Buck converter in the recent paper.

maintain performance integrity, proving it to be a reliable choice for practical applications in power electronics. The design's ability to adapt to changing conditions without compromising stability underscores its potential for widespread industrial adoption.

The paper is organized as follows: section "Mathematical model of DC-DC buck converter" covers the mathematical model of the DC-DC buck converter. Section "Motivation to use the proposed controller and optimization method" discusses the motivation to use the proposed controller and optimization method and describe the multi-stage PIDn(1+PD) controller. Section "Buck converter with proposed controller" details the placement and operation of the controller in the DC-DC buck converter, along with the optimization method. Section "Simulation and discussion" includes the simulation and analysis. Lastly, section "Conclusions and future research directions" concludes the paper.

Mathematical model of DC-DC buck converter

Buck converters, commonly employed across various electrical sectors such as computing power supplies, mobile devices, electric vehicles, and televisions, perform the task of reducing higher magnitudes of direct current (DC) voltage to lower levels. This conversion is achieved through pulse-width modulation (PWM) control, regulating the output voltage. A typical buck converter, shown in Fig. 1, consists of at least one FET power switch (MOSFET,

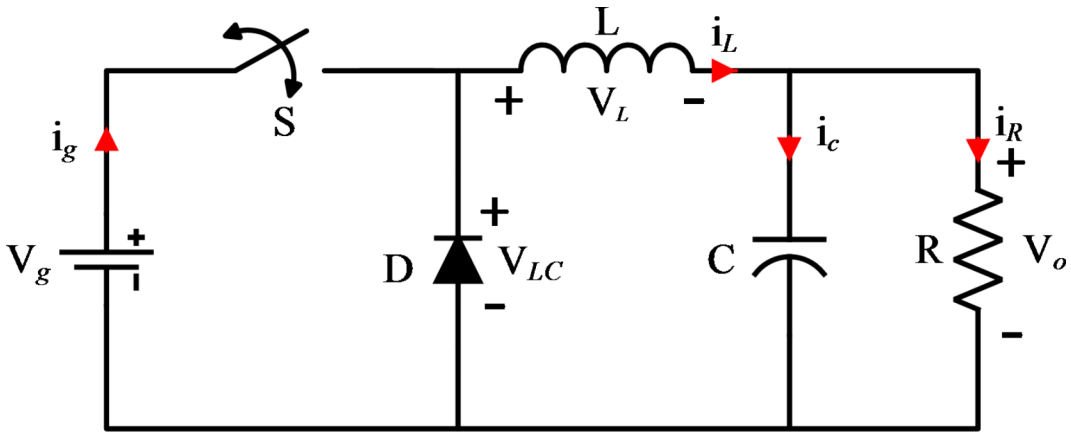

Fig. 1. Buck converter topology.

S), a diode (D), an inductor (L), a capacitor (C), and a resistor (R) as a load. In this configuration, the inductor serves the purpose of energy storage, while the capacitor is integrated into the output to reduce voltage ripple.

In a complete switching cycle with a period T_s , where T_{on} represents the time the switch S is on/closed and T_{off} represents the time it is off/open, the duty cycle (D) is set by the control loop. Equations (1) and (2) shows relation between T_s , T_{on} , T_{off} and duty cycle respectively.

$$T_{on} = DT_s \tag{1}$$

$$T_{off} = (1 - D)\, T_s \tag{2}$$

The state equations of the buck converter are determined based on Kirchhoff's circuit laws, which are expressed through the following relations depending on the open or closed state of the S switch:

- **Close mode switch**.

$$\begin{pmatrix} \hat{i}_L \\ \hat{v}_o \end{pmatrix} = \begin{pmatrix} 0 & -L^{-1} \\ C^{-1} & -(RC)^{-1} \end{pmatrix} \begin{pmatrix} i_L \\ v_o \end{pmatrix} + \begin{pmatrix} L^{-1} \\ 0 \end{pmatrix} v_g \tag{3}$$

- **Open mode switch**.

$$\begin{pmatrix} \hat{i}_L \\ \hat{v}_o \end{pmatrix} = \begin{pmatrix} 0 & -L^{-1} \\ C^{-1} & -(RC)^{-1} \end{pmatrix} \begin{pmatrix} i_L \\ v_o \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \end{pmatrix} v_g \tag{4}$$

In most power supply applications, the output voltage is controlled by adjusting the duty cycle. Therefore, in converter control studies, understanding the transfer function from diode (the Laplace transform of the duty cycle) to output voltage (V_o) is crucial. Small-signal alternating Current (AC) transfer functions can be derived using either the switching flow-graph (SFG) method or the classical method of determining the averaged state-space model. It's important to note that both methods yield the same results. Buck converter waveforms are shown in Fig. 2. By applying Laplace transform to the averaged equations of (3) and (4), the average state-space equation of the buck converter can be expressed as follows:

$$s \begin{pmatrix} I_L(s) \\ V_o(s) \end{pmatrix} - \begin{pmatrix} i_L(0) \\ v_o(0) \end{pmatrix} = \begin{pmatrix} 0 & -L^{-1} \\ C^{-1} & -(RC)^{-1} \end{pmatrix} \begin{pmatrix} I_L(s) \\ V_o(s) \end{pmatrix} + \begin{pmatrix} L^{-1} \\ 0 \end{pmatrix} v_d D(s) \tag{5}$$

Given the initial conditions are assumed to be zero, the transfer function of the buck converter from diode to V_o can be calculated as follows:

$$\frac{V_o(s)}{D(s)} = \frac{Rv_g}{RLCs^2 + Ls + R} \tag{6}$$

$$G_{vd}(s) = \frac{\hat{v}_o}{\hat{d}} = \frac{\frac{v_g}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \tag{7}$$

$$G_{vg}(s) = \frac{\hat{v}_o}{\hat{v}_g} = \frac{\frac{D}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \tag{8}$$

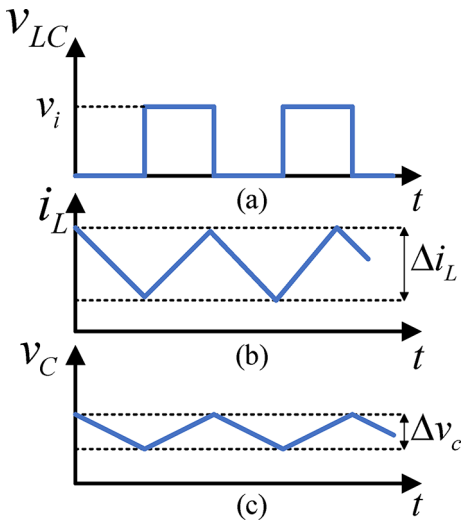

Fig. 2. Buck converter waveforms: (a) LC filter voltage, (b) Inductor current changes, (c) Capacitor voltage changes.

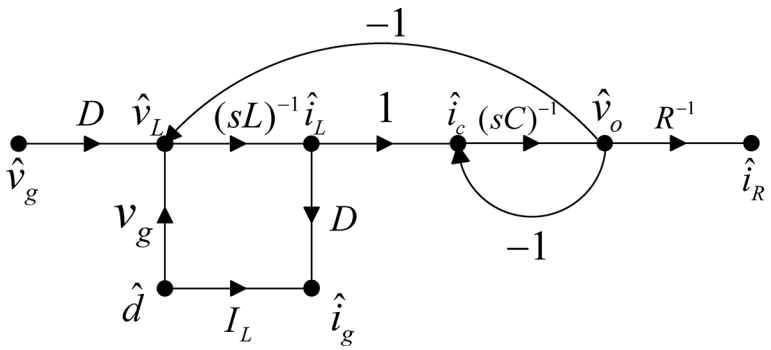

Fig. 3. Buck converter small-signal (dynamic) model.

Parameter	Definition	Value
V_g	Input voltage	36 (V)
V_{ref}	Set-point voltage	12 (V)
R	Resistance	6 (Ω)
L	Inductor	1 (mH)
C	Capacitor	100 (μF)
D	Duty cycle	1/3
F_s	Switching frequency	40 (kHz)

Table 2. Parameters of the analyzed buck converter[21,42,48,50–53].

$$G_{id}(s) = \frac{\hat{i}_L}{\hat{d}} = \frac{\frac{v_g}{L} \times \left(s + \frac{1}{RC}\right)}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \tag{9}$$

$$G_{ig}(s) = \frac{\hat{i}_L}{\hat{v_g}} = \frac{\frac{D}{L} \times \left(s + \frac{1}{RC}\right)}{s^2 + \frac{s}{RC} + \frac{1}{LC}} \tag{10}$$

Buck converter small-signal (dynamic) model is depicted in Fig. 3. The parameters for the buck converter under study, utilized for simulation purposes, are detailed in Table 2.

By using the values from the provided Table 2, we can generate an open-loop step response for the buck converter shown in Fig. 4. This response reflects a change in the duty cycle ratio, resulting in a 12 V shift in the

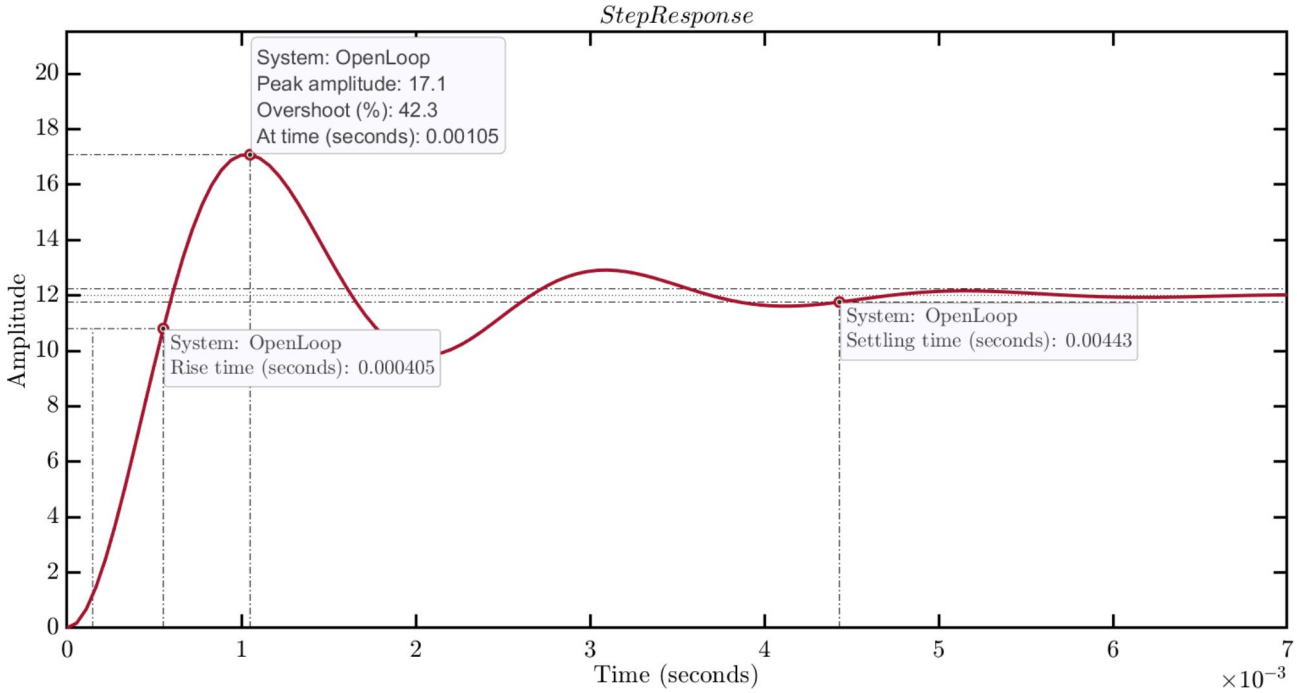

Fig. 4. Open-loop step response of the DC–DC buck converter.

output voltage. As shown in Fig. 4, the open-loop response of the buck converter displays a high overshoot and a lengthy settling time. To improve these aspects, we can employ a proposed controller, which is a straightforward and efficient solution. Details about this controller are discussed in the following subsection.

Motivation to use the proposed controller and optimization method

Proposed multi-stage controller PIDn(1+PD)

This controller amalgamates a PID controller with an N-filter for enhanced performance, effectively curbing oscillations and overshoot while swiftly adapting to dynamic process changes. Additionally, integrating the PD controller ensures rapid stabilization and robust control, empowering the system to achieve optimal setpoint tracking and disturbance rejection, even in intricate, nonlinear systems.

Compared to traditional PID controllers, the PIDn(1+PD) configuration boasts several key advantages. Firstly, the inclusion of the N-filter results in smoother response characteristics, minimizing oscillations and overshoot that commonly plague conventional PID control. This translates to enhanced system stability and better transient response, ultimately leading to tighter regulation of process variables. Furthermore, the PD component augments the PIDn module by providing anticipatory control action, enabling preemptive correction of deviations from setpoints. This feature proves invaluable in scenarios requiring swift responses to disturbances or changing operating conditions. Moreover, when compared to FOPID controllers, the PIDn(1+PD) design demonstrates superior robustness and simplicity in tuning, thanks to its intuitive structure and clearly defined parameters. Leveraging the strengths of both PIDn and PD control elements, this innovative controller emerges as a versatile solution capable of tackling the intricate control challenges encountered in various sectors.

Finally, the multi-stage PIDn(1+PD) control method is used in the DC-DC buck converter because it effectively addresses the dynamic challenges found in power electronics systems. While traditional PID controllers work efficiently in many applications, they often have difficulty handling the disturbances and fast changes required by modern power converters. The innovative multi-stage PIDn(1+PD) controller combines the advantages of a high-order PIDn with a proportional-derivative (PD) component, creating a more robust control strategy that enhances performance in several important methods.

The PIDn element offers improved tuning capabilities to manage the system's complex dynamics and increase precision in voltage regulation. This higher-order approach allows for finer adjustments, leading to reduced steady-state errors and improved system stability. Moreover, the PD component provides predictive control, which enhances the converter's transient response by quickly reacting to rapid changes in load conditions. By integrating these components, the multi-stage PIDn(1+PD) controller effectively reduces overshoot and settling time, which are crucial for maintaining output quality and efficiency in various operating modes. Block diagram of proposed controller is demonstrated Fig. 5.

The choice of the (1+PD) structure over the conventional PD controller is driven by several factors that enhance both performance and robustness, particularly in the context of DC-DC Buck Converters. The inclusion of the unity term (1) serves to improve the low-frequency behavior of the controller. In systems such as DC-DC converters, maintaining accurate control at lower frequencies or in steady-state conditions is essential. A pure PD controller may not sufficiently address steady-state error, which can persist under low-frequency conditions

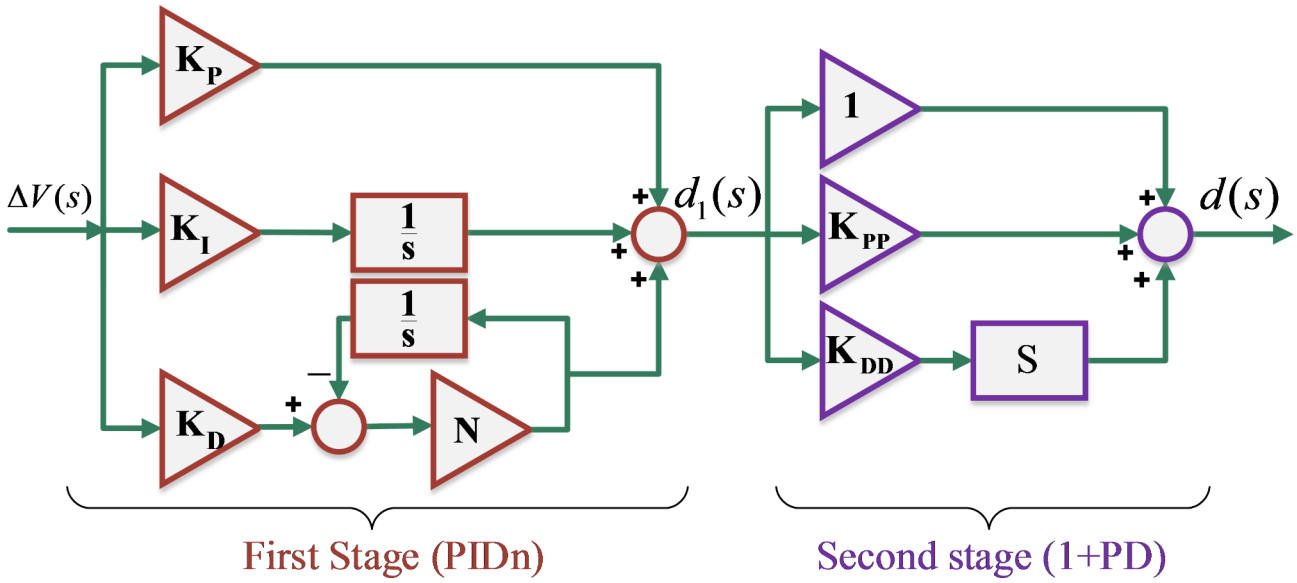

Fig. 5. Proposed PIDn(1+PD) controller structure.

or disturbances. By incorporating the unity term, the controller ensures a continuous correction even at low frequencies, effectively reducing the steady-state error. Furthermore, the unity term contributes to enhancing the stability and robustness of the control system, providing an additional degree of control in both transient and steady-state phases. It helps mitigate the sensitivity to parameter variations and external disturbances, common in real-world power electronics applications. The inclusion of this term also complements the optimization capabilities of the GEO algorithm, allowing for more flexible tuning and better optimization results. This combination enables the (1+PD) controller to provide smoother multi-stage control, better transient response, and enhanced accuracy, making it a superior choice for the application at hand.

The open-loop transfer function of the first stage controller is shown as Eq. (11):

$$G_{PIDn}(s) = \frac{d_1(s)}{\Delta V(s)} = K_P + \frac{K_I}{s} + \frac{K_D N s}{s+N} \tag{11}$$

The second stage provide stability and fine-tuned control for DC-DC buck converter. The open-loop transfer function of the second stage controller is shown as Eq. (12):

$$G_{(1+PD)}(s) = \frac{d(s)}{d_1(s)} = 1 + K_{PP} + K_{DD} \cdot s \tag{12}$$

The open-loop representation of the proposed controller can be depicted by Eq. (13).

$$G_{PIDn(1+PD)}(s) = \frac{d(s)}{\Delta V(s)} = \left(K_P + \frac{K_I}{s} + \frac{K_D N s}{s+N}\right)(1 + K_{PP} + K_{DD} \cdot s) \tag{13}$$

While the additional zero in the proposed controller results in a + 20 dB/dec slope in the Bode plot, which could amplify high-frequency noise, practical measures are implemented to mitigate this. Specifically, a low-pass filter is applied at the output of the controller to prevent the amplification of high-frequency switching noise, commonly found in power electronics circuits. This filter is tuned to have a cutoff frequency just above the system's desired bandwidth, ensuring that the controller's performance within the operating frequency range remains intact while high-frequency noise is effectively attenuated. Additionally, the term $(K_D N s/s + N)$ in the transfer function introduces a pole that limits the high-frequency gain, functioning as a derivative filter. By carefully tuning the parameter '*N*,' the controller further minimizes the impact of high-frequency noise. These combined strategies—low-pass filtering and derivative filtering—ensure that the benefits of the additional zero are retained without sacrificing the controller's practical applicability in power electronics systems. In real-world applications, additional signal conditioning techniques such as proper grounding, shielding, and input signal filtering can be employed to further minimize high-frequency interference. Finally, Eq. (14) illustrates the closed-loop system.

$$G_{closedloop}(s) = \frac{G_{openloop} G_{PIDn(1+PD)}}{1 + G_{openloop} G_{PIDn(1+PD)}} \tag{14}$$

Selection of optimization method

The selection of the GEO algorithm for estimating the parameters of the PIDn(1+PD) controller in the DC-DC buck converter is motivated by GEO's exceptional capability to navigate complex optimization landscapes with high precision and efficiency. GEO is a new and efficient optimization algorithm, and its efficiency has comparatively been shown through benchmark functions and engineering optimization problems. The GEO algorithm is inspired by the intelligent hunting and migration strategies of golden eagles, which allows it to balance exploration and exploitation effectively. This balance is crucial for optimizing the control parameters in proposed model, where the system's performance can be sensitive to parameter variations and require a finely tuned solution to achieve optimal results. The GEO algorithm's adaptive search mechanism enables it to efficiently explore the search space for the best parameter set, minimizing the risk of getting trapped in local optima, a common challenge in optimization problems. By employing the GEO algorithm, the PIDn(1+PD) controller can achieve superior performance metrics, such as reduced steady-state error, faster transient response, and improved robustness against disturbances. Additionally, GEO's relatively simple implementation and fast convergence make it an attractive choice for DC-DC buck converter.

Buck converter with proposed controller

Figure 6 depicts the block diagram of the buck converter system incorporating a PIDn(1+PD) controller. In this diagram, $V_{ref}(s)$, $E(s)$, and $V_o(s)$, represent the reference voltage, error voltage, and output voltage, respectively. Utilizing the parameters listed in Tables 2 and 3, we derive the unity feedback closed-loop transfer function of the buck converter as Eq. (15).

$$G_{closedloop}(s) = \frac{(2.0462E+07)s^3 + (1.6232E+06)s^2 + (1.7292E+07)s + (1.3081E+06)}{(6E-07)s^4 + (2.0462E+07)s^3 + (1.6232E+06)s^2 + (1.7293E+07)s + (1.3081E+06)} \quad (15)$$

The purpose of the controller design is to enhance the dynamic characteristics of the system while eliminating the steady-state error in the converter response. This involves minimizing the integral of the system response deviation from the desired value, denoted as $e(t)$. With semiconductor technologies driving high-speed dynamics in converter switches, it's crucial to maintain or even improve the response speed of the closed-loop system. Therefore, alongside minimizing the integral of the system response deviation, we must also consider the speed or time taken to clear the error. To address these requirements effectively, the ITAE is selected as the optimization cost function (CF), defined as Eq. (16):

$$CF_{min} = \int_0^{t_{sim}} t \cdot |\Delta v|^2 dt \quad (16)$$

The CF is restricted by the range of controller coefficients, defining the search space for the optimization problem as presented in Table 4. Also, Table 3 demonstrates the optimal gain obtaiend with proposed controller and GEO algorithm. The GEO optimization algorithm was iteratively executed in five distinct rounds. Using 50 iterations and participation of 10 particles, the GEO algorithm effectively identifies the optimal controller coefficient values. The duration of the simulation is $t = 6 \times 10^{-6}$ s. Similar to the other metaheuristic approaches, there are parameters that affect the efficiency of the GEO algorithm apart from population size and maximum number of iterations. The studies in the literature employ the two parameters of the GEO by setting them as follows:

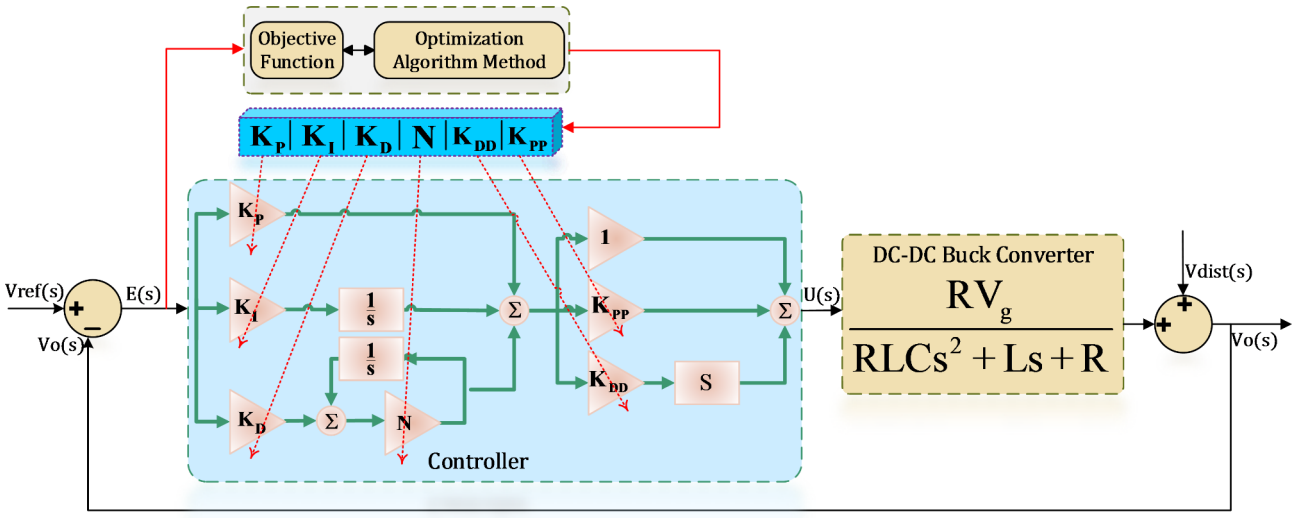

Fig. 6. Block diagram of close-loop DC-DC Buck converter with proposed controller and GEO algorithm.

Controller-Algorithm	K_P	K_I	K_D	N	K_{PP}	K_{DD}	λ	μ
GEO-PIDn(1+PD) (Proposed)	**0.001**	**25.8837**	**30.6391**	**233.7273**	**0.001**	**13.2283**	**0**	**0**
OCSANM-FOPID[46]	47.4243	5.3645	0.01	0	0	0	1.0496	1.1234
CSA-FOPID[46]	27.0475	1.6971	0.01	0	0	0	0.8699	1.1234
LFDSA-FOPID[48]	14.8853	5.1086	0.00982	0	0	0	1.0056	1.0829
IHGS-FOPID[49]	37.6492	5.4315	0.01758	0	0	0	1.0167	1.0285
HHO-FOPID[50]	22.4084	9.9634	0.00977	0	0	0	1.0081	1.0523
AEONM-PID[40]	16.8278	1.1742	0.00992	0	0	0	1	1
AEO-PID[40]	33.1153	7.9506	0.00943	0	0	0	1	1
PSO-PID[40]	37.1502	3.7255	0.00821	0	0	0	1	1
DE-PID[40]	27.6235	1.3043	0.00873	0	0	0	1	1
SA-PID[19]	40.3741	9.45461	0.007808	0	0	0	1	1
WOA-PID[19]	43.5764	7.85992	0.008994	0	0	0	1	1
WOSAT-PID[19]	16.893	3.20991	0.009948	0	0	0	1	1
HHO-PID[50]	17.1269	3.7594	0.00947	0	0	0	1	1
GA-PID[51]	24.1506	7.5391	0.00778	0	0	0	1	1

Table 3. Optimum gains of proposed and other controllers. Significant values are in [bold].

Gains	K_P	K_I	K_D	N	K_{PP}	K_{DD}
Lower limit (min)	0	0	0	0.01	0	0
Upper limit (max)	50	50	50	500	50	50

Table 4. Range of gains in proposed and other controllers.

Algorithm	GEO × 10^{-11}	HO × 10^{-11}	POA × 10^{-11}	PSO × 10^{-9}	GA × 10^{-7}
Best	**1.162**	7.201	9.557	9.852	6.551
Worst	**6.054**	21.07	13.88	17.54	785.31
Mean	**3.252**	13.85	11.02	15.11	314.12

Table 5. Values of the CF following five rounds of optimization algorithms using PIDn(1+PD) controller. Significant values are in [bold].

Propensity to attack ($P_a = [0.5,\ 2]$) and propensity to cruise ($P_c = [1,\ 0.5]$). In this regard, we have adopted similar parameters for the optimization of DC-DC Buck converter system.

Table 5 illustrates the highest, lowest, and mean CF values attained across various controllers. Figure 7 depicts the detailed flowchart showcasing the proposed controller and the GEO algorithm, utilized to improve the performance of the DC-DC buck converter's voltage control system. Figure 8 offers a comparative examination through boxplots of five distinct algorithms: GEO, hippopotamus optimization algorithm (HO), pelican optimization algorithm (POA), PSO and GA. evaluating their effectiveness in minimizing the objective function. Notably, the boxplot in Fig. 8 demonstrates that the poorest result achieved by the GEO algorithm significantly outperforms the best results obtained by fourth the HO, POA, PSO and GA algorithms. This underscores the pronounced superiority of the proposed GEO algorithm in terms of performance. Also Fig. 9 shows CF values of different algorithms with proposed controller. Figure 7 includes the Golden Eagle image, which is sourced from Vitalentum.net.

Transient response analysis

In the evaluation of controllers within the time domain, certain fundamental measurements such as rise time (T_r), settling time (T_s), percent overshoot (OS), and peak time (T_p) hold considerable importance. In Fig. 10, we can observe the step response of the buck converter system using the proposed controller, which has been fine-tuned through the GEO algorithm. Table 6 provides a comprehensive breakdown of performance metrics across different controller strategies in the time domain, encompassing parameters such as T_r, T_s, OS, and T_p. By analyzing the numerical data in the table alongside the step response visuals in the figure, it's clear that the GEO/PIDn(1+PD) controller showcases the most desirable transient response characteristics, including no overshoot, fast settling time, and swift rise time.

To enable a comprehensive numerical comparison, calculations and reporting on time domain evaluation metrics have been conducted across various scenarios. These metrics include the ISE, ITSE, IAE, and ITAE. The corresponding equations for these metrics are outlined in equations (17) through (20).

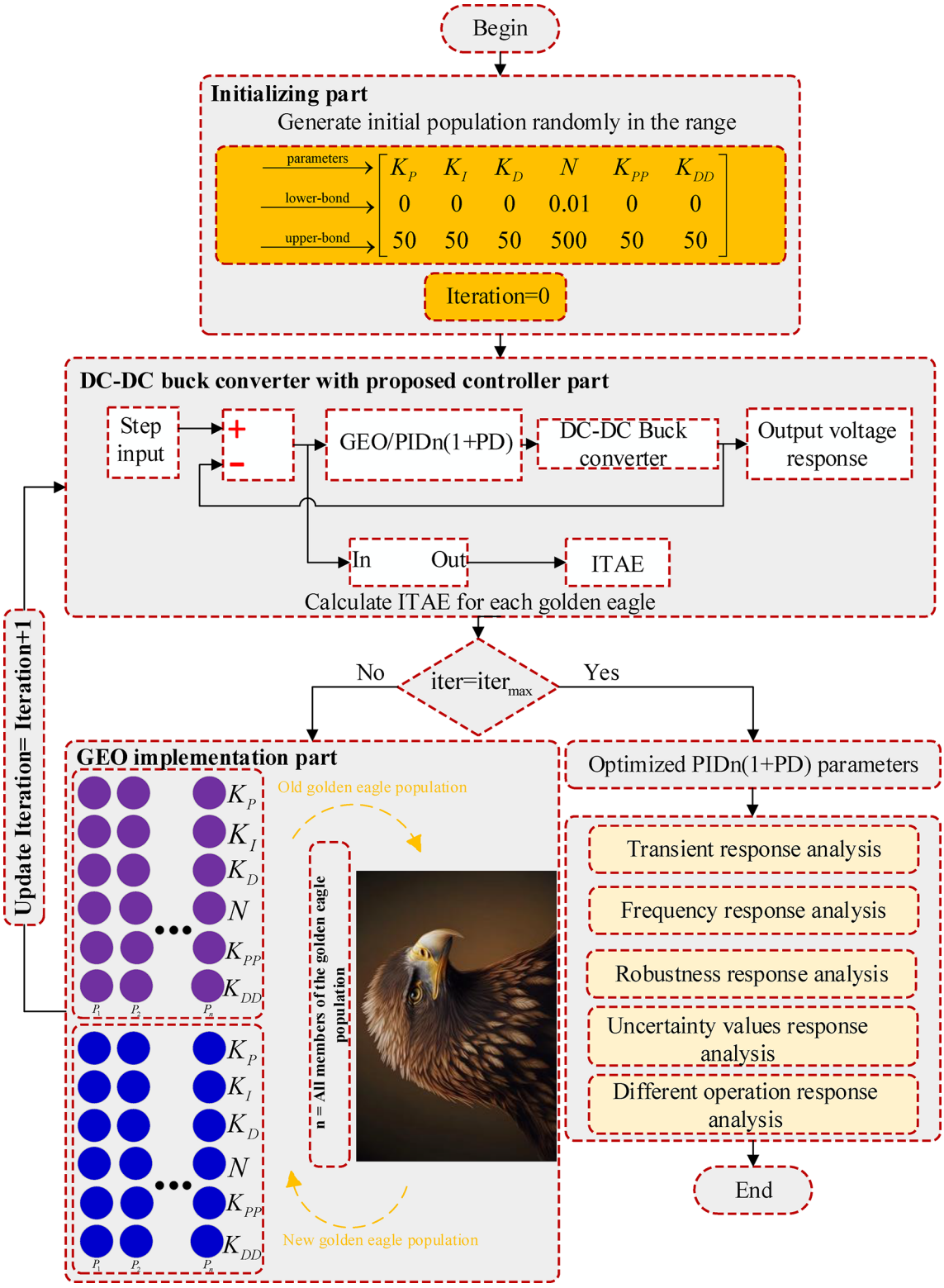

Fig. 7. The schematic of the suggested controller that uses the GEO optimization method to regulate the voltage of a DC-DC buck converter.

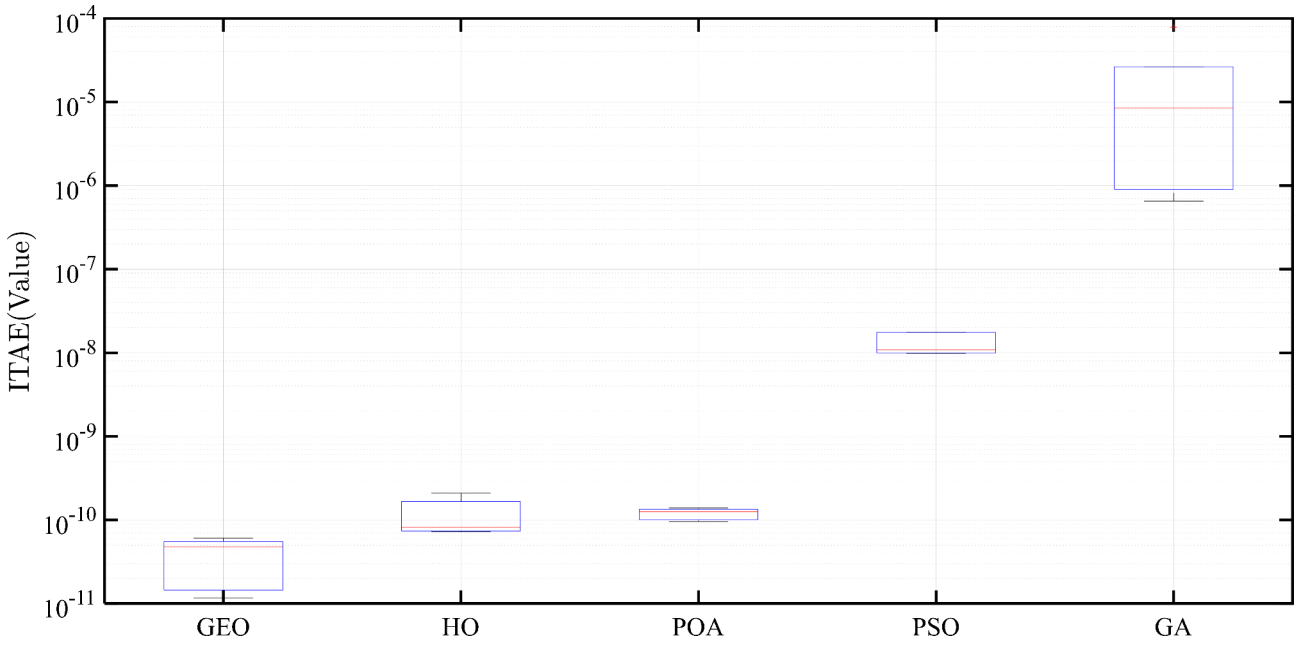

Fig. 8. Boxplot of various algorithms.

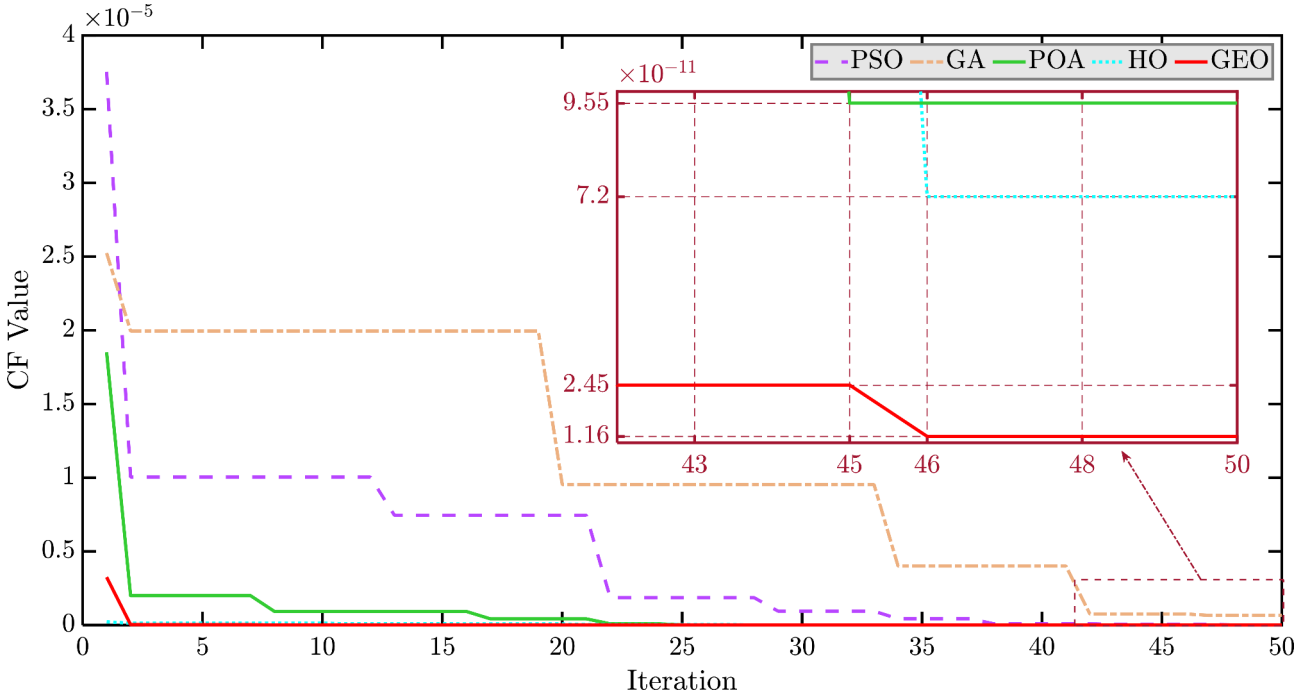

Fig. 9. CF values of different algorithms with proposed controller.

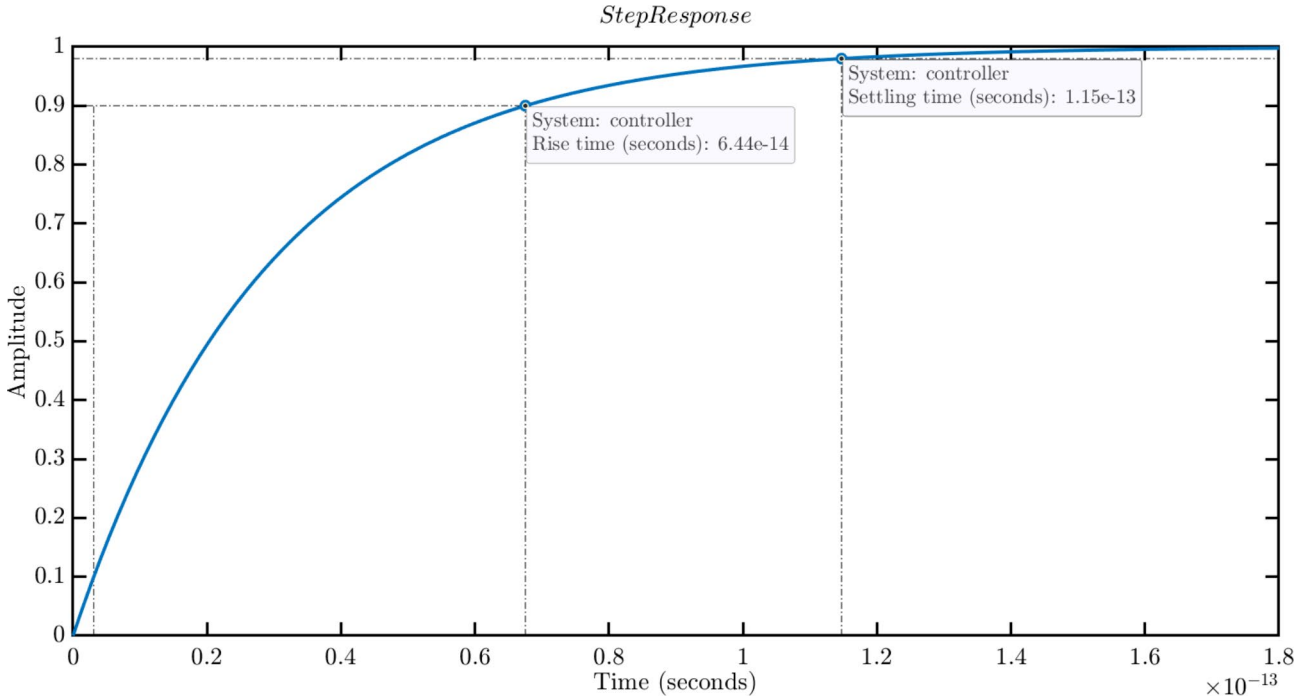

Fig. 10. Step response of proposed controller.

Algorithm-controller	Overshoot (%) × 10^{-3}	Rise time (s) × 10^{-8}	Settling time (s) × 10^{-8}	Peak time (s) × 10^{-8}
GEO-PIDn(1+PD) (Proposed)	**0**	**6.44** × 10^{-6}	**11.5** × 10^{-6}	**21.5** × 10^{-6}
OCSANM-FOPID[46]	0	26.019	46.320	86.727
CSA-FOPID[46]	0	26.023	46.353	86.718
LFDSA-FOPID[48]	0	35.06	62.519	116.81
IHGS-FOPID[49]	0	28.51	50.763	95.022
HHO-FOPID[50]	0	43.528	77.523	145.06
AEONM-PID[40]	0	61.54	109.7	205
AEO-PID[40]	7.031	64.57	114.3	215.8
PSO-PID[40]	5.159	74.06	130.6	248.0
DE-PID[40]	1.872	69.76	123.5	233.1
SA-PID[19]	0	78.26	139.4	260.8
WOA-PID[19]	2.062	67.68	119.6	226.3
WOSAT-PID[19]	0	61.37	109.4	204.5
HHO-PID[50]	0	61.11	108.9	203.6
GA-PID[51]	7.864	78.24	138.4	261.5

Table 6. Transient response of proposed and different controllers. Significant values are in [bold].

$$ISE = \int_0^K e^2(t)\,dt \tag{17}$$

$$ITSE = \int_0^K t.e^2(t)\,dt \tag{18}$$

$$IAE = \int_0^K |e(t)|\,dt \tag{19}$$

$$ITAE = \int_0^K t.\,|e(t)|\,dt \tag{20}$$

Where, K is simulation time in *s*, and $e(t)$ is an error signal between reference voltage and output voltage in DC-DC buck converter. Table 7 represents value of different cost function.

Controller-Algorithm	IAE $\times 10^{-5}$	ISE $\times 10^{-4}$	ITAE $\times 10^{-10}$	ITSE $\times 10^{-9}$
GEO-PIDn(1+PD) (Proposed)	**6.20**	**7.65**	**1.16**	**1.59**
OCSANM-FOPID[46]	5.11	5.26	1.23	1.21
CSA-FOPID[46]	5.27	5.58	1.29	1.33
LFDSA-FOPID[48]	5.37	5.78	1.32	1.41
IHGS-FOPID[49]	5.19	5.41	1.26	1.27
HHO-FOPID[50]	5.31	5.65	1.30	1.36
AEONM-PID[40]	6.92	8.00	2.03	2.30
AEO-PID[40]	6.68	7.47	1.92	2.05
PSO-PID[40]	6.62	7.35	1.90	2.02
DE-PID[40]	6.76	7.65	1.96	2.15
SA-PID [19]	6.57	7.26	1.88	1.98
WOA-PID[19]	6.52	7.16	1.85	1.93
WOSAT-PID[19]	6.92	8.00	2.03	2.30
HHO-PID[50]	6.92	7.99	2.03	2.30
GA-PID[51]	6.81	7.76	1.98	2.20

Table 7. Time-based indicators demonstrating the dynamic response of DC-DC buck converter. Significant values are in [bold].

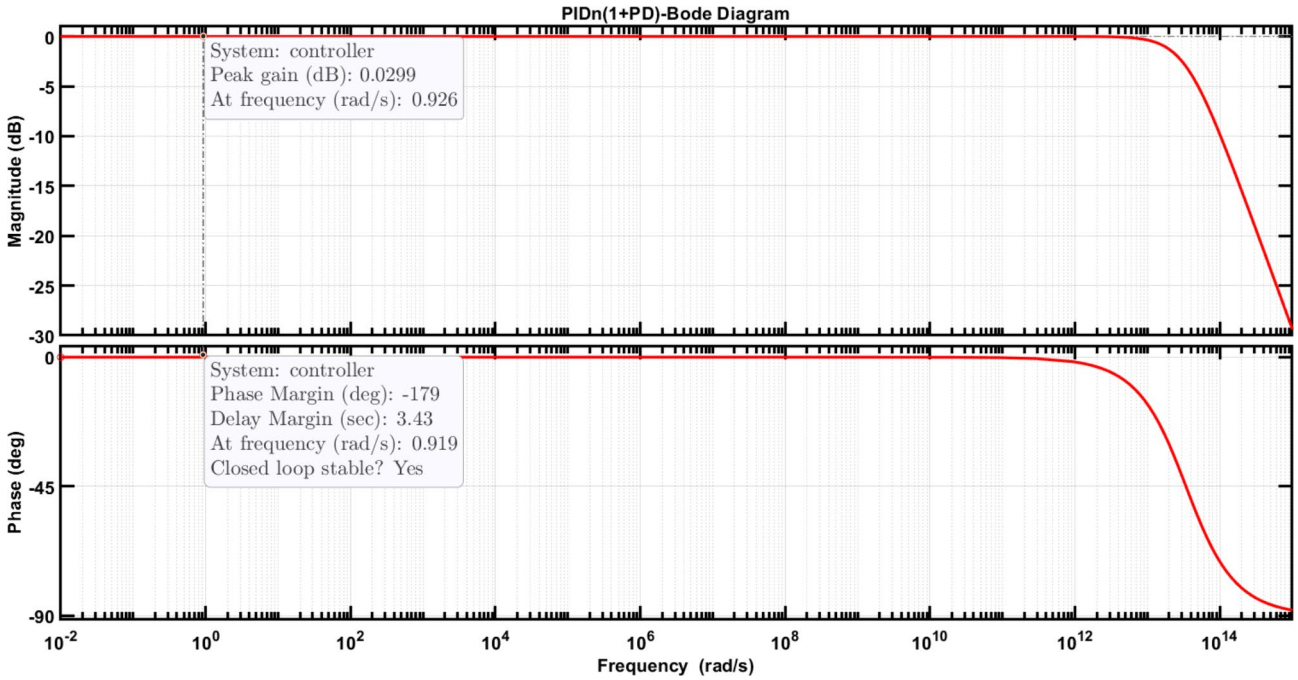

Fig. 11. The Bode diagram of the closed-loop buck converter using proposed controller.

Frequency response

When assessing controllers in the frequency domain, key factors like gain margin, phase margin, and bandwidth play a pivotal role. In Fig. 11, we observe the Bode plot of the buck converter system employing proposed controller, designed through GEO algorithm. Table 8 provides performance metrics for all approaches in the frequency domain, covering parameters such as gain margin, phase margin, and bandwidth. Comparing the numerical results in the table with the Bode plots in the figure, it becomes evident that the GEO/PIDn(1+PD) controller exhibits the most stable frequency response.

Simulation and discussion

In this section, the proposed PIDn(1+PD) controller is operationalized and integrated into the DC-DC buck converter control mechanism as discussed earlier in section "Motivation to use the proposed controller and optimization method". Moreover, these findings show a strong correlation between the results obtained from

Algorithm-controller	Gain margin (dB)	Phase margin (deg.)	Bandwidth (Hz) $\times 10^6$
GEO-PIDn(1+PD) (Proposed)	**Infinite**	**179.1728**	**3.4022** $\times 10^7$
OCSANM-FOPID[46]	Infinite	179.9974	8.4233
CSA-FOPID[46]	Infinite	179.9999	8.4231
LFDSA-FOPID[48]	Infinite	179.9994	7.6879
IHGS-FOPID[49]	Infinite	179.9990	6.2520
HHO-FOPID[50]	Infinite	180	5.0356
AEONM-PID[40]	Infinite	180	3.5628
AEO-PID[40]	Infinite	178.1149	3.3886
PSO-PID[40]	Infinite	177.4863	2.9515
DE-PID[40]	Infinite	178.2405	3.1369
SA-PID[19]	Infinite	177.1461	2.8077
WOA-PID[19]	Infinite	177.4675	3.2334
WOSAT-PID[19]	Infinite	180	3.5728
HHO-PID[50]	Infinite	180	3.5879
GA-PID[51]	Infinite	178.1775	2.7966

Table 8. Frequency response metrics of proposed and different controllers. Significant values are in [bold].

classical controllers[54,55]. Subsequently, the closed-loop system is implemented using MATLAB 2023a with Simulink.

Analyzing a DC-DC buck converter in different operating contexts provides valuable insights into its versatility and performance. Through careful examination, it is possible to understand how the converter can have a suitable output with different input voltages, load conditions, and element values. Such an analysis helps to understand the behavior and performance characteristics of the converter. By studying its response to different operating parameters, we can achieve a deeper understanding of the capabilities and limitations of the converter and design a controller that has minimum loss of efficiency and maximum efficiency against these fluctuations. Basically, a comprehensive analysis of the buck DC-DC converter in different operating scenarios allows us to evaluate the appropriate performance of the designed controller.

Scenario I: analyzed system in different 3 steps

Step 1: Setting the initial reference voltage.
Step 2: Shifting to another output voltage level.
Step 3: Applying the disturbance in the output voltage.

At first, the output voltage level is set at 12 V ($V_{ref} = 12$ V). After establishing this initial voltage, the reference voltage is decreased from 12 to 6 V at $t = 2 \times 10^{-6}$ s. Subsequently, at $t = 4 \times 10^{-6}$ s, a sudden positive disturbance of 1 V change emerges in the converter output voltage, necessitating swift resolution. This error in the output represents a significant disturbance, with the reference voltage at 6 V, constituting more than 16% of the disturbance visible at the output. This disturbance is assumed to manifest as a step increase of + 1 V at the output of the converter as shown in Fig. 12. Figure 12 shows the output voltage of the closed-loop buck converter during reference voltage changes and disturbances by employing proposed and different PID controllers. Figure 13 shows the output voltage of the closed-loop buck converter during reference voltage changes and disturbances by employing proposed and different FOPID controllers.

Scenario II: performance of DC-DC Buck converter in uncertainty inductance

The performance of DC-DC buck converters is critical in various electronic applications, particularly in efficiently regulating voltage. One significant factor influencing their performance is the inductance within the circuit. In this section, we investigate the impact of inductance uncertainty on the performance of a DC-DC buck converter. Specifically, we examine two scenarios. Through the analysis of these scenarios, our objective is to demonstrate the exceptional performance of the proposed controller and highlight its significant difference compared to other controllers under identical conditions.

Increase inductance + 10% to 1.1 (mH)

A 10% increase in inductance to 1.1 (mH) can induce substantial alterations in converter behavior. This rise might compromise the converter's capacity to regulate voltage effectively, potentially resulting in fluctuations in output voltage and ripple. However, these effects can be mitigated through the design of a robust controller, ensuring a reliable output. The proposed controller offers this assurance compared to alternative controllers.

Decrease inductance − 10% to 0.9 (mH)

On the other hand, a decrease in inductance by ten% to 0.9 (mH) also presents challenges for the DC-DC buck converter's performance. A reduction in inductance can alter the converter's dynamics, affecting its transient response and overall stability. The decreased inductance may lead to higher ripple currents and voltage spikes, posing potential risks to the converter and other components in the circuit. As depicted in Table 9, the values demonstrate the remarkable performance of the proposed controller in comparison to others.

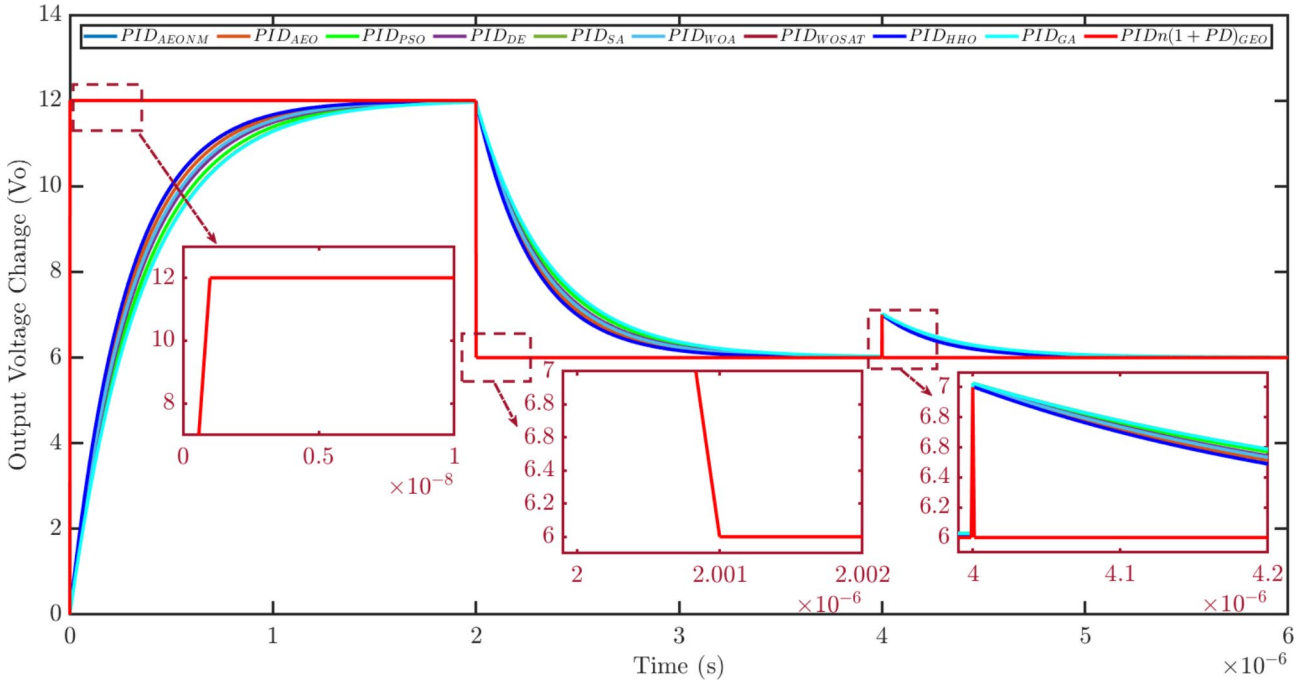

Fig. 12. Output voltage of the closed-loop buck converter during reference voltage changes and disturbances by employing proposed and different PID controllers.

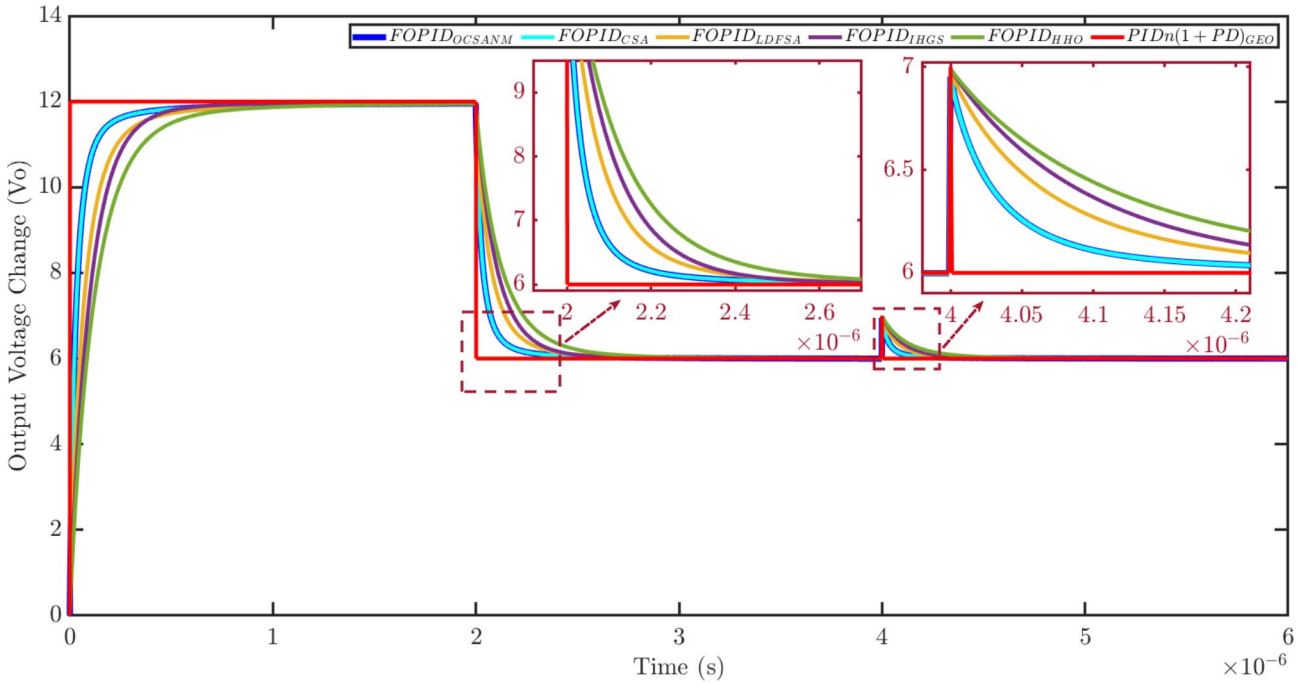

Fig. 13. Output voltage of the closed-loop buck converter during reference voltage changes and disturbances by employing proposed and different FOPID controllers.

Scenario III: performance of DC-DC Buck converter in uncertainty capacitor

Another element that affects the efficiency and reliability of DC-DC buck converters is the capacitors used in their circuits. In this section, we examine how uncertainty in capacitor values affects the performance of such converters. In particular, we investigate two scenarios. By analyzing these scenarios, we aim to demonstrate the performance of the proposed controller in the condition that the circuit capacitors are defective.

Parameter	Rate of change	Algorithm-Controller	Overshoot (%) $\times 10^{-3}$	Rise time (s) $\times 10^{-8}$	Settling time (s) $\times 10^{-8}$	Peak time (s) $\times 10^{-8}$
L	− 10%	**GEO-PIDn(1+PD) (Proposed)**	**0**	**6** $\times 10^{-6}$	**10** $\times 10^{-6}$	**19** $\times 10^{-6}$
		OCSANM-FOPID [46]	0	23.417	41.689	78.054
		CSA-FOPID [46]	0	23.421	41.714	78.046
		LFDSA-FOPID [48]	0	31.560	56.258	105.13
		IHGS-FOPID [49]	0	25.659	45.687	85.520
		HHO-FOPID [50]	0	39.175	69.768	130.55
		AEONM-PID [40]	0	55	99	185
		AEO-PID [40]	0	58	103	194
		PSO-PID [40]	198	67	118	223
		DE-PID [40]	0	63	111	210
		SA-PID [19]	446	70	124	235
		WOA-PID [19]	212	61	108	204
		WOSAT-PID[19]	0	55	98	184
		HHO-PID[50]	0	55	98	183
		GA-PID [51]	0	71	125	235
L	+ 10%	**GEO-PIDn(1+PD) (Proposed)**	**0**	**7** $\times 10^{-6}$	**12** $\times 10^{-6}$	**23** $\times 10^{-6}$
		OCSANM-FOPID[46]	0	28.621	50.950	95.400
		CSA-FOPID[46]	0	28.144	51.378	209.88
		LFDSA-FOPID[48]	0	38.577	68.783	128.49
		IHGS-FOPID[49]	0	31.361	55.839	104.52
		HHO-FOPID[50]	0	47.881	85.277	159.56
		AEONM-PID[40]	0	68	120	226
		AEO-PID[40]	0	71	126	237
		PSO-PID[40]	387	82	144	273
		DE-PID[40]	0	77	136	256
		SA-PID[19]	690	86	151	287
		WOA-PID[19]	405	74	131	249
		WOSAT-PID[19]	0	67	120	225
		HHO-PID[50]	0	67	120	224
		GA-PID[51]	0	86	153	288

Table 9. Performance comparisons for Inductance uncertainty. Significant values are in [bold].

Increase capacitor + 10% to 110 μF
A slight boost of 10% in capacitance to 110 (μF) can greatly impact the performance of the DC-DC buck converter. This adjustment might disrupt the converter's capability to uphold a steady voltage output, leading to fluctuations in voltage regulation and ripple suppression.

Decrease capacitor − 10% to 90 μF
On the other hand, a 10% decrease in capacitance to 90 (μF) creates obstacles for the buck DC-DC converter performance. Decreasing capacitance may impair the converter's ability to filter noise and react to sudden changes, possibly compromising its stability. With less capacity, there is a risk of increased voltage waves and reduced energy storage capacity, which can threaten the converter and other circuit components. As depicted in Table 10, the values demonstrate the remarkable performance of the proposed controller in comparison to others.

Scenario IV: performance of DC-DC Buck converter in uncertainty resistance

Another element that the performance of DC-DC buck converters is strongly dependent on is resistance. This resistance usually adjusts the voltage and current in the buck converter. In this part, we will examine the effect of uncertainty in the resistance values on the performance of the DC-DC buck converter. In particular, we examine two scenarios. By examining these scenarios, our goal is to reveal the effect of the strong controller in compensating the sudden increase or decrease in resistance in the buck converter circuit.

Increase resistance + 20% to 7.2 Ω
A 20% increase in resistance to 7.2 (Ω) can significantly change the behavior of the buck DC-DC converter. This change may impair the converter's ability to regulate voltage effectively, potentially leading to output voltage fluctuations and increased power losses.

Parameter	Rate of change	Algorithm-Controller	Overshoot (%) $\times 10^{-3}$	Rise time (s) $\times 10^{-8}$	Settling time (s) $\times 10^{-8}$	Peak time (s) $\times 10^{-8}$
C	− 10%	**GEO-PIDn(1+PD) (Proposed)**	**0**	**6** $\times 10^{-6}$	**10** $\times 10^{-6}$	**19** $\times 10^{-6}$
		OCSANM-FOPID[46]	0	23.419	41.698	78.052
		CSA-FOPID[46]	0	23.422	41.723	78.045
		LFDSA-FOPID[48]	0	31.562	56.275	105.12
		IHGS-FOPID[49]	0	25.661	45.698	85.518
		HHO-FOPID[50]	0	39.179	69.795	130.55
		AEONM-PID[40]	0	55	99	185
		AEO-PID[40]	0	58	103	194
		PSO-PID[40]	142	67	118	223
		DE-PID[40]	0	63	112	210
		SA-PID[19]	387	70	124	235
		WOA-PID[19]	161	61	108	204
		WOSAT-PID[19]	0	55	98	184
		HHO-PID[50]	0	55	98	183
		GA-PID[51]	0	71	125	235
C	+ 10%	**GEO-PIDn(1+PD) (Proposed)**	**0**	**7** $\times 10^{-6}$	**13** $\times 10^{-6}$	**24** $\times 10^{-6}$
		OCSANM-FOPID[46]	0	28.619	50.939	95.401
		CSA-FOPID[46]	0	28.625	50.981	95.390
		LFDSA-FOPID[48]	0	38.573	68.761	128.49
		IHGS-FOPID[49]	0	31.359	55.825	104.53
		HHO-FOPID[50]	0	47.876	85.245	159.57
		AEONM-PID[40]	0	68	120	226
		AEO-PID[40]	0	71	126	237
		PSO-PID[40]	443	81	144	273
		DE-PID[40]	0	77	136	256
		SA-PID[19]	748	86	151	287
		WOA-PID[19]	456	74	131	249
		WOSAT-PID[19]	0	67	120	225
		HHO-PID[50]	0	67	120	224
		GA-PID[51]	0	86	153	288

Table 10. Performance comparisons for capacitor uncertainty. Significant values are in [bold].

Decrease resistance − 20% to 4.8 Ω

On the other side, a 20% reduction in resistance to 4.8 (Ω) poses challenges for DC-DC buck converter performance. Reduced resistance may affect the converter's current control capabilities and efficiency, potentially affecting its overall stability. Lower resistance levels can lead to increased current flow and increased power dissipation, creating hazards for the converter and other components in the circuit. As depicted in Table 11, the values demonstrate the remarkable performance of the proposed controller in comparison to others.

Conclusions and future research directions

This study introduced and analyzed the performance of a new multi-stage PIDn(1+PD) controller for DC-DC buck converters, with parameters optimized using the GEO algorithm. Our research shows the controller's exceptional ability to achieve fast-tracking voltages and maintain robust performance across different operating modes. A thorough comparison with traditional PID and advanced FOPID controllers, along with various metaheuristic optimization techniques, confirms the superiority of the proposed controller. The PIDn(1+PD) controller demonstrates improved time and frequency domain characteristics, proving its effectiveness in handling the non-linear and fast dynamic nature of DC-DC converters. Using the GEO algorithm for parameter optimization has been successful in enhancing the controller's performance, ensuring minimal steady-state error and a quick dynamic response. This innovative approach addresses the complexities inherent in power electronic converters, offering a high-speed, robust solution that outperforms existing controllers. Overall, the findings of this research provide valuable insights into the design and optimization of controllers for DC-DC buck converters, advancing the field of power electronics.

The PIDn(1+PD) controller, with its optimized parameters, stands out as a reliable and efficient solution, paving the way for future developments in this area. The practical applicability of the proposed PIDn(1+PD) controller in power electronics systems is reinforced by the mitigation strategies employed to handle high-frequency noise. By integrating a low-pass filter and derivative filtering, the controller is capable of attenuating high-frequency noise while maintaining the advantages provided by the additional zero in the transfer function. This ensures that the proposed controller can operate effectively in real-world power electronics environments, where high frequency switching signals are prevalent. Additionally, the robust design, coupled with practical

Parameter	Rate of change	Algorithm-Controller	Overshoot (%) $\times 10^{-3}$	Rise time (s) $\times 10^{-8}$	Settling time (s)$\times 10^{-8}$	Peak time (s)$\times 10^{-8}$
R	− 20%	**GEO-PIDn(1+PD) (Proposed)**	**0**	**6** $\times 10^{-6}$	**11** $\times 10^{-6}$	**21** $\times 10^{-6}$
		OCSANM-FOPID[46]	0	26.020	46.323	86.726
		CSA-FOPID[46]	0	26.024	46.356	86.717
		LFDSA-FOPID[48]	0	35.069	62.526	116.81
		IHGS-FOPID[49]	0	28.511	50.767	95.022
		HHO-FOPID[50]	0	43.529	77.533	145.05
		AEONM-PID[40]	0	62	110	205
		AEO-PID[40]	0	65	115	216
		PSO-PID[40]	274	74	131	248
		DE-PID[40]	0	70	124	233
		SA-PID[19]	548	78	137	261
		WOA-PID[19]	291	68	120	226
		WOSAT-PID[19]	0	61	109	204
		HHO-PID[50]	0	61	109	204
		GA-PID[51]	0	78	139	262
R	+ 20%	**GEO-PIDn(1+PD) (Proposed)**	**0**	**6** $\times 10^{-6}$	**11** $\times 10^{-6}$	**21** $\times 10^{-6}$
		OCSANM-FOPID[46]	0	26.017	46.303	86.730
		CSA-FOPID[46]	0	26.021	46.336	86.720
		LFDSA-FOPID[48]	0	35.063	62.486	116.81
		IHGS-FOPID[49]	0	28.507	50.742	95.026
		HHO-FOPID[50]	0	43.521	77.475	145.06
		AEONM-PID[40]	0	62	109	205
		AEO-PID[40]	0	65	114	216
		PSO-PID[40]	386	74	131	248
		DE-PID[40]	0	70	124	233
		SA-PID[19]	666	78	137	261
		WOA-PID[19]	394	68	119	226
		WOSAT-PID[19]	0	61	109	204
		HHO-PID[50]	0	61	109	204
		GA-PID[51]	0	78	139	262

Table 11. Performance comparisons for resistance uncertainty. Significant values are in [bold].

considerations such as signal conditioning, makes this controller suitable for industrial applications requiring high stability, precision, and dynamic performance.

Future research endeavors could explore several avenues aimed at extending and refining the findings of this study. Firstly, there is a pressing need for hardware implementation to validate the proposed control strategy's efficacy in real-world applications, thereby bridging the divide between theoretical analysis and practical deployment. Robustness analysis emerges as a critical domain, necessitating investigation into the controller's resilience against diverse operating conditions, including load variations, input voltage perturbations, and voltage fluctuations, thereby ensuring stability and reliability across a spectrum of scenarios. Furthermore, the exploration of multi-objective optimization techniques presents a promising trajectory, enabling the simultaneous optimization of efficiency, transient response, and cost-effectiveness to meet the multifaceted demands of contemporary power electronics applications. Adaptive control strategies represent a compelling avenue for research, wherein dynamic parameter adjustment in response to evolving operating conditions could enhance adaptability and performance robustness in dynamic environments. Moreover, the integration of the proposed control strategy with renewable energy systems warrants scrutiny, with a focus on augmenting overall system efficiency and stability in distributed power generation contexts, thereby advancing the paradigm of sustainable energy conversion. By embarking on these research trajectories, the field stands poised to realize substantial advancements in the domain of power electronics, fostering innovation and addressing emerging challenges in energy conversion and management.

Data availability

The datasets used and/or analyzed during the current study available from the corresponding author on reasonable request.

Received: 10 June 2024; Accepted: 22 October 2024
Published online: 27 October 2024

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Competing interests

The authors declare no competing interests.

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