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High controllability soft switching step-up DC-DC converter with CI, (QBC) structure and VM technique

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In this article, an ultra-high step-up DC-DC converter inspired by the quadratic boost converters (QBC) consisting of coupled inductor (CI) and voltage multiplier (VM) technique with high controllability is introduced. The proposed converter is consisted of three boost stages managed to provide a reliable higher level of voltage into the output load. The primary windings side of the CI is incorporated with two switched-capacitor (SC) boost stages which lift up the input voltage and transfer the energy into the output load through the CI. The secondary winding side of the CI is integrated with a VM cell in order to provide the third boost stage to ultimate increase the output voltage gain. Some major drawbacks such as limited output voltage gain, high voltage stress on power switches, low efficiency due to high component count and controllability issues are observed in conventional converters. Compared with the existing QBC structures, the proposed converter can obtain a much higher output voltage under the same duty cycle while mitigating the voltage stresses on semiconductors. The significant advantages of the proposed converter include items such as high voltage gain, lower losses, continuous input current and robust performance which provide a reliable output power for various applications such as renewable energy systems and photovoltaic (PV) energy-based systems. Furthermore, using fewer components and lower voltage stress on switches and diodes, also lower current stress across switching devices due to ZCS performance are among the other advantages of the suggested structure. The presence of a common ground between source and load makes the converter suitable for a wide range of applications. The reliability of the suggested converter is investigated with the help of pole-placement control method to ensure a robust performance. Finally, to ascertain of flawless performance, a 150 W prototype of the proposed converter with 20 V input and 345 V output voltage operating under 50 kHz switching frequency with almost 93% of practical efficiency is built and tested in laboratory. By validating the theoretical analysis with practical results, in the comparison section, the characteristics of the suggested converter such as output voltage gain, voltage stress, efficiency and other major parameters are compared with similar structures to demonstrate the advantages and disadvantages of the proposed converter.

Keywords DC-DC converter, High step-up, Coupled-inductor, QBC, Soft-switching, ZCS, Voltage multiplier cell, Pole-placement method

Over the last few decades, the need to utilize renewable energy sources has literally been increasing. Global crises such as air pollution and increase in fossil fuel price have pushed us towards clean and inexpensive form of energy sources such as photovoltaic and fuel cells. Versatility, ease of access, and low-cost maintenance, along with the increasing development of technologies in the renewable energies are among their significant advantages. However, the low magnitude of the voltage value provided by the renewable energy sources is one of their drawbacks. To overcome this issue, the high step-up DC-DC converters are proposed as a solution. In recent decades, diverse structures have been introduced as voltage boost converters for various applications such as DC bus regulation in micro sources[1] or as an intermediate interface for feeding micro inverters[2]. There are various well-known techniques such as switched inductors, switched capacitors, coupled inductors in non-isolated structures[3,4] or using isolated transformers in high frequency converters which are used frequently in different applications. Bidirectional structures are another type of DC-DC converters that can transfer energy in both directions and are widely used in electric vehicles and renewable energy systems[5]. However, there are

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some advantages and disadvantages to each of these methods. The conventional converters based on switched inductors and switched capacitors have been widely used in many applications to provide high voltage gain[6], although in general, the low efficiency of these structures along with high current demand from the source and high fluctuation of the output voltage are considered as serious disadvantages[7,8]. The boost converters based on cascaded structures can be another choice, however, the need for a large number of components and low efficiency due to voltage drop in semiconductors are among the disadvantages of such structures[9,10]. In latest few decades, the interleaved configuration has been introduced as another choice for step-up DC-DC structures. Interleaved configuration utilized on some type of converters have good advantages such as low ripple on both input and output ports, leading to lower losses and lower output filter sizes[11–13]. Moreover, voltage stress is significantly reduced on the components in the interleaved converters[14]. Although, some undesired constraints are included such as power limitation at high voltage gain[15,16]. Meanwhile, as another drawback of interleaved topologies, the need for additional current control loops to balance the active current literally increase the complexity of control[7,17]. Furthermore, in recent years, some other type of interleaved structures without using of transformers have been proposed which have the advantage of simple and expandable design[18–21]. The Z-source and quasi Z-source converters are proposed in[22]. The lack of common ground feature along discontinuity in the current of input source are two major drawbacks of Z-source structures. Although, the issue of discontinuous current has been solved in quasi Z-source converter, but it operates under lower voltage gain due to the limitation of duty cycle[23]. Quadratic boost converters (QBC) are another type of topologies which can operate under continuous input current while also providing low voltage/current stress on the components[1,24,25].

The non-isolated converters based on QBC structure are literally cost-saving designed to be more compact and light weight. Moreover, common ground feature is counted as another advantage of QBC structures which are widely used in many applications[26,27]. In ref[24]. a high step- up converter integrated of a quadratic boost structure along a voltage doubler is proposed. The voltage doubler cell is implemented with cascading method along a high frequency transformer. However, implementing a large number of components such as power diodes and capacitors in the structure of these converters lead to deterioration of the efficiency. Generally, extra power loss due to transformer is imposed to the converter, moreover, the power density limitation seems as another drawback for this converter.

The combination of QBC structure with switched-capacitor cells are recently become an attractive solution for DC-DC converters. The switched capacitor cells are useful to obtain compact and light-weight converters with high efficiency and high voltage gain in moderate duty cycles. In addition, as another advantage, in the converters consisted of SC cells, the electromagnetic interface (EMI) issues are significantly less[18].

In this study, a new optimized non-isolated step-up DC/DC converter which inspired by QBC structure and taking advantage of combination of coupled inductor and voltage multiplier cell is introduced. Ultra-high voltage gain, using lower components, reduced voltage stress on power switches and diodes, soft-switching operation for both power switches along three out of five power diodes and high efficiency performance of the converter are the main features. Moreover, the leakage energy of CI is recovered and perfectly delivered to the output load to optimize the efficiency of the proposed converter performance. The proposed soft switching step-up DC-DC converter is designed for low power range applications and can be applied in small-scale renewable energy systems such as residential solar panels, fuel cells and small off-grid systems. High efficiency and reduced EMI are two major parameters obtained in ZCS performance. In addition, soft switching improves efficiency by reducing heat losses in PV systems. It is possible to re-design the components value in order to be utilized for higher power range of such applications. To assess the performance of the proposed converter, first of all, in Sects. 2 and 3, the proposed converter is analyzed in steady state mode in order to obtain major parameters such as, the voltage gain, the normalized voltage stresses of the components and the averaged and rms current values which are needed to determine the theoretical efficiency. Then, in comparison section, the proposed converter has been compared to some other step-up converters by details. Additionally, to demonstrate the stability and controllability of the proposed converter, the dynamic model analysis based on state space averaged (SSA) method is applied to extract the state equations of the system[28,29]. Next, to evaluate the reliability of the proposed system, a robust control strategy using pole-placement method is applied and the results are obtained. Eventually, in the experimental section, a prototype of the converter is built and tested in laboratory in order to provide and compare experimental result with theoretical estimations. Finally, in the last section of the study, a brief conclusion is provided.

Proposed converter topology

The power circuit of the proposed topology is shown in (Fig. 1). The suggested DC-DC structure is implemented based on a switched capacitor cell (SC), non-isolated CI and a VM cell. The CI implemented in the proposed structure is consisted with the primary turns of N_P and secondary turns of N_S. The proposed converter is included of two power switches which are placed near the source and on the primary windings side of the CI in order to alleviate the voltage stresses on them. The inductor L_1 is embedded between the source and SC cell to collaborate as the first boost stage. Furthermore, the CI, and the second SC cell as the second boost stage, are integrated in suggested topology. The power diode D_1 and capacitor C_2 are clamped to primary windings side. At the secondary windings side of CI, VM cell is implemented as voltage lift to increase the ultimate higher voltage gain. The power switches S_1 and S_2 operate synchronously with same duty ratio which results in a simple control unit. At the first step, to avoid complexity of the theoretical analysis, following assumptions can be considered as:

- All power components used in the converter are totally assumed ideal. So, the efficiency is considered to be 100%.
- The input voltage is considered as an ideal DC source without fluctuations.

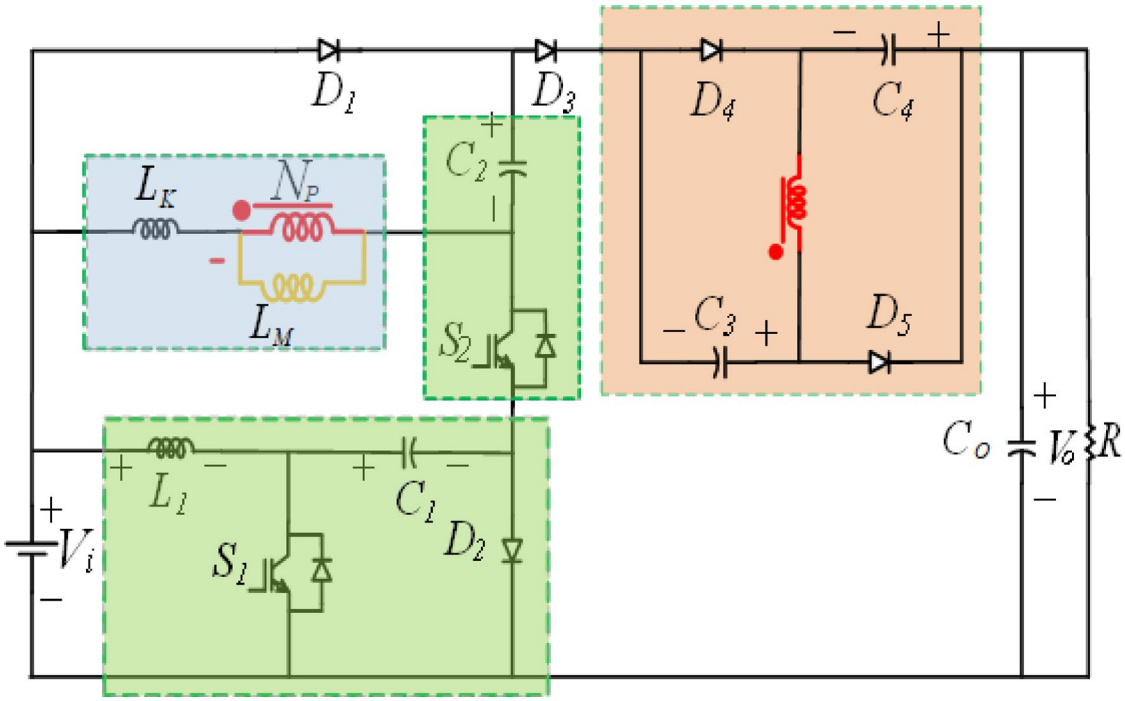

Fig. 1. The schematic of proposed structure.

- All capacitors and inductors are large enough with no fluctuations in the voltage of capacitors and the current inductors.
- In order to achieve an exact analysis, the CL is modelled and divided into three parts including a magnetizing inductor L_m, a leakage inductor L_k and finally the structure itself as an ideal transformer.
- Turns ratio of CL is $n = N_S/N_P$
- The coupling coefficient of the CL is k, which is obtained as: $k = \frac{Lm}{Lm+Lk}$

Principle of operation modes

The operation of the suggested structure is applied in one switching period (T_S). When the power switches are on-state, DT_S is considered first time interval and when are off-state, $(1\text{-}D)T_S$ is considered second time interval. Figure 2 shows all the equivalent sequences of the proposed topology in CCM (continuous conductance mode) operation.

Mode 1 $[t_0 \leq t \leq t_1]$

In this mode, the power switches S_1 and S_2 are in ON-state.

All the power diodes are in forward biased except D_2 and D_3. In the first step, the inductor L_1 is charged by the input voltage source. Simultaneously, the magnetizing inductor L_m, the leakage inductor L_k and capacitor C_2 are charged. In this interval, the current of both magnetizing inductor and also leakage inductor are linearly increased. Meanwhile, capacitors C_3 and C_4 are charged by the secondary winding of coupled inductor (N_S). During this mode, output load is being supplied by the capacitor C_O which has been charged in previous interval. In the beginning of this mode, the power diodes D_1, D_4 and D_5 are turned on with ZCS. Additionally, both switches are turned on under ZCS operation which is considered as soft switching. The following equations using KVL and KCL can be written for this mode as follows:

$$V_{Lm} = kV_1 \ (k \text{ is } coupling\ coefficient) \tag{1}$$

$$-V_i + VL1 = 0 \Rightarrow VL1 = V_i \tag{2}$$

$$V1 - VC1 - VL1 = 0 \tag{3}$$

$$V_{C2} - V_1 = 0 \ \Rightarrow V_{C2} = V_1 \tag{4}$$

$$V_{NS} = nkV_1 \tag{5}$$

$$V_{C3} = V_{C4} = nkV1 \tag{6}$$

$$V_{Co} = V_O \tag{7}$$

$$-i_{C1} = i_{in} - i_{L1} \Rightarrow \ i_{C1} = i_{L1} - i_{in} \tag{8}$$

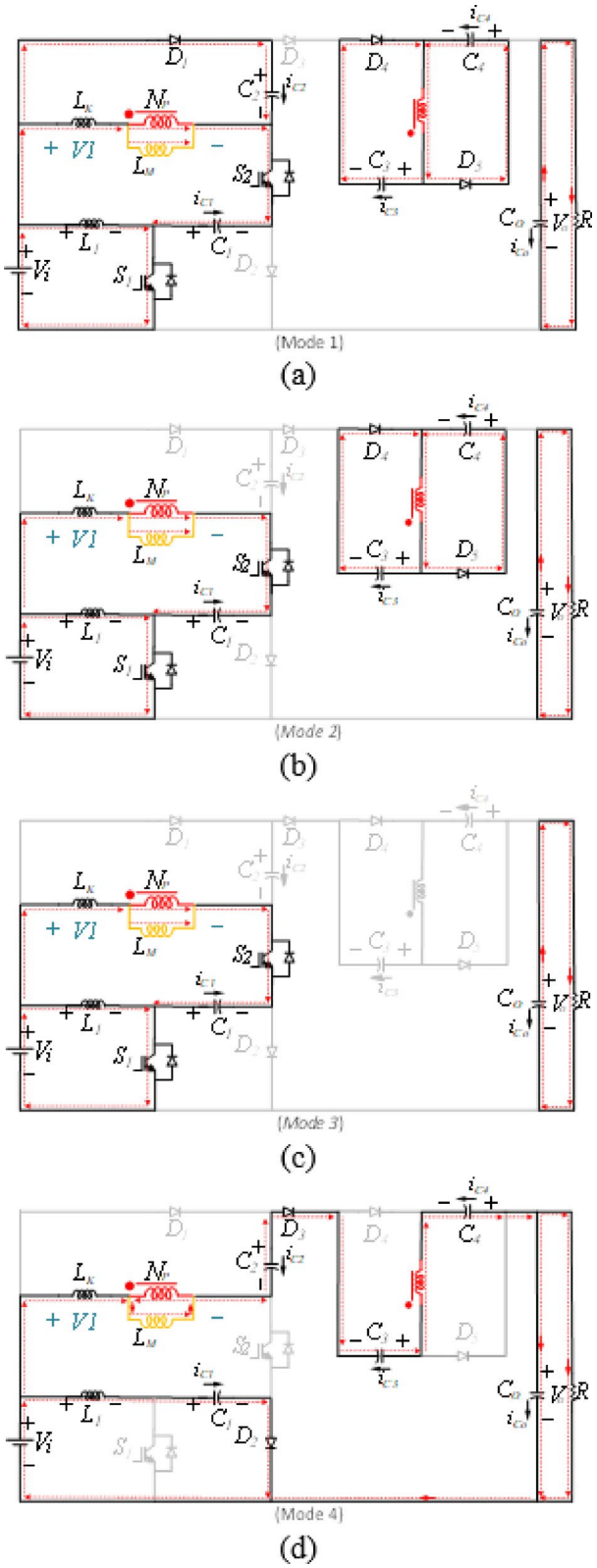

Fig. 2. The equivalent circuit of the proposed converter at CCM operation, (**a**) mode 1, (**b**) mode 2, (**c**) mode 3, (**d**) mode 4.

$$i_{Lk} = i_{Lm} + i_{N1} \tag{9}$$

$$i_{C2} = -i_{C1} - i_{Lk} \tag{10}$$

$$i_{in} = i_{L1} + i_{Lk} + i_{C2} \tag{11}$$

$$i_{C3} = i_{C4} = \frac{i_{N2}}{2} \tag{12}$$

$$i_{Co} = -I_O \tag{13}$$

Mode 2 [$t_1 \leq t \leq t_2$]
Due this mode, the power switches S_1 and S_2 are still in ON-state. The power diodes D_1, D_2 and D_3 are all in reversed biased while the other remained diodes, D_4 and D_5 are in forward biased. The capacitor C_1 discharges and releases its energy through S_1 into input source. The capacitor C_2 is open-circuited due to turned-off diodes D_1 and D_3. The capacitors C_3 and C_4 are charged by the secondary winding of coupled inductor. During this mode, output load is still being supplied by capacitor C_O. The following equations can be written for this mode as:

$$-V_i + VL1 = 0 \Rightarrow VL1 = V_i \tag{14}$$

$$VLK + VLm - VC1 - VL1 = 0 \tag{15}$$

$$V_{C3} = V_{NS} = nkV1 \tag{16}$$

$$V_{C4} = V_{NS} = nkV1 \tag{17}$$

$$V_{Co} = V_O \tag{18}$$

$$-i_{C1} = i_{in} - i_{L1} \Rightarrow \ i_{C1} = -i_{in} + i_{L1} \tag{19}$$

$$i_{Lk} = i_{Lm} + i_{Np} \tag{20}$$

$$i_{in} = i_{L1} + i_{Lk} \tag{21}$$

$$i_{C3} = i_{C4} = \frac{i_{NS}}{2} \tag{22}$$

$$i_{Co} = -I_O \tag{23}$$

Mode 3 [$t_2 \leq t \leq t_3$]
In this short interval, all the conditions are same as previous mode 2 except diodes D_4 and D_5 which are turned off under ZCS condition. Two power switches *S1* and *S2* are still in ON-state. Similarly to mode 2, the above equations are valid for this interval.

Mode 4 [$t_3 \leq t \leq t_4$]
In this mode, both S1 and S2 are turned OFF. All power diodes are in reverse biased condition except Diodes D_2 and D_3 which are in forward biased mode. The magnetizing inductor L_m and the leakage inductor L_k and all the capacitors C_2, C_3 and C_4 are being discharged into the output load R_L. Consequently, during this mode, the load is directly being supplied by the input source. At the end of this interval, due to the beginning of mode 1, the power diodes D_1, D_4 and D_5 will be turned on with ZCS. The following equations can be written:

$$-V_i + VL1 + VC1 = 0 \Rightarrow VL1 = V_i - VC1 \tag{24}$$

$$VLK + VLm = V1 \tag{25}$$

$$-V_i + V_1 - V_{C2} - V_{C3} + nkV_1 - V_{C4} + V_O = 0 \tag{26}$$

$$V_{Co} = V_O \tag{27}$$

$$V_{NS} = nkV_1 \tag{28}$$

$$i_{Lk} = -i_{C2} = -i_{C3} = -i_{C4} = i_{Co} + I_O \tag{29}$$

$$i_{in} = i_{L1} + i_{Lk} \tag{30}$$

$$i_{C1} = i_{L1} \tag{31}$$

$$i_{C1} = i_{in} - (i_{Co} + I_O) \tag{32}$$

Steady state analysis

By assuming that converter has reached its steady state, the volt second balance law for inductors can be used as follows:

$$\langle V_{L1} \rangle_{T_S} = 0 \tag{33}$$

$$\langle V_{Lm}\rangle_{T_S} = \langle V_{NP}\rangle_{T_S} = 0 \tag{34}$$

$$\langle V_{NS}\rangle_{T_S} = n\langle V_{Lm}\rangle_{T_S} = 0 \tag{35}$$

Substituting Eqs. (1)–(32) into Eqs. (33)–(35) the voltages of the capacitors in terms of duty cycle are calculated as follows:

$$V_{C1} = \frac{1}{1-D}V_i \tag{36}$$

$$V_{C2} = \frac{2-D}{1-D}V_i \tag{37}$$

$$V_{C3} = V_{C4} = \frac{nk(2-D)}{1-D}V_i \tag{38}$$

Based on Eqs. (36)–(38), the voltage gain of the proposed converter in CCM operation can be expressed by:

$$M = \frac{D^2\left[2n+2-k(n+1)\right] + D\left(2k+2nk-6n-5\right)+4n+3}{(1-D)^2} \tag{39}$$

By assumption the CL is ideal, the coupling coefficient can be considered as (k=1). Therefore, the ideal voltage gain relation of the proposed converter in can be expressed as follows:

$$M = \frac{V_{out}}{V_{in}} = \frac{D^2\left(n+1\right) - D\left(4n+3\right)+4n+3}{(1-D)^2} \tag{40}$$

Figure 3 illustrates the main waveforms of the proposed topology in one switching period.

Calculation the voltage/current stress across the power switch, the efficiency of proposed converter and capacitor/inductor design

The voltage stress across semiconductors

The voltage stress across the semiconductors can be obtained using the equivalent circuits when they are switched off or blocked. Hence, using the Eqs. (36)–(38), the voltage stress across the diodes can be expressed as below:

$$V_{D1} = \frac{D(2k-kD+D-3)+2}{D^2\left[2n+2-k(n+1)\right] + D\left(2k+2nk-6n-5\right)+4n+3} \times V_o \tag{41}$$

$$V_{D2} = V_{C1} = \frac{(1-D)}{D^2\left[2n+2-k(n+1)\right] + D\left(2k+2nk-6n-5\right)+4n+3} \times V_o \tag{42}$$

$$V_{D3} = \left(1 - \frac{nk(2-D)}{M(1-D)} - \frac{1}{M}\right) \times V_o \tag{43}$$

$$V_{D4} = V_{D5} = \frac{1}{M}\left(\frac{nk(2-D)}{(1-D)} - \frac{nkD(D-2)}{(1-D)^2}\right) \times V_o \tag{44}$$

Also, the per-unit (normalized) voltage stresses on power switches are calculates as follow:

$$\frac{V_{S1}}{V_o} = \frac{(1-D)}{D^2\left[2n+2-k(n+1)\right] + D\left(2k+2nk-6n-5\right)+4n+3} \tag{45}$$

$$\frac{V_{S2}}{V_o} = \frac{(1-D)^2 - kD(D-2)}{D^2\left[2n+2-k(n+1)\right] + D\left(2k+2nk-6n-5\right)+4n+3} \tag{46}$$

The current calculation and current stress across semiconductors

According to the capacitor charge balance (CCB) law, the average of a capacitor current in one switching period is zero.

Assuming the ideal condition due to zero power loss, the current gain relation can be obtained from Eqs. (39), (40). Considering CCB law, following averaged currents are obtained:

$$I_{Np} = nI_{Ns} = nI_o \tag{47}$$

$$P_{in} = P_{out} \;\Rightarrow\; \frac{I_i}{I_o} = \frac{V_{out}}{V_{in}} = M \;\Rightarrow\; I_i = MI_o \tag{48}$$

$$I_{L1,avg} = D \times \left(\frac{D^2\left[2n+2-k(n+1)\right] + D\left(2k+2nk-6n-5\right)+4n+3}{(1-D)^2}\right) I_{out} \tag{49}$$

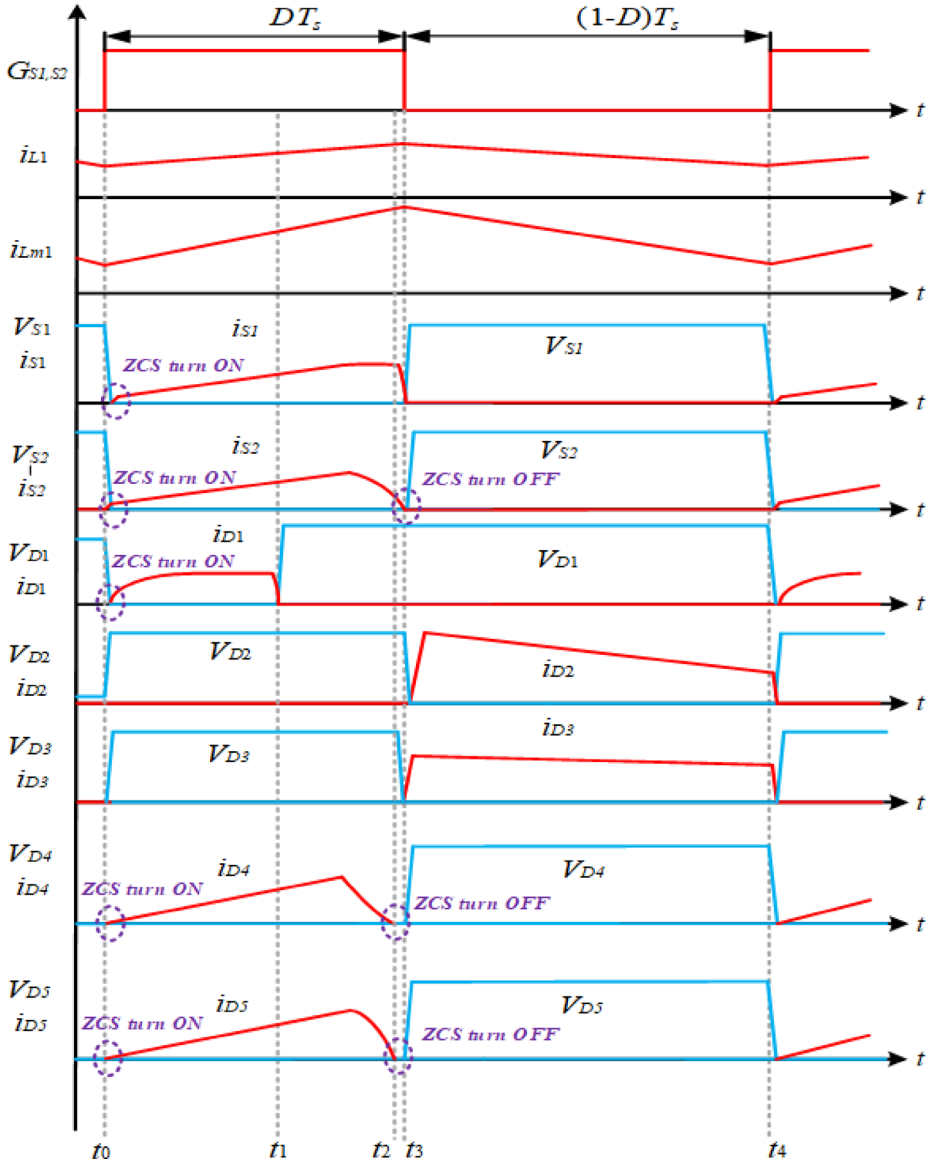

Fig. 3. The main waveforms of the proposed converter in CCM operation.

$$I_{Lm,avg} = \frac{D^2\left[2n+2-k(n+1)\right]+D\left(2k+2nk-5n-4\right)+3n+2}{(1-D)} I_o \tag{50}$$

$$I_{S1} = \frac{D^2\left[2n+2-k(n+1)\right]+D\left(2k+2nk-6n-5\right)+(4n+3)}{(1-D)^2} I_o \tag{51}$$

$$I_{S2} = \frac{D^2\left[2n+2-k(n+1)\right]+D\left(2k+2nk-6n-4\right)+4n+2}{(1-D)} I_o \tag{52}$$

Additionally, to calculate rms (root mean squared) currents of the both power switches over a conduction period, considering the averaged values in one period, the following equations are valid:

$$rms = \sqrt{\frac{1}{T_S}\int_0^{Ts}[I_S(t)]^2 dt} = \sqrt{\frac{1}{T_S}\int_0^{DTs}[I_{S,avg}]^2 dt} \tag{53}$$

$$I_{S1,rms} = \sqrt{D}\ M I_{out} \tag{54}$$

$$I_{S2,rms} = \sqrt{D}\ M I_{out}(1-D) \tag{55}$$

To estimate the rms current value of the inductor L_1 and and the magnetizing inductor L_m, the peak currents of both inductors are calculated by considering the half of the current ripple over a period which can be expressed as below:

$$I_{L1}{}^{peak} = I_{L1,avg} \pm \frac{V_{in}D}{2L_1 f_S} \tag{56}$$

$$I_{Lm}{}^{peak} = I_{Lm,avg} \pm \frac{V_{Lm}D}{2L_m f_S} \tag{57}$$

Considering the triangle waveform of the inductors current over one period according Fig. 3, from Eqs. (49), (50) and (56), (57), the rms current values can be calculated as follows:

$$I_{L1,rms} = \sqrt{\left(D \times \left(\frac{D^2\left[2n+2-k(n+1)\right]+D\left(2k+2nk-6n-5\right)+4n+3}{\left(1-D\right)^2}\right) I_{out}\right)^2 + \left(\frac{V_{in}D}{2\sqrt{3}L_1 f_S}\right)^2} \tag{58}$$

$$I_{Lm,rms} = \sqrt{\left(\frac{D^2\left[2n+2-k(n+1)\right]+D\left(2k+2nk-5n-4\right)+3n+2}{\left(1-D\right)} I_o\right)^2 + \left(\frac{V_{Lm}D}{2\sqrt{3}L_m f_S}\right)^2} \tag{59}$$

Calculation the efficiency of proposed converter

The following parameters are considered to calculate the efficiency ($\eta_{Converter}$) of the proposed converter:

- r_D: the internal resistors of diodes.
- r_S: the internal resistors of switches.
- r_{Lm}: the internal resistors of inductors.
- V_{FD}: the forward drop voltage of diodes.
- V_{FS}: the forward drop voltage of switches.

The overall efficiency is defined as follow:

$$\eta_{Converter} = \frac{P_o}{P_o + P_{losses}} \tag{60}$$

According to refs.[5,8], to accurately determine the total power loss, the losses of switches and diodes (which are calculated by sum of switching and conduction loss) can be obtained as follow:

$$P_{S,Tot} = P_{Cond,S_1} + P_{SW,S_1} + P_{Cond,S_2} + P_{SW,S_2} \tag{61}$$

$$\begin{aligned} P_{D,Tot} = {} & P_{Cond,D_1} + P_{Cond,D_2} + P_{Cond,D_3} + P_{Cond,D_4} + P_{Cond,D_5} \\ & + P_{SW,D_1} + P_{SW,D_2} + P_{SW,D_3} + P_{SW,D_4} + P_{SW,D_5} \end{aligned} \tag{62}$$

To calculate the conduction losses, the rms current values are expected as determined from (54–55)&(58–59). Assuming the turn ratio of CI as (n=1.5), the conduction and switching losses of the power switches are calculated as following, respectively:

$$\begin{aligned} & P_{Cond,S_1} = \frac{1}{T_s}\int_0^{DT_s} \left(V_{FS_1} I_{S_1}\right) dt + r_{S_1} I_{S_1,rms}^2 = \\ & D \times \left[0.6 \times \frac{D^2\left[2n+2-k(n+1)\right]+D\left(2k+2nk-6n-5\right)+\left(4n+3\right)}{\left(1-D\right)^2} I_o\right] + \left[r_{S_1} \times \left(\sqrt{D}\ M I_{out}\right)^2\right] = \\ & P_{Cond,S_1} = 2.335\text{W} \end{aligned} \tag{63}$$

$$P_{Cond,S_2} = 1.247\ W \tag{64}$$

$$P_{SW,S_1} = \frac{1}{2}\left(\frac{1}{T_s}\int_0^{t_{on}} (V_{S_1} I_{S1-(ON)})dt + \frac{1}{T_s}\int_0^{t_{off}} (V_{S_1} I_{S1-(ON)})dt = f_s V_{S_1} I_{S1-(ON)}(t_{on}+t_{off})\right) = 0.825\ W \tag{65}$$

$$P_{SW,S_2} = 0.821\ W \tag{66}$$

The conduction losses of power diodes are calculated as:

$$P_{Cond,D_1} = \frac{1}{T_s}\int_0^{(23/50)DT_s} V_{FD_1} I_{D_1,avg} + r_{D_1} I_{D_1,rms}^2 dt = 0.323\ W \tag{67}$$

$$P_{Cond,D_2} = 1.469\ W \tag{68}$$

$$P_{Cond,D_3} = 0.318\ W \tag{69}$$

$$P_{Cond,D_4} = 0.319\ W \tag{70}$$

$$P_{Cond,D_5} = 0.319\ W \tag{71}$$

The conduction loss of the both L_1 and L_m using Eqs. (58), (59) is obtained as:

$$P_{Cond,L1} = r_{L1}(I_{L1,rms})^2 = 0.438\ W \tag{72}$$

$$P_{Cond,Lm} = r_{Lm}(I_{Lm,rms})^2 = 0.494\ W \tag{73}$$

The core power loss formula related to inductor L_1 and CI is obtained as:

$$P_C = k f_s^{\alpha} B_m^{\beta} \tag{74}$$

The power loss (P_C) is determined in SI unit as W/kg. α, β and k are called Steinmetz parameters which usually provided by manufacturers for different core materials. Typical values of α can vary from 1 to 2 for ferrite materials ($1 \le \alpha \le 2$). According to, Faraday's Law, which is as follows:

$$V_L = N\frac{d\varphi(t)}{dt} = NA_c\frac{dB(t)}{dt} \tag{75}$$

The A_c parameter is the core area which has been presented by manufactures for different types of magnetic cores. N is the number of windings turn of inductor. Therefore, the peak flux density of ΔB for coupled inductor is expressed as:

$$\Delta B = \frac{1}{NA_c}\int_0^{DT_s} V_{core}dt = \frac{V_{core}DT_s}{N_pA_c} = \frac{V_{core}D}{N_pA_cf_s} \tag{76}$$

The core loss formula related to the inductor is equal to $P_{Core}=P_CM$, where M is mass of the core. By considering $B_m = \Delta B/2$, the core loss of coupled inductor is calculated as:

$$P_{Core} = k f_s^{\alpha}\left(\frac{V_{core}D}{2N_pA_cf_s}\right)^{\beta} M \tag{77}$$

Now, the core power losses can be simplified as follows:

$$P_{Core\_total} = P_{Core\_CI} + P_{Core\_L1} = k f_s^{\alpha} B_m^{\beta} M$$

$$= k f_s^{\alpha} M\left\{\left(\frac{V_{Lm}D}{2N_pA_cf_s}\right)^{\beta}\right\} + k f_s^{\alpha} M\left\{\left(\frac{V_{L1}D}{2N_pA_cf_s}\right)^{\beta}\right\} = 0.461 + 0.025 = 0.486\ W \tag{78}$$

Finally, the total power loss P_{Loss} is calculated as:

$$P_{Losses} = P_{S,Tot} + P_{D,Tot} + P_{Cond,Lm} + P_{Cond,L1} + P_{Core\_total} = 9.4\ W \tag{79}$$

The overall efficiency of the suggested converter is intended as follows:

$$\eta_{Converter} = \frac{P_o}{P_o + P_{losses}} \times 100\% = \frac{162}{162 + 9.4} \times 100\% = 94.51\% \tag{80}$$

According to (79–80), the graphs of the theoretical efficiency versus duty cycle and output power are depicted in (Figs. 4 and 5), respectively.

As shown in (Fig. 4), the efficiency of the proposed converter is plotted for both ($n=1.5$) and ($n=2$) turn ratios versus output power, simultaneously. The maximum efficiency is achieved for 150 W output power, furthermore, the proposed converter is obtained nearly more than 94% of efficiency for rated output power of 400 W. Figure 5 represents the efficiency of the proposed converter for a constant load ($R=800$ ohm) versus the wide change of duty cycles. As it illustrated in (Fig. 5), in the range of duty cycles from 0.25 to 0.65, the proposed converter is managed to operate 92 and 91% for $n=1.5$ and $n=2$, respectively. To observe the contribution of each element, the distribution of power losses is depicted in (Fig. 6). As shown, the contribution of power switches in total loss is the highest compared to the others, followed by the conduction loss of the power diodes. It is necessary to be mentioned that the power loss of switching devices is calculated without considering soft-switching performance in the proposed converter. Therefore, in the condition of considering the ZCS performance, the losses of the switches and the diodes are obviously reduced.

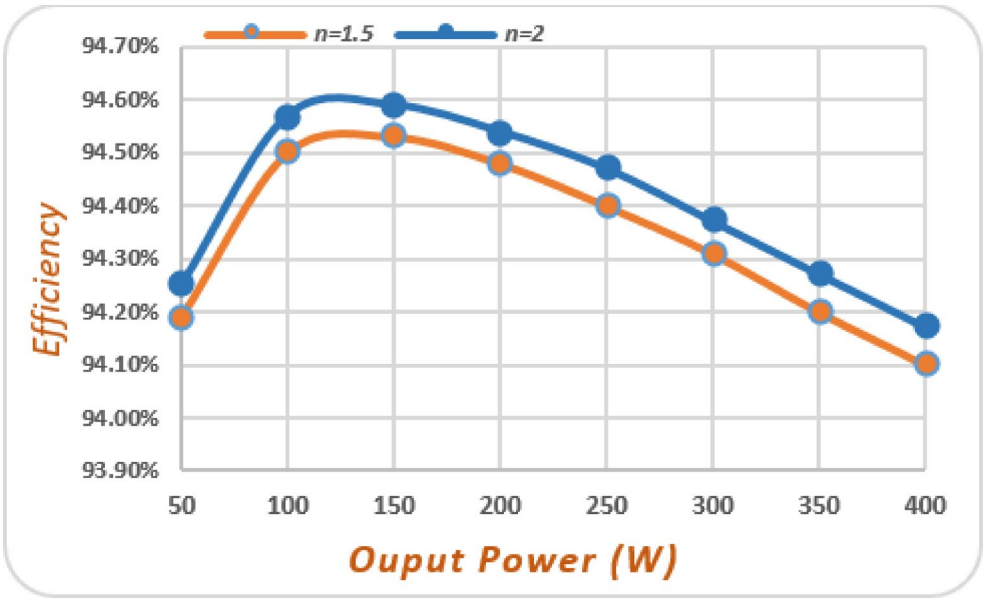

Fig. 4. Curve of the theoretical efficiency vs. (W).

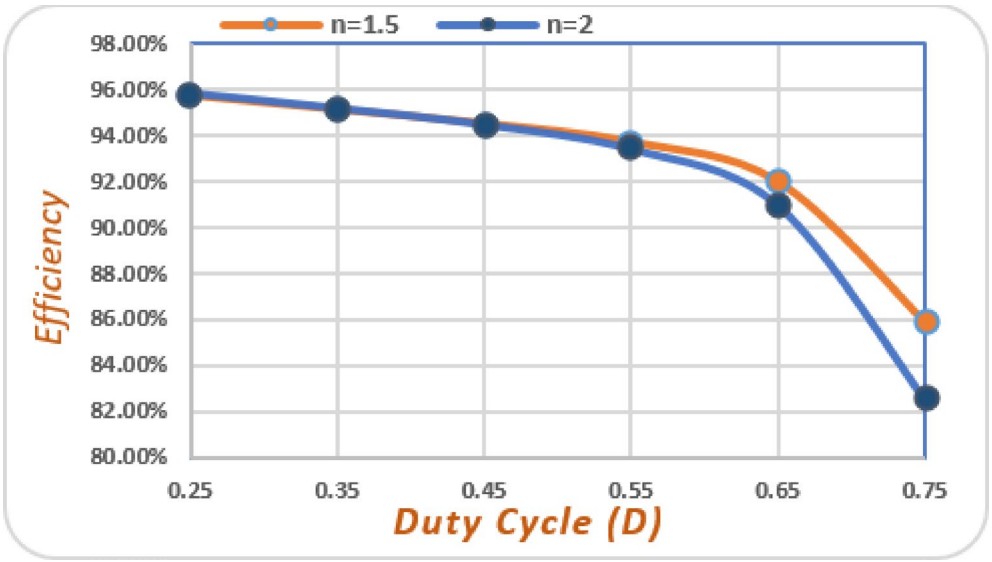

Fig. 5. Curve of the theoretical efficiency vs. (D).

Desired values of passive components

Capacitors design

The value of the capacitors mainly depends on the switching frequency, duty cycle, output current and permitted voltage ripple (x_C). Hence, for proper design, the desired values of capacitors are calculated according to Eqs. (36)–(38) as follows:

$$x_C\,(\%) = \frac{\Delta V}{V_C} \times 100 \tag{81}$$

$$C_1 \geq \frac{I_o M D (D-1)^2}{f_s \times V_i \times x_C\%} \tag{82}$$

$$C_2 \geq \frac{(1-D) I_o}{d_1 \times f_s (2-D) V_i \times x_C\%} \tag{83}$$

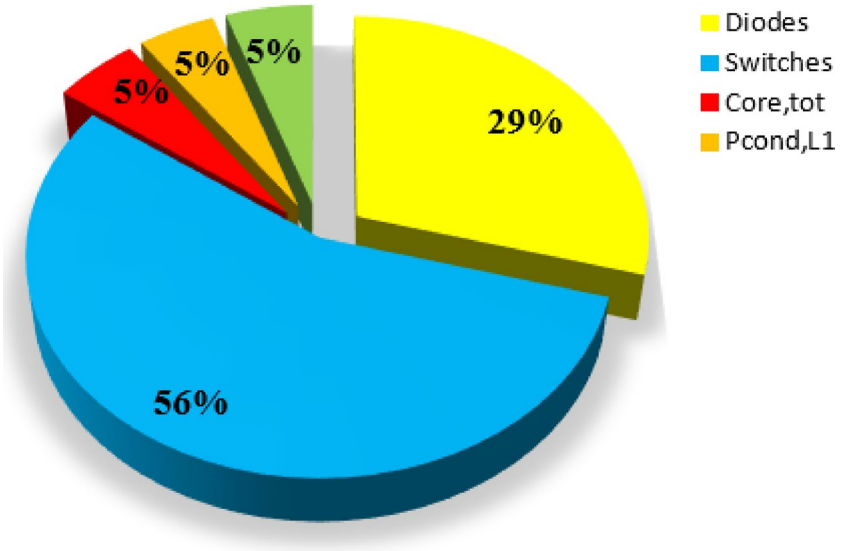

Fig. 6. Power loss distribution.

$$C_3 = C_4 \geq \frac{(1-D)I_o}{f_s(2-D)nkV_{in} \times x_C\%} \tag{84}$$

Inductor design
To determine the suitable value for L_1 in terms of inductor's desirable current ripple (x_L), following calculation is obtained:

$$x_L\,(\%) = \frac{\Delta I}{I_L} \times 100 \tag{85}$$

$$L_1 \geq \frac{R_L}{f_s \times M^2 \times x_{L\%}} \tag{86}$$

Calculation of CI specifications
The design procedure of the utilized CI is similar to the inductor design. Therefore, in order to obtain the minimum value of the magnetizing inductor in terms of desirable current ripple (x_{Lm}) and by using (50), following calculation is expressed:

$$x_{Lm}\,(\%) = \frac{\Delta I}{I_{Lm}} \times 100 \tag{86-1}$$

$$L_m \geq \frac{KD(2-D) \times R_L}{f_s \times M \times (D^2\,[2n+2-k(n+1)] + D\,(2k+2nk-5n-4)+3n+2) \times x_{L\%}} \tag{86-2}$$

As represented in Table 2, the obtained value of leakage inductor L_k is 3μH. The value of magnetizing inductor using coupling coefficient of CI is calculated as follows:

$$L_m = \frac{k \times L_k}{1-k} = \frac{3k \times 10^{-6}}{1-k} \tag{87}$$

The type of magnetic core used for the CI is E55/28/25. Hence, based on the dimensions presented in the core datasheet, the core air gap of the coupled inductor can be calculated as:

$$l_g = \frac{L_m {I_{Lm}}^2 \mu_0}{{B_m}^2 A_{Air\ \mathrm{Gap}}} = \frac{\frac{3k\times10^{-6}}{1-k} \times \left(\frac{D^2[2n+2-k(n+1)]+D(2k+2nk-5n-4)+3n+2}{(1-D)} I_o\right)^2 \times 4\pi \times 10^{-7}}{0.1^2 \times [(17.2+18.7) \times 25 \times 10^{-6}]} \tag{88}$$

As a result, the number of primary windings turns of the CI can be obtained by using the following equation:

$$N_p \geq \sqrt{L_m \times \frac{l_g}{\mu_0 A_{Air\ \mathrm{Gap}}^{Equivalent}}} \tag{89}$$

The turn's ratio of the CI is assumed as $n = N_s/N_p$. Likewise, the number of secondary windings turns of the CI can be calculated in terms of its turn ratio:

$$N_s = n \times N_p = \frac{3}{2} \times N_p \tag{90}$$

Review of stability and controller design

Dynamic model using the SSA method

To discuss reliability of the proposed converter, the major issue is the stability of the converter. A proper solution to model the system and achieve a suitable control method is the goal of this section. In Ref[29], the decoupling method is suggested for a MIMO DC-DC converter which appears a suit solution. However, as applied in[28], the pole-placement method for SISO (single-input single-output) systems due to flexibility and precise control is an appropriate solution. Hence, for the proposed converter the pole-placement method is applied. In single-input single-output converters, to provide an accurate output load power, it is necessary to have a suitable dynamic model of the system in order to design and implement an optimum control strategy. For this purpose, to form the dynamic equation systems, following assumptions are considered. All the power switches, the inductors, and the capacitors are assumed to be ideal. To provide more accuracy, for both leakage and magnetizing inductors, the parasitic series resistors r_{Ll} and r_{Lm} are considered. Moreover, parasitic series resistors of capacitors (ESR) are implemented as r_C. The effect of parallel capacitors with switching elements are neglected due to their very small values. Then, the average model and the small-signal model can be obtained by using the SSA method[28]. In this method, the system equations are achieved in all operating states, and averaged during one commutation period by taking into account the time interval of each state. The SSA equations of the proposed converter are obtained as follows:

$$\frac{dI_{L1}}{dt} = \frac{-r_{L1} + r_{C1}(D-1)}{L_1} I_{L1} + \frac{(D-1)}{L_1} V_{C1} + \frac{1}{L_1} V_{in} \tag{91}$$

$$\begin{cases} \frac{dI_{Lm}}{dt} = \frac{DKr_C}{L_m} I_{L1} + D\left[\frac{-Kr_{Lm}}{L_m} - \frac{K}{L_m(nK+1)} \times \frac{(-r_{Lm}(n+1) - 3r_C)}{n+1}\right] + \frac{K}{L_m(nK+1)} \times \frac{(-r_{Lm}(n+1) - 3r_C)}{n+1} I_{Lm} \\ + \frac{KD}{L_m} V_{C1} + \left(\frac{-KD}{L_m(nK+1)} + \frac{K}{L_m(nK+1)}\right) V_{C2} + \left(\frac{-KD}{L_m(nK+1)} + \frac{K}{L_m(nK+1)}\right) V_{C3} + \left(\frac{-KD}{L_m(nK+1)} + \frac{K}{L_m(nK+1)}\right) V_{C4} \\ + \left(D\left[\frac{-KMr_C}{L_m R_{Load}} + \frac{K}{L_m(nK+1)}\right] - \frac{K}{L_m(nK+1)}\right) V_{Cout} + \frac{nK^2D + K}{L_m(nK+1)} V_{in} \end{cases} \tag{92}$$

$$\begin{aligned} \frac{dV_{C1}}{dt} = &\left(D\left[\frac{-0.46}{2C_1} + \frac{0.54}{C_1} + \frac{1}{C_1(n+1)}\right] - \frac{1}{C_1(n+1)}\right) I_{Lm} - \frac{0.46\mathrm{D}}{2r_C C_1} V_{C1} + D\left[0.46\left(\frac{1-2n^2K}{2r_C C_1}\right) + 0.54\frac{-2n^2K}{r_C C_1}\right] V_{C2} \\ &+ \left[\frac{0.46nD}{2r_C C_1} + \frac{0.54nD}{r_C C_1}\right](V_{C3} + V_{C4}) + \frac{M(1-D)}{C_1 R_{Load}} V_{Cout} - \frac{0.46\mathrm{D}}{r_C C_1} V_{in} \end{aligned} \tag{93}$$

$$\begin{aligned} \frac{dV_{C2}}{dt} = &\left(D\left[\frac{-0.46}{2C_2} + \frac{1}{C_2(n+1)}\right] - \frac{1}{C_2(n+1)}\right) I_{Lm} + \frac{0.46\mathrm{D}}{2r_C C_2} V_{C1} + \frac{0.46\mathrm{D}(-1-2n^2K)}{2r_C C_2} V_{C2} \\ &+ \frac{0.46nD}{2C_2 r_C}(V_{C3} + V_{C4}) + \frac{M(D-1)}{C_2 R_{Load}} V_{Cout} + \frac{0.46\mathrm{D}}{2C_2 r_C} V_{in} \end{aligned} \tag{94}$$

$$\frac{dV_{C3}}{dt} = \frac{D-1}{C_3(n+1)} I_{Lm} + \frac{nDk}{r_C C_3} V_{C2} - \frac{D}{r_C C_3} V_{C3} + \frac{M(D-1)}{C_3 R_{Load}} V_{Cout} \tag{95}$$

$$\frac{dV_{C4}}{dt} = \frac{D-1}{C_4(n+1)} I_{Lm} + \frac{nDk}{r_C C_4} V_{C2} - \frac{D}{r_C C_4} V_{C4} + \frac{M(D-1)}{C_4 R_{Load}} V_{Cout} \tag{96}$$

$$\frac{dV_{Cout}}{dt} = \frac{1-D}{C_{out}(n+1)} I_{Lm} - \frac{D}{C_{out} R_{Load}} V_{Cout} \tag{97}$$

The SSA method is considered to provide the small signal model which is required to design a closed loop controller for the proposed topology. Therefore, the state variables and the control inputs which are consisted of two fixed parts $(\bar{X}, \bar{D})$ and small variables of the states $(\tilde{x}, \tilde{d})$ parts, are described as:

$$\begin{cases} X = \bar{X} + \tilde{x} \\ D = \bar{D} + \tilde{d} \end{cases} \tag{98}$$

Afterward, by implementing the SSA model and neglecting the second order values, the small signal model is obtained as:

$$\begin{cases} \dot{\tilde{x}} = A\tilde{x} + B\tilde{u} \\ y = C\tilde{x} + D\tilde{u} \end{cases} \tag{99}$$

The variable states ($\tilde{x}$), control input ($\tilde{u}$), and the output signals (y) are determined as below:

$$\tilde{x}^T = \begin{bmatrix} \tilde{i}_{L1} & \tilde{i}_{Lm} & \tilde{v}_{C1} & \tilde{v}_{C2} & \tilde{v}_{C3,4} & \tilde{v}_{Cout} \end{bmatrix} \tag{100}$$

$$\tilde{u} = \begin{bmatrix} \tilde{d} \end{bmatrix} \tag{101}$$

$$y^T = \begin{bmatrix} I_{L1} & I_{Lm} & 0 & 0 & 0 & V_{Cout} \end{bmatrix} \tag{102}$$

The pole-placement method implementation

It is important to clarify that both C_3 and C_4 capacitors which embedded in VM cell, form a capacitor loop due to the same values and the schematic of the proposed converter where depicted in (Fig. 2). Consequently, as calculated in (95) and (96), the state equations of both C_3 and C_4 are equal which leads to the reduction of one state. According to pole-placement method, poles of a closed-loop system can be located at any desired location, provided that the mentioned system has been assumed completely state-controllable. The controllability matrix of the suggested converter can be written in the following form:

$$\Phi_C = \left[B \vdots AB \vdots A^2B \vdots \cdots \vdots A^{n-1}B \right] \tag{103}$$

For this system, if rank(Φ_C) = n = 6 (rank of Φ_C equals to number of variable states ($\tilde{x}$)), the system would be completely state-controllable. Next, two further integral states are obtained as follows:

$$\begin{cases} \dot{q}_1(t) = r_1(t) - y_1(t) = r_1(t) - \tilde{i}_{L1}(t) \\ \dot{q}_2(t) = r_2(t) - y_2(t) = r_2(t) - \tilde{i}_{Lm}(t) \\ \dot{q}_3(t) = r_3(t) - y_3(t) = r_3(t) - \tilde{v}_{Cout}(t) \end{cases} \tag{104}$$

The Eq. (104) can be re-written as follows:

$$\begin{cases} \dot{q}_1(t) = I_{L1,ref} - I_{L1}(t) \\ \dot{q}_2(t) = I_{Lm,ref} - I_{Lm}(t) \\ \dot{q}_3(t) = V_{Cout,ref} - V_{Cout}(t) \end{cases} \tag{105}$$

Subsequently, the new integral states, the state and output equations can be expressed as:

$$\begin{aligned} \begin{bmatrix} \dot{\tilde{x}}(t) \\ \cdots \\ \dot{q}(t) \end{bmatrix} &= \begin{bmatrix} A & \vdots & 0 \\ \cdots & \vdots & \cdots \\ -C & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} + \begin{bmatrix} B \\ \cdots \\ 0 \end{bmatrix} \tilde{u}(t) + \begin{bmatrix} 0 \\ \cdots \\ I \end{bmatrix} r(t) \\ y(t) &= \begin{bmatrix} C & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} \end{aligned} \tag{106}$$

In (106), $r(t)$ is the input reference vector which is determined as:

$$r(t) = \begin{bmatrix} I_{L1,ref} & I_{Lm,ref} & V_{C1,ref} & V_{C2,ref} & V_{C3,4,ref} & V_{Co,ref} \end{bmatrix}^T \tag{107}$$

Considering (106), the new matrices $\bar{A}$ and $\bar{B}$ are defined as:

$$\bar{A} = \begin{bmatrix} A & \vdots & 0 \\ \cdots & \vdots & \cdots \\ -C & \vdots & 0 \end{bmatrix}, \bar{B} = \begin{bmatrix} B \\ \cdots \\ 0 \end{bmatrix} \tag{108}$$

The controllability matrix for the system ($\bar{\Phi}_C$) in (106) can be arranged as:

$$\bar{\Phi}_C = \begin{bmatrix} B & \vdots & A\Phi_C \\ \cdots & \vdots & \cdots \\ 0 & \vdots & -C\Phi_C \end{bmatrix} = \underbrace{\begin{bmatrix} B & \vdots & A \\ \cdots & \vdots & \cdots \\ 0 & \vdots & -C \end{bmatrix}}_{M} \begin{bmatrix} I & \vdots & 0 \\ \cdots & \vdots & \cdots \\ 0 & \vdots & \Phi_C \end{bmatrix} \tag{109}$$

Considering Φ_C is complete-rank, the system defined in (106) would be completely state-controllable under the condition that the rank of the matrix M is $n+m$ (n and m are the number of the variable states ($\tilde{x}$) and output signals (y), respectively. Using the code in MATLAB to place the eigenvalues by entering the matrices and determining the location of the eigenvalues of the closed loop as follows:

$$\begin{aligned} \mathrm{K} = [\mathrm{K_x},\ \mathrm{K_q}] &= \text{place}\ \left(\hat{A}', \hat{B}', \hat{\lambda}\right) \\ \mathrm{K} = [\mathrm{K_x},\ \mathrm{K_q}] &= \text{place}\ \left(\hat{A}\right) \end{aligned} \tag{110}$$

Consequently, the control coefficients matrices K_x and K_q can be obtained. It should be mentioned that since the type of the designed control system is one (due to presence of an integrator), it tracks the input references $I_{L1,ref}$ and $I_{Lm,ref}$ without steady-state error by the poles which have been assigned by the matrices K_x and K_q at the desired places. Therefore, there is a matrix K which satisfies the following equation:

$$\tilde{u}(t) = -K \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} = -\begin{bmatrix} K_x & \vdots & K_q \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} \tag{111}$$

Substituting (111) in (106) the following equation can be written as:

$$\begin{bmatrix} \dot{\tilde{x}}(t) \\ \cdots \\ \dot{q}(t) \end{bmatrix} = \begin{bmatrix} A - BK_x & \vdots & -BK_q \\ \cdots & \vdots & \cdots \\ -C & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} + \begin{bmatrix} 0 \\ \cdots \\ I \end{bmatrix} r(t)\ ,\ y(t) = \begin{bmatrix} C & \vdots & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ \cdots \\ q(t) \end{bmatrix} \tag{112}$$

Eventually, the point is to find the control signal $\tilde{u}(t)$using state feedback gain matrix K, so that the closed-loop system eigenvalues are placed at the desired locations. There are some practical methods to establish the system controller matrix K=[K_x, K_q]. The control systems toolbox of the MATLAB software provides a useful pole-placement function, which inputs the system (106) and the desired eigenvalues locations to find the state feedback gain matrices. Ultimately, using the trial & error method, the desired values for gain margin and phase margin (GM ≥ 10 and 60 ≤ PM ≤ 80) are ascertained and determined. The result is depicted in (Fig. 7a), which represents the bode diagram of the control system. As shown in Fig. 7a, the value of gain margin for the magnetizing inductor L_m is limitless (inf) and greater than 10, also, the phase margin (closed loop) path is 70 (deg) which is greater than 60. Therefore, both values are within the allowed range.

The block diagram of the closed-loop control is depicted in Fig. 7b which has been implemented for the proposed converter.

Comparison study

In this section, to discuss the advantages and disadvantages of the proposed converter, it is compared to some other similar structures presented in[1–4,6–8,10,15,16,18,20,30]. All the converters are consisted of at least one coupled inductor and also the selected topologies are similar to the proposed converter. Table 1 covers the detailed information of all selected converters including the number of components, voltage gain versus duty cycle, normalized voltage stress of switches, maximum voltage stress of diodes, maximum efficiency and input current ripple respectively. The comparison results are shown in Fig. 8 in terms of all structures features.

In order to obtain a strict result of the comparison, turns ratio of the implemented CI in the proposed structure is considered once as (n = 2) and again as (n = 1.5) while all other structures are kept with a constant turns ratio of (n = 2). This would be a fair comparison to evaluate the proposed converter capability under a same condition and also with less turn ratio of the CI compared to the others.

1) As depicted in Fig. 8a, the voltage gain of the proposed converter with (n = 2) is explicitly higher than all other structures. Although, the voltage gain obtained by[1,7] is obviously higher for the range $D \geq 0.5$ and $D \geq 0.7$, respectively. However, due to higher values of duty cycles, the conduction losses are increased extremely which leads to lower efficiency. Considering (n = 1.5) for the proposed converter as shown in Fig. 8a simultaneously, it still provides a reasonable higher voltage gain compared to the other structures listed in (Table 1). In this case, for $D \leq 0.7$, the voltage gain obtained by the proposed converter is higher than converters presented in refs[2,3,6,7,10,15,18,20,30]. In the range of $D \geq 0.7$, only two converters presented in[7,20] acquire higher voltage gain with a slight difference. The converter presented in[4] achieves a better performance of voltage gain due to duty cycles higher than 50%. However, its optimal operating point to obtain the maximum efficiency is calculated under D = 0.43 condition which clearly acquires literally same result of voltage gain compared to the proposed structure. In total, the suggested topology exhibits a

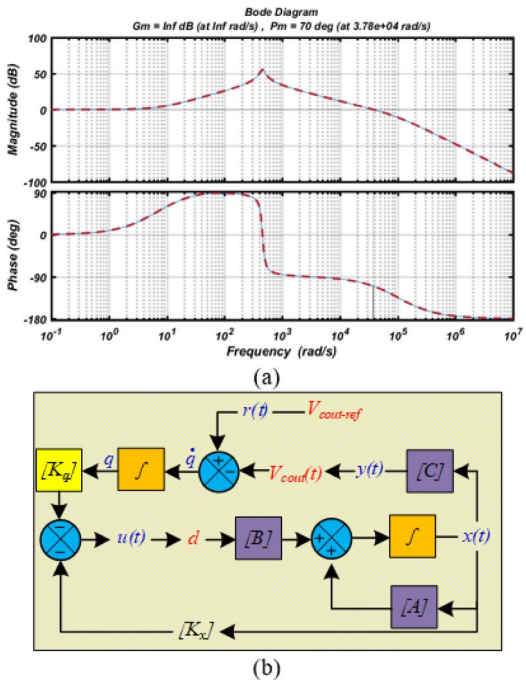

Fig. 7. Bode diagram and closed loop control of the proposed converter, (**a**) Bode diagrams for the transfer functions of the inductor currents, (**b**) Closed-loop control of the suggested topology.

robust performance even due to wide changes of duty cycle rate specifically at lower duty cycles rate which provides less conduction loss in order to obtain better performance and maximum efficiency.

As represented in Table 1; Fig. 8, the proposed converter provides following advantages:

2) As shown in Fig. 8b, the normalized voltage stress curves of the power switches versus duty cycle are presented. The voltage stress of power switches in refs[2,6,15,30]. is obviously severe compared to other topologies which is considered as a major drawback. As an advantage, the voltage stress across the switch (*S1*) of the proposed converter along the converters presented in[4,8,16,18] obtain the lowest values. Additionally, in the previously mentioned converters, the changes in the voltage stress rate are relatively constant in term of the duty cycle increment, however, for the switch (*S*1) of the proposed converter, the slope of the stress curve is reduced due to higher values of duty cycles that is considered as another advantage. In the range of ($D \geq 0.5$), the switch (*S*1) obtains the lowest voltage stress compared to all other converters. As illustrated in Fig. 8b, in the range of ($D \leq 0.55$), the voltage stress of (*S2*) in the proposed converter compared to[1–3,6,7,10,15,30] acquires the lowest values. Although, considering to the range ($D \geq 0.7$), the voltage stress of power switch (*S*2) increases slightly which leads to pass[7,10,20].

3) In Fig. 8c, the normalized voltage stress of power diodes is plotted. Refs[3,8,16,18]. obtain the lowest values. The maximum voltage stress of diodes in the load side of the proposed converter is applied to power diodes (*D*4 & *D*5). In comparison with[1,2,4,6,7,10,15,20,30], the proposed converter obtains the lowest values as an advantage. Moreover, the constant slope of the voltage stress for the proposed converter is considered as another advantage due to higher duty ratios. The voltage stress of power diodes of converters presented in[2,15,30] obtain the highest values compared to others which is considered as a drawback. Finally, the approximate stability of voltage stress values for power diodes in a wide range of different duty cycles is another advantage for the suggested converter.

Another comparison is illustrated in Fig. 9, which represents the normalized RMS current flowing through the switching devices at a given voltage gain of the proposed converter. The converters in[10,15,20] are selected to be compared due to their topology similarity. The converter in[20] has the most similar structure along the equal number of components to the proposed converter compared to[10,15]. Regarding to Fig. 9, in the entire range of voltage gain, the switch *S*1 of[20] tolerates the highest current stress compared to other converters.

Additionally, the current stress for power switches S2 from[20] and S1 from proposed converter has lower values and almost similar to each other. The current stress value for S1 of the proposed converter ranks third after[15,20] in the voltage range lower than 20, meanwhile for gain values greater than 20, switch *S*1 of the proposed converter retains the second place after[20]. However, by inspecting Fig. 8a, the proposed converter has the greater voltage gain value in the whole range of duty cycles compared to[15,20] which considered as an advantage. The both power switches used in the converter[10] are obtained the lowest current stress compared to all others. Nevertheless, by inspecting Fig. 8a, the proposed converter along the converters in[15,20] are obtained higher gain values compared

Converter	Number of S	D	C	L	CI	T	Voltage gain	Normalized Voltage Stress of Switches (V_S/V_O)	Normalized Voltage Stress of Diodes (V_D/V_O)	Max Eff. (%)	CG	SS	Input CR
[1]	1	5	5	1	1	13	$\frac{n(3D+2)+(2-D)}{2(1-D)^2}$	$\frac{2+D(n-1)}{n(3D+2)+(2-D)}$	$\frac{2n}{n(3D+2)+(2-D)}$	92.96	✓	×D ×S	Low
[2]	1	4	2	1	1	9	$\frac{1+nD}{(1-D)^2}$	$\frac{1}{1+nD}$	$\frac{(2-D+nD)}{1+nD}$	88.11	✓	×D ×S	–
[3]	1	3	4	1	1	10	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	$\frac{1}{1+n}$	95.01	✓	✓D ×S	Low
[4]	2	5	5	1	1	14	$\frac{2+2n+nD(1-D)}{(1-D)^2}$	$\frac{1}{2+2n+nD(1-D)}$	$\frac{(1+2n-nD)}{2+2n+nD(1-D)}$	94.2	✓	×D ×S	Low
[5]	1	7	5	1	1	15	$\frac{1+n}{(1-D)^2}$	$\frac{1}{2}$	$\frac{1+nD}{(n+1)}$	–	✓	×D ×S	Low
[6]	1	5	4	1	1	12	$\frac{n+2}{(1-D)^2}$	$\frac{1}{n+2}$	$\frac{1+n}{2+n}$	≤89	✓	×D ×S	Low
[8]	2	8	8	0	2	20	$\frac{5-2nD+4n-D}{(1-D)}$	$\frac{1}{(5-n_1D+2n_1-D-n_2D+2n_2)}$	$\frac{1+n}{(5-n_1D+2n_1-D-n_2D+2n_2)}$	94.6	×	✓D ×S	Low
[10]	4	2	4	2	1	13	$\frac{2(n+2)}{(1-D)}$	$\frac{1}{2(n+2)}$	$\frac{n+1}{(n+2)}$	94.4	✓	✓D ✓S	Low
[15]	2	4	4	1	1	12	$\frac{1+D+2n(1-D)}{(1-D)^2}$	$\frac{(1+D)}{1+D+2n(1-D)}$	$\frac{2n}{1+D+2n(1-D)}$	96.1	✓	✓D ✓S	Low
[18]	3	5	4	0	2	14	$\frac{2n+2}{1-D}$	$\frac{1}{2n+2}$	$\frac{2}{2n+2}$	96	×	✓D ✓S	Low
[20]	1	5	4	0	2	12	$\frac{n(D-D^2)+nD+1}{(1-D)^2}$	$\frac{1}{n(D-D^2)+nD+1}$	$\frac{n}{n(D-D^2)+nD+1}$	90.5	✓	×D ×S	High >80%
[24]	1	8	8	0	1	18	$\frac{4+n(2-D)-D}{1-D}$	$\frac{1}{4+n(2-D)-D}$	$\frac{n(2-D)-D}{4+n(2-D)-D}$	92.7	✓	×D ×S	Med 55%
[26]	2	5	5	1	1	14	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{1}{3+2n-D(3+n-D)}$	$\frac{n(2-D)}{3+2n-D(3+n-D)}$	≤94	✓	×D ×S	High >80%
Prop.	2	5	5	1	1	14	$\frac{D^2(n+1)-D(4n+3)+4n+3}{(1-D)^2}$	$S_1: \frac{(1-D)}{D^2[2n+2-k(n+1)]+D(2k+2nk-6n-5)+4n+3}$ $S_2: \frac{(1-D)^2-kD(D-2)}{D^2[2n+2-k(n+1)]+D(2k+2nk-6n-5)+4n+3}$	$\frac{nD-n^2D+2n^2-2n}{M(1-D)(n-nD+D-1)}$	94.51	✓	✓D ✓S	Med 50%

Table 1. Comparison between the proposed converter and other topologies. (S, D, C, L, CI, T, indicate the number of switches, diodes, capacitors, inductors, coupled inductors and total components respectively). *Eff* efficiency, *CG* common ground, × = No, ✓ = Yes, *SS* soft switching on semiconductors (D: diodes, S: switches), *CR* current ripple, Low = less than 30%.

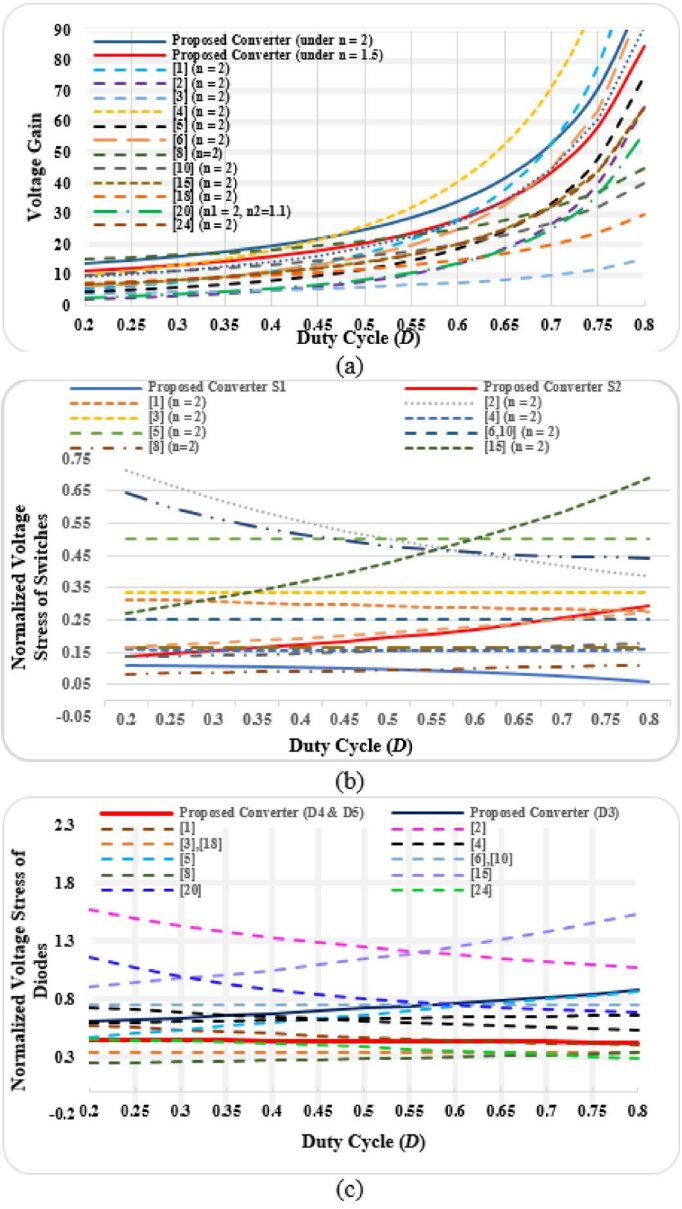

Fig. 8. Comparison between the proposed converter and other structures. (**a**) Voltage gain versus duty-cycle, (**b**) Normalized voltage stress across power switches versus duty-cycle, (**c**) Normalized voltage stress across power diodes versus duty-cycle.

to[10], prospectively. As it shown in Fig. 9, the rms current across all power diodes of the proposed converter are plotted. In comparison with all power diodes implemented in the proposed converter, $D2$ reaches slightly higher values compared to the rest. The power diode $D1$ used in[10] has the lowest value along $D1$, $D3$, $D4$ and $D5$ of the proposed converter which all are nearly equal. However, power diode $D1$ used in[15] has reached the highest current stress compared to all other structures as a major disadvantage.

The input current ripple comparison is presented in the last column on the (Table 1). As it shown, regarding to the simulator results and also as illustrated in the experimental section Fig. 11j, the input current ripple of the proposed converter is obtained in medium range compared with other structures in this section. The observed input current ripple range for Refs[1,3,4,6–8,10,15,16]. are considered as low ripple while high ripple range is obtained for refs.[20,30].

Experimental results

To investigate the functionality of the proposed topology and evaluate its actual performance, a prototype is built and tested in laboratory. The prototype is tested with input voltage of 20 V under rated power of 150 W. All the characteristics of the prototype converter are given in Table 2 including the selected type of the MOSFET switches, the power diodes, the capacitors and designed values for the inductor and turn ratio of the CI. As depicted in (Fig. 10k), the output voltage is measured about 345 V.

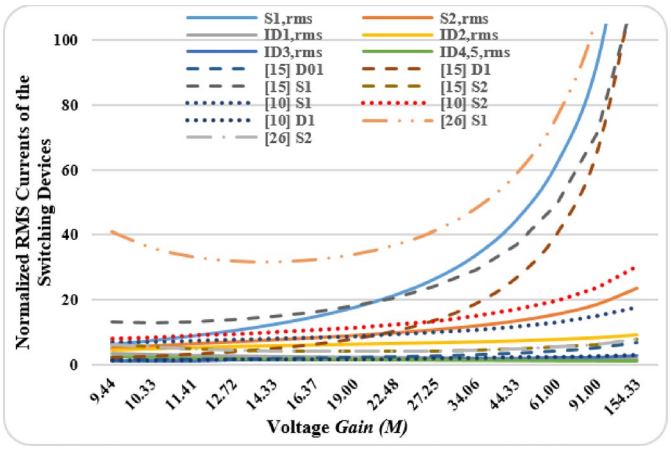

Fig. 9. Comparison between the normalized rms currents of switching elements versus the voltage gain.

Components	Parameters
Input voltage	20 V
Output voltage	345 V
Rated power	150 W
Switching frequency	50 kHz
Duty cycle	0.45
Power switches	S1: IRFP260NPBF S2: IRFP460PBF
Power didoes	MUR1560G
Magnetizing inductor L_m	500μH, EE55/28/25
Leakage inductor L_{k1} & L_{k11}	3μH
Turns ratio of the coupled-inductor n_1	1.5
Inductor L_1	300 μH
Capacitors C1	330 μF
Capacitors C_2	330 μF
Capacitors C_3	330 μF
Capacitors C_4	330 μF
Capacitor C_o	470 μF
R_{out}	800 Ω

Table 2. Characteristics of the power components.

Considering the actual losses, the obtained voltage value is almost close to the theoretical analysis based on Eq. (39), which is calculated by substituting the parameters determined in Table 2 and estimated output voltage of 358 V. The voltage value of the capacitor C_1 is about 36 V as illustrated in (Fig. 10b). The Fig. 10c shows the voltage of capacitor C_2 which is about 53 V. As shown in Fig. 10d, the voltage values of the both capacitors C_3 and C_4 are measured 78 V which are identical due to the loop law for capacitors. The observed all values are nearly close to the calculated equations from (36) to (38). By replacing the parameters from Table 2, the estimated voltages are 36.3, 56.36 and 84 V respectively.

As depicted in (Fig. 11a, d), the power diodes D_1 and D_4 are turned on under ZCS condition, the power diode D_4 is turned off under pseudo ZCS condition, furthermore, the power diode D_5 is turned off under ZCS condition. The soft-switching capability is in compliance with (Fig. 3). Additionally, as shown in (Fig. 11a–f), the voltage stresses of the diodes D_1, D_2, D_3, D_4 and D_5 are measured 99, 34.3, 245, 140 and 140 V, respectively. The measured voltages are almost in accordance with Eqs. (41–44), which utilizing the parameters given in Table 2, the estimated values for D_1, D_2, D_3, D_4 and D_5 are 102.2, 36.36, 256, 150.8 and 150.8 respectively. As illustrated in (Fig. 11f, g) the voltage stress of S_1 and S_2 is measured 35 V and 64 V, correspondingly. The observed values are almost match with Eqs. (45), (46) where using the parameters presented in Table 2, the theoretical values for S_1 and S_2 are estimated to be 36.36 V and 65.84 V, respectively. Furthermore, the current/voltage waveforms of the power switches are illustrated in (Fig. 11f, g) where both S_1 and S_2 are turned on under ZCS condition. The soft-switching performance of S_1 and S_2 are in accordance with (Fig. 3). In Fig. 11h, i, the current waveforms of the leakage inductor L_k and inductor L_l are shown. As shown in Fig. 11i, considering ripple current of the inductor L_1 which is less than 20%, the designed value of 300 μH for L_1 seems appropriate. Additionally, as depicted in

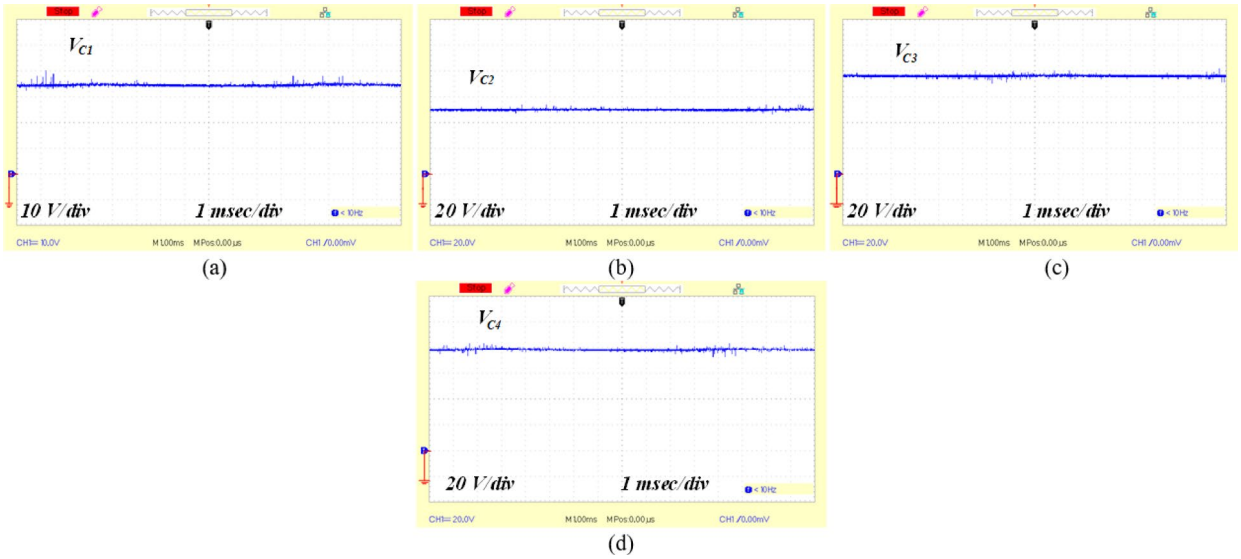

Fig. 10. The voltage waveforms of the capacitors, (**a**) C_1, (**b**) C_2, (**c**) C_3, (**d**) C_4.

(Fig. 11j), the continuous waveform of the input current is clearly observed which proves the theoretical analysis. The output voltage/current waveforms are shown in (Fig. 11k). As illustrated, the prototype operates under 150 W full load in steady state where output current and voltage results are obtained. By inspecting Fig. 11k, the obtained output voltage is estimated 345 V which represents actual value for voltage gain about 17.25 under 0.45 of duty cycle. The dynamic response of a DC-DC converter is a predominant factor to determine the stability and reliability of its performance. As shown in Fig. 12, the dynamic response of the proposed converter during a sudden change in load is illustrated. In Fig. 12a, the output power immediately drops from 246.24 to 136.8 W, which means a 55% reduction in power load. Next, as shown in Fig. 10b, the output power is increased 55% again. In both cases, the output voltage change is very small in the manner that capable to be stabilized in fewer than 300 milliseconds which means a robust performance of the proposed converter.

The acquired experimental efficiency under the rated power of 150 W is obtained 93%. In the comparison of theoretical approximation which is calculated 94.51% based on Eq. (80), represents a reasonable performance of the proposed converter.

Eventually, by investigating the entire experimental results, the theoretical analysis of the proposed converter has a good accordance with actual lab results.

Conclusions

An ultra-high step-up DC/DC converter inspired from QBC topology consisted of a non-isolated coupled inductor alongside a voltage multiplier cell is suggested. The proposed structure is equipped with three main boost stages which utilized with two simultaneous power switches to achieve high voltage gain with simple control capability. An input inductor is embedded in the primary winding side of CI along with two other boost stage cells, afterward the third boost stage as VM cell is placed in the secondary winding side to deliver ultimate volage gain into the output port. The design of the proposed converter successfully reduces voltage stress on power MOSFETs and diodes along with soft-switching performance for enhanced efficiency. The presence of common ground and continuous input current features make the converter particularly suitable for renewable energy systems. High voltage gain, low rms current stress on switching devices, moderated number of components and low-cost solution are among the advantages of the proposed converter. The overall efficiency of the proposed converter is estimated about 94.51% for high power level. Furthermore, dynamic modeling and implementation of pole-placement method has been carried out to investigate the robust performance of the proposed converter. Eventually, the proposed structure is built and tested in the laboratory to evaluate the theoretical analysis of the proposed converter. All the experimental results are compared and interpreted to confirm the proper performance of the proposed structure.

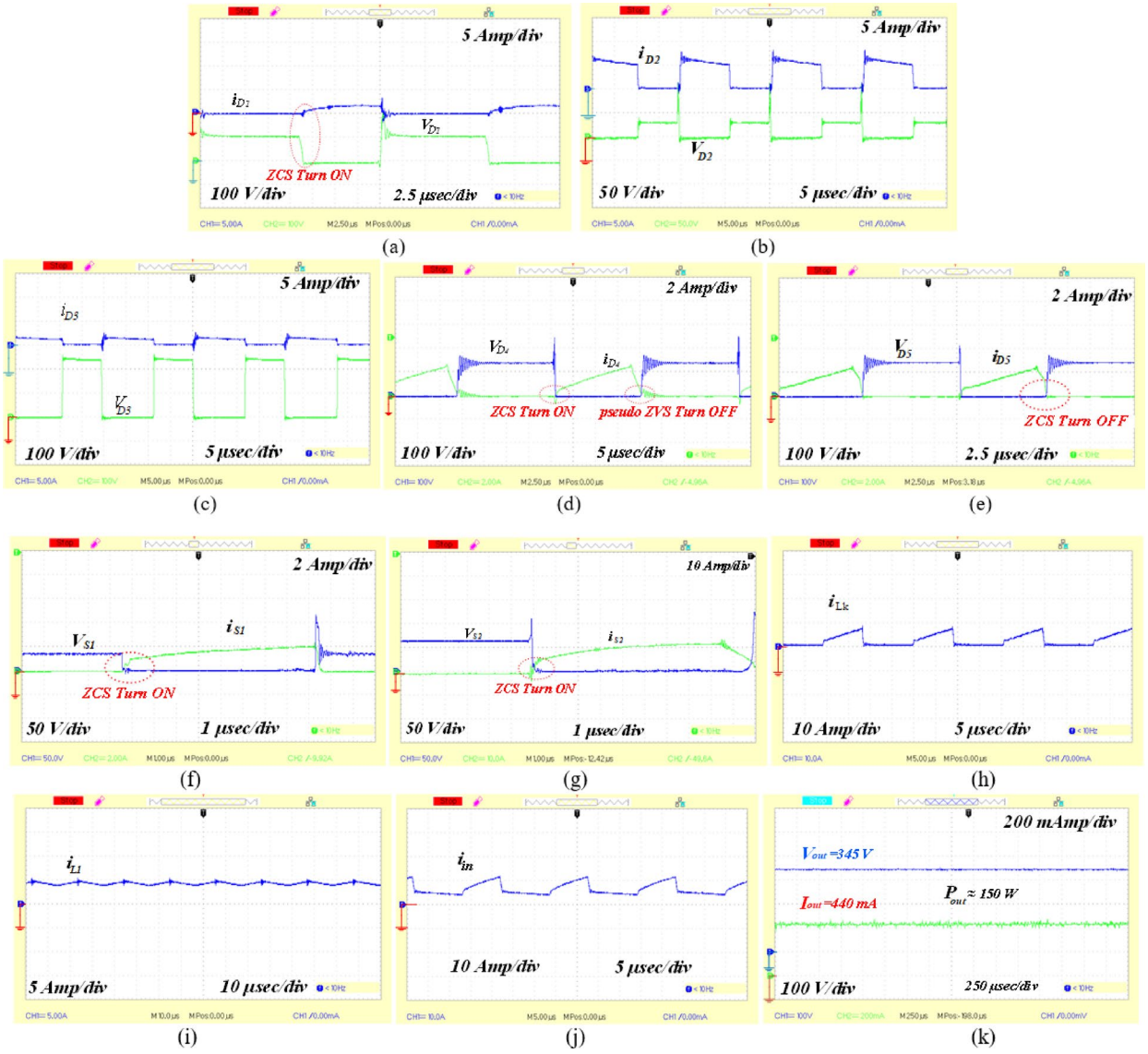

Fig. 11. The experimental waveforms of the inductors current, semiconductors, input current, output voltage/current, (**a**) V_{D1}, i_{D1} (**b**) V_{D2}, i_{D2} (**c**) V_{D3}, i_{D3} (**d**) V_{D4}, i_{D5} (**e**) $V_{D5,}$, i_{D5} (**f**) i_{S1}, V_{S1}, (**g**) i_{S2}, V_{S2}, (**h**) iL_k, (**i**) iL_1, (**j**) i_{in}, (**k**) i_{out} ,V_{out}.

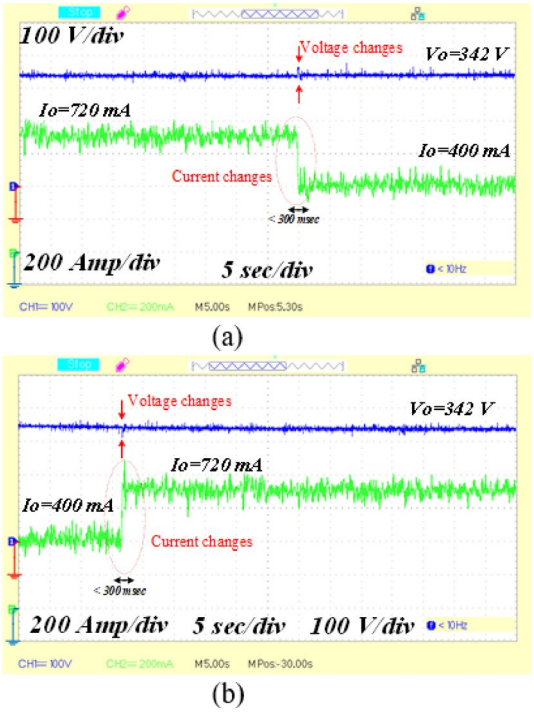

Fig. 12. The dynamic response of the proposed converter, (**a**) with 55% increasing changes in the load, (**b**) with 55% decreasing change in the load.

Data availability

The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

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Author contributions

Y. B. (Formal analysis, Methodology, Software, Writing—original draft) M. M. (Formal analysis, Methodology, Project administration, Validation, Supervision) S. N. (Formal analysis, Software, Writing—original draft) P. J. (Formal analysis, Software, Writing—original draft) M. R. F. (Project administration, Supervision, Validation, Writing—review) S. H. H. (Project administration, Supervision, Validation, Writing—review).

Declarations

Competing interests

The authors declare no competing interests.

Additional information

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