scientific reports

OPEN

Small signal modelling and analysis of quasi Z-source direct matrix converter for wind energy conversion system

K. T. Maheswari[1], C. Kumar[2], T. Dharma Raj[3] & Hady H. Fayek[4✉]

To enhance the voltage gain and regulate the output voltage under various loading and wind speeds, the Quasi Z-Source Direct Matrix Converter (QZSDMC) is proposed for PMG-based Direct Drive Wind Energy Conversion Systems (DDWECS). At first, using state space analysis, the small signal model of the QSDMC in space domain has been attained, and the transfer function of QZSDMC has been further calculated and analyzed. The stability analysis of the QZSDMC was conducted and proved that the system remains stable for all ranges of output power without using filter. The proposed QZSDMC based DDWECS with Improved Space Vector Pulse Width Modulation (ISVPWM) Control Scheme was simulated using Matlab and compared with existing methods. The simulation results are validated with 1 kW, 415 V, 50 Hz experimental setup with FPGA Processor. The outcomes are examined using the following metrics: switching stress, boost factor, total harmonic distortion, and efficiency.

Keywords Boost factor, Quasi z source direct matrix converter, Modified space vector pulse width modulation, Small signal model, Total harmonic distortion, Voltage gain

In the variable speed WECS, power converters play a major role since they act as an intermediary between the generator and the load[1]. Many literatures have proposed about the various topologies of power converters for Variable Speed Direct Drive Permanent Magnet Generators[2]. A simple low cost power converter configuration made up of a AC-DC converter, a boost/buck converter and an inverter was proposed in[3]. Back to back power converter with two level are also presented in[4,5]. Using a traditional rectifier and a Z-Source inverter, a two-stage conversion was first introduced in[6]. Next, Neutral Point Converter (NPC) which is connected back to back with three level has also been discussed by[7]. An integrated diode rectifier power converter, a 3-level boost converter and a clamped Neutral Point inverter that connects the output of generator to grid was presented at[8]. Currently, the employment of Matrix Converter for PMSG based WECS connected with the grid has gained more attention as presented by at[9–11].

Since traditional ac-dc-ac power converters provide three stages of power conversion, it increases system size, expense, loss and reduces system reliability and performance[12–14]. A bridge rectifier with diode is employed to rectify the PMG voltage at the output in the three-stage conversion of power[15]. To attain the required output, the dc chopper is then utilized to control the voltage in the capacitor that is supplied to the inverter. Some of the limitations of Voltage Source Inverters (VSI) are bulky, increase in losses, rich current harmonics, higher output Total Harmonic Distortion (THD), and requires output LC filter and unidirectional power handling capability. This system's total efficiency is reduced since it employs three stages of power conversion.

The conceptual and theoretical restrictions of conventional VSI and CSI has proposed an Z-Source Power Converter that affords a novel power conversion idea[16]. It has many advantages such as increasing or decreasing the voltage, higher efficiency and higher reliability[17]. Using a special impedance network, the Z-source inverter links the inverter's focal circuit to the input supply via a rectifier[18].

The primary function of this paper is to predict the most efficient power converter with a suitable PWM control technique for Variable Speed PMG based direct drive WECS[19]. For its compactness, Matrix Converter

[1]Electrical and Electronics Engineering, Bannari Amman Institute of Technology, Sathyamangalam 638401, India. [2]Electrical and Electronics Engineering, Karpagam College of Engineering, Coimbatore 641032, India. [3]Electrical and Electronics Engineering, Muthaysammal Engineering College, Rasipuram 637408, India. [4]Energy and Renewable Energy Engineering Department, Egyptian Chinese University, Cairo 11786, Egypt. ✉email: Hadyhabib@hotmail.com

(MC) was an outstanding competitor among conventional converters, which does not need any dc link and provides direct ac to ac conversion that facilitates maximum wind power extraction[20,21]. But the voltage transfer ratio of Matrix Converter was restricted to 0.866[22].

Z-Source Direct Matrix Converter (ZSDMC), which connects an Impedance-Source circuit to the Direct Matrix Converter, was developed to get around this problem[23]. Although ZSDMC offers buck boost ability with fewer LC components, the Z-Source network of ZSDMC has an intrinsic phase shift which ends in imprecise control and increased switching stresses, increasing the system's loss. The maximum voltage transfer ratio is 1.15[24–26]. Additionally, it generates irregular input current, necessitating the need of a sizable filter circuit to decrease the current harmonics at the input.[27].

The paper introduces a direct drive wind energy conversion system (DDWECS) built around a Quasi Z source matrix converter (QZSMC) to enhance the voltage transfer ratio. PWM techniques are now the most crucial control methods, which includes many types of boost control methods[28]. However, conventional CBPWM for QZSMC, has higher switching stresses, higher losses, higher THD, and lower efficiency. A unique Improved Space Vector Pulse Width Modulation Scheme (ISVPWM) for QZSMC based DDWECS has been suggested in order to overcome the limitations of standard CBPWM[29,30]. It is possible to raise the quasi Z source network's duty ratio by altering the shoot through dispersal in space vector modulation[31,32]. Furthermore, control, modeling and utilization of QZSDMC to WECS, have not yet been discussed[33]. Hence, this paper objects to focus on modeling, control and evaluating QZSDMC's stability for interfacing PMG-WECS and load. The small signal model and its transfer function have been developed for both QZSDMC, to confirm the stability of the system.

To clearly highlight the advancements over existing works, the following novel contributions of the proposed Quasi Z-Source Direct Matrix Converter (QZSDMC) and its PWM techniques are summarized:

- **Enhanced Voltage Gain:** The proposed QZSDMC achieves a voltage gain of 1.15, surpassing traditional converters, which are typically limited to a maximum of 1.1.
- **Improved PWM Scheme:** The introduction of the Improved Space Vector PWM (ISVPWM) scheme significantly reduces switching losses and Total Harmonic Distortion (THD) compared to conventional Carrier-Based PWM (CBPWM).
- **Reduced Switching Stresses:** The ISVPWM-based QZSDMC demonstrates a 12% reduction in voltage stress and lower current stress (1 A), improving efficiency and extending converter lifespan.
- **Optimized Shoot-Through Control:** A novel shoot-through control strategy is implemented, optimizing the duty ratio to enhance the voltage boosting capability without compromising stability.

Additionally, this paper is arranged as explained: In Sect. 2, the working modes of QZSDMC have been explained and the small signal model of QZSDMC in space domain has been attained. The transfer function of proposed QZSDMC has been derived and the effect of inductive and capacitive elements and the shoot through state on the transient response of proposed converter has been analysed. The QZSDMC is used in Sect. 3 as an interface between the separate load and PMG-WECS, and the controller is made to produce the required output. In Sects. 4 and 5 of this paper, the performance of the suggested QZSDMC with ISVPWM control technique was compared with the CBPWM strategy.

Quasi Z-source direct matrix converter
Topology
QZSDMC topology has four parts specifically input filter, QZS network, DMC and three phase load as given in Fig. 1[34,35].

The QZS network consists of six inductors (Lx1,Lx2,Ly1,Ly2,Lz1,Lz2) and six capacitors (Cx1,Cx2,Cy1,Cy2,Cz1,Cz2) along with three additional bidirectional switches (S1,S2,S3). These additional switches can be operated by a single gate signal since they share the same switching status as S0. The special network with impedance source permits the proposed circuit to run in the buck- boost mode as well as offering the innovative features that other conventional converters cannot achieve[36].

The operating concept of envisaged QZSDMC topology can be separated into Shoot through State (ST) and Active or Non shoot through state (NST)[37]. At the time of Shoot through State (ST), the switch S0 is turned OFF and the output of QZSDMC such as x', y' and z' has been shorted for enhancing the voltage. Whereas in the course of Non Shoot through State (NST), the switch S0 is switched on in order to carry out regular switching operation of Direct Matrix Converter[38]. Since the system is symmetrical, the inductance L of all the inductors (Lx1 to Lz2) and also, the capacitance C of all the capacitors (Cx1 to Cz2) of the QZS network are same[39]. Let the total time period for full complete switching cycle is T, the time period for Zero State is T0 and the Time period for Active State is T1 and hence, T = T0 + T1. The shoot through time period's duty ratio can be given by D = T0/T1.

Small signal model
The suggested small signal modeling and investigation continues through the supposition that while supplied by variable voltage and frequency sinusoidal voltage source, the QZSDMC is feeding an RL load[40–42]. In the QZS network, the switch S0 is closed during active state. Let the state variables (inductor currents, capacitor voltages in the QZS network and output current vector) can be defined based on space vector as Eqs. (1),

$$x(t) = \begin{bmatrix} i_{L1}(t) & i_{L2}(t) & v_{C1}(t) & v_{C2}(t) & i_L(t) \end{bmatrix} \tag{1}$$

Let's specify the input voltage vector of QZS network as $V_{iq,}$ input variable. Assuming,

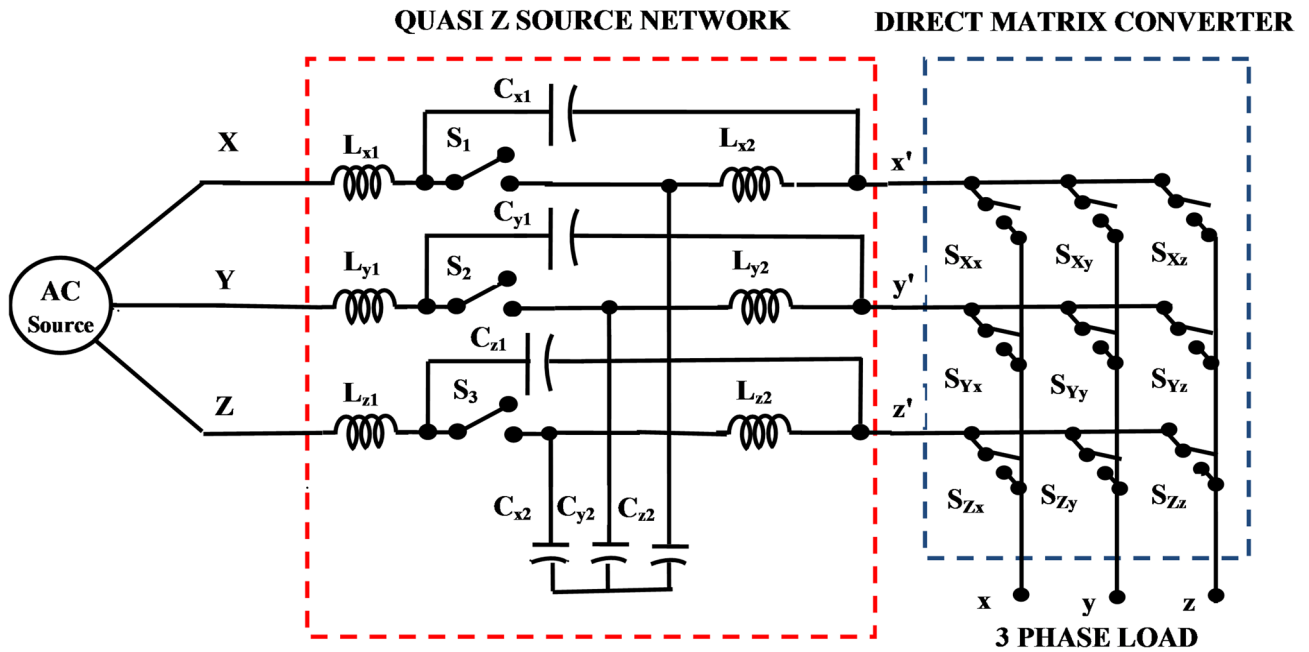**QUASI Z SOURCE NETWORK** **DIRECT MATRIX CONVERTER**

Fig. 1. Topology of voltage fed QZSDMC.

$$\begin{aligned}
C_1 &= C_{x1} = C_{y1} = C_{z1} \\
C_2 &= C_{x2} = C_{y2} = C_{z2} \\
L_1 &= L_{x1} = L_{y1} = L_{z1} \\
L_2 &= L_{x2} = L_{y2} = L_{z2}
\end{aligned} \tag{2}$$

Furthermore, assume that R_L and L_L gives the resistance and inductance of the RL load, respectively.

State-space representation during shoot-through state

By turning on all of the switches for one, two, or three phase legs, a shoot-through state can be reached. At shoot through state, the differential equation can be given in the state space form as given by Eq. (3)

$$K\ \dot{x} = A_1 \cdot x + B_1 \cdot u \tag{3}$$

From the equal model of shoot through state, the state space form in Eq. (3) can be derived as shown in Eq. (4) to (8),

$$L_1 \frac{di_{L1}(t)}{dt} = V_{C1}(t) \tag{4}$$

$$L_2 \frac{di_{L2}(t)}{dt} = V_{C2}(t) \tag{5}$$

$$C_1 \frac{dV_{C1}(t)}{dt} = -i_{L1}(t) \tag{6}$$

$$C_2 \frac{dV_{C2}(t)}{dt} = -i_{L2}(t) \tag{7}$$

$$L_L \frac{di_L(t)}{dt} = -R_L i_L(t) \tag{8}$$

From Eq. (4) to (8), state space equations for shoot through duty period is given by Eqs. (9),

$$\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & L_L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_L(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0R_L \end{bmatrix} \cdot \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_L(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \cdot Viq(t) \tag{9}$$

Where

$$K = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & L_L \end{bmatrix}, \; A1 = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \text{-R}_L \end{bmatrix}, \; B1 = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (10)$$

State space representation during non-shoot through state

Similarly, the state space representation of QZSDMC during active state can be given as in Eqs. (11),

$$K\dot{x} = A_2 \cdot x + B_2 \cdot u \tag{11}$$

The following Eqs. (12) to (16) can be obtained from the equivalent circuit of active state,

$$L_1 \frac{di_{L1}(t)}{dt} = -V_{C2}(t) \tag{12}$$

$$L_2 \frac{di_{L2}(t)}{dt} = -V_{C1}(t) + V_{iq} \tag{13}$$

$$C_1 \frac{dV_{C1}(t)}{dt} = -i_{L2}(t) + i_L \tag{14}$$

$$C_2 \frac{dV_{C2}(t)}{dt} = -i_{L1}(t) + i_L \tag{15}$$

$$L_L \frac{di_L(t)}{dt} = -V_{C1}(t) - V_{C2}(t) + R_L i_L(t) \tag{16}$$

From Eqs. (12) to (16), the state space equations during non-shoot through state in matrix form can be written as Eqs. (17),

$$\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & L_L \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_L(t) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & -1 & 0 & 0 & 1 \\ -1 & 0 & 0 & C_2 & 1 \\ 0 & 0 & -1 & -1 & -R_L \end{bmatrix} \cdot \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \\ i_L(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_{iq}(t) \quad (17)$$

Where

$$K = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & L_L \end{bmatrix}, \; A2 = \begin{bmatrix} 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & -1 & 0 & 0 \\ 0 & -1 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 & 1 \\ 0 & 0 & -1 & -1 & \text{-R}_L \end{bmatrix}, \; B2 = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (18)$$

Equation (3) can be resolved to identify the equilibrium of the state vector. The equilibrium values of state variable is given by Eq. (19) to (21)

$$0 = AX + BU \tag{19}$$

$$0 = CX + EU \tag{20}$$

$$0 = \left(DA_1 + D'A_2\right)X + \left(DB_1 + D'B_2\right)U, \tag{21}$$

Where,

$$A = DA_1 + D'A_2$$

$$B = DB_1 + D'B_2$$

$$C = DC_1 + D'C_2$$

$$E = DE_1 + D'E_2$$

Assume

$$\text{L} = \text{L}_1 = \text{L}_2 \text{ and C} = \text{C}_1 = \text{C}_2. \tag{22}$$

By resolving Eq. (17), the converter steady state equation can be given by Equations (23) to (24),

$$i_{L1} = i_{L2} = \frac{1-D}{1-2D}I_L \tag{23}$$

$$V_{C1} = \frac{1-D}{1-2D}V_{iq} \tag{24}$$

$$V_{C2} = \frac{D}{1-2D} V_{iq} \tag{25}$$

Let V_{im} be the output voltage vector of QZSDMC.

$V_{im}=0$ in shoot through state.

Whereas,

$$V_{im} = V_{C1} + V_{C2} \quad \text{in non-shoot through state} \tag{26}$$

From (26) considering (24) and (25), we get, Eq. (27)

$$V_{im} = \frac{1}{1-2D} V_{iq} \tag{27}$$

From Eq. (19), it is concluded that QZSDMC can achieve an ideal unlimited boost factor.

The small signal association among the state variables can be achieved by relating small signal perturbations $\widehat{v}_{i1}(t)$ to input voltage and to the shoot through duty ratio of S_0 given by Eqs. (28),

$$v_{i1}(t) = V_{i1} + \widehat{v}_{i1}(t), \; d(t) = D + \widehat{d}(t) \tag{28}$$

The perturbations results in small signal differences in the state variable.

Let

$$\mathrm{x} = \mathrm{X} + \mathrm{x} \tag{29}$$

Merging equations of mode 1 and mode 2, we get small signal state Eqs. (30),

$$K\widehat{X} = (D \cdot A_1 + D\prime \cdot A_2) \cdot \widehat{X} + (DB_1 + D\prime B_2) \cdot U + (A_1 - A_2)X + (B_1 + B_2)U \tag{30}$$

Solving above equations, the Laplace transform of small signal Equations in space domain can be derived and is given by Equations (31) to (33),

$$sL\widehat{i}_{L1}(s) = D\widehat{V}_{C1}(s) - D\prime \widehat{V}_{C2}(s) + (V_{C1}+V_{C2})\widehat{d}(s) \tag{31}$$

$$sL\widehat{i}_{L2}(s) = -D\prime \widehat{V}_{C1}(s) + D\widehat{V}_{C2}(s) + (V_{C1}+V_{C2})\widehat{d}(s) + \widehat{V}_{iq} \tag{32}$$

$$sC\widehat{V}_{C1}(s) = -D\widehat{i}_{L1}(s) + D\prime \widehat{i}_{L2}(s) - D\prime \widehat{i}_L(s) + (-i_{L1}-i_{L2}+I_L)\widehat{d}(s) \tag{33}$$

$$sC\widehat{V}_{C2}(s) = D\prime \widehat{i}_{L1}(s) - D\widehat{i}_{L2}(s) + D\widehat{i}_L(s) + (-i_{L1}-i_{L2}+I_L)\widehat{d}(s) \tag{34}$$

$$(R_L + sL_L)\widehat{i}_L(s) = D\prime \left(\widehat{V}_{C1}(s) + \widehat{V}_{C2}(s)\right) - (V_{C1}+V_{C2})\widehat{d}(s) \tag{35}$$

By substituting $\widehat{\overline{i_L}} = \widehat{\overline{i_{L1}}} + \widehat{\overline{i_{L2}}}, \overline{I_L} = \overline{I_{L1}} + \overline{I_{L2}}, \widehat{v}_c = \widehat{\overline{v_{c1}}} + \widehat{\overline{v_{c1}}}, \overline{V}_C = \overline{V}_{C1} + \overline{V}_{C2}$ in above equations we get Equations (36) to (38),

$$sL\widehat{\overline{i_L}}(s) = (D - D\prime)\widehat{\overline{v_c}}(s) + \left(2\overline{V}_c\right)\widehat{d}(s) + \widehat{V}_{iq} \tag{36}$$

$$sC\widehat{\overline{v_C}}(s) = (D\prime - D)\widehat{i}_L(s) - 2D\prime \widehat{i}_L(s) + 2(i_L - I_L)\widehat{d}(s) \tag{37}$$

$$(R_L + sL_L)\widehat{i}_L(s) = D\prime \widehat{\overline{v_c}}(s) - \overline{V}_c \widehat{d}(s) \tag{38}$$

Transfer function model

The reaction of one state variable to various small signal disturbances can be obtained in small signal modeling and transitory analysis through linear combinations of adjustable response to individual disturbances[43,44]. Hence, the capacitor voltage small signal expression can be given by Eqs. (39),

$$\widehat{v}_C(s) = G_{viq}(s) \cdot \widehat{V}_{iq}(s) + G_{vd}(s) \cdot \widehat{d}(s) \tag{39}$$

where, $G_{viq}(s)$ represents the transfer function of input to capacitor voltage and $G_{vd}(s)$ the transfer function of control to capacitor voltage.

$$G_{viq}(s) = \frac{\overset{\wedge}{v_C}(s)}{\overset{\wedge}{V_{iq}}(s)}\Bigg|_{\overset{\wedge}{d(s)}=0} = \frac{sL(D\prime - D)}{s^2 LC + (D - D\prime)^2 + \frac{2(1-D)sL}{R_L + sL_L}} \tag{40}$$

$$G_{vd}(s) = \frac{\overset{\wedge}{v_C}(s)}{\hat{d}(s)}\Bigg|_{\overset{\wedge}{v_{iq}(s)}=0} = \frac{(1-2D)2V_C - \frac{2V_C(1-D)sL}{R_L + sL_L} + 2(i_L - I_L)sL}{s^2 LC + (D - D\prime)2 + \frac{2(1-D)^2}{R_L + sL_L}} \tag{41}$$

Figure 2 shows the simulated Bode magnitude and phase response of the output voltage-controlled QZSDMC using MATLAB's Control System Toolbox. The Bode plot was generated by linearizing the small signal state-space equations derived in Equations (31) to (38), with input as the shoot-through duty ratio and output as the capacitor voltage. A Proportional-Integral (PI) compensator was used in the outer voltage control loop to regulate the capacitor voltage. The PI gains were tuned using the Ziegler-Nichols method followed by manual fine-tuning to meet the desired dynamic response. The system exhibits a gain margin of 10.5 dB and a phase margin of 52°, indicating robust stability. These margins are maintained across various operating points, including wind velocities ranging from 4 m/s to 12 m/s, due to the gain scheduling approach embedded within the control loop. This ensures consistent closed-loop performance of the QZSDMC under variable loading and wind conditions.

Modulation schemes for QZSDMC
The shoot through control methods such as simple boost, maximum boost, maximum constant boost and space vector PWM can be applied to QZDMC after certain modification in the carrier envelope. The Carrier Based PWM Technique and Modified Space Vector PWM Technique are employed to analyze the performance of QZSDMC.

Carrier based PWM scheme
In this PWM technique, the carrier waveform has been bounded by the same envelope of three phase voltages V_x, V_y and V_z. The top and bottom envelope of carrier waveform formed by the maximum and minimum voltages amongst the three input source voltages[45]. During each switching time period, the triangular carrier is matched with the output reference voltage V_X, V_Y and V_Z to get the PWM signals (S_X, S_Y and S_Z). The shoot through pulses are produced by comparing the carrier waveforms with the shoot through reference and these pulses are inserted in the final output PWM signals as shown in Fig. 3.
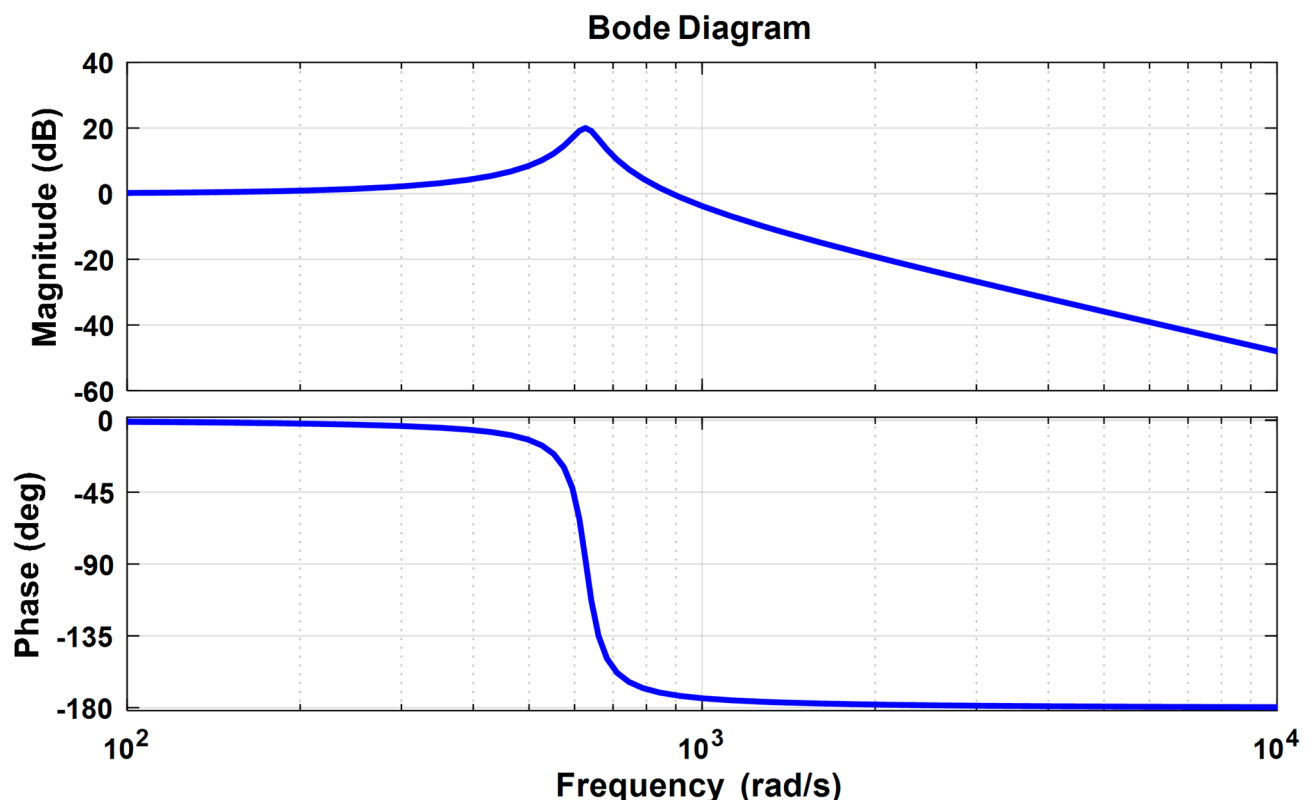

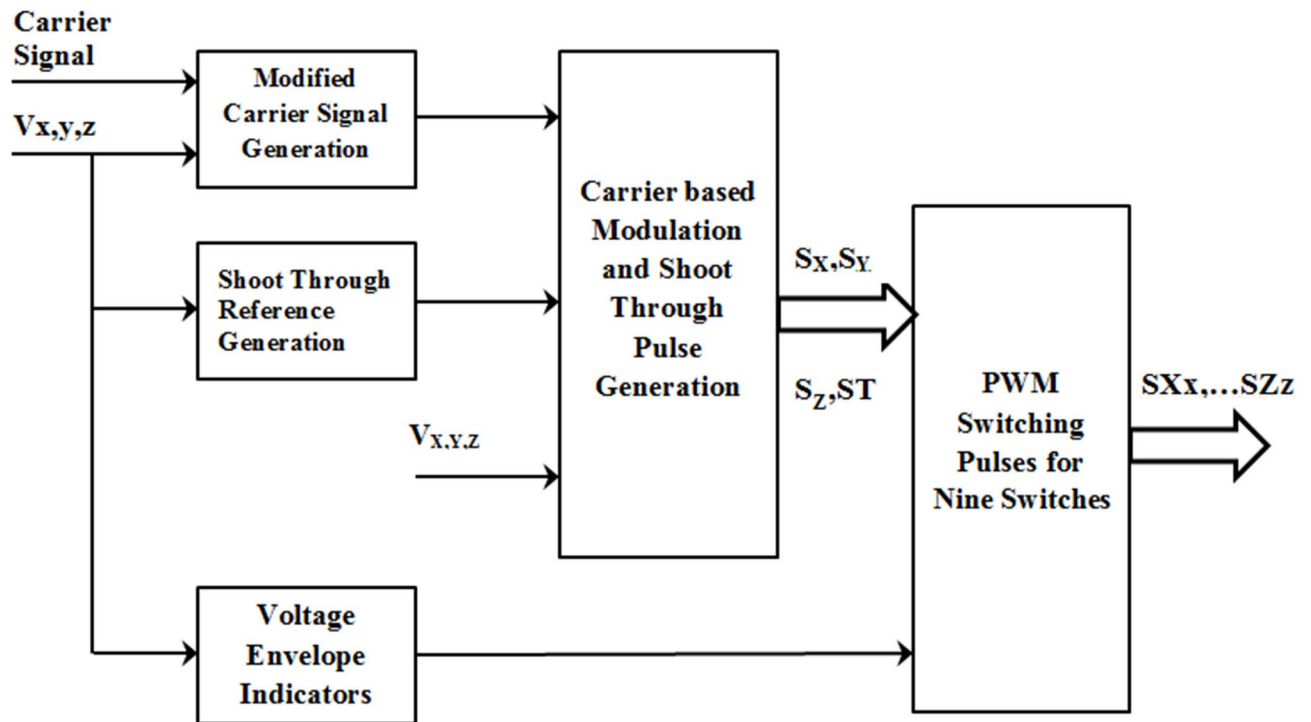**Fig. 2**. Magnitude and phase plot of output voltage controlled QZSDMC.

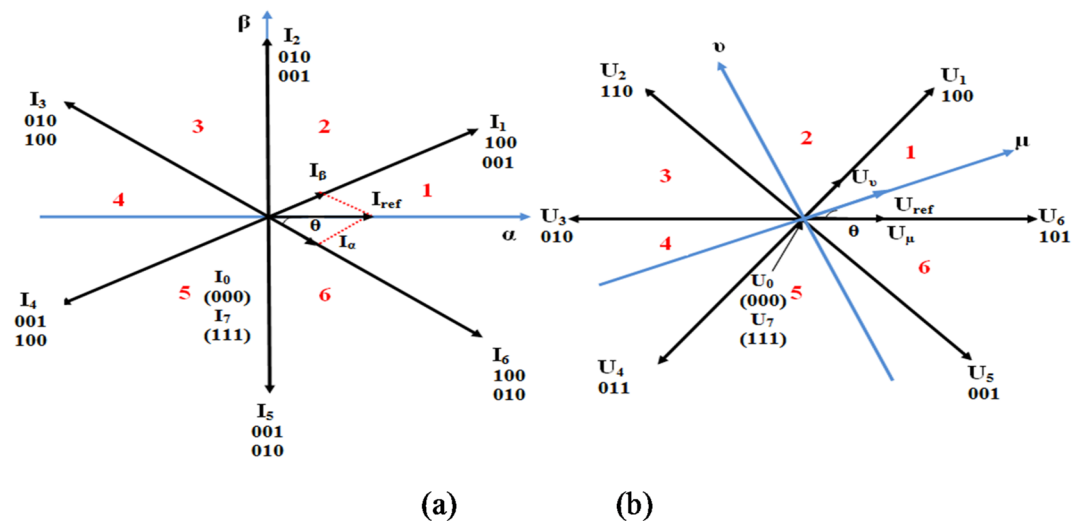**Fig. 3**. Block Diagram for QZSDMC Pulse Generation with Shoot through Insertion.

(a)   **(b)**

Fig. 4. Modified space vector pulse width modulation technique (**a**) input current space vector (**b**) output voltage space vector.

Modified space vector PWM scheme

In MSVPWM of QZSDMC, the conventional space vector modulation method is introduced with the control of shoot through state[46]. The active states of traditional DMC is maintained as same in the non-shoot through mode of QZSDMC and portion of the zero vector is replaced by the shoot through states in one complete switching period. Based on the number of phases short circuited, there are three possible groups of shoot through vectors such as single phase, two phases and three phases shoot through.

When related to other two techniques, the single output phase shoot through efficiently diminish the switching period of bidirectional switches. Thus, the voltage boosting in modified modulation strategy is achieved by employing single phase shoot through zero vectors. For instance, assume that the input current vector is situated in sector 1 and output line voltage vector is situated in sector 2. As shown in Fig. 4, the active vectors are formed

by the active current vectors I_1, I_6 and the active voltage vectors U_1, U_2. Then four active vectors such as xyy, xyx, xzx, xzz and two zero vectors yyy, zzz are formed. The equivalent shoot through zero vectors are denoted as S_tyy, xyS_t, xS_tx, xzS_t, S_tzz. The law of sines is used to calculate the duty ratio of input current ad output voltage vectors as given by Eqs. (42),

$$d_\alpha = \frac{T_\alpha}{T_s} = m_i \sin(60° - \theta_{mi})$$
$$d_\beta = \frac{T_\beta}{T_s} = m_i \sin\theta_{mi}$$
$$d_\mu = \frac{T_\mu}{T_s} = m_\nu \sin(60° - \theta_{mv})$$
$$d_\nu = \frac{T_\nu}{T_s} = m_\nu \sin\theta_{m\nu}$$

(42)

Also, we have

$$d_{\alpha\mu} = d_\alpha \cdot d_\mu$$
$$d_{\alpha\nu} = d_\alpha \cdot d_\nu$$
$$d_{\beta\mu} = d_\beta \cdot d_\mu$$
$$d_{\beta\nu} = d_\beta \cdot d_\nu$$

(43)

where,
$d\alpha$, $d\beta$ - Duty ratios of active input current vectors of rectifier stage.
$d\mu$, dv - Duty ratios of active output voltage vectors of inverter stage.
mi - Modulation index of rectifier stage.
mv- Modulation index of inverter stage.
Tx, where x = α,β,μ,v specifies the period of an active vector in a switching cycle Ts.
Then, the output voltage modulation and input current modulation can be combined to obtain four pairs of active vectors and one zero vector.

$$T_1 = d_{\alpha\mu}T_s = m\sin(60° - \theta_{mi})\sin(60° - \theta_{m\nu})T_s$$
$$T_2 = d_{\alpha\nu}T_s = m\sin\theta_{m\nu}\sin(60° - \theta_{mi})T_s$$
$$T_3 = d_{\beta\mu}T_s = m\sin(60° - \theta_{m\nu})\sin\theta_{mi}T_s$$
$$T_4 = d_{\beta\nu}T_s = m\sin\theta_{m\nu}\sin\theta_{mi}T_s$$
$$T_0 = d_{ST}T_s$$
$$T_z = 1 - T_1 - T_2 - T_3 - T_4 - T_0$$
$$m = m_i m_v$$

(44)

where, $0 \leq \theta_{mi} \leq 60^o, 0 \leq \theta_{m\nu} \leq 60^o$, T_1, T_2, T_3, T_4 specifies the switching period of active vectors in a switching period T_s, T_0 denotes shoot through time period, T_z denotes the switching sequence of zero vectors in a switching cycle T_s, m denotes modulation index and d_{ST} denotes shoot through duty ratio. The switching time period of shoot through zero vectors is adjusted to improve the performance of QZSDMC. However, the active vector remains unchanged.

Controller for QZSDMC based WECS

The most important factor in controlling the QZSDMC's output voltage is the dispersion of the shoot through period. The QZSDMC promises continuous input current, lower harmonics of the output waveform, higher voltage gain, and less switching stresses when the shoot through period is inserted using an appropriate control method. To produce fixed output voltage and frequency a closed loop controller has been used for the suggested QZSDMC. Figure 5 gives the block diagram of Closed Loop Controller for QZSDMC with PMG based DDWECS[47]. To produce PWM pulses for QZSDMC, the PWM controller receives the 3 phase reference voltages (Vx, Vy, and Vz) that were acquired from the closed loop controller. PWM controller provides PWM pulses using two different modulation algorithms, such as CBPWM and ISVPWM[48]. The rotor speed reference ωr* at which maximum power can be harvested has been computed using the measured wind velocity in the closed loop controller's MPPT control technique. The actual speed of rotor ωr obtained from the PMG is compared with the rotor speed reference ωr* at each wind speed Vω and the resultant signal is fed to a PI controller. After comparing the PI controller's output with the carrier signal, a control signal that serves as a speed regulator to modify the shoot through duty ratio D is produced.

To regulate active and reactive powers, the closed loop controller has an inner and an outer loop. The Park/Clark Transformation, which converts electrical quantities into a dqo reference frame, is the primary foundation of the closed loop controller. The Park/Clark Transformation is used to convert the three phase load voltages and load currents into dq axis components, such as Vds, Vqs, id, and iq. The actual dq axis current (id and iq) is related with the reference dq axis current (id* and iq*) valued from the obtained reactive power and capacitor voltage separately and the obtained error signals are managed via the PI controllers to provide the reference dq axis voltages (Vds*and Vqs*).
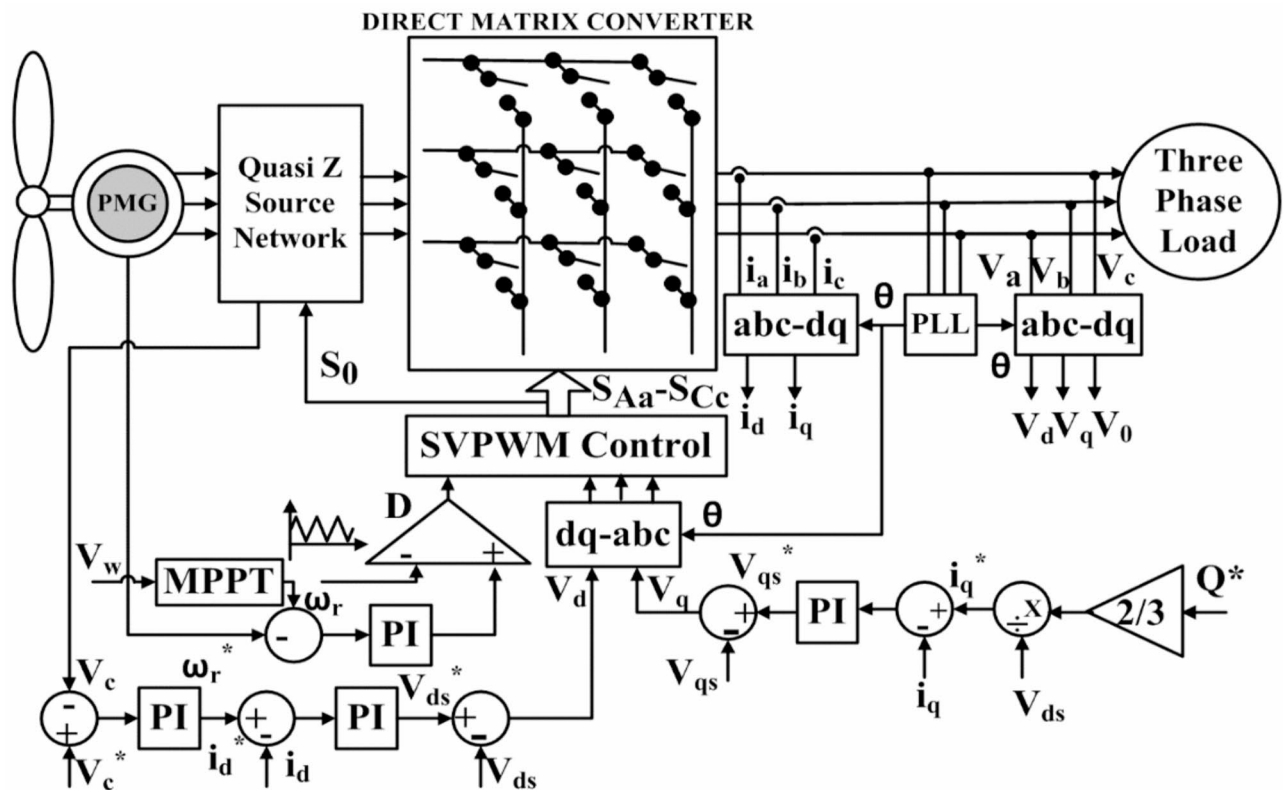
Fig. 5. Closed Loop Controller for QZSDMC with PMG based Direct Drive Wind Energy Conversion System.

Then, the inverse Park/Clark transformation is used to transform the produced dq-phase voltages into the three-phase reference voltages respectively. The PWM controller receives the attained sinusoidal reference signal as input and uses it to create PWM pulses for the QZSDMC. In QZSDMC, the gain G and Boost Factor B is dependent on Modulation Index M and Shoot through Duty Ratio D. By varying these parameters constant output voltage and frequency can be obtained. Also, the THD in the output voltage and current has to be reduced[49].

The proposed QZSDMC are known for their ability to handle wide input voltage ranges. However, they can also experience increased voltage stress due to the high voltage boost capability, which may require components with higher voltage ratings. Also, handling faults in quasi-Z-source DMCs can be complex and Ensuring fault tolerance and safe operation under various fault conditions requires sophisticated fault management and protection strategies. These are some of the limitations of QZSDMC[50,51].

Results and discussion

Based on characteristics like switching stress, THD and for numerous wind velocity and load situations, the investigations of QZSDMC with CBPWM and ISVPWM schemes, has been conducted. To predict the effectiveness of CBPWM and ISVPWM scheme, the QZSDMC has been simulated in MATLAB/SIMULINK environment and its operation was analyzed for various input and load conditions. The results obtained under two cases are also compared to envisage the better PWM scheme for QZSDMC.

Figure 6a–c shows the voltage in the capacitor, current through the inductor and ac link voltage of QZSDMC with CBPWM technique. It was observed that the voltage across the capacitor was 205 V, the current through the inductor was 90 A and that of AC link voltage was 510 V. To enhance the performance of QZSDMC a novel improved space vector PWM scheme has been investigated. Figure 7a–c shows the capacitor voltage, inductor current and ac link voltage of QZSDMC under ISVPWM scheme for the generated voltage of PMG as 173 V, turbine speed of 130 rpm, D_0 as 0.2 and modulation index 0.8.

Figures 8 and 9 represents the line voltage and phase voltage of CBPWM and ISVPWM based QZSDMC for three phases without filter respectively. According to the results, the ISVPWM scheme's voltage gain is more than the CBPWM scheme's. Figure 10 represents the three-phase individual output current of the QZSDMC based on CBPWM and ISVPWM at a 0.25 kW load, respectively.

Performance analysis of QZSDMC at different loading conditions

The foremost objective of the simulation is to analyse the QZSDMCs harmonic spectra of output parameters such as line voltage and current under two different PWM Schemes. Figures 11 and 12 represents simulated output voltage and output current harmonic spectra of QZSDMC for both CBPWM and ISVPWM schemes at a load of 0.25 kW. For the CBPWM and ISVPWM schemes, the QZSDMC output line voltage THD is around
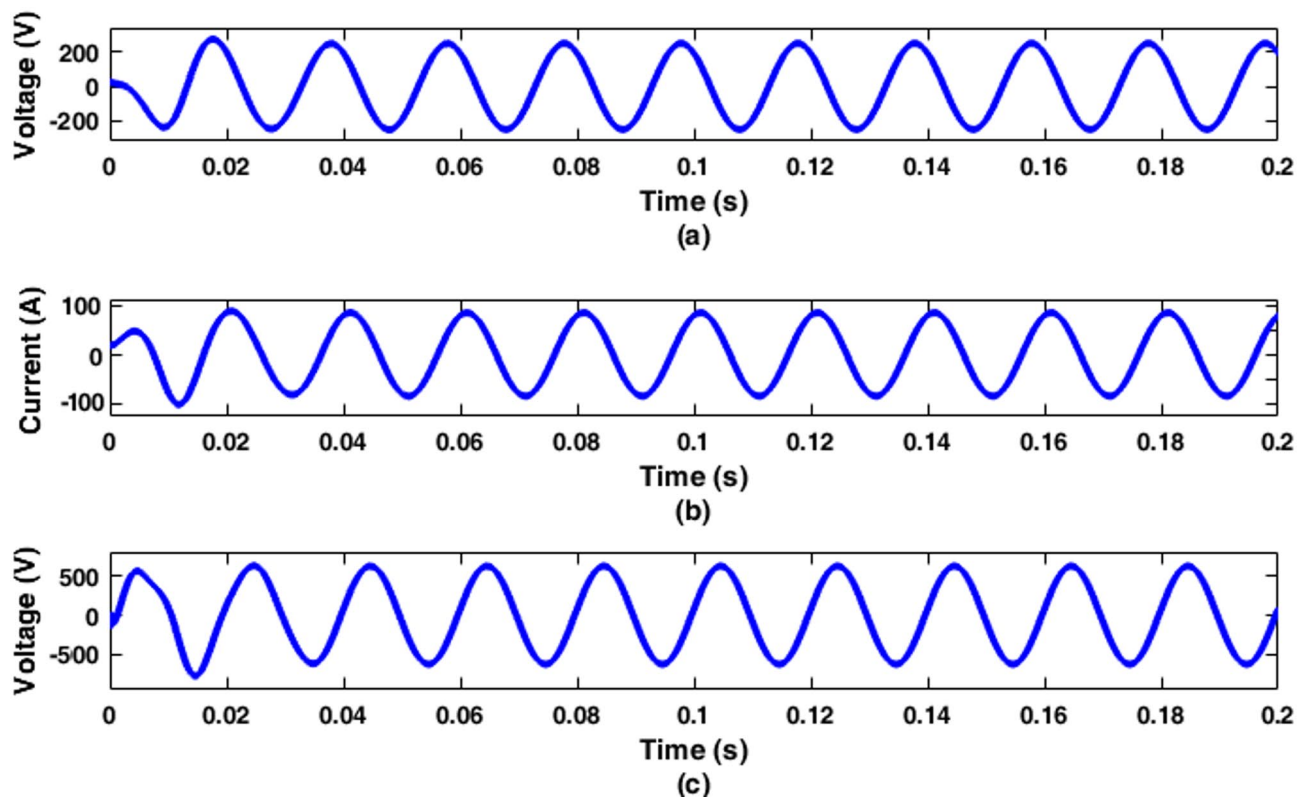
Fig. 6. Simulated Outputs of CBPWM based QZSDMC for (**a**) Capacitor Voltage (**b**) Inductor Current and (**c**) AC link Voltage.

2.6% and 1.2%, respectively. The percentage output current THD of CBPWM is 1.05% greater than that of ISVPWM scheme employed in QZSDMC. Thus, the ISVPWM scheme is considered to be the best for efficient operation of QZSDMC.

Figure 13 compares the voltage and current THD at the output of QZSDMC for two PWM methods. The figure makes it clear that, in comparison to the CBPWM scheme for QZSDMC, the THD parameters of the ISVPWM method are lower.

Analysis of switching stress

By raising shoot through duty ratio D0 and the modulation index M, QZSDMC's voltage gain can be enhanced. By partially or completely substituting shoot-through states for zero states without interfering with active states, the voltage gain of QZSDMC can be boosted. Figures 14 and 15 show the changes in current and voltage stresses in the QZSDMC power switches under the CBPWM and ISVPWM schemes for different shoot through duty ratios, respectively.

The current stress of CBPWM scheme is almost higher than that of ISVPWM scheme for QZSDMC for various D_0. Figures 14 and 15 show that, with D_0 of 0.3, the ISVPWM scheme-based QZSDMC's voltage stress is 12% lower than the CBPWM scheme's, and the ISVPM scheme's current stress is 1 A lower than the CBPWM scheme's.

Figures 16 and 17 shows the variations in the current stresses and Voltage stresses of power switches for QZSDMC with CBPWM and ISVPWM scheme at different load conditions. At 1 kW load, the voltage stress of power switches for ISVPWM scheme is about 95 V less than that of CBPWM scheme. Also the current stress of power switches under CBPWM scheme is 1.6 A greater than that of ISVPWM scheme.

Experimental setup

A model has been developed as shown in Fig. 18 to validate the modulation technique and the simulation results of the proposed QZSDMC.

The control algorithms in Quasi Z Source DMC and ISVPWMM techniques are complex. Implementing these in experimental setups involves hardware-in-the-loop simulations or real-time control, which can introduce uncertainties in the system due to computational limitations or control implementation errors. Limitations in hardware, scalability, and real-time implementation can affect the fidelity of the experimental study. These challenges have been addressed by developing and implementing robust control algorithms that can handle uncertainties and variations in the system's operation. Also, by employing filtering and noise reduction methods in signal processing the impact of noise on measurements and system performance analysis is reduced.
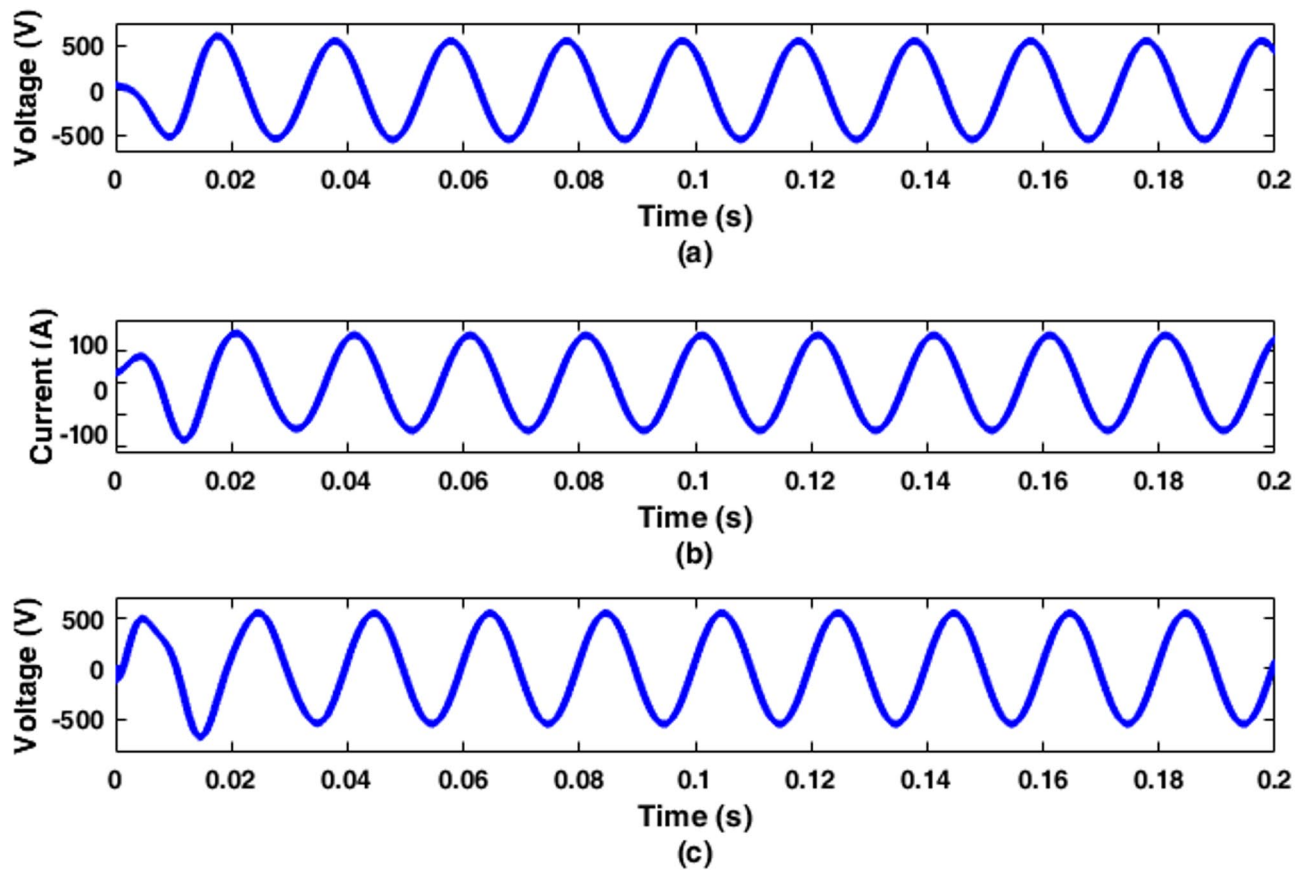
Fig. 7. Simulation results of ISVPWM based QZSDMC for (**a**) Capacitor Voltage (**b**) Inductor Current and (**c**) AC Link Voltage.
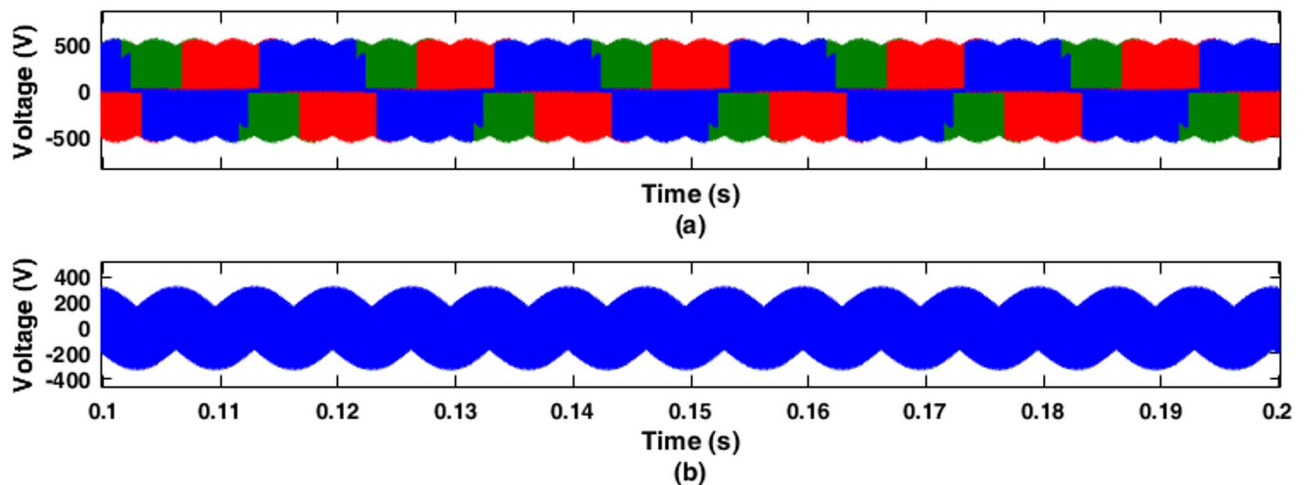

Fig. 8. Simulated Outputs of CBPWM based QZSDMC for Three Phase (**a**) Line Voltage and (**b**) Phase voltage without filter.

However, to address the problem of uncertainties and noise encountered in simulation studies of quasi Z-source D-MC based wind energy conversion systems model validation has to be done in which Simulink model results are related with benchmarks to authorize the correctness of the model and ensure it behaves realistically under different conditions. Furthermore, noise disturbances can be reduced by conducting noise analysis to understand its impact on results and applying appropriate filtering methods. By employing these strategies, researchers aim to address.
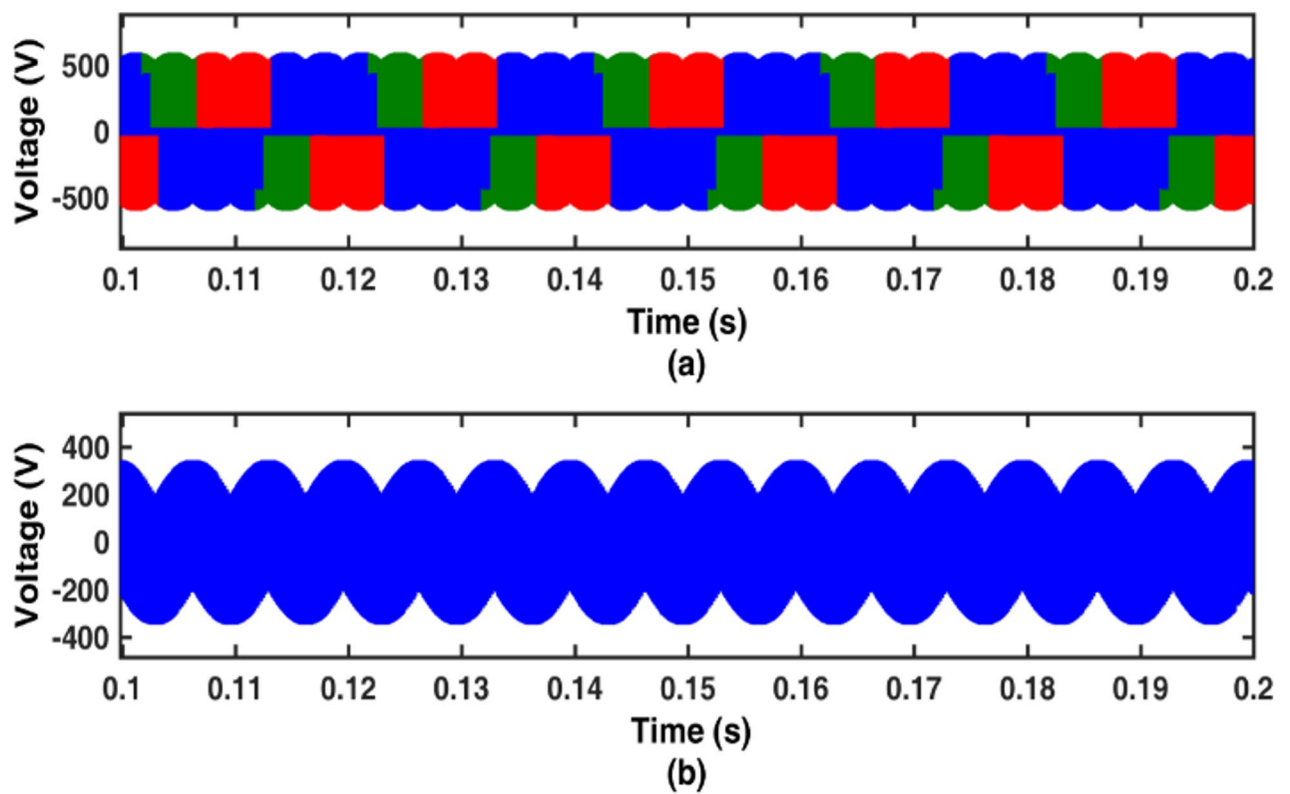
Fig. 9. Simulated Outputs of ISVPWM based QZSDMC for Three Phase (**a**) Line Voltage and (**b**) Phase Voltage without filter.
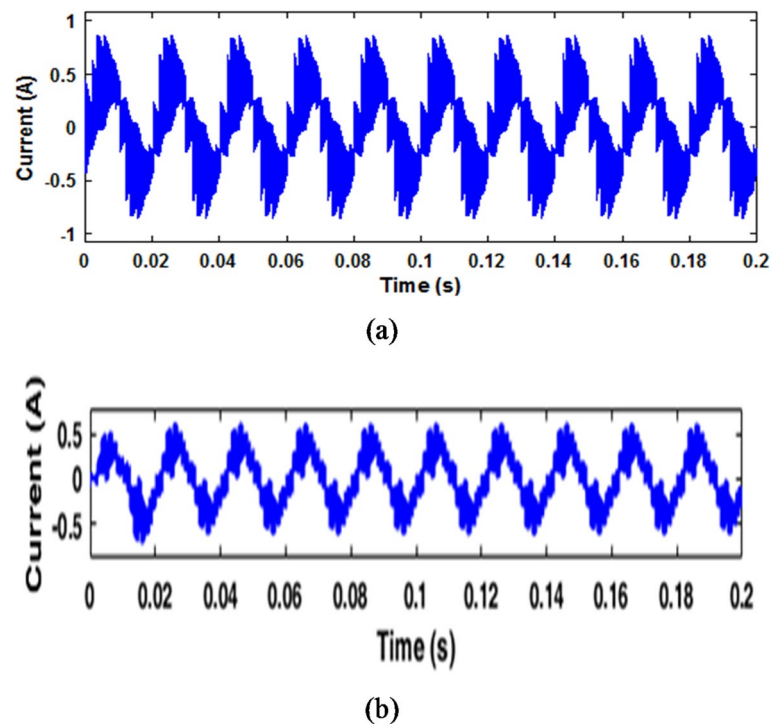
Fig. 10. Simulation results for (**a**) CBPWM and (**b**) ISVPWM based QZSDMC Output Current.

(a)

(b)
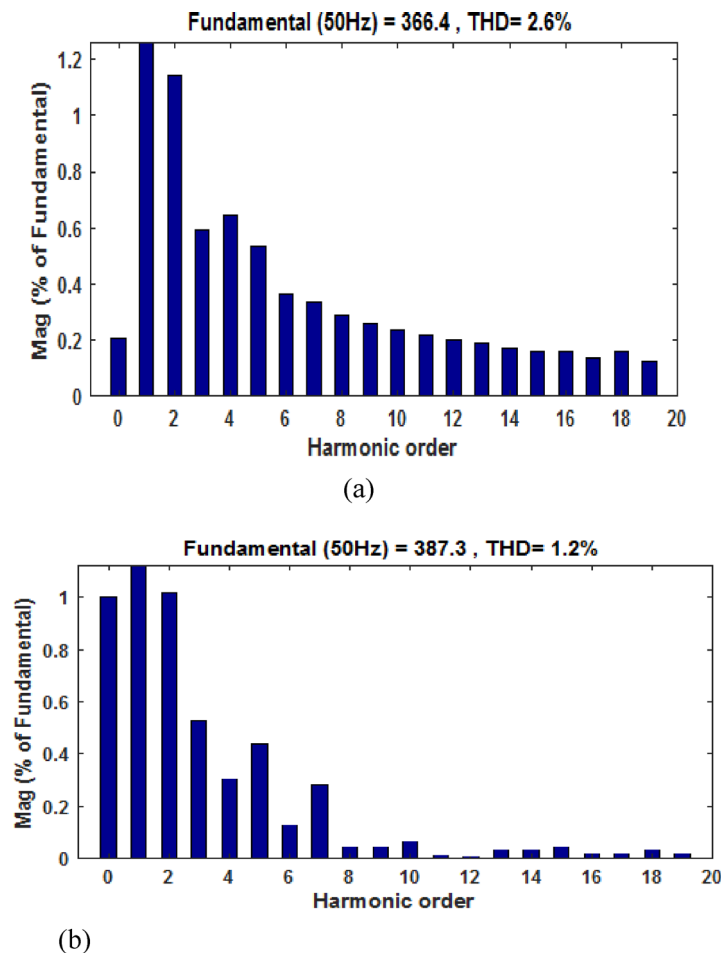
Fig. 11. Simulated output line voltage THD of QZSDMC for (**a**) CBPWM (**b**) ISVPWM.

The experimental validation method is shown in a flowchart in Fig. 19. A power quality analyser is used to measure the output parameters. The shoot-through pulse generation is a critical part of the QZSDMC control scheme, as it directly influences the converter's voltage gain and system efficiency. The FPGA is used to synchronize the shoot-through pulses with the main switching signals. This synchronization is achieved by modulating the shoot-through time within the switching period to regulate the duty cycle.

A timing diagram depicting the main switching signals (S1, S2, S3) along with the shoot-through pulse (ST) is shown below. The shoot-through pulses are inserted into the modulation scheme during the zero states of the switching period to avoid overlap with the active states, thereby boosting the voltage gain without compromising system stability. The clock frequency for the FPGA-based pulse generation is set to 100 MHz, ensuring high precision and minimal jitter in the timing control.

The synchronization of the shoot-through pulse with the main switching signals is achieved using a 50% duty cycle for the shoot-through period within each switching cycle. This ensures a balanced voltage boost without causing excessive current stress or harmonics.

The clock precision for the FPGA is maintained within 10 ns, ensuring that the timing control for shoot-through pulses is highly accurate and synchronized with the PWM signal.

The logic diagram illustrating shoot-through pulse generation and synchronization with the main switching signals has been given in Fig. 20. Figures 21 and 22 represent the phase voltage, line voltage, and load current of QZSIMC and QZSDMC respectively.

The experimental phase voltage at the output of QZSDMC under the ISVPWM scheme is shown in Fig. 23. The recommended QZSDMC produces an output phase voltage of 239 V at 50 Hz. The line voltage at the output from experimental set up under ISVPWM scheme is shown in Fig. 24. The experimental line voltage obtained from the QZSDMC is 415.1 V. The experimental output current waveform for all the three phases are revealed in Fig. 25. The magnitude of the output load current is 0.55 A for a load of 0.25 kW. It is apparent that the simulation outputs can be authorized with the investigational results. The shoot through insertion in ISVPWM technique is complex, but it has lesser switching stress and improved voltage transfer ratio.

The output voltage and current THD of ISVPWM for a load of 0.25 kW is shown in Figs. 26 and 27. The voltage and current THD at the output is almost 4.3% and 2.4%. Thus, from the investigation it can be resolved that the ISVPWM based QZSDMC produces less THD and so, switching losses will be decreased which rises the efficiency of the system. To address the concern about the quantitative comparison with previous publications
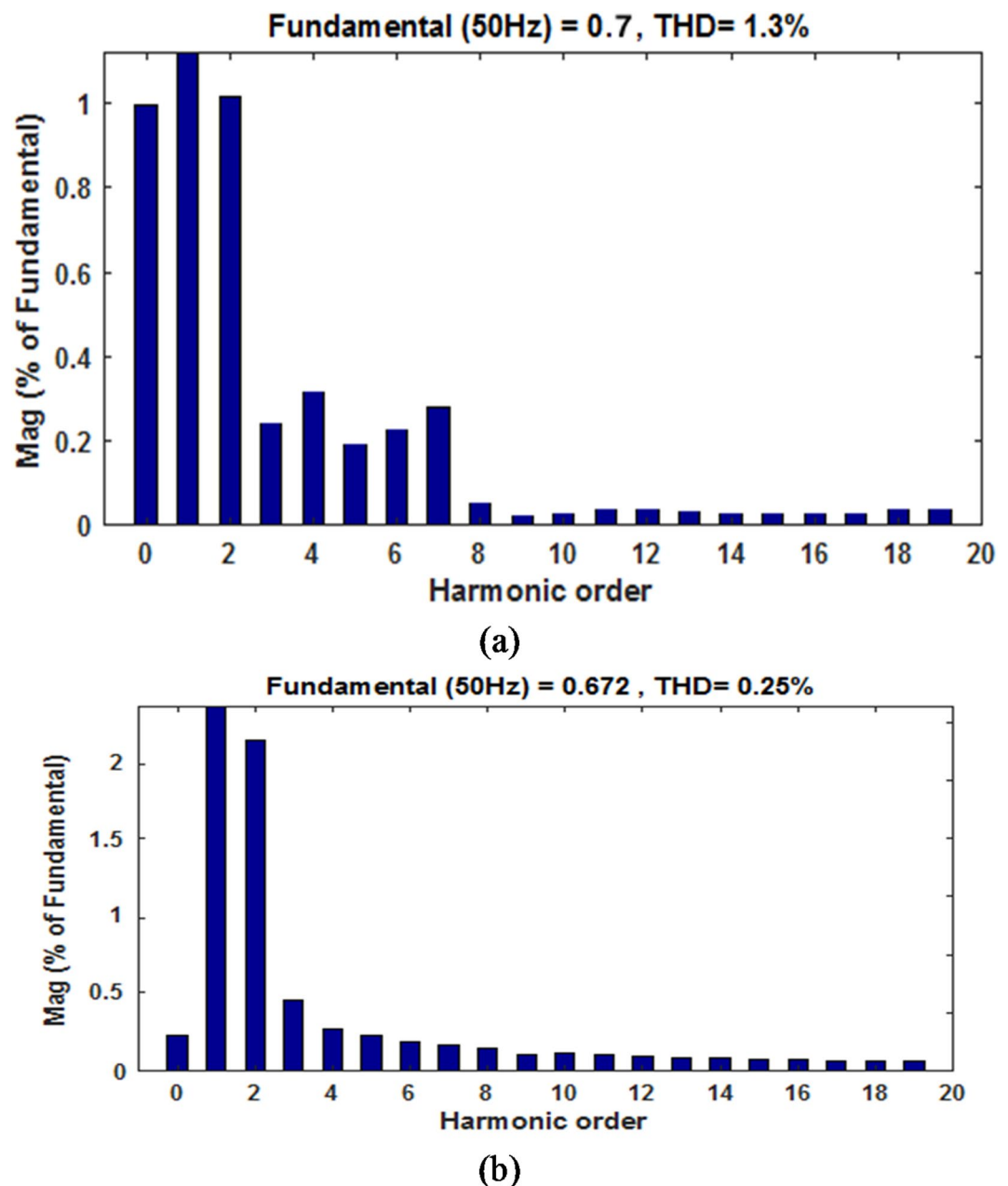
Fig. 12. Simulated output current THD of QZSDMC for (**a**) CBPWM (**b**) ISVPWM.

in terms of key performance metrics, a comparative table that summarizes the performance of the proposed QZSDMC against recent works has been included. This table will focus on key parameters like Total Harmonic Distortion (THD), voltage stress, current stress, voltage gain, control method, and implementation platform. Table 1 shows the comparative performance of the proposed QZSDCM and its comparison with the five recent papers.

This comparative table will clearly show how the QZSDMC with ISVPWM (the proposed converter) outperforms the others in terms of voltage stress, current stress, voltage gain, and other parameters.

Table 2 represents the evaluation of simulation and hardware outputs of QZSDMC for a load of 0.25 kW. From the results that could be observed that the error percentage is very minimal for the line voltage, phase voltage and current parameters at the output. Whereas the voltage and current THD of hardware result is about 3.1% and 2.05% greater than that of simulation results.

Conclusion

The circuit and working principle of a novel QZSDMC topology is examined in the paper together with comprehensive modelling, control techniques, and simulation results. In this work, an extensive analytical evaluation of QZSDMC for PMG based DDWECS has been carried out. A small signal model using state space
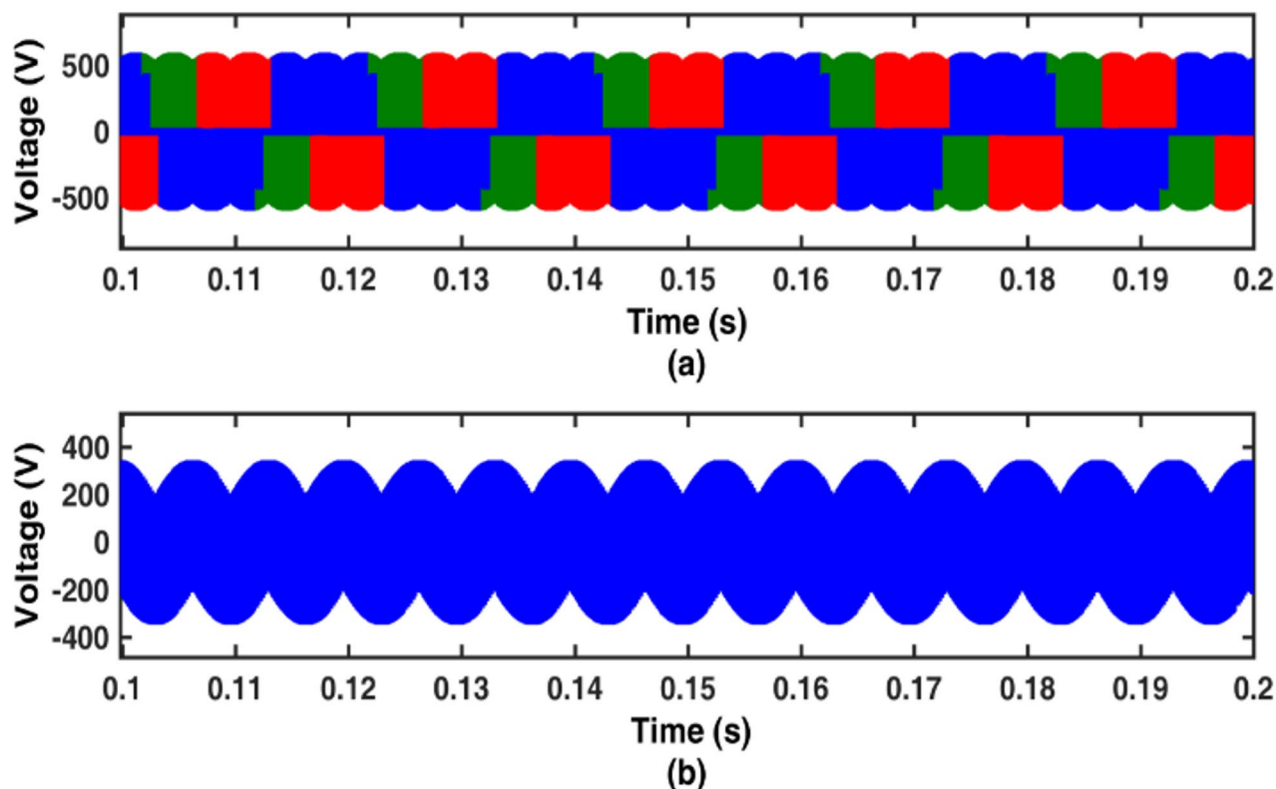
Fig. 13. Comparison of output line voltage and current THD for QZSDMC.
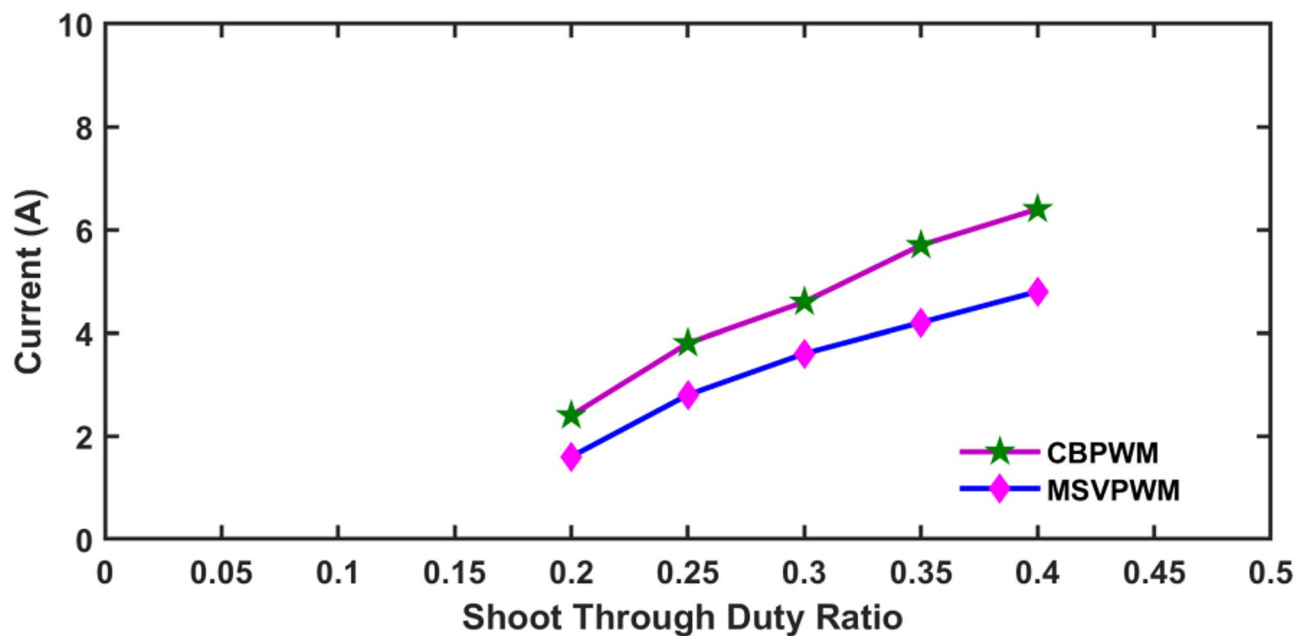
Fig. 14. Current stress versus shoot through duty ratio of QZSDMC.

domain has been derived for QZSDMC and the stability of the system was analysed which showed that the proposed QZSDM converter is stable. The performance of QZSDMC was investigated for different values of input voltages and load conditions. It is verified that the input voltage can be boosted to get the desired constant output voltage by adjusting the shoot through duty ratio between 0.4 and 0.1. The controller was designed with two different switching strategies such as CBPWM and ISVPWM for QZSDMC and its performance were
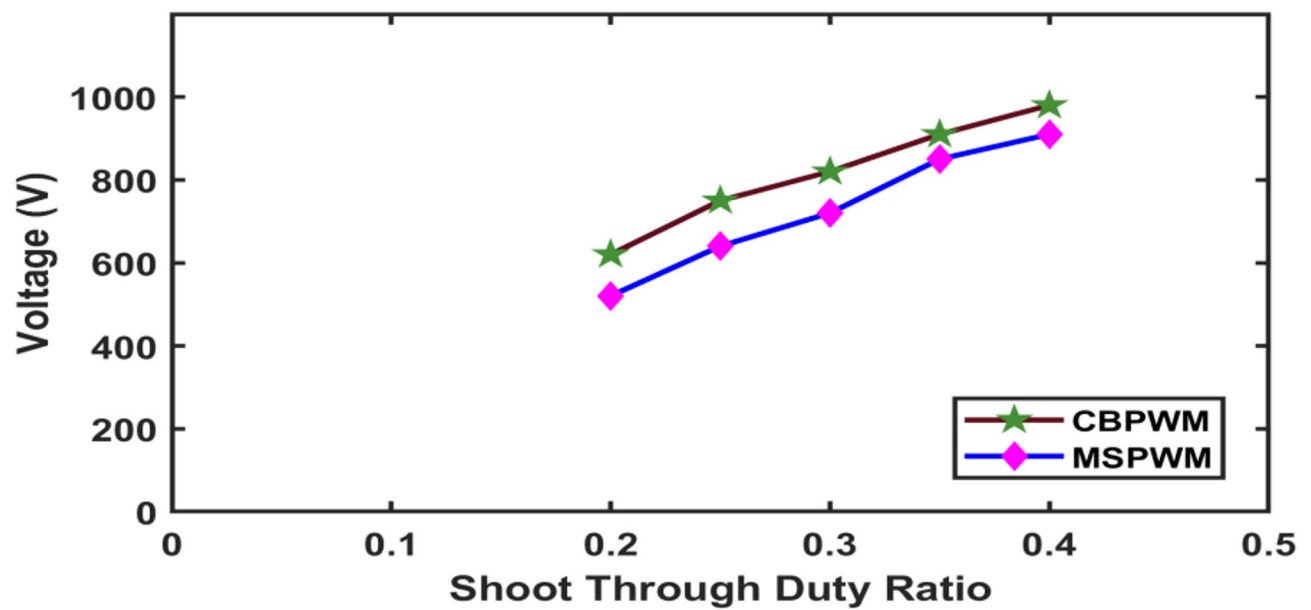
Fig. 15. Voltage Stress Versus Shoot Through duty Ratio of QZSDMC.
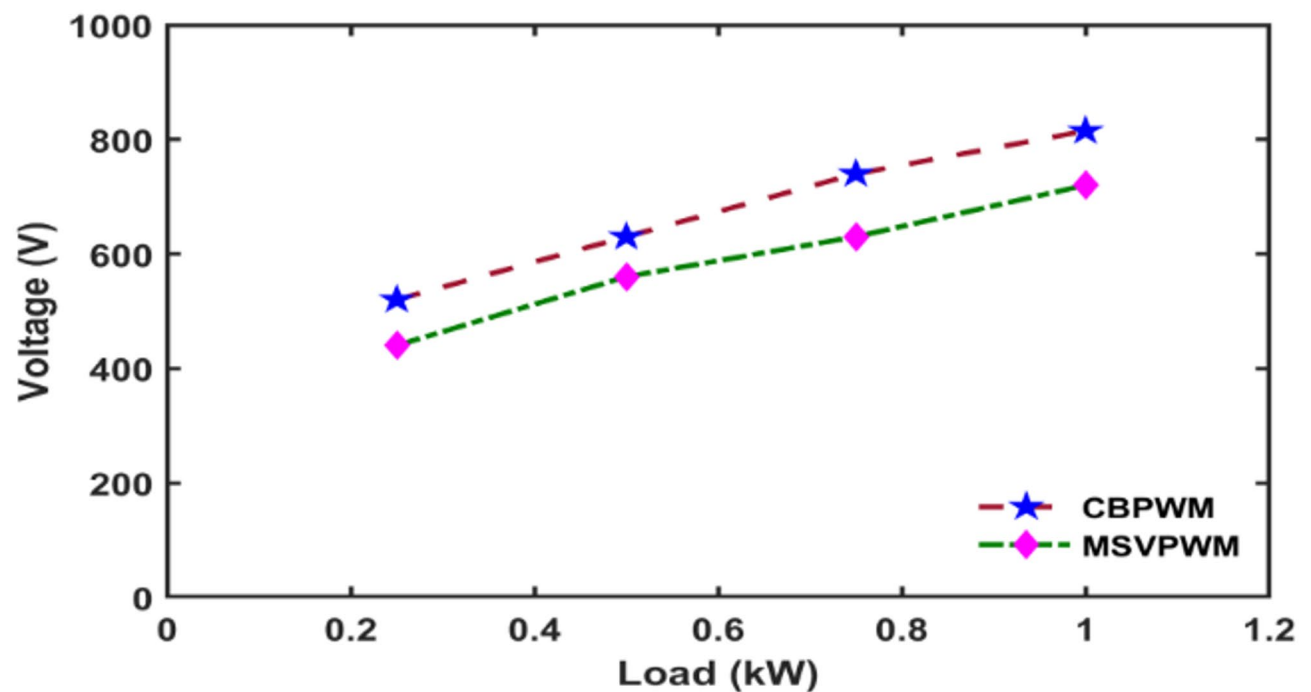
Fig. 16. Current Stress of QZSDMC at Different Loading Conditions.

compared by considering the parameters like shoot through duty ratio, output current THD, output voltage THD and switching stress. According to the analysis, the voltage stress of ISVPWM is 100 V lesser than that of the CBPWM scheme for D_0 value of 0.3. Also, an investigational prototype set up for proposed QZSDMC has been fabricated and tested. From the investigational results, it has been found that the output voltage and current THD of the simulation results are 3.1% and 2.05% higher than those of the hardware results, respectively, whereas the actual output voltage and current values are nearly identical. Therefore, it has been demonstrated that the suggested QZSDMC topology is a promising one for PMG-based WECS.
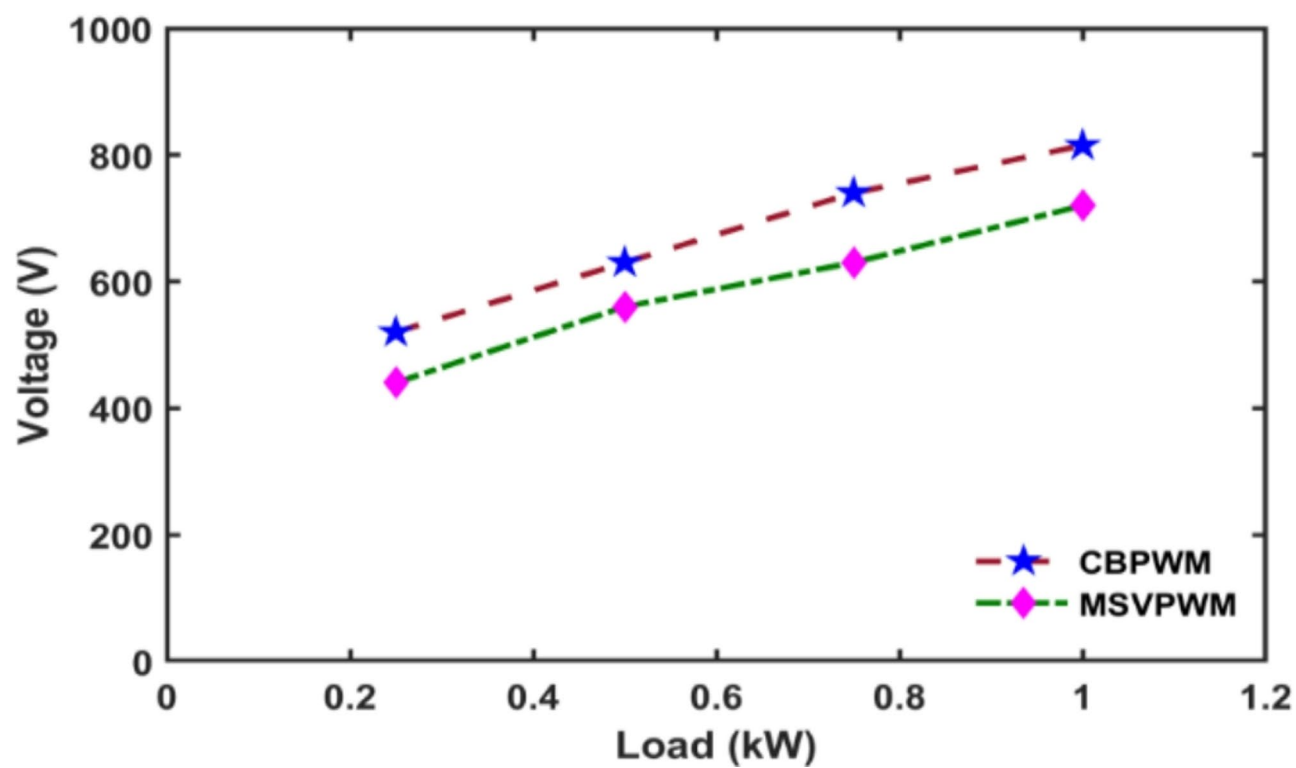
Fig. 17. Voltage Stress of QZSDMC at Different Loading Conditions.
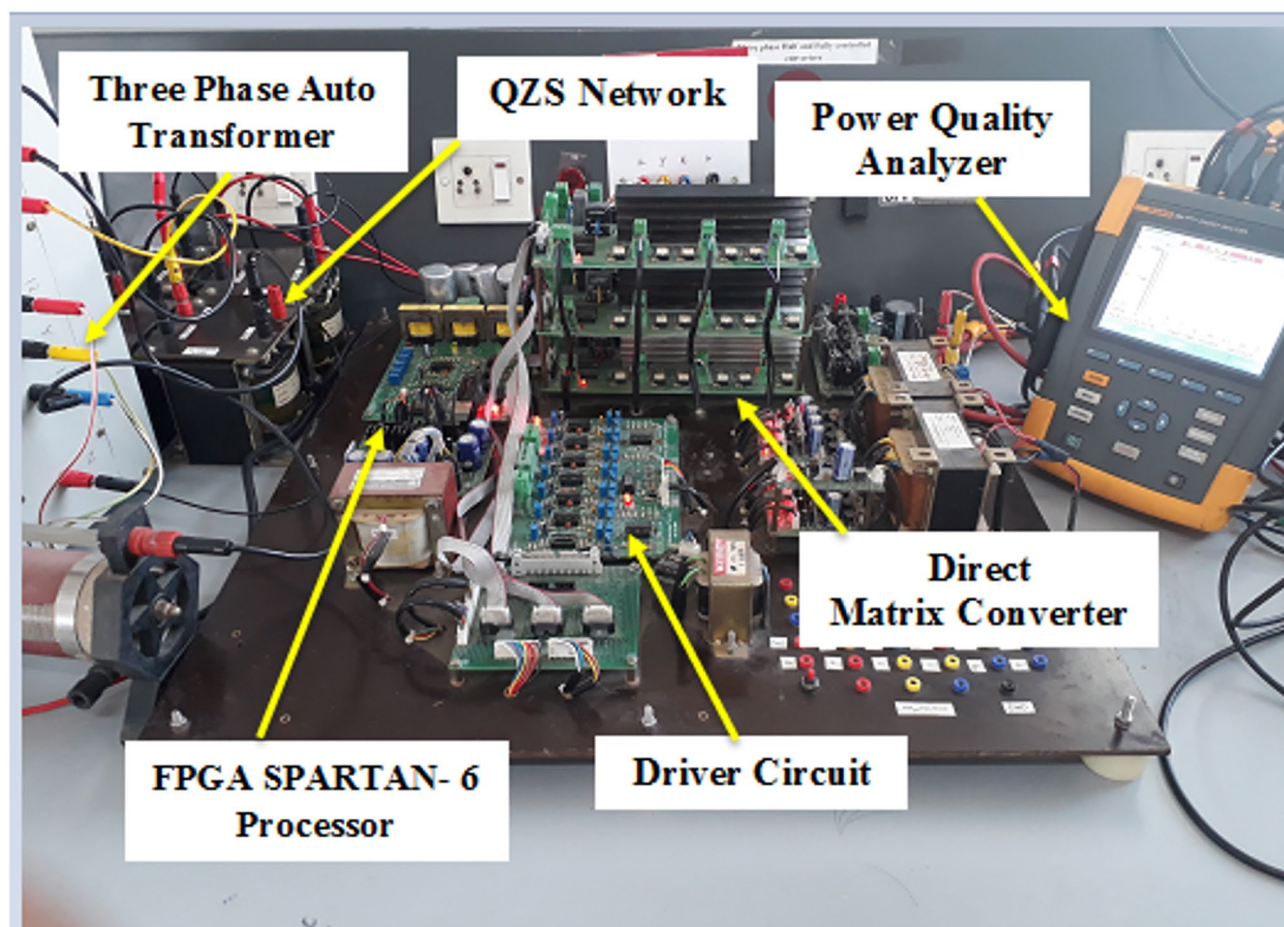
Fig. 18. Prototype experimental setup of QZSDMC.
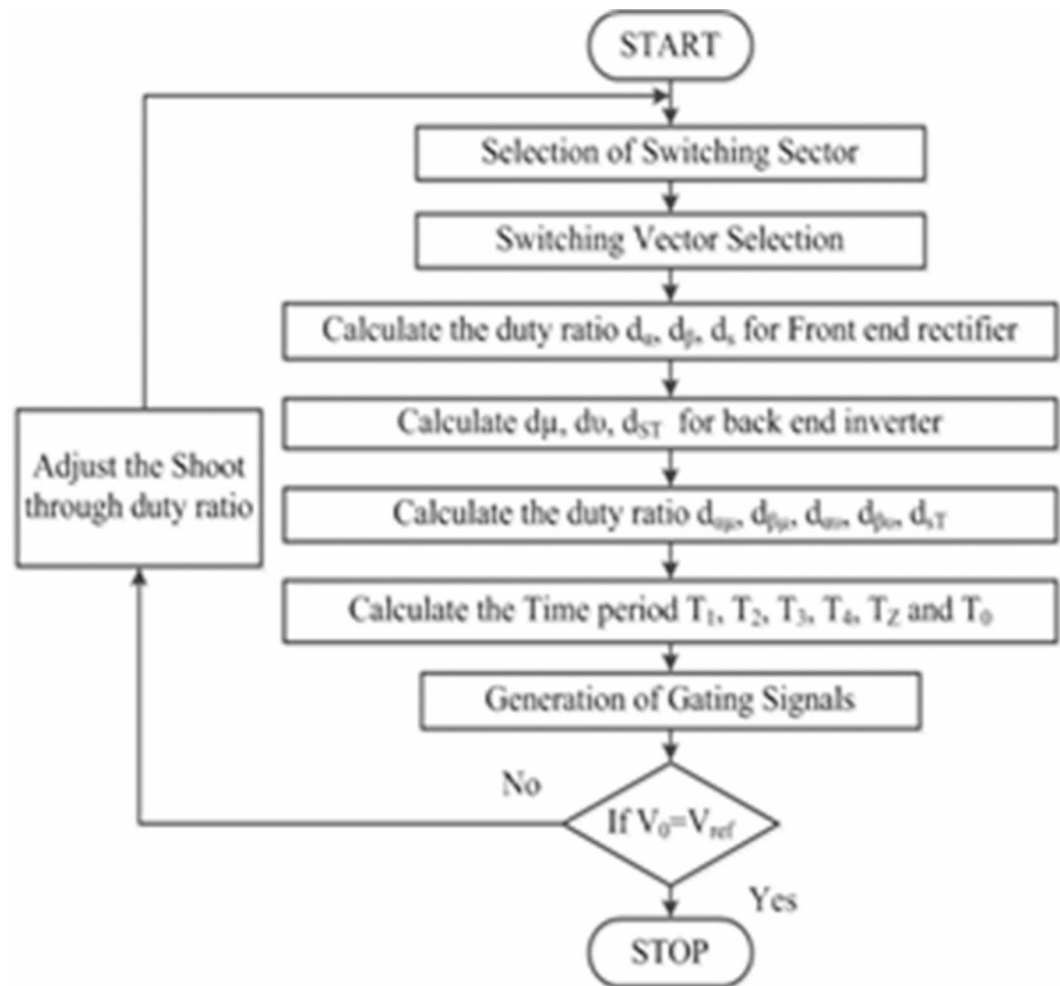
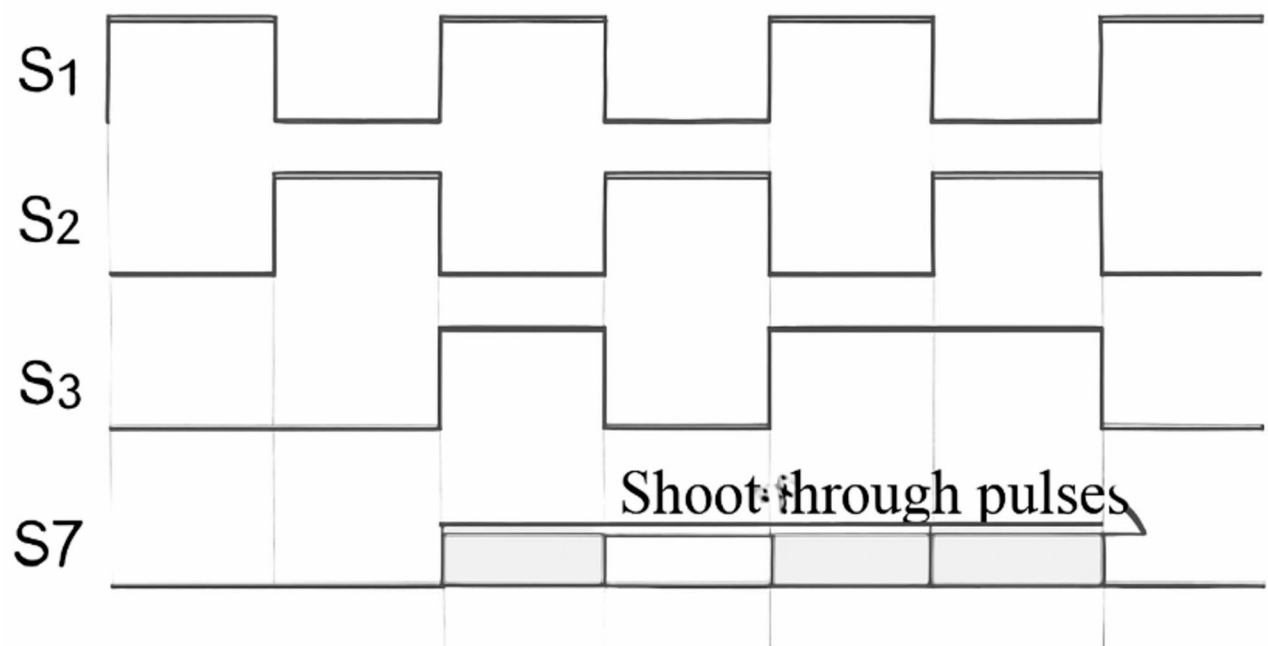**Fig. 19**. Flowchart for Experimental Validation of control scheme employed in QZSDMCs.

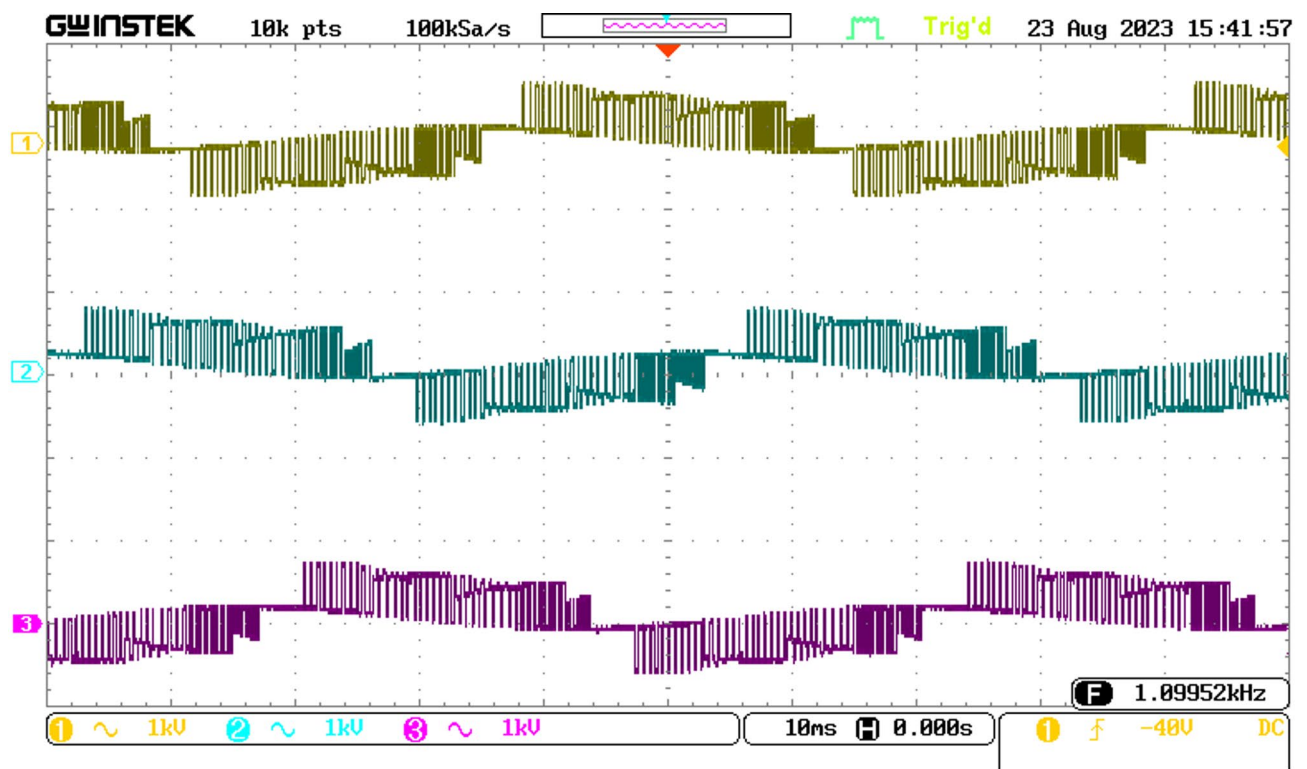**Fig. 20**. Shoot-through pulse generation and its synchronization with the main switching signals.

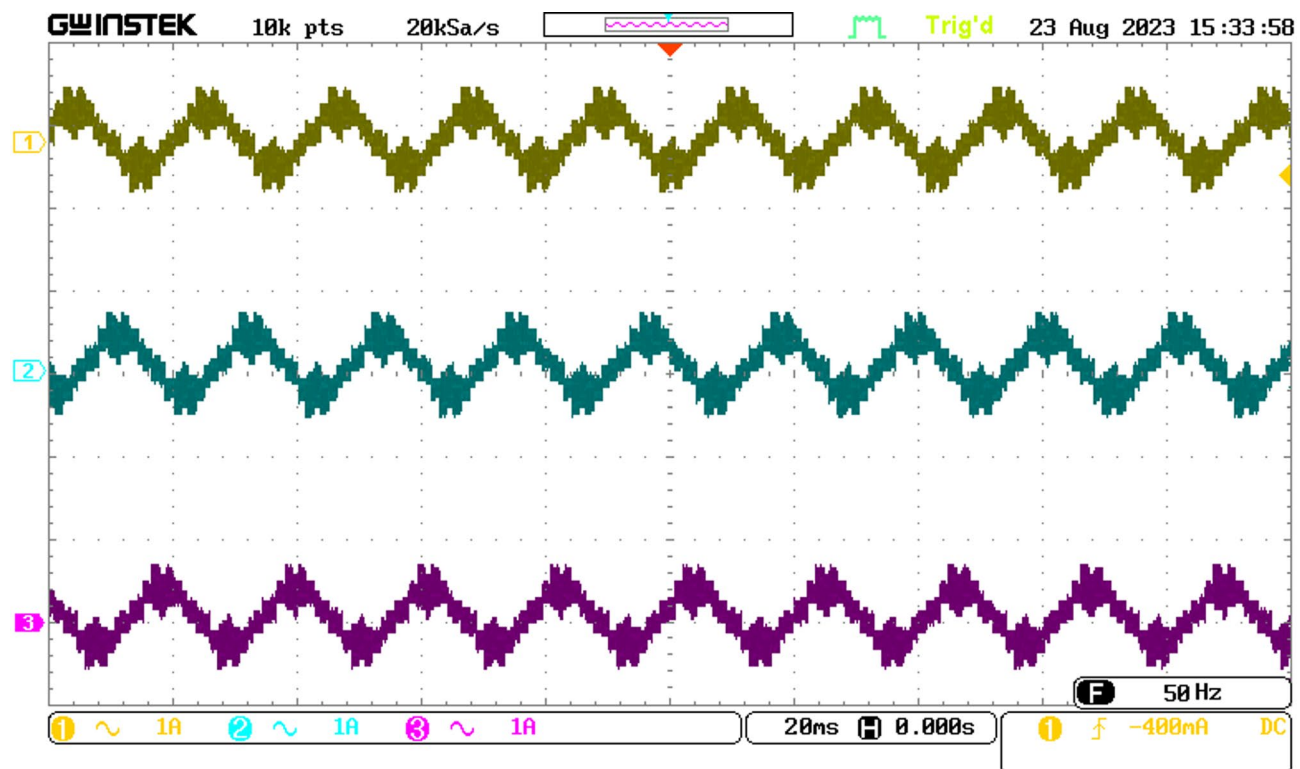**Fig. 21**. Experimental results of ISVPWM-based QZSDMC for line voltages in volts.
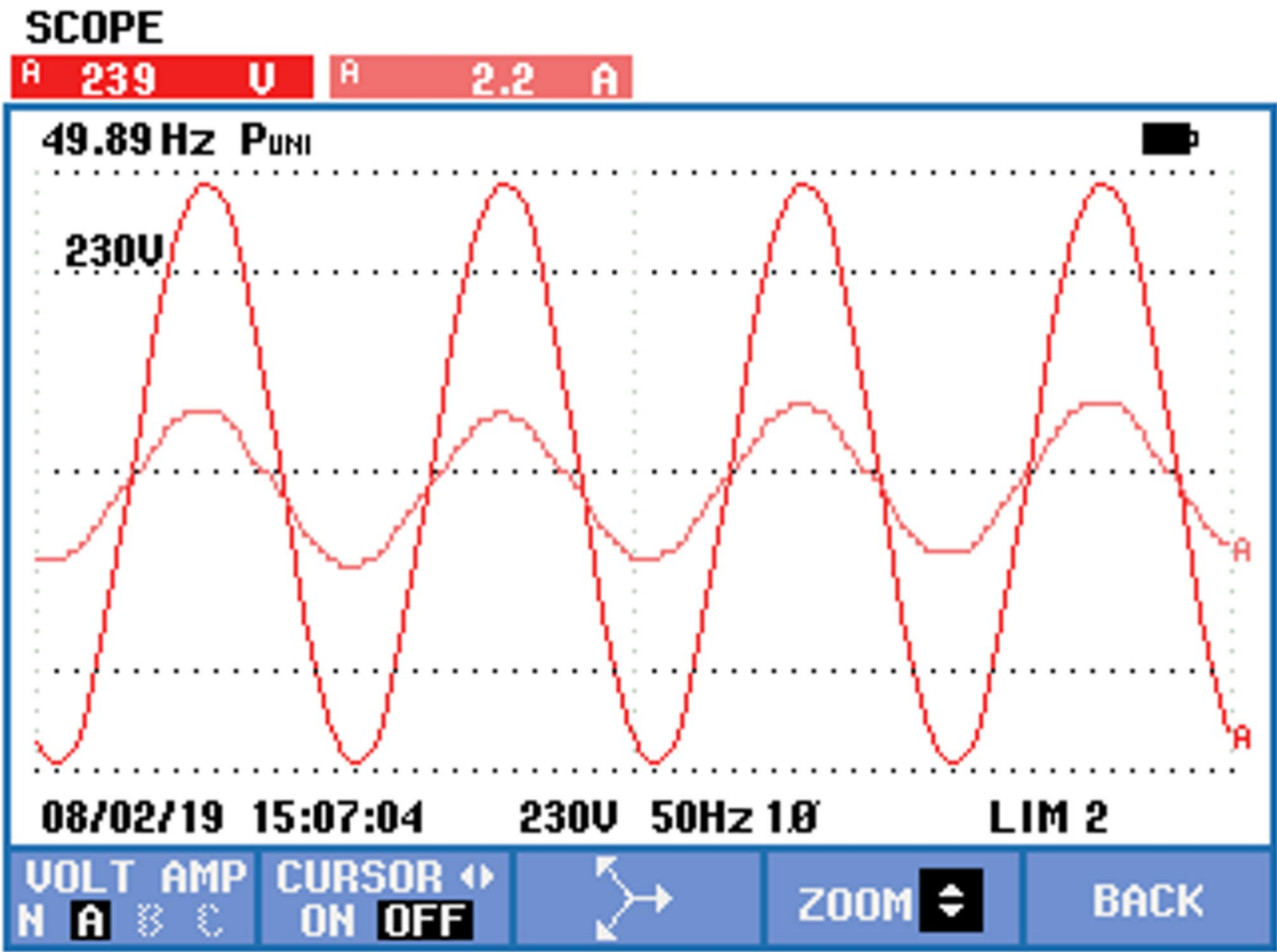
Fig. 22. Experimental results of ISVPWM-based QZSDMC for load current in Amps.
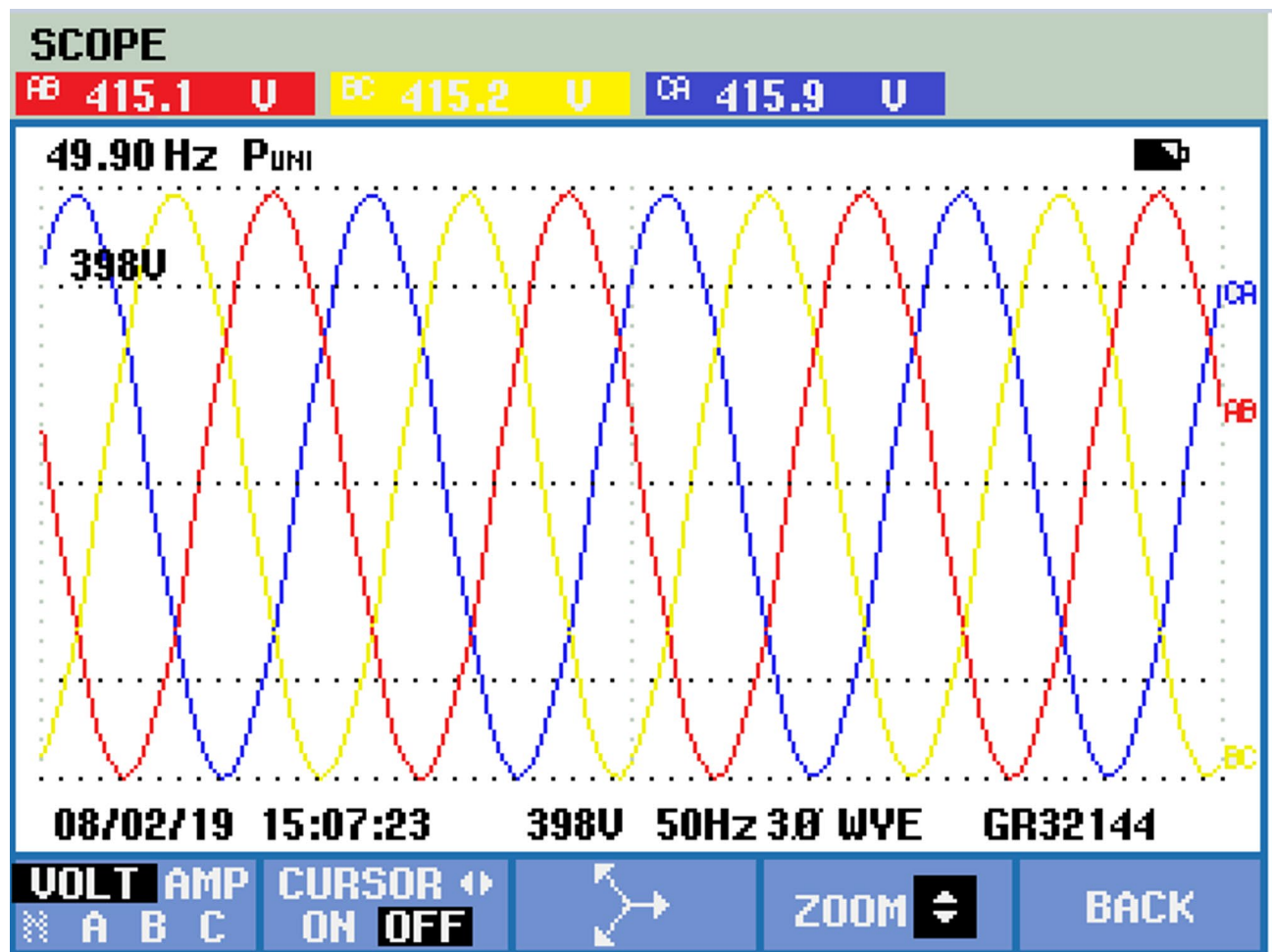
Fig. 23. Experimental phase voltage of QZSDMC.

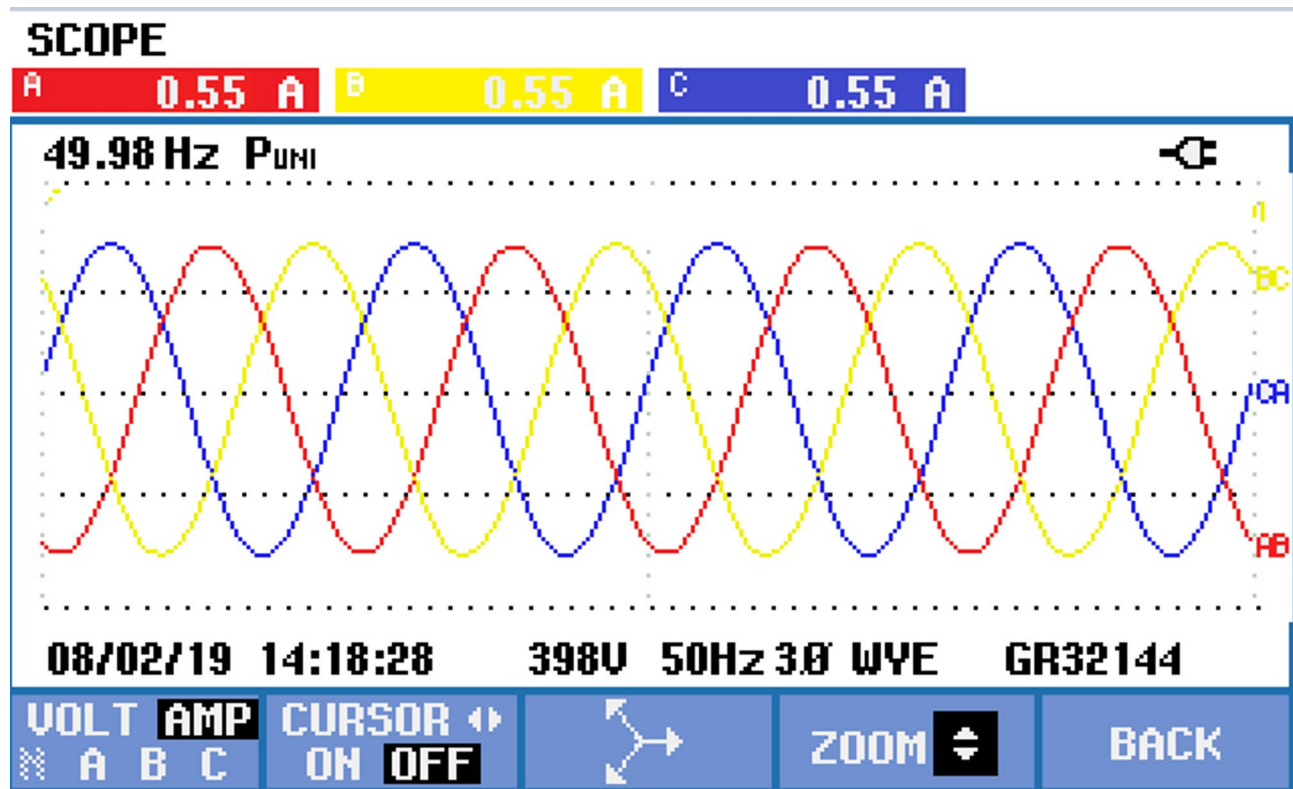**Fig. 24**. Experimental Output Line Voltage of QZSDMC.

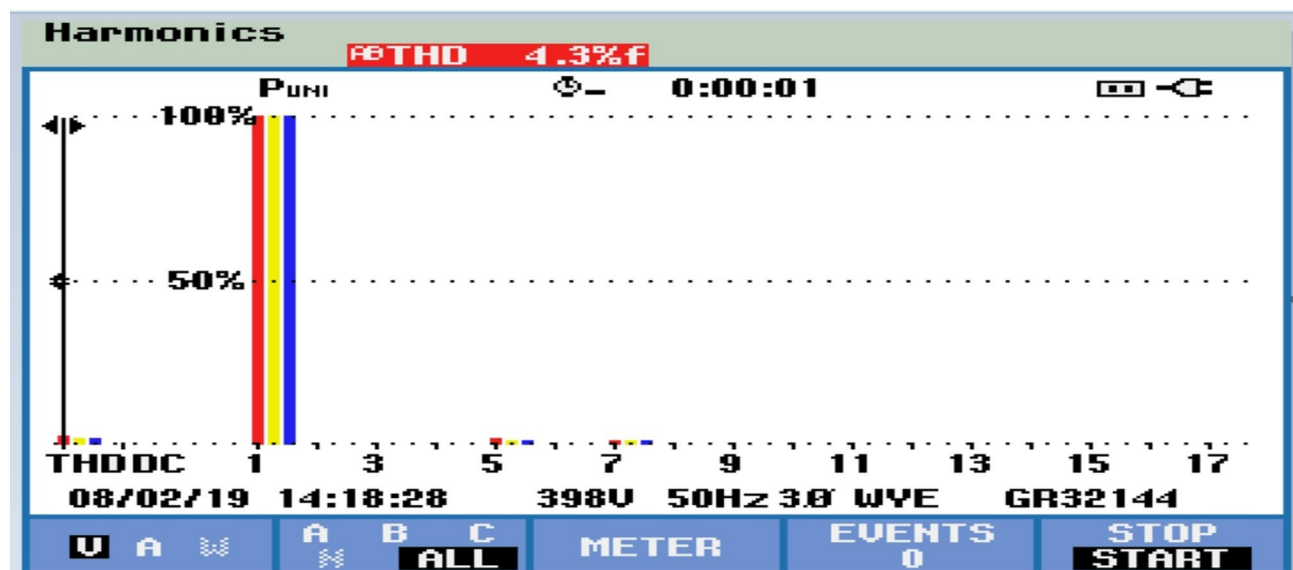**Fig. 25**. Experimental output current of QZSDMC.

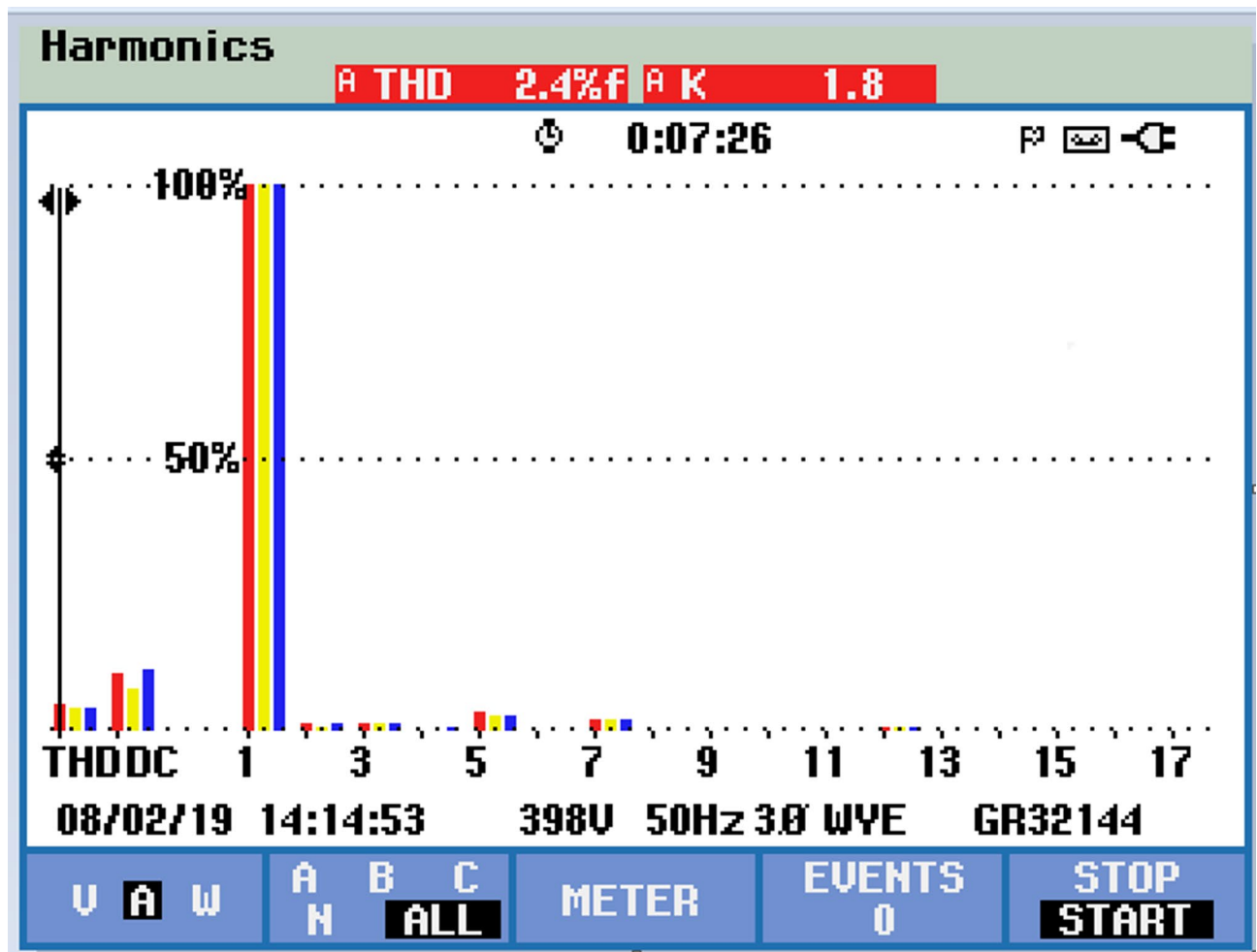
Fig. 26. Experimental output voltage THD of QZSDMC for ISVPWM.

Fig. 27. Experimental output current THD of QZSDMC ISVPWM.

References	Control Method	Voltage Gain	THD (Output Voltage)	THD (Output Current)	Voltage Stress	Current Stress	Implementation Platform
Proposed QZSDMC in this paper	ISVPWM, PI Controller	1.15	1.2%	2.4%	95 V (lower)	1 A (lower)	FPGA, MATLAB/ Simulink
K. Amei (2020)	CBPWM, PI Controller	1.1	2.6%	3.1%	130 V	2.5 A	DSP
Q. Lei (2021)	SVPWM, FOC	1.05	4.5%	4.8%	150 V	3 A	FPGA
J. Li (2022)	CBPWM, PID Controller	1.12	3.0%	2.8%	120 V	1.5 A	MCU
Y. Xu (2023)	Modified SVPWM, Fuzzy Logic	1.08	3.5%	3.0%	140 V	2 A	FPGA

Table 1. Comparative performance of the proposed QZSDMC.

Output Parameters	QZSDMC	
	Simulation results	Experimental results
Output Line voltage	415 V	415.1 V
Phase voltage	230 V	239 V
Output current	0.5 A	0.55 A
Output line Voltage THD (%)	1.2%	4.3%
Output Current THD (%)	0.25%	2.4%

Table 2. Comparison of simulation and hardware results of QZSDMC.

Data availability

The datasets used and/or analysed during the current study available from the corresponding author on reasonable request.

References

1. Amei, K., Takayasu, Y., Ohji, T. & Sakui, M. A maximum power control of wind generator system using a permanent magnet synchronous generator and a boost chopper circuit. *Proc. PCC* **3**, 1447–1452 (2002).
2. Lei, Q., Peng, F. Z. & Ge, B. Pulse-width-amplitude modulated voltage-fed quasi-Z-source direct matrix converter with maximum constant boost. *The 27th Annual IEEE Applied Power Electronics Conference and Exposition* Vol 6, 641–646 (2012).
3. Wang, Y., Meng, J., Zhang, X. & Xu, L. Control of PMSG-based wind turbines for system inertial response and power Oscillation damping. *IEEE Trans. Sustain. Energy.* **6** (2), 565–574. https://doi.org/10.1109/TSTE.2015.2394363 (2015).
4. Li, J., Keqing, Q., Song, X. & Chen Guo, C. Study on control methods of direct drive wind generation system based on three phase Z-source inverter. *IEEE Int. Conf. Power Electronics Motion Control* 644–649 (2009).
5. Rodriguez, J., Bernet, S., Steimer, P. K. & Lizama, I. E. A survey on neutral point clamped inverters. *IEEE Trans. Ind. Electron.* **57** (7), 2219–2230. https://doi.org/10.1109/TIE.2009.2032430 (2010).
6. Yaramasu, V. & Wu, B. Predictive control of three-level boost converter and NPC inverter for high power PMSG-based medium voltage wind energy conversion systems. *IEEE Trans. Power Electron.* **29** (10), 5308–5322. https://doi.org/10.1109/TPEL.2013.2292068 (2014).
7. Xu, Y. et al. The modular Current-Fed High-Frequency isolated matrix converters for wind energy conversion. *IEEE Trans. Power Electron.* **37** (4), 4779–4791. https://doi.org/10.1109/TPEL.2021.3123204 (2022).
8. Sofiane, O., Hatem, G. & Tahar, B. Robust control of an associated PMSG-Matrix converter wind plant. *2019 1st International Conference on Sustainable Renewable Energy Systems and Applications (ICSRESA)* 1–5. https://doi.org/10.1109/ICSRESA49121.2019.9182479 (2019).
9. Hojabri, H., Mokhtari, H. & Chang, L. Reactive power control of permanent magnet synchronous wind generator with matrix converter. *IEEE Trans. Power Deliv.* **28** (2), 575–584. https://doi.org/10.1109/TPWRD.2012.2229721 (2013).
10. Xu, Y., Wang, Z., Zou, Z., Buticchi, G. & Liserre, M. Voltage-fed isolated matrix-type AC/DC converter for wind energy conversion system. *IEEE Trans. Ind. Electron.* **69**(12), 13056–13068. https://doi.org/10.1109/TIE.2022.3140524 (2022).
11. Siwek, P. & Urbanski, K. Improvement of the torque control dynamics of the PMSM drive using the foc-controlled simple boost QZSDMC converter. *2018 23rd International Conference on Methods & Models in Automation & Robotics (MMAR)* 29–34. https://doi.org/10.1109/MMAR.2018.8486123 (2018).
12. Rodriguez, J., Rivera, M., Kolar, J. W. & Wheeler, P. W. A review of control and modulation methods for matrix converters. *IEEE Trans. Ind. Electron.* **59** (1), 58–70. https://doi.org/10.1109/TIE.2011.2165310 (2012).
13. Kim, S., Sul, S. & Lipo, T. A. AC/AC power conversion based on matrix converter topology with unidirectional switches. *IEEE Trans. Ind. Appl.* **36** (1), 139–145. https://doi.org/10.1109/28.821808 (2000).
14. Wheeler, P. W., Rodriguez, J., Clare, J. C., Empringham, L. & Weinstein, A. Matrix converters; a technology review. *IEEE Trans. Ind. Electron.* **49** (2), 276–288. https://doi.org/10.1109/41.993260 (2002).
15. Jung, G., Cho, Gyu, H. & Cho Soft-switched matrix converter for high frequency direct AC-to-AC power conversion. *Int. J. Electron. Vol* **72**, 4, 669–680 (2013) .
16. Zahra, M., Mohammad, J., Dan, X. & Jianguo, Z. Analysis of direct matrix converter operation under various switching patterns. *IEEE Conference on Power Electronics and Drives Systems (PEDS)* 630–634 (2015).
17. Bharani Kumar Ramasamy, K. T. M. Single stage power conversion for wind energy system using Ac-ac matrix converter. *J. Electr. Eng.* **17**(4), 1–7 (2017).
18. Kandavel, B., Uvaraj, G., Manikandan, M. & Gobi, R. Comparative study of total harmonic distortion in VSI and matrix converter based WECS. *Fourth International Conference on Advances in Electrical, Electronics, Information, Communication and Bio-Informatics (AEEICB)* 1–5. https://doi.org/10.1109/AEEICB.2018.8481002 (2018).
19. Maheswari, K. T., Bharanikumar, R. & Bhuvaneswari, S. A review on matrix converter topologies for adjustable speed drives. *Int. J. Innov. Technol. Explor. Eng.* **8**(5), 53–57 (2019).
20. Trentin et al. Experimental efficiency comparison between a direct matrix converter and an indirect matrix converter using both Si IGBTs and SiC mosfets. *IEEE Trans. Ind. Appl.* **52** (5), 4135–4145 (2016).
21. Park, K., Jou, S. T. & Lee, K. B. Z-source matrix converter with unity voltage transfer ratio. *Proc. 35th IEEE IECON* 4523–4528 (2009).
22. Fang, X., Li, C., Chen, Z., Liu, J. & Zhao, X. Three-phase voltage-fed Z-source matrix converter. *Proc. Int. Conf. Electr. Mach. Syst.* 1–4 (2011).
23. Huang, Z., Deng, W., Guo, Y. & Ju, X. Series Z-source dual output two-stage matrix converter with its modulation strategy. *Proc. CSEE* **24**, 6489–6498 (2015).
24. Palma, L. & Quasi, A. Z -Source Matrix Micro inverter for Grid Connected PV Applications. *International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)* 526–531 (2020). https://doi.org/10.1109/SPEEDAM48782.2020.9161972
25. Ramasamy, B. K., Palaniappan, A. & Mohamed Yakoh, S. Direct-drive low-speed wind energy conversion system incorporating axial-type permanent magnet generator and Z-source inverter with sensorless maximum power point tracking controller. *IET Renew. Power Gener.* **7** (3), 284–295. https://doi.org/10.1049/iet-rpg.2012.0248 (2013).
26. Guo, Y. & Dai, F. Current predictive control of Quasi-Z source three-phase four-leg direct matrix converter. *18th International Conference on AC and DC Power Transmission (ACDC 2022), Online Conference* 994–1001. https://doi.org/10.1049/icp.2022.1326 (2022).
27. Jussila, M. & Tuusa, H. Comparison of direct and indirect matrix converters in induction motor drive. *Proc. 32nd Annu. Conf. IEEE Ind. Electron* 1621–1626 (2006).
28. Zou, B., Guo, Y., Deng, W. & Wang, Z. A new quasi Z-source network applied to direct matrix converter. *The 16th IET International Conference on AC and DC Power Transmission (ACDC 2020), Online Conference* 570–576. https://doi.org/10.1049/icp.2020.0214 (2020).
29. Wang, Z., Guo, Y., Guo, Y., Deng, W. & Wang, X. Study of quasi Z-source direct matrix converter based on new strategy of dual space vector modulation. *IECON 2017–43rd Annual Conference of the IEEE Industrial Electronics Society* 1592–1597. https://doi.org/10.1109/IECON.2017.8216270 (2017).
30. Ellabban, O. & Abu-Rub, H. Grid connected quasi-Z-source direct matrix converter. *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.* 798–803 (2013).
31. Ellabban, O., Abu-Rub, H. & Baoming, G. Field oriented control of an induction motor fey by a quasi-Z-source direct matrix converter. *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.* 4850–4855 (2013).

32. Ellabban, O., Abu-Rub, H. & Baoming, G. A quasi-Z-source direct matrix converter feeding a vector controlled induction motor drive. *IEEE J. Emerg. Select. Topics Power Electron.* **03**(2), 339–348 (2015).
33. Ellabban, O., Abu-Rub, H. & Bayhan, S. Z-source matrix converter: an overview. *IEEE Trans. Power Electron.* **31** (11), 7436–7450 (2016).
34. Vidhya, D. S. & Venkatesan, T. Quasi Z source indirect matrix converter fed induction motor drive for flow control of dye in paper mill. *IEEE Trans. Power Electron.* **33** (2), 1476–1486 (2018).
35. Ge, B., Lei, Q., Qian, W. & Peng, F. Z. A family of Z-source matrix converters. *IEEE Trans. Ind. Electron.* **59** (1), 35–46. https://doi.org/10.1109/TIE.2011.2160512 (2012).
36. Liu, S. et al. Modeling, analysis, and parameters design of LC-filter-integrated quasi-Z-source indirect matrix converter. *IEEE Trans. Power Electron.* **31** (11), 7544–7555. https://doi.org/10.1109/TPEL.2016.2553582 (Nov. 2016).
37. Andreu, J. et al. FPGA solution for matrix converter double sided space vector modulation algorithm. *Int. J. Electron.* **95** (11), 1181–1200 (2008).
38. Mojtaba, A. & Shokrollah, S. K. Modelling, control, and stability analysis of quasi-Z-source matrix converter as the grid interface of a PMSG-WECS. *IET Gener. Transm. Distrib.* **11**(14), 3576–3585 (2017).
39. Thangavel, M. K., Ramasamy, B. K. & Ponnusamy, P. Performance analysis of dual space vector modulation technique-based quasi Z-Source direct matrix converter. *Electr. Power Compon. Syst. Vo* **48**(11), 1185–1196 (2020).
40. Bharanikumar, R., Kumar, A. N. & Maheswari, K. T. Novel MPPT controller for wind turbine driven permanent magnet generator with power converters. *Int. Rev. Electr. Eng.* **5** (4),2010
41. Bharanikumar, R., Nirmalkumar, A. & Maheswari, K. T. Modelling and simulation of wind turbine driven axial type permanent magnet generator with Z-source inverter. *Aust. J. Electr. Electron. Eng.* **9** (1), 27–42 (2010).
42. Adak, S. Harmonics mitigation of Stand-Alone photovoltaic system using LC passive filter. *J. Electr. Eng. Technol.* **16**, 2389–2396 (2021).
43. Frede Blaabjerg, M. KeMa,'Power electronics converters for wind turbine systems'. *IEEE Trans. Ind. Appl.* **48** (2), 708–719 (2012).
44. Li, J., Liu, J. & Zeng, L. Comparison of Z-source inverter and traditional two stage boost-buck inverter in grid-tied renewable energy generation. *IEEE Conference* 1493–1497 (2009).
45. Peng, F. Z. & Inverter', Z. S. *IEEE Trans. Ind. Appl.*, **39**, 2, 504–510. (2003).
46. Upma, S. & Rizwan, M. Analysis of wind turbine dataset and machine learning based forecasting in SCADA-system. *J. Ambient Intell. Humaniz. Comput.* **14**, 8035–8044 (2023).
47. Shweta, S., & Liu, X. Ensemble approach for short term load forecasting in wind energy system using hybrid algorithm. *J. Ambient Intell. Humaniz. Comput.* **11**, 5297–5314 (2020).
48. Roy, S. S. et al. Forecasting heating and cooling loads of buildings: a comparative performance analysis. *J. Ambient Intell. Humaniz. Comput.* **11**, 1253–1264 (2020).
49. Xia, S., Song, D. & Wang, D. A short-term power load forecasting method based on k-means and SVM. *J. Ambient Intell. Humaniz. Comput.* **13**, 5253–5267 (2022).
50. Aksu, I. O. & Coban, R. Sliding mode PI control with back stepping approach for MIMO nonlinear cross-coupled tank systems. *Int. J. Robust. Nonlinear Control.* **29**, 1854–1871. https://doi.org/10.1002/rnc.4469 (2019).
51. Aksu, I. O. & Coban, R. Second order sliding mode control of MIMO nonlinear coupled tank system, *14th International Conference on Advanced Trends in Radioelectronics, Telecommunications and Computer Engineering (TCSET)* 826–830. https://doi.org/10.1109/TCSET.2018.8336325 (2018).

Author contributions

K.T.Maheswari - Conceptualization, Methodology, Software, Resources, Validation, Visualization, Project Administration, and Writing-original draft. C.Kumar - Supervision, Writing-review and editing. T.Dharma Raj - Conceptualization, Methodology, Software, Data curation, Writing-review and editing. Hady H. Fayek - Conceptualization, Methodology, Funding, Data curation, Writing-review and editing.

Declarations

Competing interests

The authors declare no competing interests.

Additional information

Correspondence and requests for materials should be addressed to H.H.F.

Reprints and permissions information is available at www.nature.com/reprints.

Publisher's note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.