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Engineering the ferroelectric polarization to optimize the GIDL and negative output conductance in negative capacitance FET

Vijay Sai Thota, Sandeep Moparthi✉ & Kalyanbrata Ghosh

This paper presents the optimization of the gate induced drain leakage (GIDL) and negative output conductance (NOC) effect in ferroelectric negative capacitance (NC) FET by engineering the polarization of ferroelectric. The improvement in NOC and GIDL is presented with reworked polarization and hence the channel potential at the drain side through gate workfunction modulation. An NC SOI device structure is considered in this work, as this study is intended to investigate the proposed optimization technique. With the metal length ratios of 1:1 and 1:2, the proposed structure offered an enhanced ferroelectric polarization via surface potential amplification at the drain end of the channel. The onset of NOC is delayed by 0.21 V with an improved GIDL current of 3.18 nA and a minimum subthreshold swing of 33.45 mV/decade for the metal length ratio of 1:1.

Keywords Negative differential resistance, GIDL, Negative capacitance, Ferroelectric, Industry, Innovation, Infrastructure

Ferroelectric negative capacitance (NC) FETs are promoted as a feasible option for achieving a steep subthreshold slope, enabling faster switching and low-power design[1–4]. The ferroelectric offers NC during its polarization transition. When placed in the gate stack of MOSFET, the NC can enhance the MOSFET's overall gate capacitance/control. This, in turn, results in gate voltage amplification in MOSFET[5–8]. Unlike conventional FET, NC FET offers negative drain-induced barrier lowering (N*DIBL)* besides a steep subthreshold slope. However, the *NDIBL* of NC FET manifests the negative output capacitance (*NOC*)[9,10], which can be observed in the output characteristics of the device. The *NOC* has resulted from the deterioration of ferroelectric polarization at the drain end of the device at higher drain voltages[10]. The poor gate voltage control at higher drain voltage hampers ferroelectric polarization reversal and its negative capacitance. As a result, the channel potential of NC FET dampens at the drain side when the drain voltage is higher, and hence, the drain current falls, which can be seen in the output characteristics. Though the steep switching of NC FET is desired in digital circuits, the *NOC* is not desirable for analog applications, as it de-amplifies the intrinsic gain. There are methods proposed in the literature to optimize the *NOC* in NC FET. An asymmetric source and drain parasitic capacitance approach is proposed to tune the *NOC*, which adjusts the capacitance matching between the baseline FET and ferroelectric[11]. Apart from this, the material parameters of ferroelectric, namely remnant polarization and coercive field, are tuned to optimize the *NOC* of NC FET[12]. In the literature, it is also shown that the *NOC* increases with a decrease in the ratio of remnant polarization (P_r) to the coercive field (E_c) in a ferroelectric material[12]. However, the material parameters P_r and E_c of ferroelectric (primarily doped-HfO_2 based) are greatly influenced by the fabrication process, such as annealing temperature and doping concentration.

Our group proposed reducing the *NOC* in NC Silicon nanotube FET by increasing its core gate radius[13]. This approach minimises the *NOC* by tuning the capacitance matching[13]. Though the proposed method is more suitable for gate-all-around nanowires and nanotubes, it leads to an increase in the effective radius of the channel. A gate underlap at the drain side is proposed in the literature to minimize drain dominance on the gate and, hence, the better *NOC*[14]. However, this approach increase the device length and limit the gate control over the channel. A local Gaussian heavy doping (pocket) at the top surface of the channel near the drain is proposed to improve the channel potential at the drain end[15]. In this approach, it is crucial to control the doping profile of the channel, and it also affects the carrier mobility[15]. In the literature, it is proposed to introduce a charge trapping layer between the ferroelectric and dielectric layers of the gate stack[16]. The induced trap charges near the drain side enhance the surface potential and hence the better *NOC*. However, introducing an extra trap charge layer in the gate stack influences the capacitance matching of the device[16].

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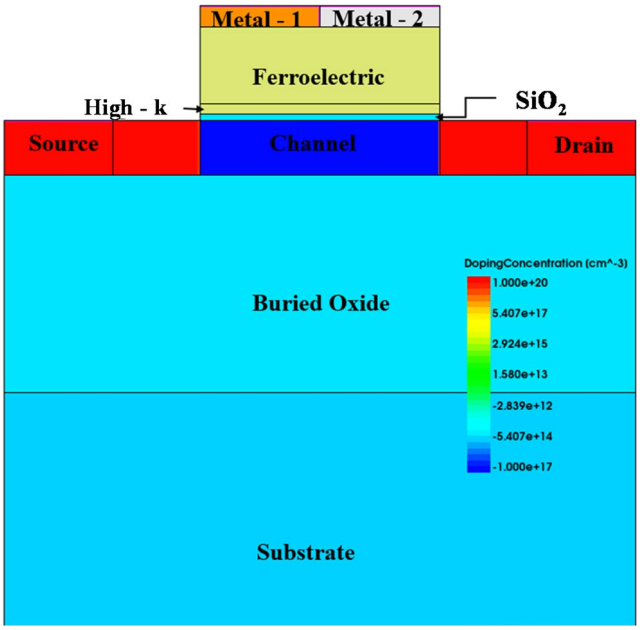

Fig. 1. Device structure of DM NC SOI FET.

Parameter	Values
Channel length (L)	22 nm
Channel doping (N_A)	10^{17} cm^{-3}
Channel thickness (t_{si})	5 nm
Gate oxide thickness (t_{SiO2})	0.9 nm
High-k dielectric thickness ($t_{high\text{-}k}$)	1.2 nm
Ferroelectric thickness (t_{fe})	7 nm
Gate-metal workfunction	Metal-1 (Φ_{M1}): 4.65 eV Metal-2 (Φ_{M2}): 4.5 eV

Table 1. Device parameters.

In addition to NOC, the NC FET exhibits a poorer GIDL than its conventional counterpart due to the steep energy band profile. The literature proposes that lightly doped source and drain regions improve the GIDL of the NC FET by altering the steep profile of the energy band diagram[17]. However, this approach deteriorates the device's drive current due to the limited carrier availability in the source[17]. A gate-drain overlap is proposed in the literature[18] to control the GIDL of NC tunnel FET with enhanced gate control. However, it requires a precise control of overlap/underlap of gate at nano scale.

The aforementioned literature mainly focused on tuning capacitance matching in NC FET to optimize the *NOC*. However, these proposals in the literature lead to more delay owing to higher parasitic capacitances. As per the studied literature, there are very limited works focused on the GIDL of NC FET which is a major contributor to the standby leakage. Moreover, it is essential to combinedly analyse and optimize the impact of GIDL and NOC on NC FET to make it more adaptable to both analog and digital applications. With these observations, this paper proposes a surface potential modulation approach through dual metal (DM) workfunction to improve the *NOC* and *GIDL* with channel potential amplification at the drain end. An SOI device structure is considered for investigation in the proposed optimization technique. The following sections of this paper explain the device structure and simulation methodology, followed by the discussion and conclusion.

Device structure and simulation methodology

A 2D NC SOI FET structure is considered in this work, as this study is intended to investigate the proposed optimization technique. The considered device structures are simulated using Sentaurus TCAD from Synopsys. The device structure and its parameters are shown in Fig. 1; Table 1, respectively. To account for the quantum confinement effects at a channel thickness of 5 nm, QuantumPotential model of Senataurus TCAD is used. The doping dependent (Philips unified), high field saturation, Enormal (Lombardi, inversion and accumulation layer), OldSlotboom, Bandgap Narrowing model, and Schenk bandgap models are used in the simulation. The ferroelectric polarization model is invoked in the ferroelectric layer. Figure 2 shows the calibration of the simulation methodology as per Fig. 1 (d) of[19]. This is based on the experimental data of [20] for SOI FET and with the ferroelectric P_r and E_c values extracted from the experimental P-E curve of [21] for NC SOI FET. The values of the ferroelectric material parameters are calculated as $\alpha = -1.1e11$ cm/F, $\beta = 2.5e21$ cm^5/FC^2 from the

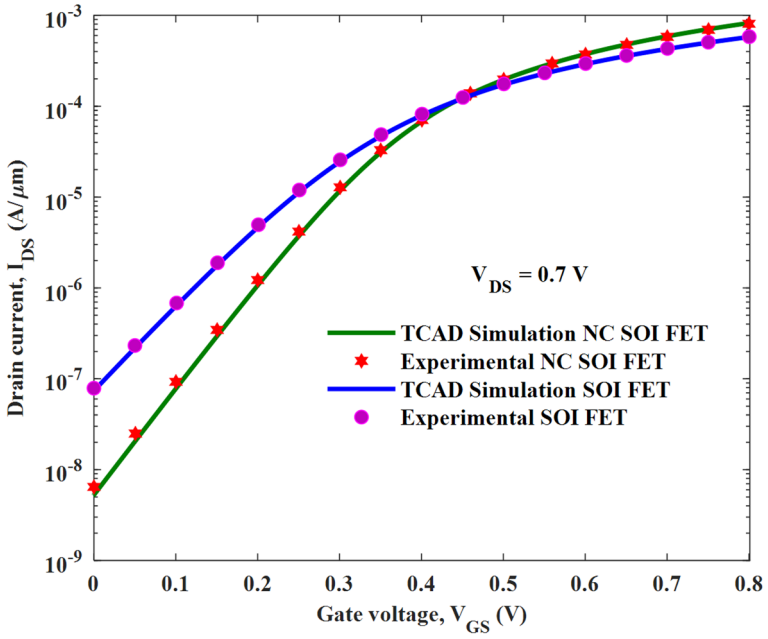

Fig. 2. Validation of TCAD simulation models for NC SOI FET.

extracted P_r and E_c values of 14.83μC/cm^2 and 1.25MV/ cm, respectively. The coupling coefficient of ferroelectric polarization gradient (g) and viscosity (ρ) are considered as 1e-4 cm^3/F and 0.18 Ω.cm, respectively.

Result analysis

The result analysis is carried out as follows. Section A presents a comparative study of the Single Metal (SM) NC SOI FET and the conventional SM SOI FET. Section B presents the NOC and GIDL optimization of the NC SOI FET with surface potential modulation.

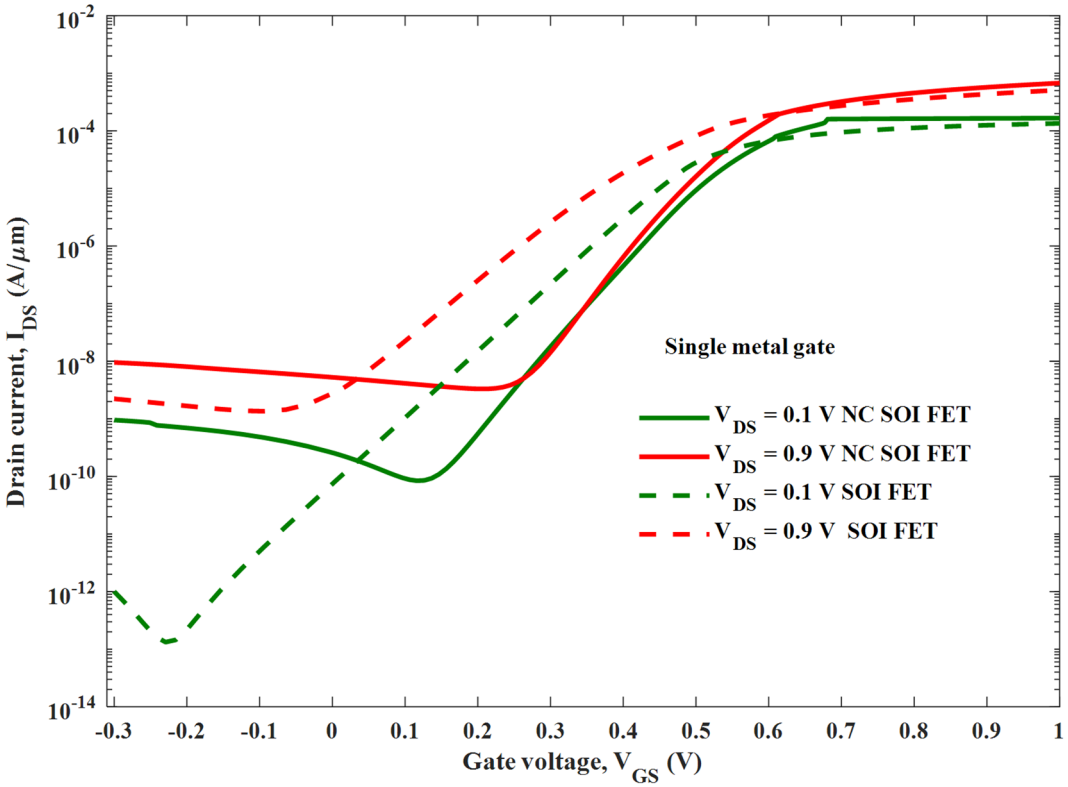

Fig. 3. Transfer characteristic of SM SOI FET and SM NC SOI FET.

	$SS_{average}$ (mV/decade) at V_{DS} of		V_{th} (V) at V_{DS} of		I_{ON} (mA) at V_{DS} of	
	0.1 V	0.9 V	0.1 V	0.9 V	0.1 V	0.9 V
SOI FET	86	96	0.433	0.413	0.13	0.50
NC SOI FET	70	79.13	0.636	0.548	0.166	0.67

Table 2. Electrical metrics comparison of SOI FET and NC SOI FET.

	SM NC SOI FET (I_{GIDL})		SM SOI FET (I_{GIDL})	
	V_{DS} = 0.1 V	V_{DS} = 0.9 V	V_{DS} = 0.1 V	V_{DS} = 0.9 V
V_{GS} = − 0.3 V	9.5e − 10 A	9.5e − 9 A	9.73e − 13 A	2.22e − 9 A
V_{GS} = 0 V	2.57e − 10 A	5.26e − 9 A	7.39e − 11 A	2.79e − 9 A

Table 3. GIDL comparison of SOI FET and NC SOI FET.

Comparative study of SM NC and conventional SOI fets

The transfer characteristics of the SM SOIFET are plotted with and without NC, as shown in Fig. 3. Electrical metrics of NC SOI FET and SOI FET are tabulated in Table 2. The analysis shows improved SS, I_{ON}, and threshold (V_{th}) voltage roll-up in NC SOI FET, which can be attributed to the negative capacitance induced by the ferroelectric. It is seen that, despite steep subthreshold slope, the SM NC SOI FET exhibited measurable leakage current due to GIDL (I_{GIDL}) compared to conventional SOI FET at V_{GS}=-0.3 V and V_{GS}=0 V for the V_{DS} of 0.1 V and 0.9 V, as shown in the Table 3.

This is due to the gate-to-drain leakage caused by the steeper energy band profile of NC FET (especially at the drain end), as shown in Fig. 4. The shift in the threshold voltage of NC SOI FET observed in Fig. 3 is analyzed along with surface potential modulation, as depicted in Fig. 7.

Moreover, the SM NC SOI FET depicted the negative output conductance (NOC), which is unlike a conventional device, as seen from the output characteristics in Fig. 5. It is worth noting that the NC SOI FET exhibited the NOC despite a very high saturation current observed in its conventional counterpart owing to the short-channel effect. The NOC in the NC SOI FET is due to dampened ferroelectric polarization at the drain

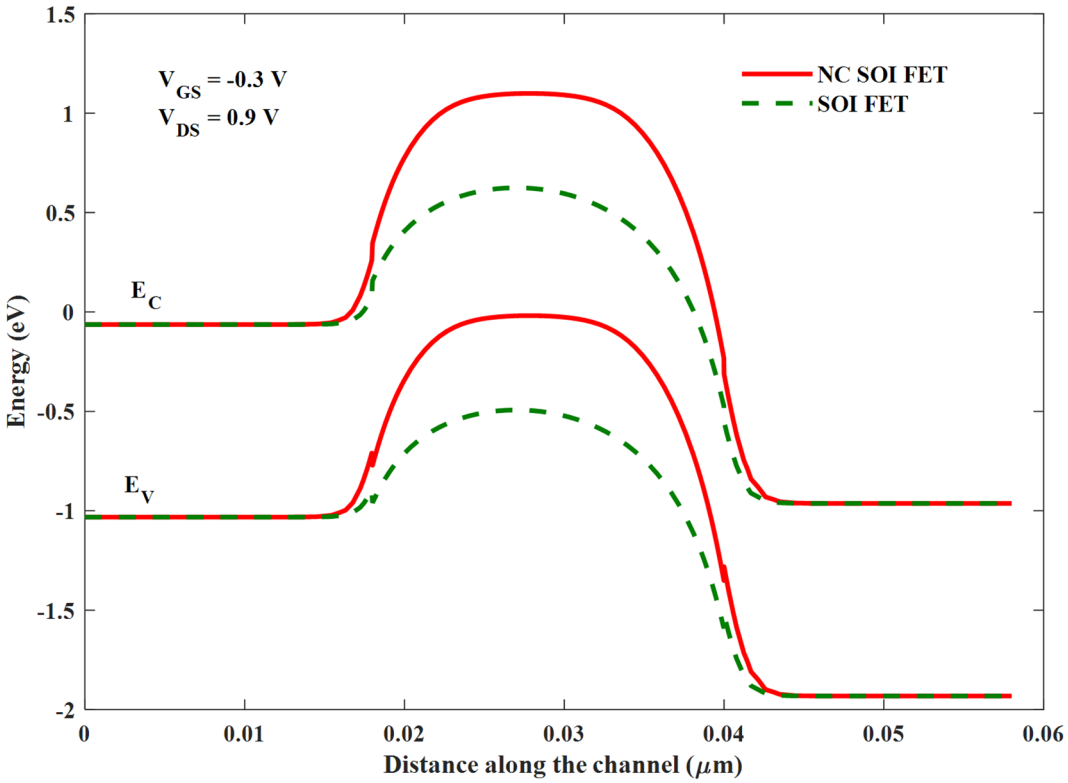

Fig. 4. Energy band profile of SM SOI FET and SM NC SOI FET.

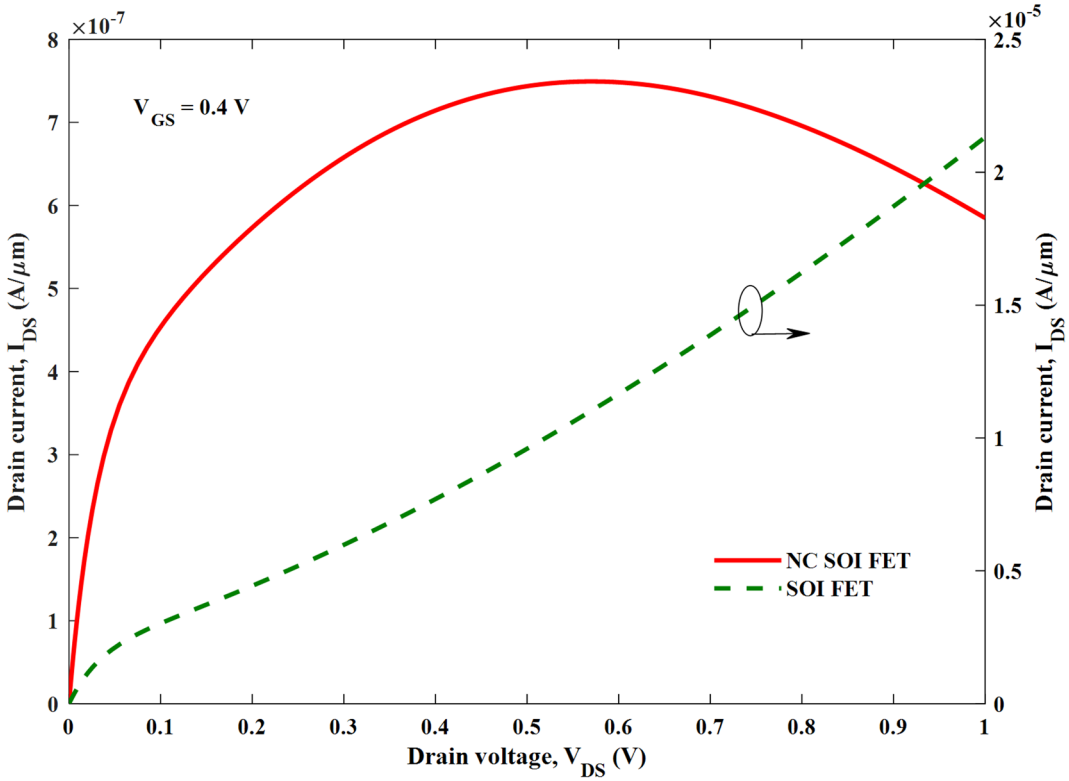

Fig. 5. Output characteristics of the SM SOI FET and NC SOI FET (NOC in NC SOI FET despite significant short channel effect in conventional SOI FET).

side, as shown in Fig. 6, owing to poor gate control at higher drain voltages. This dampened polarization of NC SOI FET resulted in the depression of the surface potential of SM NC SOI FET compared to conventional SOI FET, as shown in Fig. 7. This depressed surface potential, in turn led to the increment in the threshold voltage of NC SOI FET as shown in Fig. 3. The aforementioned rise in threshold voltage of the NC SOI FET can also be observed in Fig. 4 in terms of the height of the energy band profile. As the aforementioned results show, NC SOI FET suffers from GIDL and NOC despite improved DIBL compared to conventional SOI FET.

Optimization of NOC and GIDL in NC SOI FET with surface potential modulation

The following section of the results presents the optimization of the GIDL and NOC of NC FET through the modulation of the height of the energy band and surface potential along the channel by gate metal workfunction engineering. The surface potential profiles (along the channel) of the NC SOI FET and conventional SOI FET are compared in Fig. 8 for SM and DM gates. The gate workfunction at the drain side of the channel is lowered

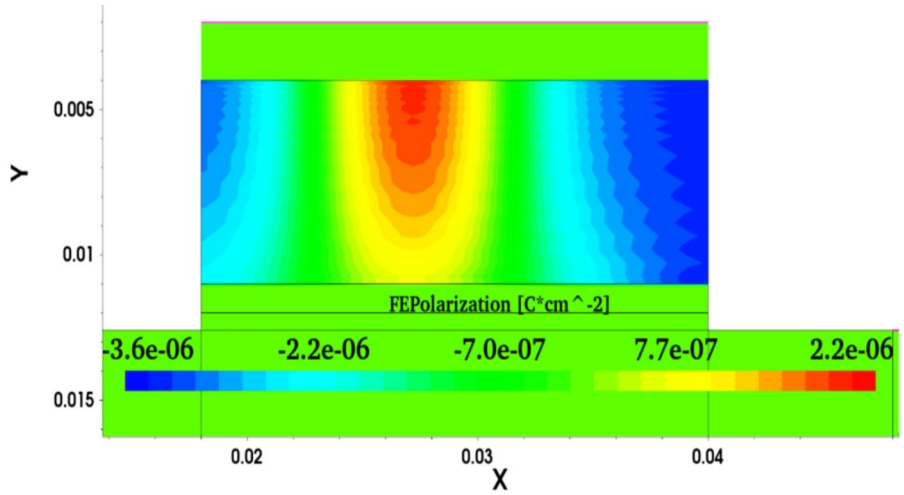

Fig. 6. Ferroelectric polarization of the SM NC SOI FET at $V_{GS} = 0.4$ V and $V_{DS} = 0.9$ V along the channel.

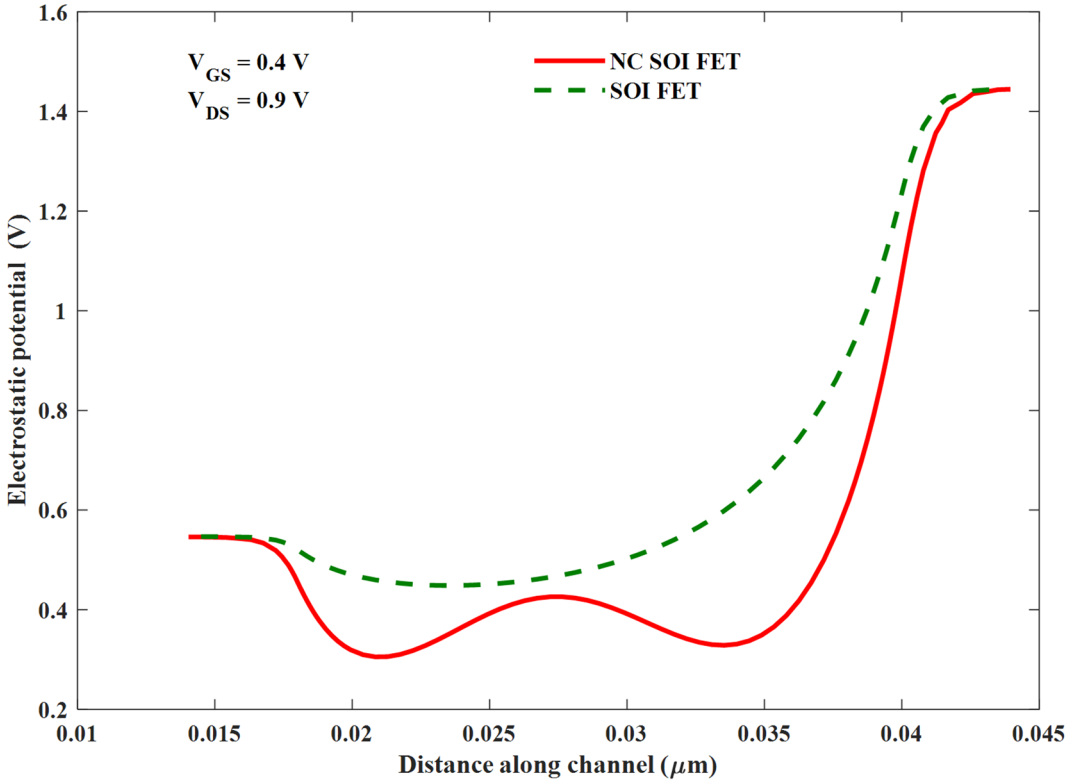

Fig. 7. Surface potential of the SM SOI FET and NC SOI FET.

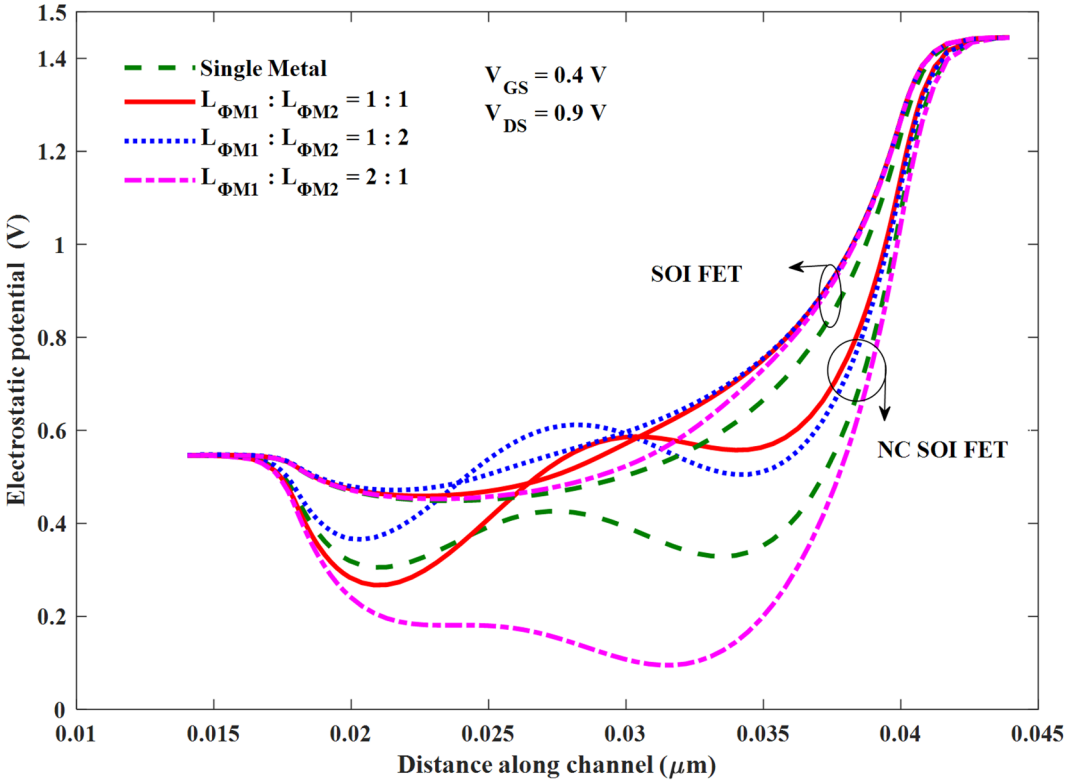

Fig. 8. Surface potential of the SM and DM gate SOI FET and NC SOI FET.

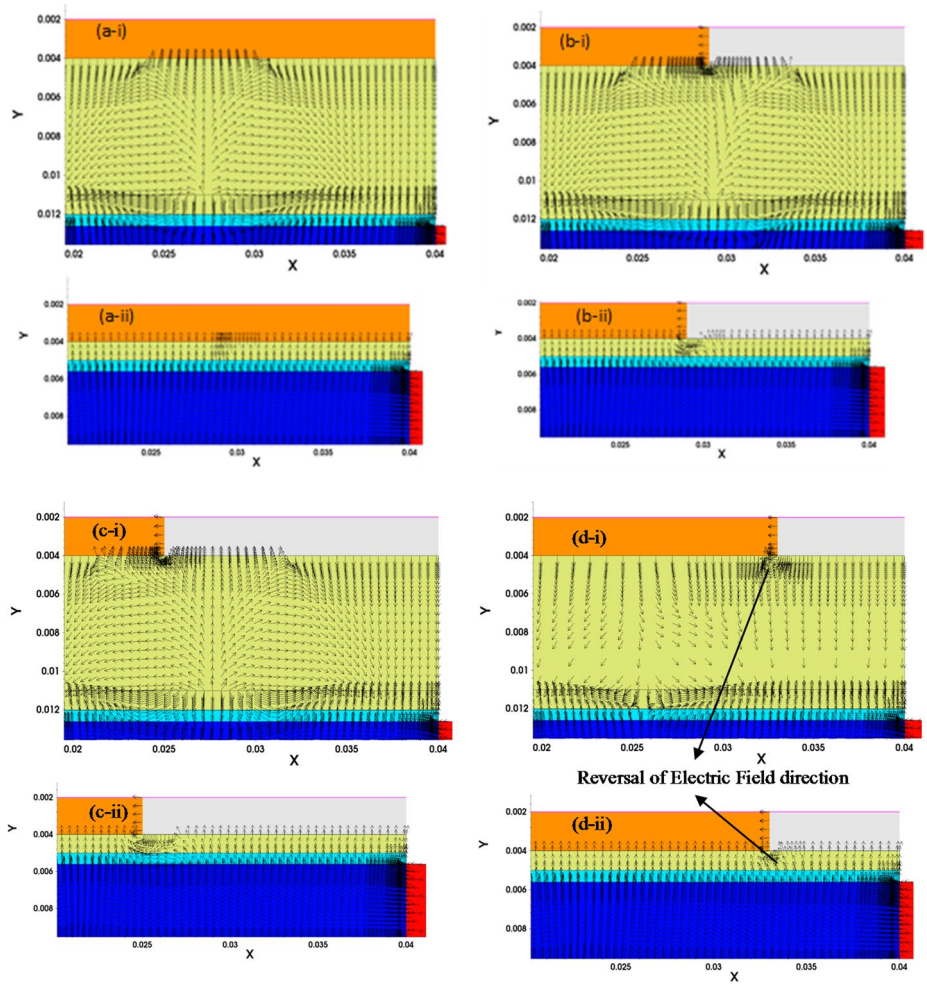

Fig. 9. Electric field vector representation of: (i) NC SOI FET and (ii) SOI FET for (**a**) SM, (**b**) $L_{\phi M1}$:$L_{\phi M2}$ = 1:1, (**c**) $L_{\phi M1}$:$L_{\phi M2}$ = 1:2, and (**d**) $L_{\phi M1}$:$L_{\phi M2}$ = 2:1 at V_{GS} = 0.4 V and V_{DS} = 0.9 V.

to amplify the surface potential and thereby increase the ferroelectric polarization in NC SOI FET through better gate control at higher drain voltages. For the DM FETs, the workfunction of the gate is considered as ϕ_{M1}=4.65 eV and ϕ_{M2}=4.5 eV at the source side and drain side, respectively. The ratio of the lengths of the DM gate ($L_{\phi M1}$:$L_{\phi M2}$) is taken as 2:1, 1:1, and 1:2.

As seen from Fig. 8, the surface potential of the conventional SOI FET is increased proportionally along the length of the gate with workfunction ϕ_{M2} ($L_{\phi M2}$). This, in turn, makes the device conduct early due to the channel inversion at the lower gate voltage (threshold voltage). On the other hand, it is observed from the surface potential profiles of the NC SOI FET that the trend is similar to that of the conventional SOI FET, except for the 2:1 case. The reason for the anomaly in the 2:1 case of NC SOI FET can be understood with the help of the electric field and ferroelectric polarization profiles shown in Figs. 9 and 10, respectively. From Fig. 9 (d-i, ii), it is observed that the electric field direction of the NC SOI FET with $L_{\phi M1}$:$L_{\phi M2}$ of 2:1 is in the opposite direction to the electric field of the SOI FET. This contrasts with the electric field directions observed in the remaining cases of $L_{\phi M1}$:$L_{\phi M2}$ shown in Fig. 9.

This abnormality in the electric field direction of NC SOI FET for the $L_{\phi M1}$:$L_{\phi M2}$ of 2:1 is attributed to the extended polarization dampening of ferroelectric at the drain end, as seen from Fig. 10 (d). In NC SOI FET with $L_{\phi M1}$:$L_{\phi M2}$ of 2:1, the interface potential of gate metals aids the drain voltage since the interface of ϕ_{M1} and ϕ_{M2} is located near the drain. Therefore, the gate control at the drain end of the NC SOI FET with $L_{\phi M1}$:$L_{\phi M2}$ of 2:1 further weakens, which results in poor ferroelectric polarization and hence surface potential.

Whereas in the other cases of $L_{\phi M1}$:$L_{\phi M2}$, polarization dampening (at the drain end) of DM NC SOI FET is controlled compared to SM, as seen in Fig. 10 (a-c). The ferroelectric polarization along the channel is compared in Fig. 11 for all cases of $L_{\phi M1}$:$L_{\phi M2}$ with SM SOI FET, which depicts the above observations of polarization dampening in the case of $L_{\phi M1}$:$L_{\phi M2}$ of 2:1 and improved polarization in 1:1 and 1:2 cases.

The output characteristics of the NC SOI FET are depicted in Fig. 12 at a gate voltage of 0.4 V for different $L_{\phi M1}$:$L_{\phi M2}$. It is clear that the SM NC SOI FET suffers from the NOC despite short-channel effects, as discussed in

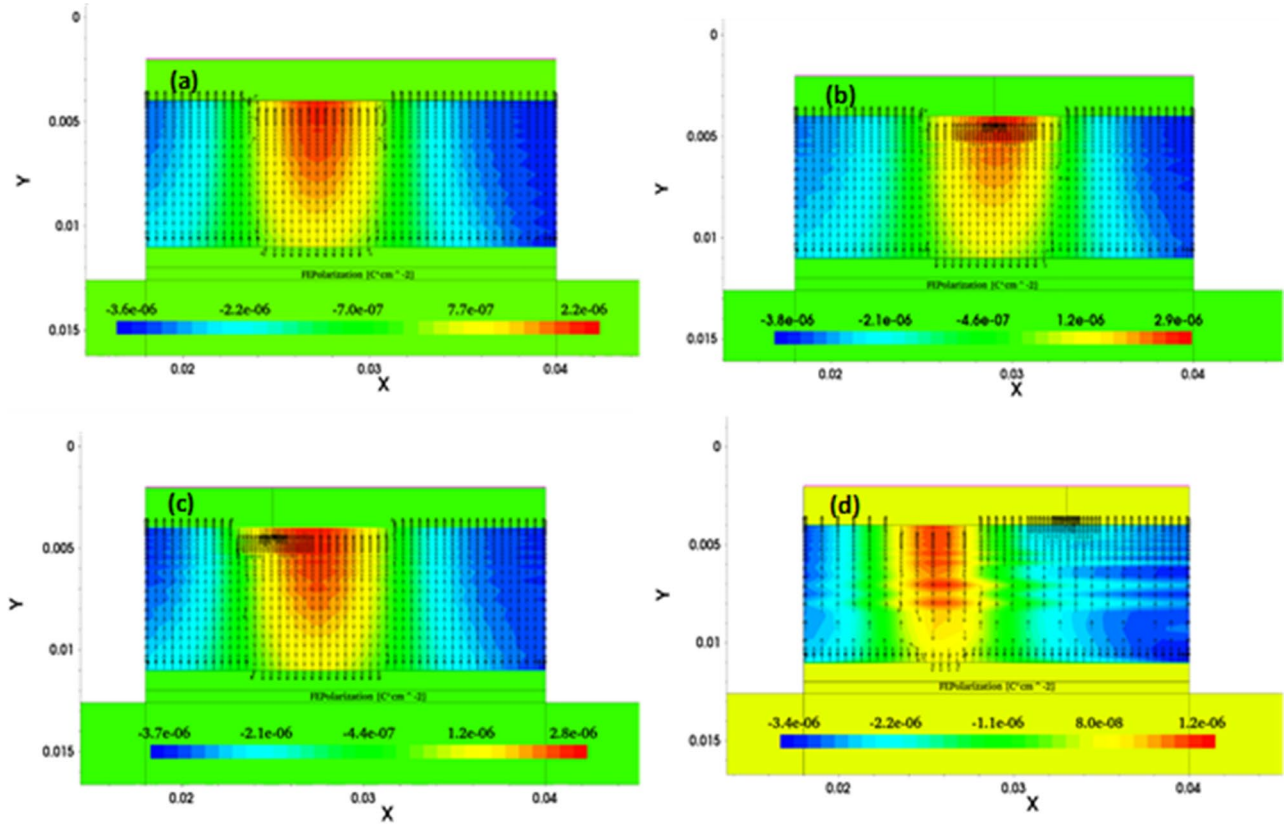

Fig. 10. Ferroelectric polarization contour with its vector representation of the NC SOI FET along the channel (**a**) SM and DM for cases of $L_{\phi M1}$:$L_{\phi M2}$ of (**b**) 1:1, (**c**) 1:2, (**d**) 2:1 at V_{GS} = 0.4 V and V_{DS} = 0.9 V.

Fig. 5. The improvement in the negative slope of output characteristics i.e. NOC is seen with $L_{\phi M1}$:$L_{\phi M2}$ of 1:1 and 1:2. The same trend is reflected in the output conductance as shown in Fig. 13, for the respective combinations of $L_{\phi M1}$:$L_{\phi M2}$. In case of $L_{\phi M1}$:$L_{\phi M2}$ of 1:1, the occurrence of NOC is observed at a V_{DS} of 0.77 V, which is delayed by 0.21 V compared to V_{DS} of 0.56 V for SM NC SOI FET. Besides, in the case of $L_{\phi M1}$:$L_{\phi M2}$ of 1:2, NOC is mitigated as seen in Figs. 12 and 13.

The aforementioned improvement in NOC can be attributed to improved ferroelectric polarization as seen from Fig. 10 (b, c). However, for $L_{\phi M1}$:$L_{\phi M2}$ of 2:1, the NOC is further deteriorated than SM NC SOI FET due to poor ferroelectric polarization as observed in Fig. 10 (d). From Figs. 12 and 13, it is required to note that the NOC for $L_{\phi M1}$:$L_{\phi M2}$ of 2:1 is more prominent at the drain voltages greater than the gate voltage of 0.4 V due to weaker gate control.

The transfer characteristics are plotted in Fig. 14 for the considered combinations of $L_{\phi M1}$:$L_{\phi M2}$. From Fig. 14; Table 4, it is observed that the $L_{\phi M1}$:$L_{\phi M2}$ of 1:2 offered poor subthreshold swing (SS) of 125.87 mV/decade compared to the remaining cases, though there is no NOC seen in Figs. 12 and 13. Whereas the $L_{\phi M1}$:$L_{\phi M2}$ of 1:1 offered the best average and minimum SS of 75.49 mV/decade and 33.45 mV/decade respectively, besides it's improved *NOC* depicted in Fig. 12. On the other hand, $L_{\phi M1}$:$L_{\phi M2}$ of 2:1 offered a moderate improvement in SS compared to SM NC SOI FET. However, its NOC is measurably deteriorated as discussed from Figs. 12 and 13. The energy band profiles of the considered combinations of $L_{\phi M1}$:$L_{\phi M2}$ are plotted in Fig. 15 at a V_{GS} of 0 V. As observed from Figs. 14 and 15; Table 4, $L_{\phi M1}$:$L_{\phi M2}$ of 1:1 has the best I_{GIDL} of 3.18 nA due to a lesser extent of band to band tunnelling (BTBT) resulted from its comparatively wide band gap at the drain end. Furthermore, this work is compared with the literature based on performance metrics such as I_{ON}, I_{ON}/I_{OFF}, NOC, and GIDL, as shown in Table 5. It demonstrates the mitigation/optimization of both NOC and GIDL, whereas other studies have focused only on optimizing NOC. The I_{ON} and I_{ON}/I_{OFF} values of this work are consistent with the literature.

Conclusion

The comparative performance analysis of NC SOI FET is carried out by tuning the ferroelectric polarization and surface potential of the channel through gate workfunction modulation. From the analysis, it is understood that the NC SOI FET with gate metal length ratio ($L_{\phi M1}$:$L_{\phi M2}$) of 1:1 offered an optimum trade-off between NOC, GIDL, and SS. Though the $L_{\phi M1}$:$L_{\phi M2}$ of 1:2 exhibited no NOC, its SS_{min} and $SS_{average}$ are deteriorated to 67.5 mV/decade and 125.87 mV/decade, respectively. On the other hand, the NOC of NC SOIFET is greatly deteriorated

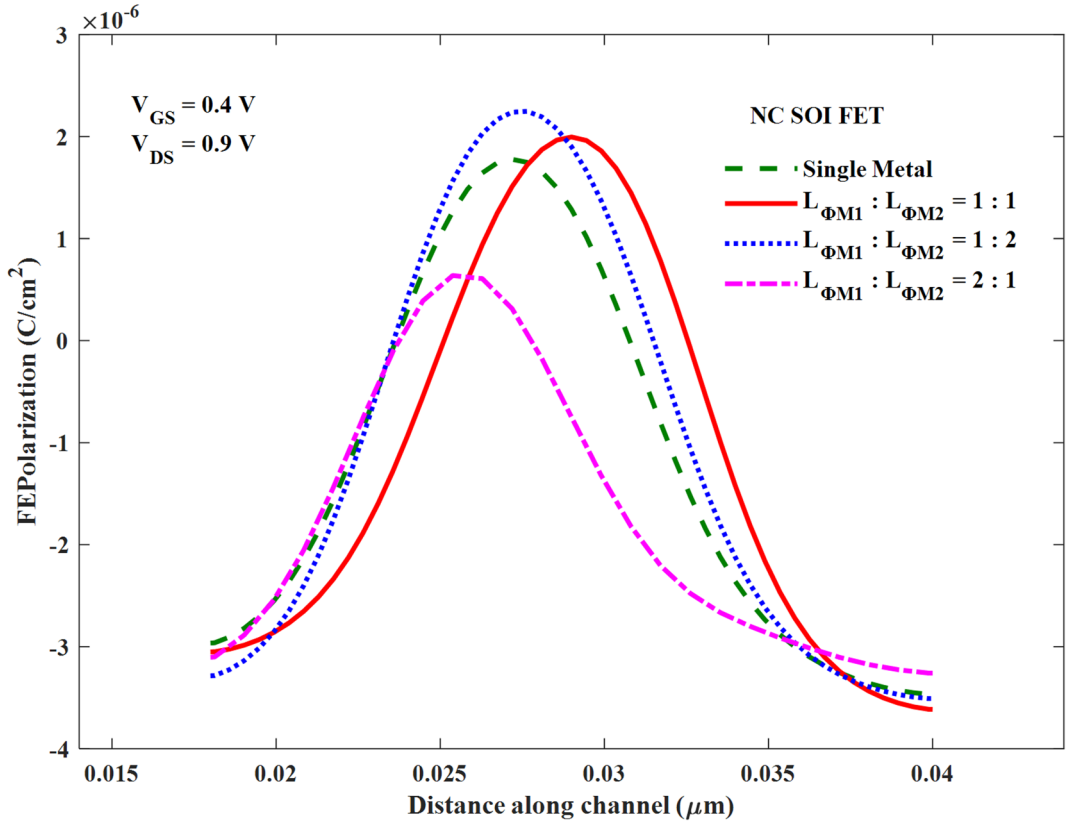

Fig. 11. Comparison of ferroelectric polarization along the channel of NC SOI FET.

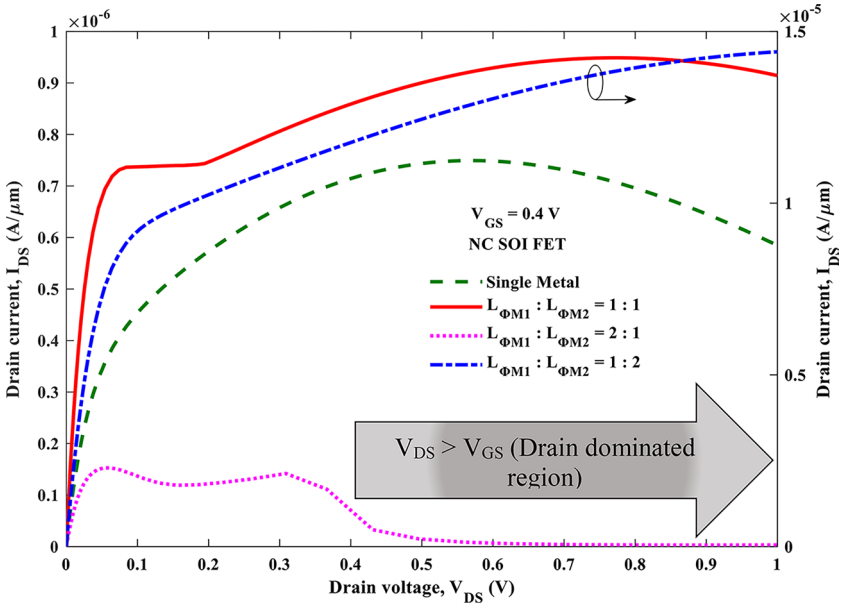

Fig. 12. Output characteristics of SM and DM NC SOI FET.

at a gate metal ratio of 2:1 due to dampened ferroelectric polarization despite the improvement in SS_{min} and $SS_{average}$ when compared to a SM metal NC SOI FET. The ON-OFF current ratio of NC SOI FET is increased in all cases of workfunction modulation. From the findings, it is concluded that the ferroelectric polarization can be

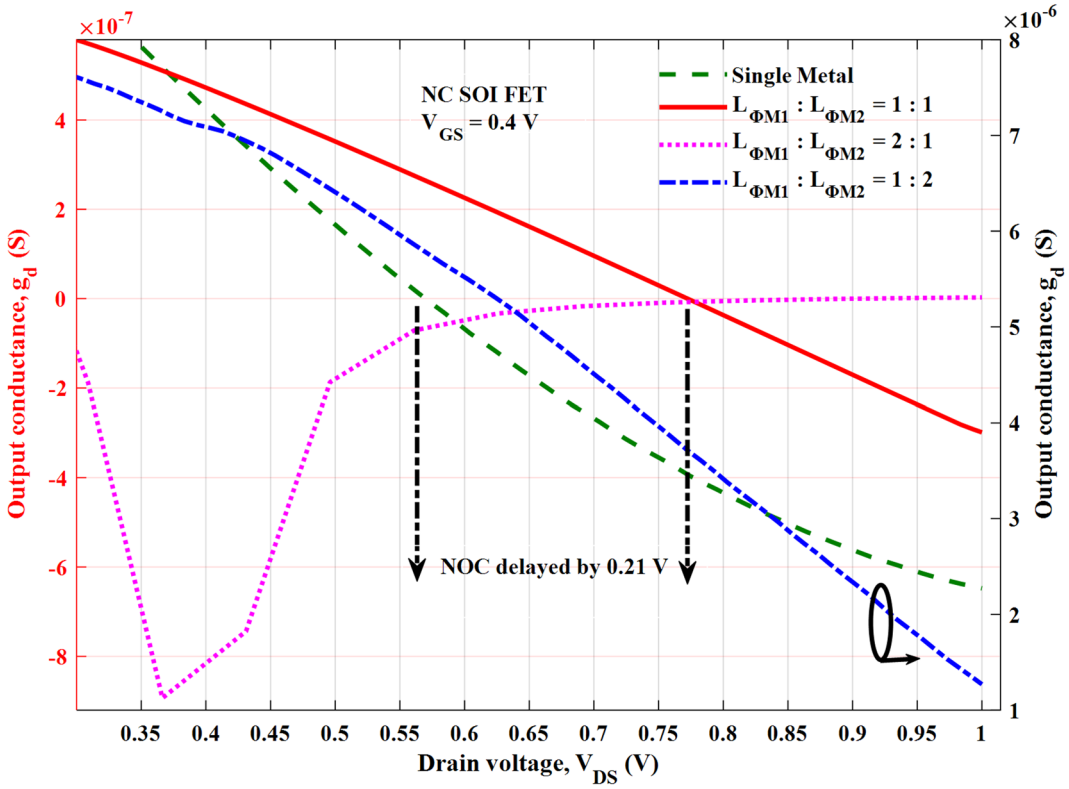

Fig. 13. Output conductance of SM and DM NC SOI FET.

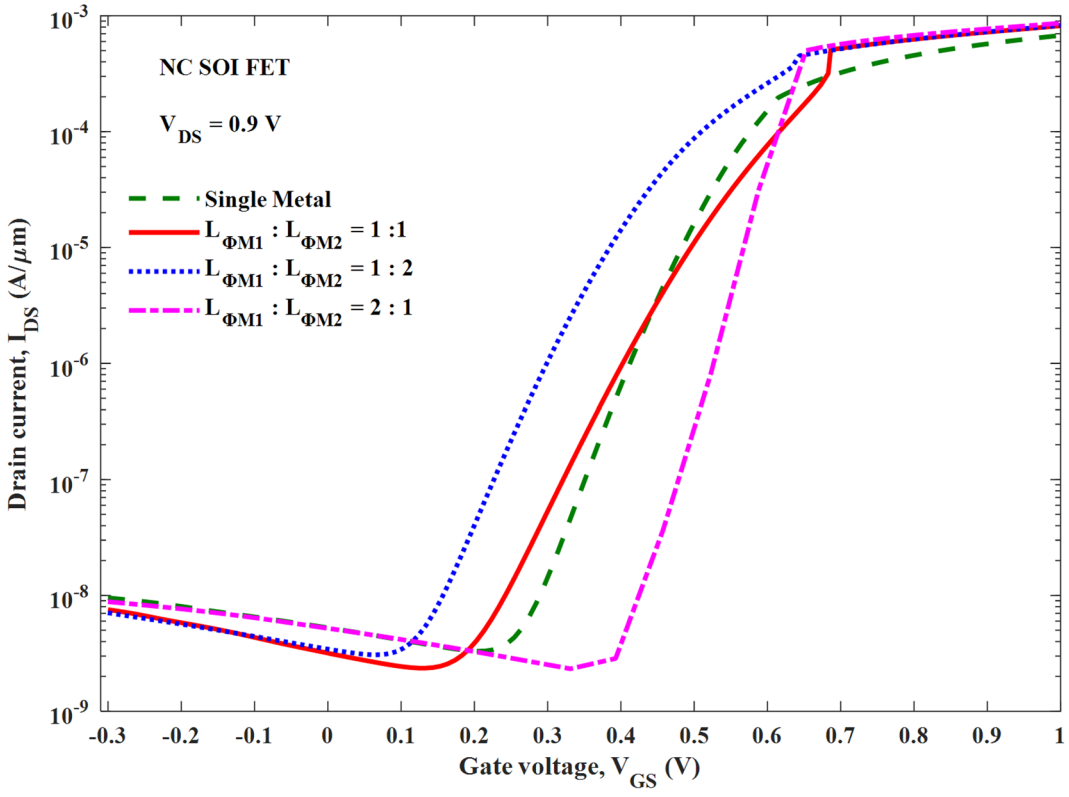

Fig. 14. Transfer characteristics of SM and DM NC SOI FET.

$L_{\phi M1}$:$L_{\phi M2}$	SS_{min}. (mV/decade) at V_{DS} = 0.9 V	$SS_{average}$. (mV/decade) at V_{DS} = 0.9 V	V_{th} (V) at V_{DS} = 0.9 V	I_{ON} (mA) at V_{DS} = 0.9 V	I_{GIDL} (nA) at V_{DS} = 0.9 V V_{GS} = − 0.3 V	I_{GIDL} (nA) at V_{DS} = 0.9 V V_{GS} = 0 V
SM	58.79	79.13	0.548	0.674	9.51	5.26
1:1	33.45	75.49	0.672	0.818	7.52	3.18
1:2	67.50	125.87	0.574	0.824	7.06	3.44
2:1	44.45	73.25	0.65	0.868	8.812	5.199

Table 4. Comparison of minimum SS, average SS, I_{ON}, $V_{th,}$ I_{GIDL} for SM and DM NC SOI FET.

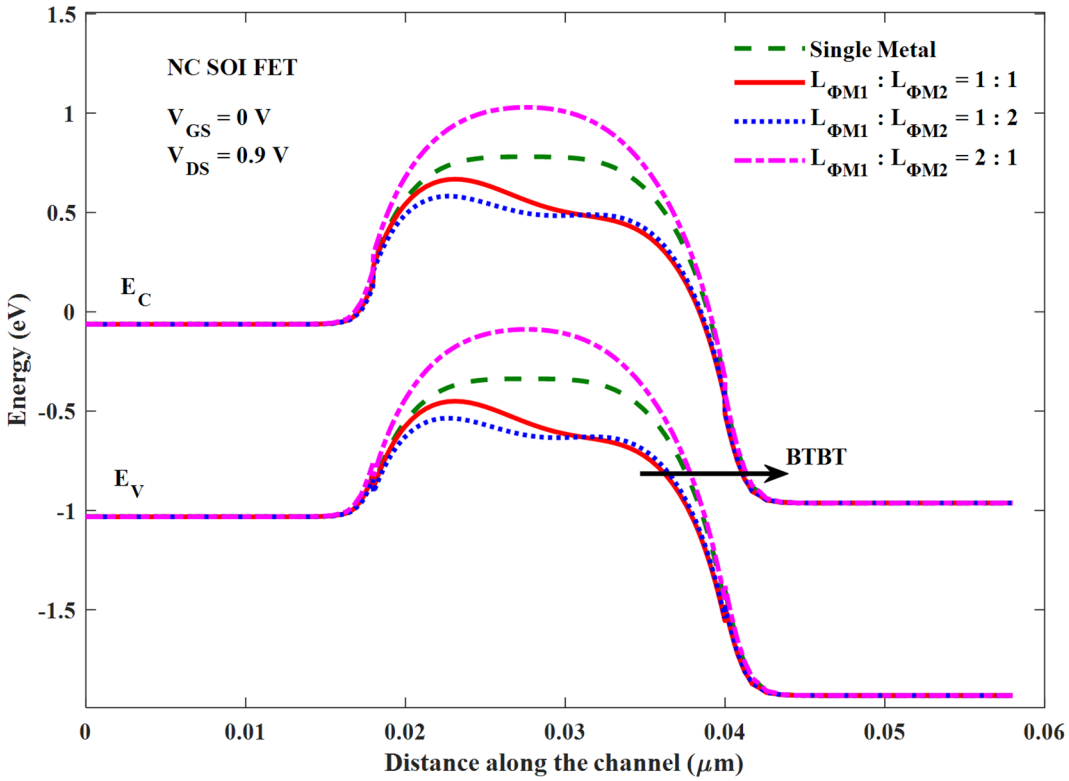

Fig. 15. Energy band profile of SM and DM NC SOI FET.

Device type	Methodology	L (nm)	T_{FE} (nm)	I_{ON} (mA/μm)	I_{ON}/I_{OFF}	NOC optimized/mitigated	GILD effect
NC SOI FET[12]	P_r = 6 μC/cm^2 & E_c = 3 MV/cm	20	4	~ 0.8	~ 10^6	Yes	Not analyzed
NC SOI FET[22]	FE layer at BOX &gate oxide	20	3	1.18	~ 10^5	Yes	Not analyzed
NC SOI FET[22]	FE layer at gate oxide	20	3	1.05	~ 10^7	No	Not analyzed
NC SOI FET[19]	With T_{FE} variation	20	7	~ 2.5	~ 10^6	No	Not analyzed
NC SOI FET[19]	With T_{FE} variation	20	1.7	~ 1	~ 10^5	Yes	Not analyzed
NC SOI FET (SM)	This work	22	7	0.674	~ 10^6	No	Analyzed
NC SOI FET ($L_{\phi M1}$:$L_{\phi M2}$ of 1:1)	This work	22	7	0.818	~ 10^6	Yes (optimized)	Analyzed & optimized
NC SOI FET ($L_{\phi M1}$:$L_{\phi M2}$ of 1:2)	This work	22	7	0.824	~ 10^6	Yes (mitigated)	Analyzed & optimized

Table 5. Comparison of the proposed NC SOI FET with the literature.

tuned carefully through gate workfunction modulation due to its significant impact. However, this method has limited choice in short channel regime as it is difficult to control the gate workfunction variations.

Data availability

The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

Received: 23 June 2025; Accepted: 28 August 2025
Published online: 03 October 2025

References

1. Luk'yanchuk, I. et al. The ferroelectric field-effect transistor with negative capacitance. *Npj Comput. Mater.* **8**, 52. https://doi.org/10.1038/s41524-022-00738-2 (2022).
2. Rahi, S. B., Tayal, S. & Upadhyay, A. K. A review on emerging negative capacitance field effect transistor for low power electronics. *Microelectron. J.* **116** (105242). https://doi.org/10.1016/j.mejo.2021.105242 (2021).
3. Moparthi, S., Tiwari, P. K., Samoju, V. R. & Saramekala, G. K. Investigation of temperature and source/drain overlap impact on negative capacitance silicon nanotube FET (NC Si NTFET) with Sub-60mV/decade switching. *IEEE Trans. Nanotechnol.* **19**, 800–806. https://doi.org/10.1109/TNANO.2020.3033802 (2020).
4. Cristoloveanu, S., Wan, J. & Zaslavsky, A. A Review of Sharp-Switching Devices for Ultra-Low Power Applications, in IEEE Journal of the Electron Devices Society, vol. 4, no. 5, pp. 215–226, Sept. (2016). https://doi.org/10.1109/JEDS.2016.2545978
5. Salahuddin, S. & Datta, S. Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano Lett.* **8** (2), 405–410. https://doi.org/10.1021/nl071804g (2008).
6. Lamba Ayushi, R., Chaujar & Jamal Deen, M. Negative capacitance FinFETs for low power applications: A review. Micro and nanostructures, **205**, 208177, (2025). https://doi.org/10.1016/j.micrna.2025.208177
7. Amrouch, H. et al. Unveiling the impact of IR-Drop on performance gain in NCFET-Based processors. *IEEE Trans. Electron. Devices*. **66** (7), 3215–3223. https://doi.org/10.1109/TED.2019.2916494 (July 2019).
8. Kwon, D. et al. Improved subthreshold swing and short channel effect in FDSOI n-Channel negative capacitance field effect transistors. *IEEE Electron Device Lett.* **39** (2), 300–303. https://doi.org/10.1109/LED.2017.2787063 (Feb. 2018).
9. Gupta, S. et al. Device-Circuit analysis of ferroelectric fets for Low-Power logic. *IEEE Trans. Electron. Devices*. **64** (8), 3092–3100. https://doi.org/10.1109/TED.2017.2717929 (Aug. 2017).
10. Zhou, J. et al. Negative differential resistance in negative capacitance fets. *IEEE Electron Device Lett.* **39** (4), 622–625. https://doi.org/10.1109/LED.2018.2810071 (April 2018).
11. Agarwal, H. et al. Engineering negative differential resistance in NCFETs for analog applications. *IEEE Trans. Electron. Devices*. **65** (5), 2033–2039. https://doi.org/10.1109/TED.2018.2817238 (May 2018).
12. Tianyu, Y., Weifeng, L., Zhifeng, Z., Peng, S. & Zhang, K. Negative drain-induced barrier lowering and negative differential resistance effects in negative-capacitance transistors, Microelectron. J., vol. 108, Feb. Art. no. 104981, (2021). https://doi.org/10.1016/j.mejo.2020.104981
13. Moparthi, S., Tiwari, P. K. & Saramekala, G. K. Impact of drain voltage coupling on device and Circuit-Level performance of negative capacitance silicon nanotube FET. *IEEE Trans. Nanotechnol.* **21**, 547–554. https://doi.org/10.1109/TNANO.2022.3208208 (2022).
14. Vanlalawmpuia, K. & Medury, A. S. Analysis of negative differential resistance and rf/analog performance on drain engineered negative capacitance dual Stacked-Source tunnel FET. *IEEE Trans. Electron. Devices*. **70** (3), 1417–1424. https://doi.org/10.1109/TED.2023.3237507 (March 2023).
15. Ziqiang Xie, W., Lü, M., Guo & Zhao, M. LoGHeD: an effective approach for negative differential resistance effect suppression in negative-capacitance transistors. *Semicond. Sci. Technol.* **37** (3), 035001. https://doi.org/10.1088/1361-6641/ac4819 (January 2022).
16. Lee, K., Kim, S., Lee, J. H., Kwon, D. & Byung-Gook, P. Suppression of reverse drain induced barrier Lowering in negative capacitance FDSOI field effect transistor using oxide charge trapping layer. *Semicond. Sci. Technol.* **35** (12), 125003. https://doi.org/10.1088/1361-6641/abb5e4 (2020).
17. Gaidhane, A. D., Pahwa, G., Verma, A. & Chauhan, Y. S. Gate-Induced drain leakage in negative capacitance FinFETs. *IEEE Trans. Electron. Devices*. **67** (3), 802–809. https://doi.org/10.1109/TED.2020.2967463 (March 2020).
18. Anil Kumar Pathakamuri and & Pandey, C. K. Impact of back gate-drain overlap on DC and analog/hf performance of a ferroelectric negative capacitance double gate TFET. *Phys. Scr.* **98** (124001). https://doi.org/10.1088/1402-4896/acf5ae (2023).
19. Prakash, O., Gupta, A., Pahwa, G., Chauhan, Y. S. & Hussam Amrouch. On the critical role of ferroelectric thickness for negative capacitance device-circuit interaction. *IEEE J. Electron. Devices Soc.* **9**, 1262–1268. https://doi.org/10.1109/JEDS.2021.3110486 (2021).
20. Liu, Q. et al. High performance UTBB FDSOI devices featuring 20nm gate length for 14nm node and beyond, *2013 IEEE International Electron Devices Meeting*, Washington, DC, USA, p. 9.2.1–9.2.4, (2013). https://doi.org/10.1109/IEDM.2013.6724592
21. Hoffmann, M. et al. Demonstration of High-speed Hysteresis-free Negative Capacitance in Ferroelectric Hf0.5Zr0.5O2, 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, p. 31.6.1–31.6.4, (2018). https://doi.org/10.1109/IEDM.2018.8614677
22. Chauhan Navjeet, N., Shashank, B., Chirag, B. et. al. (2022) BOX engineering to mitigate negative differential resistance in MFIS negative capacitance FDSOI FET: an analog perspective Abstract *Nanotechnology*, **33**(8), 085203. https://doi.org/10.1088/1361-6528/ac328a (2021).

Acknowledgements

The authors thank and acknowledge the Ministry of Electronics and Information Technology, Government of India, for providing the EDA tools through the Chip to Start-up (C2S) programme.

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Vijay Sai Thota: Methodology; Simulation; Data curation; Writing original draft. Sandeep Moparthi: Conceptualization; Investigation; Validation; Formal Analysis; Writing original draft.Kalyanbrata Ghosh: Visualization; Writing– review & editing.

Funding

Open access funding provided by Vellore Institute of Technology. The authors did not receive support from any organization for the submitted work.

Declarations

Competing interests
The authors declare no competing interests.

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