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Self-balanced switched capacitors based thirteen level three-fold multilevel inverter for solar PV applications

Niraj Kumar Dewangan[1]✉, Kasinath Jena[2], Tarun Kumar Tailor[3], Devesh Umesh Sarkar[4] & Murli Manohar[5]

While the conventional topologies of multilevel inverters (MLIs) operate with unity voltage gain, switched capacitors-based MLIs (SCMLIs) offer a solution to realize an inherent voltage gain of more than one, thereby stepping up the voltage in the process of DC to AC conversion. This work proposes a novel SCMLI constituting thirteen levels, requiring only one DC input and 3-capacitors to achieve an inclusive three-fold gain in voltage. The number of power switches employed in the proposed module is thirteen, where nine switches peak-inverse-voltage (PIV) is considered as one-third of the output voltage amplitude. Experimental results validate the proposed inverter (PI), demonstrating its efficacy. The superior performance of the PI with respect to component count, power switch voltage ratings, and cost function (CF) is highlighted by comparison with other SCMLIs. The total standing voltage (TSV) per level, expressed in per unit with respect to V_{in} is 1.307, while the PIV per level is 0.153, which is competitive with recent literature. Additionally, the CF is 4.538, lower than other designs, enhancing the performance of the structure for real-time applications.

Keywords Cost function, Multilevel inverter topologies, Switched capacitors, TSV

Many applications favor multilevel inverters (MLIs) over two-level inverters due to numerous advantages. Power switches with a PIV than the multilevel AC output operating voltage increase efficiency and reliability. Due to their improved harmonic profile, MLIs require less filtering, simplifying system design, and saving costs. Reduced dv/dt stress on the load extends its lifespan and improves reliability. Fault-tolerant MLIs are more resilient in crucial applications. Neutral point clamped (NPC), flying capacitors (FC), and cascaded H-bridge (CHB) MLI topologies are used in renewable energy systems, electric motors, and vehicle electrification. MLIs improve voltage quality, electromagnetic interference, and operational flexibility for these applications. As a result, MLIs continue to advance power electronics and meet the growing demand for reliable and effective energy conversion in modern technological systems[1–3]. These classical topologies operate with a gain of unity, and hence, there is no inherent stepping up of voltage. In the past few years, a new family of MLIs has emerged with the capability of operating with a voltage gain of more than unity. These structures use switched capacitors (SC) to step up the voltage magnitude and are generally referred to as SCMLIs[4]. Inductor-less configuration and self-balancing of capacitors are other attractive features of SCMLIs[5].

As a result of their various advantages, numerous SCMLI topologies have recently evolved[4–17]. In[4], the authors have proposed a switched-capacitors module with minimal switch count and TSV. Still, it is incapable of synthesizing a bipolar waveform. Hence, multiple modules are to be used in a cross-connected fashion to realize an alternating waveform, leading to the requirement of multiple isolated DC sources. The 13-level inverter proposed in[5] operates with a gain of 6. However, it consists of PIV switches equal to the operating voltage. The SCMLI presented in[6] needs switches with a PIV equal to the input source voltage; however, its component count rises significantly as the number of levels increases. Barzegarkhoo et al.[7] have presented an easily extendable SCMLI structure using

[1]Department of Mechatronics, Manipal Institute of Technology, Manipal Academy of Higher Education, Manipal 576104, India. [2]Department of Electrical and Electronics Engineering, ARKA JAIN University, Jharkhand, India. [3]Electrical Engineering Department, Institute of Technology, Nirma University, Ahmedabad, Gujarat, India. [4]Department of Electrical Engineering, Indian Institute of Technology Palakkad, Kanjikode, India. [5]Centre for Internet of Things, Madhav Institute of Technology & Science, Madhya Pradesh, Gwalior, India. ✉email: niraj.dewangan@manipal.edu

low voltage bearing power switches. Still, the switches are a mix of unidirectional and bidirectional configurations, thereby limiting the modularity. The single-stage SCMLI module proposed by S.S. Lee[8] is extremely advantageous in terms of PIV ratings of switches, but the overall component count is high. Similarly, highly modular topologies are proposed in[9,10], but they involve two-stage conversion with the help of four H-bridge power switches, capable of handling the operating voltage. An innovative approach that uses traditional H-bridges and switched capacitors is proposed in[11] with some additional power switches. However, the capacitor voltage balancing requires a complex methodology in it. A different cascaded module approach for SCMLI is shown in[12]. However, it is limited in its applicability to high-voltage applications since each module requires two power switches to be rated at operational voltage. A different approach modular strategy that has been proposed[13] includes several components at each level. The generalized structure of single-phase SCMLIs presented in[14] requires fewer switching devices. Still, the involvement of a two-stage operation requires the use of H-bridge switches having PIV, which is the same as the operating voltage. The topology proposed by He and Cheng[15] utilizes flying capacitors clamping for the SCMLI in order to attain a large gain, but the approach leads to a high number of elements per level. Highly modular and low PIV topologies[16,17] provide advantages in some applications.

The topology described in[8] incorporates switches with a low PIV rating. However, it has a limited voltage gain and requires a relatively high number of switches. A similar trend can be observed in the configurations presented in[18]. Research studies from[19–24] delve into single-stage, 13-level SC-MLI designs. The converter introduced in[19] offers moderate voltage gain and a reduced switch count, but its TSV is comparatively higher. Moreover, the number of capacitors required to increase with the rise in load power factor. SC-MLI designs with higher voltage gain have been explored in[20,21], and[22–24]. The approach in[20] requires more components, while the design in[21] depends on switches with higher PIV ratings. The converter discussed in[24] utilized a higher quantity of switches among these designs. On the other hand, the configurations presented in[22] and[23] require capacitors with higher voltage ratings, which add to the overall cost of the system. Additionally, the designs in[20] and[21] face challenges with charge balancing across capacitors, especially at lower modulation indices. The SC-MLI design presented in[25] attains a gain of 3 but is characterized by a relatively large switch count. This configuration also exhibits a high-cost function (CF), requires switches with significant PIV ratings, and shows elevated TSV levels. However, its voltage balancing capabilities deteriorate when operating at lower modulation indices. Furthermore, the asymmetrical topology proposed in[26] integrates power devices with elevated PIV and TSV ratings, making voltage balancing in this design particularly challenging. These advantages come with drawbacks, such as poor voltage gain and high semiconductor demand, which can reduce efficiency and practicality.

References[27,28] present common-ground SC based five-level inverter topologies. These configurations enable efficient high-voltage gain while minimizing the part count and suppressing leakage current, making them highly suitable for compact and low-loss power conversion systems. Additionally, the work presented in[29] introduces a nine-level single-phase SC inverter capable of achieving 4-X gain. This design further enhances performance by reducing the total number of components, minimizing TSV across the switches, and ensuring cost-effective implementation.

Given these factors, SCMLIs with high-resolution output, low PIV switches, high voltage gain, and minimal semiconductor utilization have enormous potential. SCMLIs could become more adaptable and efficient for a broader range of power electronics applications with such improvements. The presented study unveils a single-stage SCMLI module, highlighting the following attributes: (a) a voltage gain of three; (b) generation of a thirteen-level waveform through a single DC source, three capacitors, and thirteen power switches; (c) inherent self-balancing of all capacitors; and (d) ensuring the PIVs of the switches remain substantially lower compared to the operating voltage.

The paper is structured as follows: Section II describes the proposed module structure and operation. The same section also compares it with other topologies mentioned in[4–26]. Section III describes the switching process used in the suggested module. Section IV presents the experimental findings, and section V discusses the conclusions.

The proposed 13-level inverter and it's working

Figure 1 shows the power circuit diagram of the thirteen-level inverter suggested in this work. It comprises twelve power switches a diode 'D', capacitors ($C_1, C_2,$ and C_3), and one DC source (shown with voltage V_{in}). Of the twelve switches, the power switch S_{12} is required to be of bidirectional-blocking-bidirectional-conducting type, while rest of the switches are of unidirectional-blocking-bidirectional-conducting type. The load voltage is represented as 'v_{ab}'. The capacitor C_1 is to be kept at voltage equal to V_{in}, while the capacitors C_2 and C_3 are to be maintained at $0.5V_{in}$ each. The structure is capable of synthesizing thirteen voltage levels (viz. $\pm 0.5V_{in}, \pm V_{in}, \pm 1.5V_{in}, \pm 2V_{in}, \pm 2.5V_{in}, \pm 3V_{in}$ and 0) at the load terminals. The PIV rating of the switches used in the designed inverter is tabulated in Table 1.

The working principle of the PI can be comprehended with the description of fourteen states $\emptyset_k\{k = 1 \text{ to } 14\}$. Each state is a distinct switching combination to synthesize the desired voltage level at the load terminals. Moreover, the capacitors are placed parallel to the input supply so that the voltage across them can be maintained at its desired voltage levels. Consequently, for each state, the route for generating the output voltage is indicated by a bold red line, while a narrow blue line represents the charging pathway for the capacitor(s). These states are elaborated as follows:

(i) State $\emptyset_1$: Fig. 2 describes this state, where S_1, S_5, S_8 and S_{10} are all conducting simultaneously, and the output voltage $v_{ab} = 0$. Additionally, C_1 is charged to V_{in} when conduction of S_4 brings it in parallel with the dc source through diode D. Similarly, by simultaneously conducting S_5, S_6, S_8 and S_9, a series connection of C_2 and C_3 is placed in parallel with the dc source and charged to a voltage of $0.5V_{in}$ each.

(ii) State $\emptyset_2$*:* Fig. 3 shows switches S_1, S_5, S_8 and S_{12} connecting load terminals to capacitor C_2consequently, the output voltage $v_{ab} = v_{C2} = 0.5V_{in}$. Moreover, switch S_4 conducts capacitor C_1 in parallel with the dc

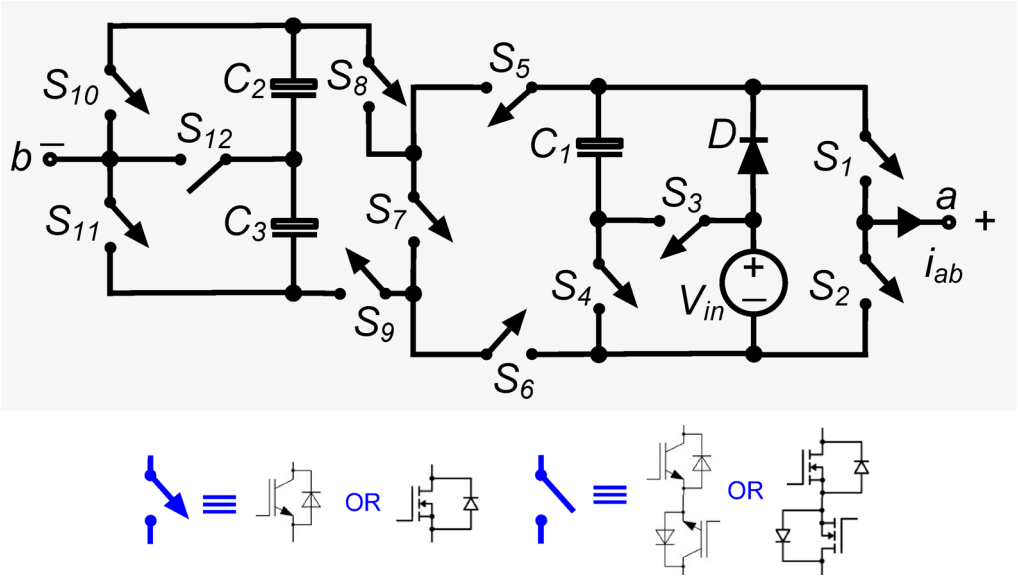


Fig. 1. The proposed 13-level inverter.

PIV	Power switches
$0.5V_{in}$	S_{12}
V_{in}	S_3, S_4, S_7, S_8, S_9, S_{10}, S_{11}, D,
$2V_{in}$	S_1, S_2, S_5, S_6

Table 1. PIV rating of the switches.

(i) State $\emptyset_1$**:** Figure 2 describes this state, where S_1, S_5, S_8 and S_{10} are all conducting simultaneously, and the output voltage $v_{ab} = 0$. Additionally, C_1 is charged to V_{in} when conduction of S_4 brings it in parallel with the dc source through diode D. Similarly, by simultaneously conducting S_5, S_6, S_8 and S_9, a series connection of C_2 and C_3 is placed in parallel with the dc source and charged to a voltage of $0.5V_{in}$ each.

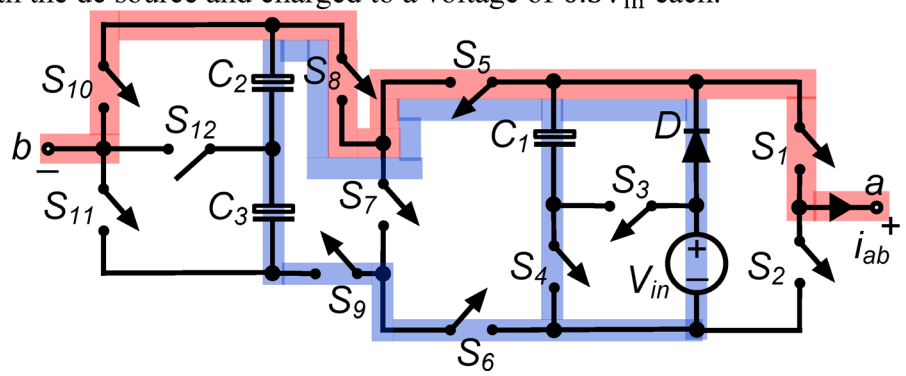


Fig. 2. Working state $\emptyset_1$ of the PI $[v_{ab} = 0]$.

source via diode D, charging it to V_{in}. In parallel with the dc source, switches S_5, S_6, S_8 and S_9 link capacitors C_2 and C_3 in series. The abovementioned arrangement charges capacitors C_2 and C_3 to $0.5V_{in}$. To run the inverter system efficiently, this state regulates capacitor charging and discharging, optimizing voltage levels and maintaining the desired output.

(iii) State $\emptyset_3$: Fig. 4 shows switches S_1, S_4, S_6, S_9 and S_{11} connecting load terminals to capacitor C_1. The output voltage: voltage $v_{ab} = v_{C1} = V_{in}$, supplying the whole input voltage to the load. Moreover, switch S_4 conducts capacitor C_1 via diode D, maintaining its value to V_{in}. Parallel to the dc supply, switches S_5, S_6, S_8

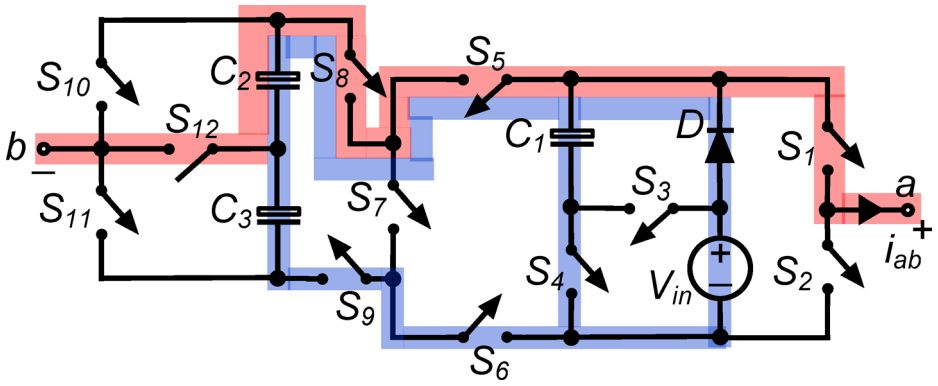


Fig. 3. Working state $\emptyset_2$ of the PI [$v_{ab} = 0.5V_{in}$].

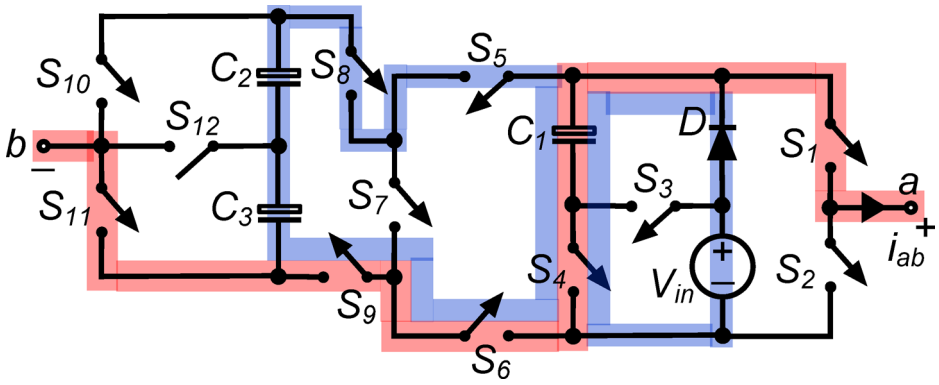


Fig. 4. Working state $\emptyset_3$ of the PI [$v_{ab} = V_{in}$].

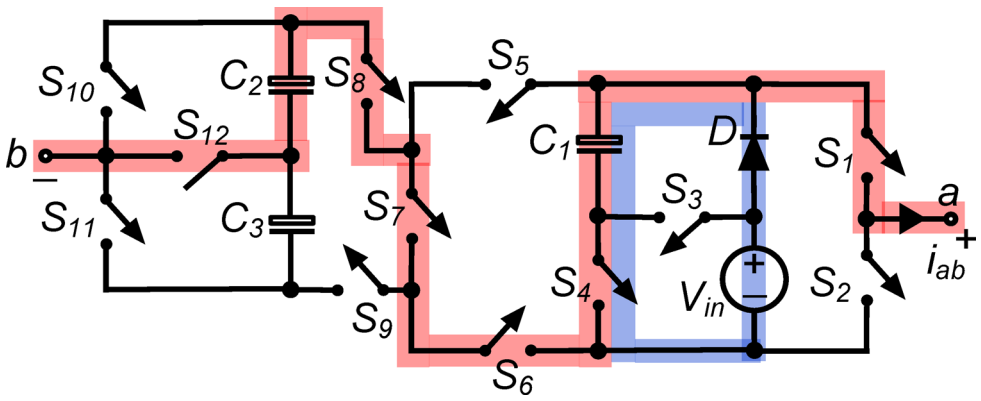


Fig. 5. Working state $\emptyset_4$ of the PI [$v_{ab} = 1.5V_{in}$].

and S_9 connect capacitors C_2 and C_3 in series. This setup charges capacitors C_2 and C_3 to $0.5V_{in}$. Maintaining capacitor voltage levels and inverter energy flow in this stage ensures efficient operation and appropriate output.

(iv) State $\emptyset_4$: In the state depicted in Fig. 5, the load terminals are connected to C_1 and C_2 through the simultaneous conduction of S_1, S_4, S_6, S_7, S_8 and S_{12}. So, the output voltage $v_{ab} = v_{C1} + v_{C2} = 1.5V_{in}$. Moreover, the conduction of S_4 places C_1 in parallel with the dc source via diode D, thereby charging it to V_{in}.

(v) State $\emptyset_5$: As shown in Fig. 6, the switches S_1, S_4, S_6, S_7, S_8, and S_{11} conduct simultaneously, and the load is connected in series with the capacitors. The output voltage, v_{ab}, is therefore equal to $v_{C1} + v_{C2} + v_{C3} = 2V_{in}$. Additionally, the conduction of S_4 places C_1 in parallel with the dc source through diode D, allowing it to charge to V_{in}.

(v) State $\emptyset_5$: As shown in Figure 6, the switches S_1, S_4, S_6, S_7, S_8, and S_{11} conduct simultaneously, and the load is connected in series with the capacitors. The output voltage, v_{ab}, is therefore equal to $v_{C1} + v_{C2} + v_{C3} = 2V_{in}$. Additionally, the conduction of S_4 places C_1 in parallel with the dc source through diode D, allowing it to charge to V_{in}.

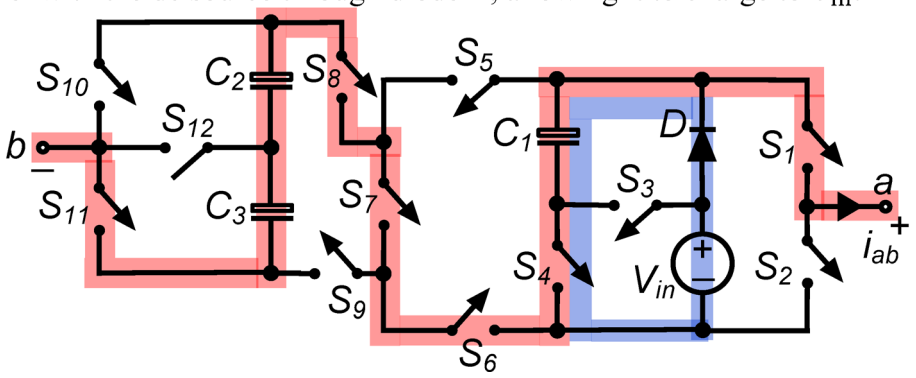


Fig. 6. Working state $\emptyset_5$ of the PI [$v_{ab} = 2V_{in}$].

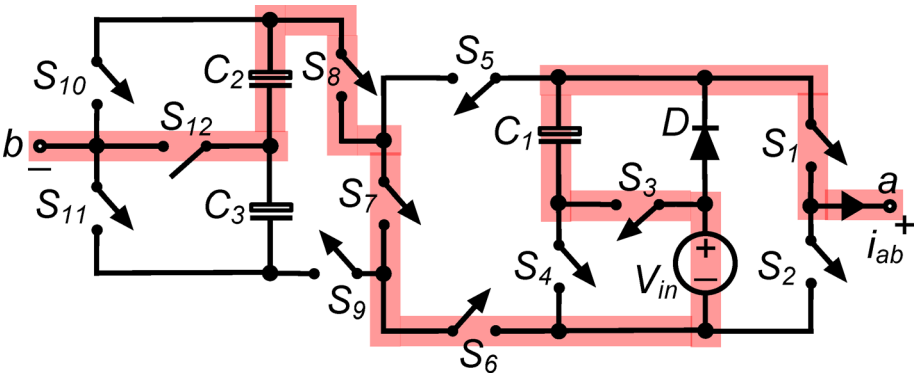


Fig. 7. Working state $\emptyset_6$ of the PI [$v_{ab} = 2.5V_{in}$].

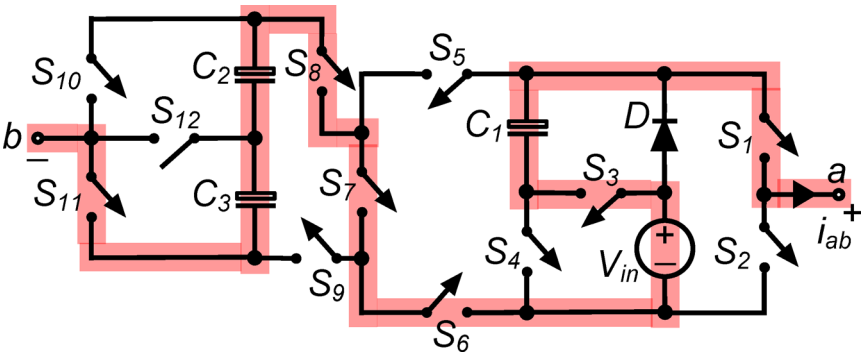


Fig. 8. Working state $\emptyset_7$ of the PI [$v_{ab} = 3V_{in}$].

(vi) State $\emptyset_6$: The load terminals in this condition, seen in Fig. 7, are linked to C_1, C_2 and V_{in} in a series arrangement, while S_1, S_3, S_6, S_7, S_8 and S_{12} are in conduction simultaneously. As a result, the output voltage $v_{ab} = v_{C1} + v_{C2} + V_{in} = 2.5V_{in}$.

(vii) State $\emptyset_7$: In the state illustrated in Fig. 8, S_1, S_3, S_6, S_7, S_8 and S_{11} are all simultaneously conducting when the load is in series with C_1, C_2, C_3 and V_{in}. As a result, the output voltage $v_{ab} = v_{C1} + v_{C2} + v_{C3} + V_{in} = 3V_{in}$.

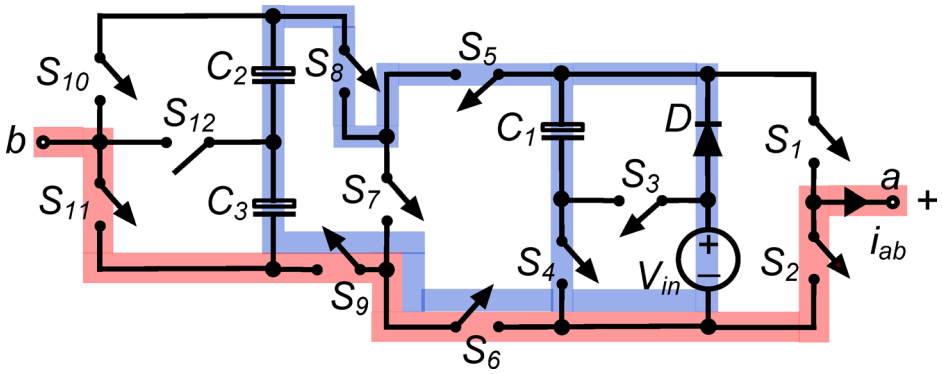


Fig. 9. Working state $\emptyset_8$ of the PI [$v_{ab} = 0$].

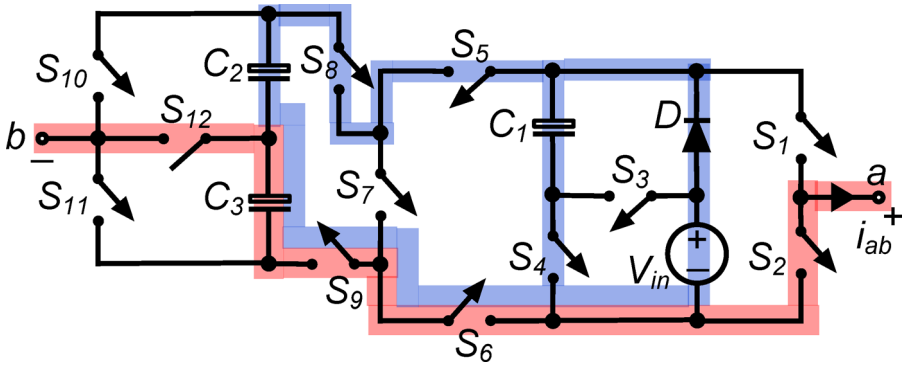


Fig. 10. Working state $\emptyset_9$ of the PI [$v_{ab} = -0.5V_{in}$].

(viii) State $\emptyset_8$*:* In the state depicted in Fig. 9, switches of S_2, S_6, S_9 and S_{11} all conduct simultaneously to provide the output voltage $v_{ab} = 0$. Furthermore, C_1 is charged to V_{in} by being placed in parallel with the dc source through diode D with S_4 in conduction. Similar to this, the concurrent conduction of S_5, S_6, S_8 and S_9 connects the series combination of C_2 and C_3 in parallel with the dc source, charging each capacitor to $0.5V_{in}$.

(ix) State $\emptyset_9$*:* The load is connected to C_3 in this state (Fig. 10), where S_2, S_6, S_9 and S_{12} are all conducts simultaneously. $v_{ab} = -v_{C3} = -0.5V_{in}$ is the output voltage as a result. Additionally, C_1 is charged to V_{in} through diode D, which is connected in parallel with the dc source with S_4 in conduction. Also, $0.5V_{in}$ is achieved by the capacitors C_2 and C_3, which are parallel with the input and conduct the switches S_5, S_6, S_8 and S_9 simultaneously.

(x) State $\emptyset_{10}$: In Fig. 11, switches S_2, S_4, S_5, S_8 and S_{10} operate simultaneously to connect load terminals to capacitor C_1. The output voltage $v_{ab} = -v_{C1} = -V_{in}$ causes the load to receive a negative full input voltage. With switch S_4, capacitor C_1 is charged to V_{in} via diode D in parallel with the dc source. In parallel with the dc source, switches S_5, S_6, S_8 and S_9 link capacitors C_2 and C_3 in series. The setup charges both capacitors, C_2 and C_3, to $0.5V_{in}$ each. This condition efficiently inverts the output voltage while maintaining capacitor charge levels, ensuring the inverter outputs the desired negative voltage and operates efficiently.

(xi) State $\emptyset_{11}$: In this state, as shown in Fig. 12, the load, C_1 and C_3 are in series, when simultaneous conduction of S_2, S_4, S_5, S_7, S_9 and S_{12} occurs. Thus, output voltage $v_{ab} = -(v_{C1} + v_{C3}) = -1.5V_{in}$. Again, the conduction of S_4 connects C_1 in parallel with the DC source through diode 'D', and it is charged to V_{in}.

(xii) State $\emptyset_{12}$: As shown in Fig. 13, capacitors C_1, C_2, C_3 and load are in series through switches S_2, S_4, S_5, S_7, S_9 and S_{10}, resulting in an output voltage of $v_{ab} = -(v_{C1} + v_{C2} + v_{C3}) = -2V_{in}$. By conducting switch S_4, capacitor C_1 is connected in parallel with the dc source via diode D, allowing it to charge to V_{in}.

(xiii) State $\emptyset_{13}$: As shown in Fig. 14, the load and capacitors C_1 and C_3 are connected consecutively, and the input voltage V_{in} via switches S_2, S_3, S_5, S_7, S_9, and S_{12}. Output voltage $v_{ab} = -(v_{C1} + v_{C3} + V_{in}) = -2.5V_{in}$ is delivered to the load as a negative voltage 2.5 times the input voltage.

(xiv) State $\emptyset_{14}$: Fig. 15 shows the capacitors C_1, C_2, and C_3 are connected in series with the load and the input voltage V_{in} via switches S_2, S_3, S_5, S_7, S_9, and S_{10}. In this state, the output voltage $v_{ab} = -(v_{C1} + v_{C2} + v_{C3} + V_{in}) = -3V_{in}$ giving a negative voltage to the load three times the input voltage.

Thus, the AC terminals may obtain 13 voltage levels for both directions of load current regardless of load type—resistive, inductive, or capacitive. This verifies the proposed structure works under diverse loads. It is

(x) State $\emptyset_{10}$: In Figure 11, switches S_2, S_4, S_5, S_8 and S_{10} operate simultaneously to connect load terminals to capacitor C_1. The output voltage $v_{ab} = -v_{C1} = -V_{in}$ causes the load to receive a negative full input voltage. With switch S_4, capacitor C_1 is charged to V_{in} via diode D in parallel with the dc source. In parallel with the dc source, switches S_5, S_6, S_8 and S_9 link capacitors C_2 and C_3 in series. The setup charges both capacitors, C_2 and C_3, to $0.5V_{in}$ each. This condition efficiently inverts the output voltage while maintaining capacitor charge levels, ensuring the inverter outputs the desired negative voltage and operates efficiently.

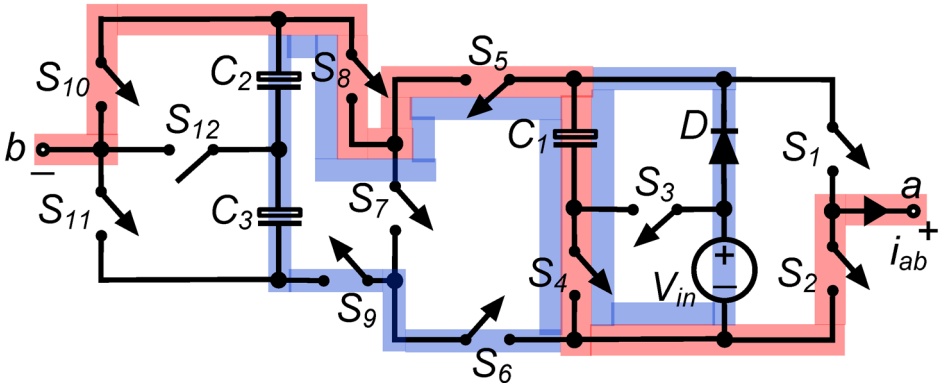


Fig. 11. Working state $\emptyset_{10}$ of the PI $[v_{ab} = -V_{in}]$.

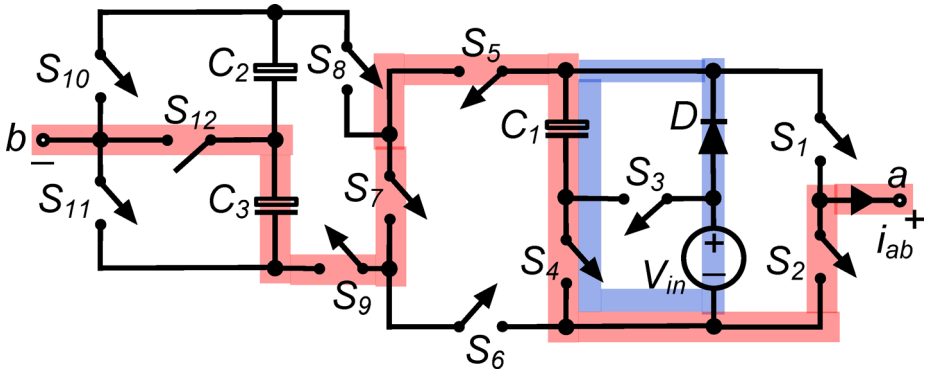


Fig. 12. Working state $\emptyset_{11}$ of the PI $[v_{ab} = -1.5V_{in}]$.

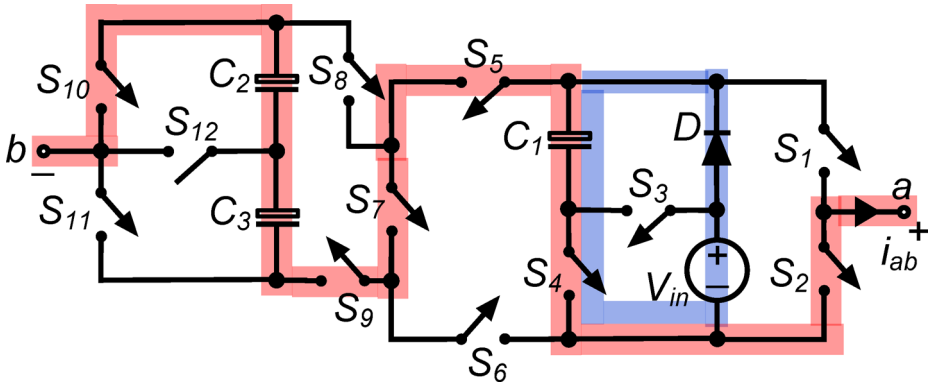


Fig. 13. Working state $\emptyset_{12}$ of the PI $[v_{ab} = -2V_{in}]$.

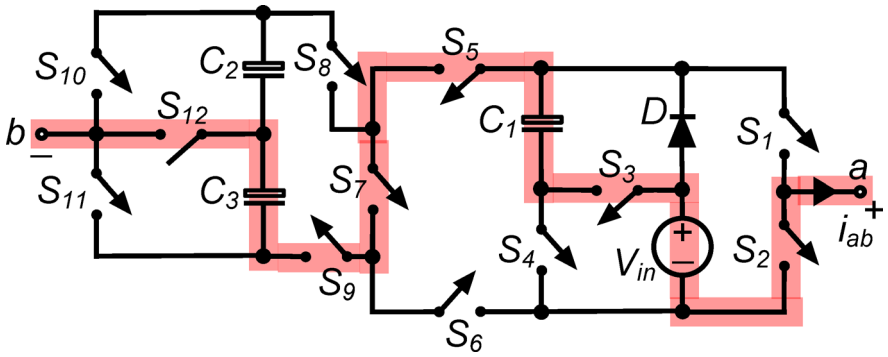


Fig. 14. Working state $\emptyset_{13}$ of the PI [$v_{ab} = -2.5V_{in}$].

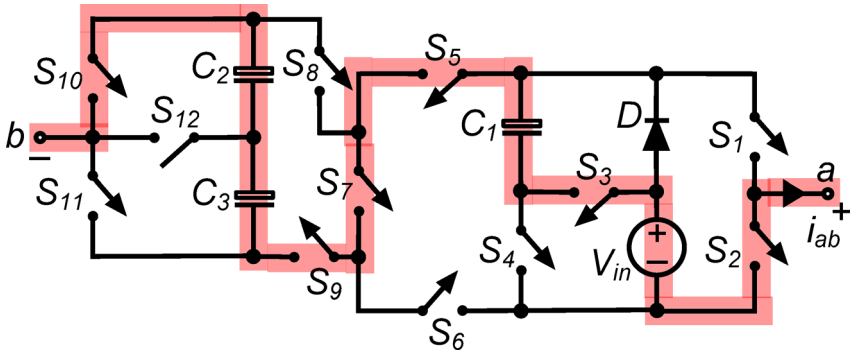


Fig. 15. Working state $\emptyset_{14}$ of the PI [$v_{ab} = -3V_{in}$].

observed that capacitor C_1 is connected in parallel with the input DC source in ten of the fourteen states; however, in six of the states, the combination of capacitors C_2 and C_3 is in parallel with the input DC source, preserving its charge. This property keeps three capacitors self-balance. Since each capacitor is in a non-charging phase, the amount each capacitor discharges is dependent on the time spent in each state, the c3urrent across the load, and the angle between the voltage and current. This characteristic is given as follows.

$$Q_C = \int_{t_x}^{t_y} I_{ab} \sin(2\pi f_o t - \varphi)\, dt \tag{1}$$

In this analysis, f_o represents power frequency, φ represents load power factor angle, I_{ab} is the peak load current i_{ab}, and ($t_y - t_x$) shows the duration of the operating situation. In order to ensure that the capacitors remain self-balanced without the need for additional control, the value of capacitors is ascertained and determined as per the load requirement of a particular application. To minimize voltage ripples and deliver the specified load power, the capacitance needs to be large enough. The required capacitance can be calculated as follows:

$$C = \frac{P}{2\pi * 2f_o * (\Delta V_c) * V_{ab}^2} \tag{2}$$

where P is active power, V_{ab} is the root-mean-squared value of the load voltage v_{ab} and ΔV_C is the capacitor voltage ripple.

Thus, the designed SCMLI, has the following valid conditions:

$$\text{No. of levels}, N_L = 13 \tag{3}$$

$$\text{No. of main power switches}, N_S = 13 \tag{4}$$

$$\text{No. of main diodes}, N_D = 13 \tag{5}$$

$$\text{No. of auxiliary diodes}, N_{AD} = 1 \tag{6}$$

$$\text{No. of gate driver units}, N_{GD} = 12 \tag{7}$$

$$\text{No. of input dc sources}, N_{IS} = 1 \tag{8}$$

$$\text{No. of capacitors, } N_C = 3 \tag{9}$$

$$\text{Voltage gain, } V_G = 3 \tag{10}$$

Here, the bidirectional-blocking-bidirectional-conducting switch is accounted for using two power switches in a common emitter connection. Hence, the total number of power switches in (4) is taken as thirteen. Also, as a common emitter connection is used, a common gate driver unit will suffice, and hence, the total number of gate driver units is taken to be twelve in (7) above.

Comparison with other scmlis

While classical topologies typically achieve a voltage gain of unity, switched capacitor-based structures provide gains exceeding unity. Therefore, the PI is evaluated against recent literature of various switched capacitor-based structures. Table 2 outlines a comparison with contemporary topologies based on device count, while Table 3 extends this comparison to TSV and PIV requirements, both crucial for reliability and applicability[2,11]. Regardless of the total number of output levels produced, a standardized matching between structures can be obtained through the evaluation of the number of components employed per synthesized output level. Analysis presented in the ninth column of Table 2 shows the component efficiency of each structure, which allows for an unbiased assessment of their relative performance.

From Table 2, it is evident that the PI entails a reduced number of components per level in contrast to[5,26], with the latter exhibiting even lower component counts. However, on examining Table 3, the TSV and PIV of topologies in[5,26] are high as compared to the PI. In fact, a methodology to incorporate the component count and TSV in a single parameter (called cost function 'CF') is presented in[7] for evaluating a topology and is widely used to determine the merit of an SCMLI[5]. It is defined as[7]:

$$CF = \frac{N_{IS}}{N_L} * (N_S + N_D + N_{AD} + N_{GD} + N_C + TSV) \tag{11}$$

Table 3 records the C.F. for all the topologies under comparison, and it can be observed that the suggested topology is the most competent amongst the contemporary ones in terms of C.F. The THD comparison with similar structures is presented in Table 4, highlighting the superior performance of the proposed design. Figure 16 illustrates the graphical representation of CF, device count per level, TSV per level per unit with respect to V_{in} (X), PIV per level per unit with respect to V_{in}(Y) and voltage THD.

Literature	N_L	N_{IS}	N_S	N_D	N_{AD}	N_{GD}	N_C	Device count per level
[4]	13	2	16	16	2	16	4	4.30
[5]	13	1	10	10	4	10	4	3.00
[6]	5	1	9	9	0	9	1	5.80
[7]	9	1	10	10	1	8	2	3.55
[8]	9	1	12	12	0	11	2	4.22
[9]	7	1	10	10	0	10	2	4.71
[10]	5	1	6	6	2	6	1	4.40
[11]	7	1	16	16	0	14	2	7.00
[12]	5	1	6	6	2	6	2	4.60
[13]	5	1	9	9	1	8	1	5.80
[14]	5	1	6	6	1	6	1	4.20
[15]	5	1	12	12	0	12	2	7.80
[16]	5	1	7	7	3	7	2	5.40
[17]	9	1	11	11	0	10	2	3.88
[8]	9	1	12	12	0	11	2	4.22
[18]	9	1	11	11	0	10	2	3.89
[19]	13	1	14	14	1	14	3	3.62
[20]	13	1	13	13	2	13	3	3.46
[21]	9	1	11	11	0	10	2	3.89
[22]	13	1	13	13	2	13	3	3.46
[23]	13	1	13	13	2	13	3	3.46
[24]	13	1	15	15	-	15	3	3.77
[25]	5	1	8	8	1	8	2	5.60
[26]	13	2	11	11	1	11	2	2.92
Proposed	13	1	13	13	1	12	3	3.30

Table 2. Comparison of the PI with other switched capacitors-based topologies.

Reference	N_L	TSV	PIV	X	Y	C.F
[4]	13	$34V_{in}$	$6V_{in}$	2.615	0.462	13.538
[5]	13	$33V_{in}$	$5V_{in}$	2.538	0.385	5.462
[6]	5	$9V_{in}$	V_{in}	1.800	0.200	7.400
[7]	9	$11V_{in}$	$2V_{in}$	1.222	0.222	4.667
[8]	9	$11V_{in}$	V_{in}	1.222	0.111	5.333
[9]	7	$18V_{in}$	$3V_{in}$	2.571	0.428	7.143
[10]	5	$12V_{in}$	$2V_{in}$	2.400	0.400	6.600
[11]	7	$16V_{in}$	$2V_{in}$	2.285	0.285	9.143
[12]	5	$8V_{in}$	V_{in}	1.600	0.200	6.000
[13]	5	$9V_{in}$	V_{in}	1.800	0.200	7.400
[14]	5	$11V_{in}$	$2V_{in}$	2.200	0.400	6.200
[15]	5	$20V_{in}$	V_{in}	4.000	0.200	11.600
[16]	5	$9V_{in}$	V_{in}	1.800	0.200	7.000
[17]	9	$10V_{in}$	V_{in}	1.111	0.111	4.889
[8]	9	$11V_{in}$	V_{in}	1.222	0.111	5.333
[18]	9	$10V_{in}$	V_{in}	1.111	0.111	4.889
[19]	13	$28V_{in}$	$3V_{in}$	2.154	0.231	5.692
[20]	13	$33V_{in}$	$3V_{in}$	2.538	0.231	5.923
[21]	9	$10V_{in}$	V_{in}	1.111	0.111	4.889
[22]	13	$32V_{in}$	V_{in}	2.462	0.077	5.846
[23]	13	$33V_{in}$	$3V_{in}$	2.538	0.231	5.923
[24]	13	$30V_{in}$	$3V_{in}$	2.308	0.231	6.000
[25]	5	$12V_{in}$	$2V_{in}$	2.400	0.400	7.800
[26]	13	$31V_{in}$	$5V_{in}$	2.385	0.385	5.154
Proposed	13	$17V_{in}$	$2V_{in}$	1.307	0.153	4.538

Table 3. Evaluation of the suggested topology against other SCMLI topologies based on TSV, PIV for input DC voltage V_{in}, and cost function.

Reference	Voltage THD	Current THD
[19]	7.2	0.7
[22]	7.4	0.8
[23]	7.2	0.6
[24]	7.4	0.8
[25]	7.2	0.6
[26]	7.5	1
[P]	7.2	0.6

Table 4. THD comparison with similar structure.

Switching methodology

The suggested topology can be generalized for different multilevel inverter topologies with proper modifications. Thus, this work uses the multicarrier PWM scheme proposed in[30] because it has the possibility of using both null states. The technique, as depicted in Fig. 17(a), employed 12-triangular high-frequency waveforms $V_{crj}\{j = 1 \text{ to } 12\}$ as carriers in phase opposition. The waveforms are exhibited at low frequency for clarity. A sinusoidal waveform V_{ref} with frequency f_o serves as the reference signal. In Fig. 17(b), reference and carrier signals are shown. Comparators continuously compare reference and carrier signals. Comparators output values of 1, 2, 3, 4, 5, 6, 0, −1, −2, −3, −4, and -5 when $V_{ref} > V_{crj}$. On the other hand, comparators produce the corresponding outputs as 0, 1, 2, 3, 4, 5, −1, −2, −3, −4, −5, and −6 if the $V_{ref} < V_{crj}$. An aggregated signal 'a' is obtained by adding signals $a_j\{j = 1 \text{ to } 12\}$, as shown in Fig. 17(c).

The signal 'a' is an aggregated waveform consisting of seven discrete positive levels, ranging from 15 to 21 in increments of + 1, and seven discrete negative levels, ranging from −15 to −21 in decrements of −1. The triggering pulses are produced in a 1:1 relationship with the levels at the output waveform as depicted in Fig. 17(a).

Power losses

Three forms of power losses occur in a switched-capacitor-based MLI: capacitor, switching, and conduction[9,10,31]. The following losses are briefly discussed:

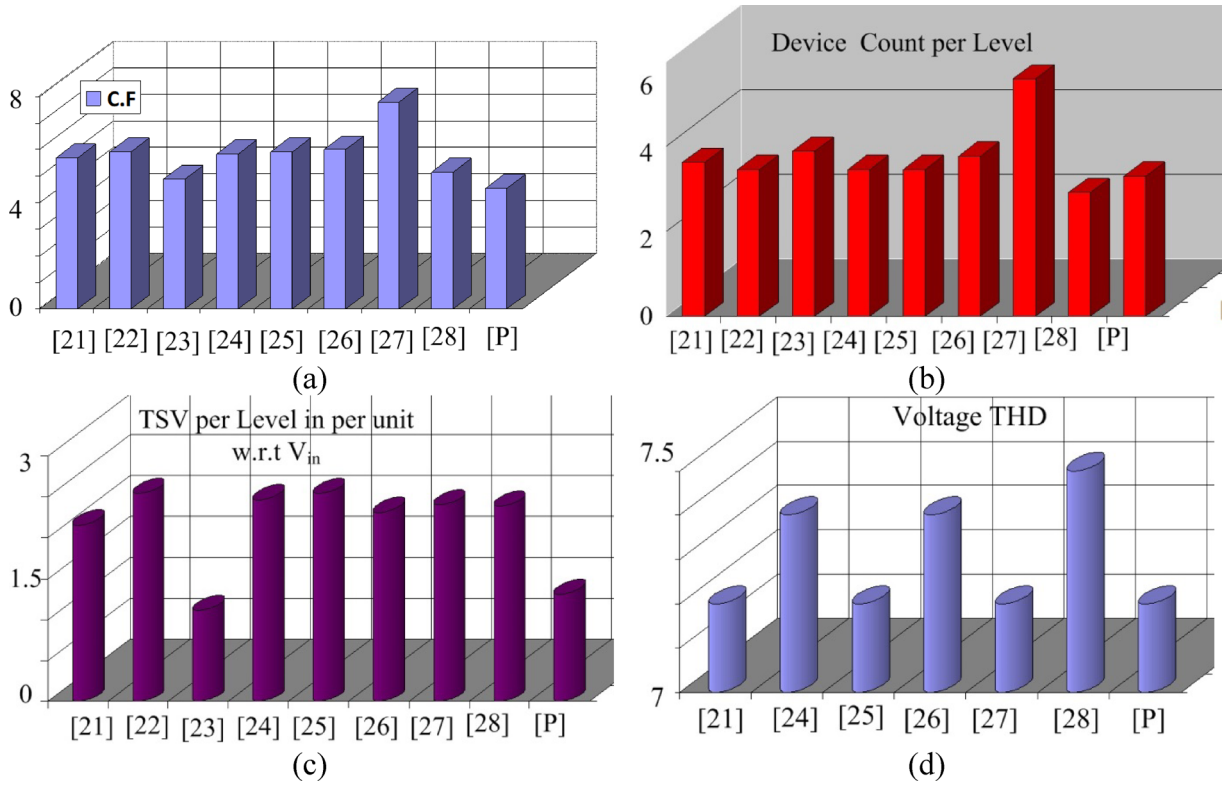


Fig. 16. Graphical representation (**a**) CF (**b**) Device count per level (**c**) TSV level per unit w.r.t V_{in} (**d**) Voltage THD.

(a) Power losses in capacitors: The following equation[9] calculates capacitor voltage ripple for each inverter operational state:

$$\Delta V_C = \frac{1}{C}\int_{t_x}^{t_y} i_C dt \tag{12}$$

Here, i_C is the current through a switched capacitor, (t_y—t_x) is the discharging time span, and C is the capacitance value. Hence, for each of the states used for level generation, the power losses due to capacitor ripples as (f_o being the power frequency):

$$P_{\text{Ripple Losses}} = \frac{f_o}{2} C (\Delta V_c)^2 \tag{13}$$

In switched capacitors of the topology, power losses also take place due to equivalent series resistance (ESR) of a given capacitor (R_{ESR}). Thus, the conduction losses in each switched capacitor can be calculated as:

$$P_{\text{Conduction losses in C}} = \frac{R_{ESR} f_o}{2}\int_{t_x}^{t_y} i_C^2 dt \tag{14}$$

So, adding (13) and (14) gives the total power losses taking place in a given switched capacitor of an SCMLI.

(b) Switching power losses: During switching in a power semiconductor device, the intrinsic delays lead to switching losses. For each of the power switches, the losses during turning ON and OFF can be obtained as [9]:

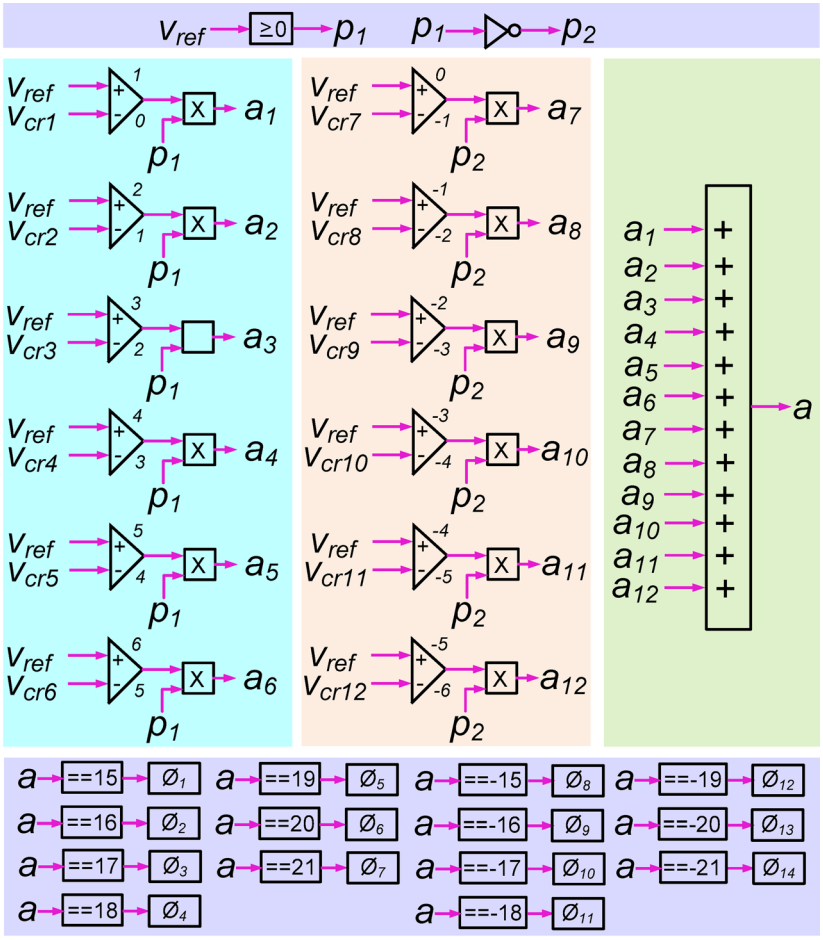
$$P_{\text{Switching Losses}} = \frac{1}{6} V_{in} i(t) \{t_{ON} + t_{OFF}\} f_s \tag{15}$$

where, V_{in} = voltage stress bear by the switch during its OFF state; i(t) = current bearing capability of the switch during conduction; t_{ON} = the time at which the switch is ON; t_{OFF} = the time at which the switch is OFF; f_s = switching frequency.

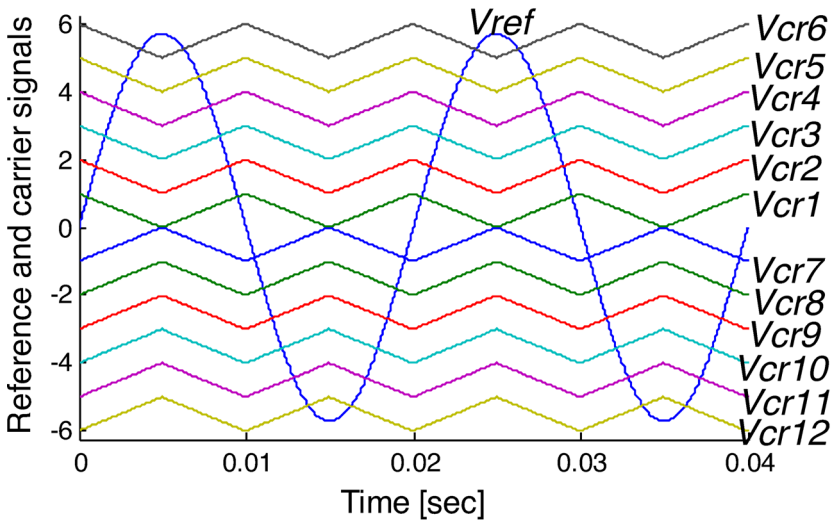
(c) Conduction sosses: Conduction losses for the transistor and diode part of a given power switch are obtained using the following equations with the description of the variables given in[17]:

$$P_{\text{Conduction Losses of Transistor}} = V_{on,\,sw} I_{sw,\,avg} + R_{on,\,sw} I^2_{sw,\,rms} \tag{16}$$

$$P_{\text{Conduction Losses of Diode}} = V_{on,\,d} I_{d,\,avg} + R_{on,d} I^2_{d,rms} \tag{17}$$

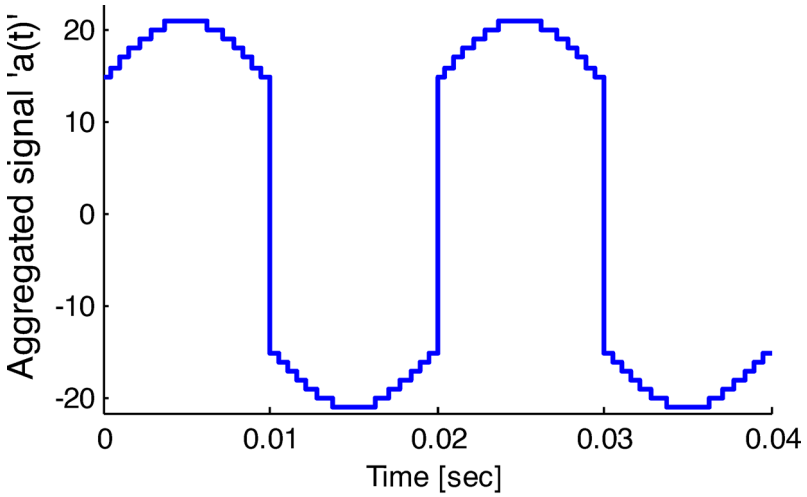


(a)



(b)

Fig. 17. (**a**) Switching strategy of designed SCMLI; (**b**) V_{ref} and V_{crj}; and (**c**) Aggregated signal 'a'.



(c)

Fig. 17. (continued)

Losses	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{10}	S_{12}
Switching loss	0.273	0.221	1.33	0.622	0.78	0.73	1.01	1.02	0.597	0.624	0.385	0.534
Conduction loss	0.87	0.906	1.99	2.44	1.27	1.30	1.54	1.054	4.09	3.99	4.20	0.87

Table 5. Individual losses (in Watt).

Therefore, the power losses of the proposed SCMLI can be calculated as an aggregation of these losses. The losses occurred by individual switches are analyzed and presented in Table 5.

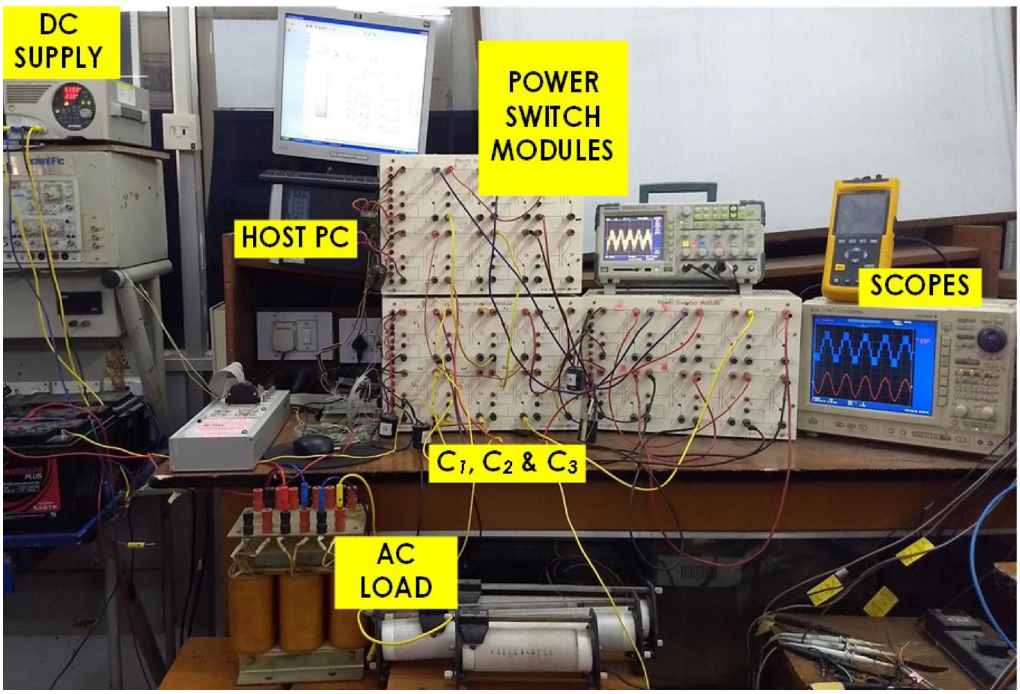


Fig. 18. Prototype of the PI.

Experimental verification

To experimentally verify the designed converter, a lab test bench was implemented with discrete switches, such as IRF460 MOSFETs, and appropriate gate drivers, as depicted in Fig. 18. The input voltage was calibrated to 100 V, and capacitances of 2200, have been adopted for C_1, C_2 and C_3. The dSPACE DS1103 was employed to create a gate pulse. The carrier and reference signal were at 1 kHz and 50 Hz, respectively, with a modulation index of 0.95. The load terminals were connected to an inductive load, a 50-Ω resistor (R), and a 170 mH inductor (L).

The voltage waveforms across the power switches are illustrated in Fig. 19, demonstrating adherence to the PIV values specified in Table 1, with V_{in} set at 100 V.

Figure 20(a) depicts the start-up response of the inverter, where the capacitors C_1, C_2, and C_3 achieve self-balancing at 100 V, 50 V, and 50 V, respectively. As shown in Fig. 20(b), even when the load varies, the voltage waveforms remain unchanged. The output is a 13-level waveform with 50 V step increments, as anticipated. Hence, the feasibility of the PI is confirmed through its performance and the capacitors' ability to self-balance. Figure 20(c) presents the results for a purely resistive load. It is observed that under resistive loading conditions, the capacitors maintain self-balancing, and the output voltage remains stable. Figure 20(d) illustrates the results under varying modulation index conditions. It is observed that despite the change in modulation index, the capacitors sustain self-balancing, while the output voltage adjusts correspondingly. The harmonic spectra of the voltage and current waveforms are illustrated in Fig. 20(e) and (f). The corresponding THD values for the voltage and current waveforms are 7.2% and 0.6%, respectively. Figure 20(g) presents both theoretical and experimental efficiencies, indicating that the experimental efficiency, at 96.7%, is slightly lower than theoretical value.

SBased on the literature review, MLIs have potential applications in the following areas:

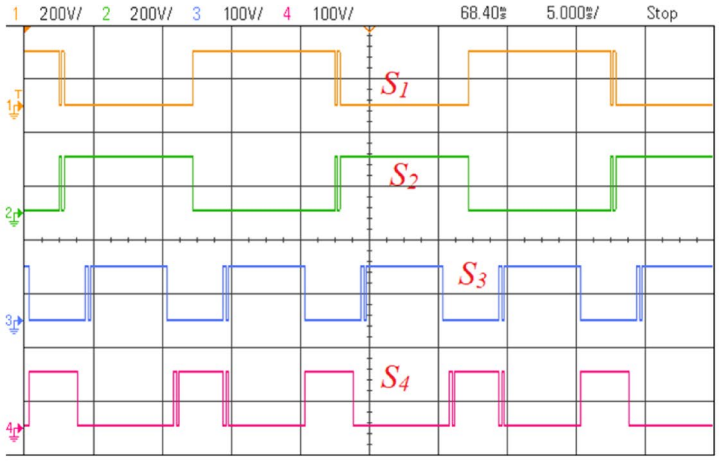
(i) The power distribution system for high-frequency alternating current (HFAC): The elimination of filter stages and rectifiers from high-frequency alternating current (HFAC) power distribution systems (PDS) enhances power density, heat distribution, efficiency, and reduces the number of components compared to typical direct current (DCPDS) systems[26,30]. HFAC PDS improves system efficiency and finds use in electric vehicles, lights, microgrids, computers, and telecommunications[31]. One common method for making HFAC PDS more reliable is to use SCMLIs[4].

(ii) Based on photovoltaic power generation systems: Photovoltaic systems produce minimal electricity, necessitating voltage amplification for grid integration. This can be accomplished using PV module cascading, DC-DC converters, or step-up transformers on the inverter's AC side. However, these strategies elevate expenses, mass, and inefficiencies. SCMLIs provide benefits such as capacitor self-balancing, decreased filtering, enhanced voltage gain, and grid-compatible waveforms[9,27].

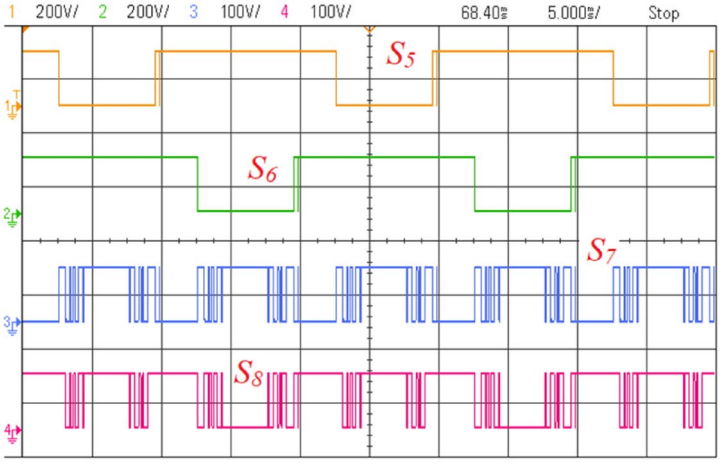
(iii) Electric vehicle traction system (EVTS): EVTS are generally arranged in two configurations: (a) a direct connection from the battery to the inverter or (b) a connection from the battery- DC-DC converter. The former necessitates more series cells for elevated DC-link voltage, whereas the latter escalates expense and complexity. SCMLIs effectively tackle these difficulties, improving output voltage and system speed[7,28].

Conclusion

This paper presents a single-phase thirteen-level inverter with three capacitors for three-fold voltage boosting capability. The proposed switched capacitor inverter presents PIVs much lower than the operating voltage for most of the power-switching devices. The suggested topology and control strategy enables the capacitors to self-balance their voltage. A comparison with the existing topologies shows that the proposed design provides a smaller number of components, a lesser total standing voltage, and a more economical cost. The findings demonstrate that the proposed 13-level SC-MLI not only meets the harmonic standards but also offers a reliable and efficient solution with fewer components, making it a competitive option for high-performance multilevel inverter applications. Due to its high-resolution AC waveforms with increased output voltage, this inverter is ideal for applications where low voltage power supply is used as DC source input, such as integration of renewable energy sources into the grid, photovoltaic systems, and electric vehicles.



(a)



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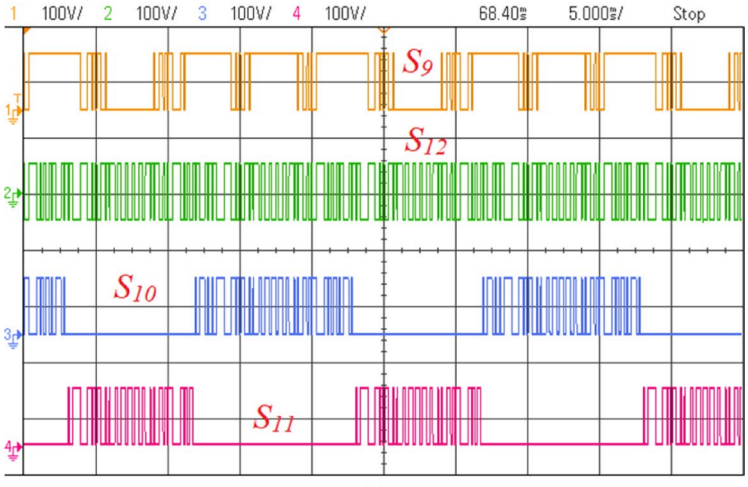
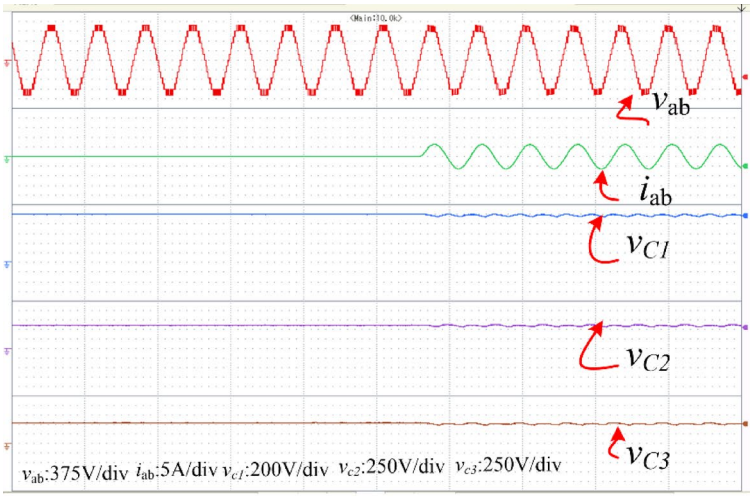


(c)

Fig. 19. (**a**–**c**) Voltage waveforms across power switches.



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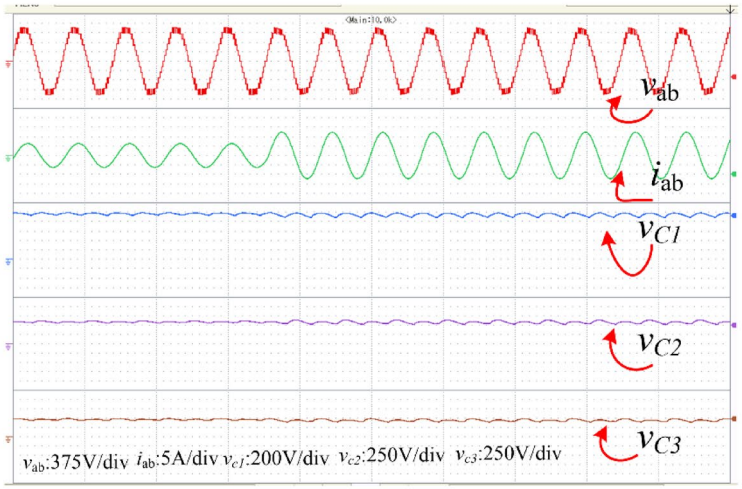

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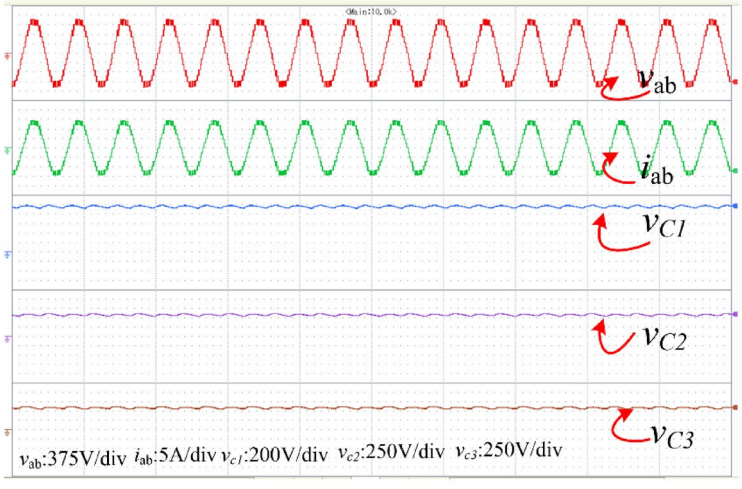
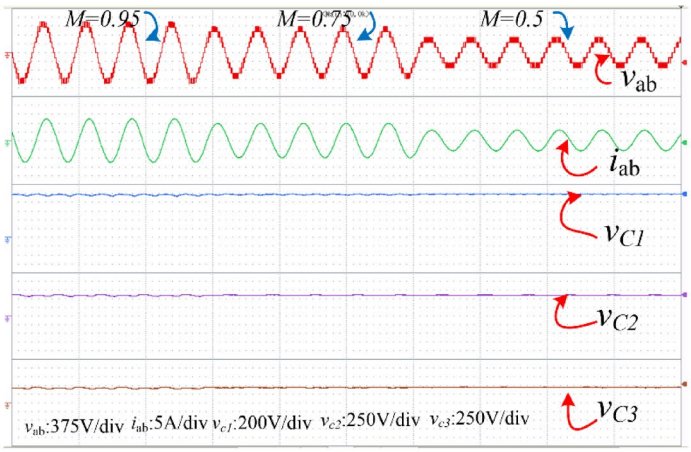
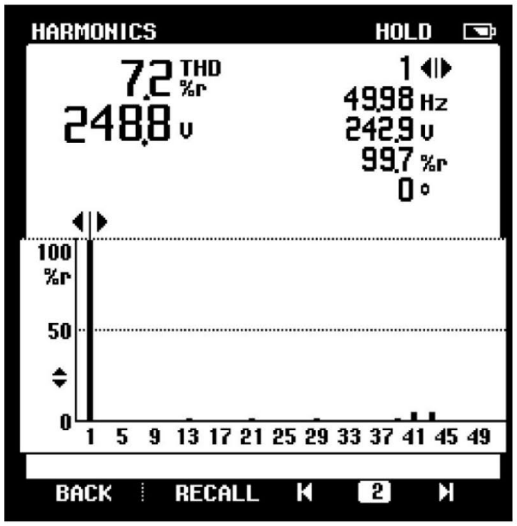


(c)

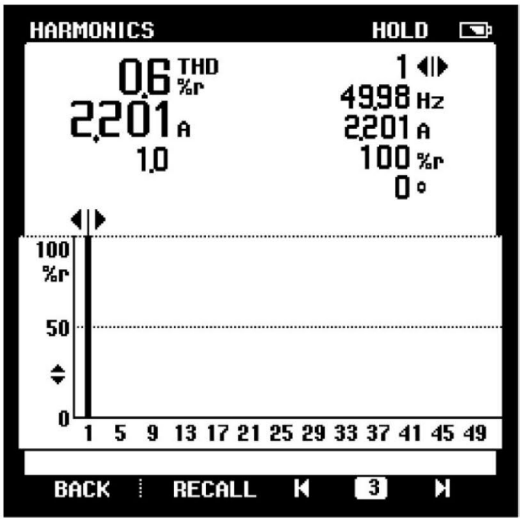
Fig. 20. Experimental results: (**a**) Start-in response with waveforms of load voltage, load current, and capacitor voltages; and (**b**) Waveforms when the load is increased. (**c**) R-load (**d**) Change in Modulation index (**e**) THD of the output voltage and (**f**) THD of Load current (**g**) Efficiency comparison.



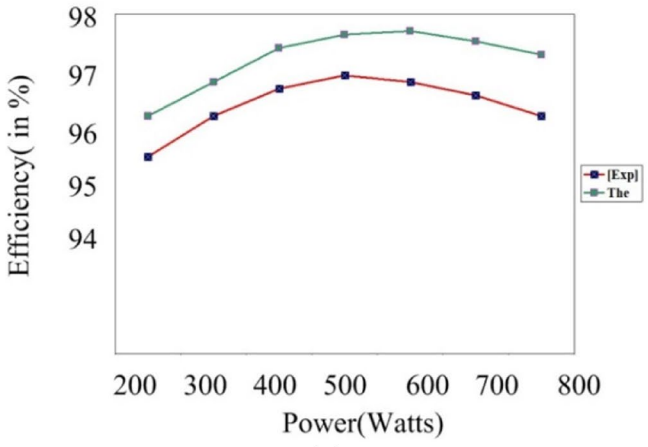
(d)



(e)



(f)



(g)

Fig. 20. (continued)

Data availability

The datasets used and/or analyzed during the current study available from the corresponding author on reasonable request.

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Author contributions

Methodology: NKD, and KJ; Conceptualization: NKD, KJ, DUS; visualization: NKD, KJ, DUS, TKT, MM; writing—original draft preparation: NKD, KJ, DUS, MM; writing—review and editing: NKD, KJ, TKT, DUS, MM; Revising manuscript: NKD, KJ, TKT, DUS, MM.

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Declarations

Competing interests
The authors declare no competing interests.

Ethical approval
This is to confirm that all methods were carried out in accordance with relevant guidelines and regulations in this research work. All the protocols received approval from Manipal Institute of Technology, Manipal Academy of Higher Education, Manipal, 576104, India.

Additional information
Correspondence and requests for materials should be addressed to N.K.D.

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