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A new coupled-inductor-free bidirectional DC-DC converter with low current ripple in both sides

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The proposed bidirectional converter exhibits a superior voltage gain compared to conventional designs and maintains low current ripple on both sides, making it highly suitable for photovoltaic and fuel cell applications. Notable features include the use of compact output filter capacitors, adequate voltage gain in both operational modes, and the elimination of coupled inductors. In step-up operation, switches S_1 and S_2 are activated simultaneously, while in step-down operation, switches S_3, S_4, and S_5 are triggered at the same time. This switching scheme enables the converter to operate in each mode with a single PWM control signal, thereby simplifying the control circuitry. A thorough analysis has been carried out for both operating modes, and experimental verification using a 400 W prototype has confirmed a peak efficiency of 96.3%, validating the theoretical predictions.

Keywords Bidirectional converter, Step-up, Low ripple, Power density

Bidirectional converters support power transfer in both directions, making them ideal for EVs, smart grids, UPS, aerospace, and renewable energy applications[1–3]. Their ability to interface sources with storage removes the need for separate converters, resulting in more compact designs and higher efficiency. Bidirectional DC–DC converters (BDCs) can be classified as either isolated or non-isolated. In isolated architectures, a high-frequency transformer facilitates the DC–AC–DC conversion process while ensuring galvanic isolation between the low-voltage side (LVS) and the high-voltage side (HVS). In applications where isolation is unnecessary, non-isolated BDCs are generally preferred owing to their reduced structural complexity and simplified control requirements.

Non-isolated converter configurations include Cuk, SEPIC/Zeta, coupled-inductor, conventional buck–boost, three-level[4–7], multilevel, and switched-capacitor types[8]. For Cuk and SEPIC/Zeta designs, the cascaded two-stage arrangement leads to lower conversion efficiency[9,10]. While coupled-inductor converters can deliver high voltage gain by adjusting the turns ratio[11], they face persistent issues with leakage inductance, and their power processing capability is constrained by the magnetic core capacity. A coupled-inductor-based modification of the SEPIC converter was proposed in[12], achieving high efficiency, high voltage gain, and soft-switching operation, but at the expense of additional active switches and capacitors. Battery charging and discharging are typically managed by bidirectional DC-DC converters (BDDCs), which must provide high buck gain during charging and high boost gain during discharging, while minimizing or eliminating current ripple on the battery side[13–16]. A wide range of converter designs and control techniques have been developed to address source current ripple. Coupled-inductor high-gain converters can significantly suppress ripple by selecting an appropriate turns ratio, but this enables either high voltage gain or ripple cancellation, not both at once. Non-coupled-inductor converters aimed at low source current ripple are generally classified into two groups: methods that decrease ripple amplitude and those that completely eliminate it at a specific duty ratio[17].

Switched-capacitor converters offer a straightforward structure, simple control, and high scalability. By directing capacitor charge and discharge through different paths, energy can be transferred between the low- and high-voltage sides to attain high voltage gain. Early single-capacitor bidirectional designs[18,19] exhibited low efficiency, leading to the development of interleaved switched-capacitor converter[20] aimed at minimizing input current ripple. An interleaved configuration can effectively suppress significant current ripple on the low-voltage side (LVS)[21]. Complete ripple cancellation, however, requires the duty cycle to be locked to a specific ratio determined by the interleaving phase count. Ripple injection circuits, classified as active or passive, offer another suppression method. In the active scheme[22], a ripple mirror circuit offset the inherent LVS ripple. Yet, eliminating the ripple entirely necessitates a fixed duty cycle, thereby constraining the attainable voltage conversion range. Reference[23] introduced a DC–DC converter using voltage multiplier cells, providing high conversion ratio and low voltage stress. However, attaining such high gain necessitates multiple multiplier cells, which reduces power density and raises cost. In other works[24–27], coupled-inductor designs achieve high voltage

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gain by adjusting the turns ratio of the magnetic components. A persistent drawback is leakage inductance, which induces voltage spikes on the switches, requiring snubber circuits to recover the associated energy. Reference[28] introduces an active filter for source current ripple suppression, consisting of two switches, an inductor, and two capacitors. Although the converter's voltage gain is preserved, the added components increase size and lower power density. The filter capacitors are regulated by separate converters operating at different frequencies and duty cycles, necessitating additional control circuitry and an isolation transformer. In[29], a synchronous-switching bidirectional DC–DC converter was studied for LV-side ripple elimination, though it produced high HV-side ripple and used many switches.

The main contributions of this work are as follows: the development of a converter topology capable of maintaining low current ripple on both the high- and low-voltage sides; improved voltage gain in step-up operation and reduced gain in step-down operation; and the introduction of a design free from coupled inductors and switched capacitors, thereby enhancing power density while mitigating problems associated with leakage inductance and inrush current. In summary, this work presents a new bidirectional high step-up/step-down DC–DC converter topology that achieves high voltage gain with low device stress. Unlike most existing converters, the proposed design is free from coupled inductors and switched-capacitor networks, resulting in a simpler structure, reduced component count, and higher overall efficiency.

In this paper, Sect."The proposed bidirectional converter" presents the description of the proposed converter along with its operation in both step-up and step-down modes. The steady-state analysis and design equations are provided in Sect. "Steady-state analysis of the proposed converter". In Sect. "Small-signal analysis and controller design of the converter", the small-signal model of the proposed converter for both operating modes is developed, and stability considerations are discussed. To benchmark the proposed topology against prior works, a comprehensive comparison is conducted in Sect. "Comparative assessment with recent advances". Finally, Sect. "Loss analysis of a bidirectional DC-DC converter" provides the experimental results of a 400 W prototype to validate the theoretical analyses.

The proposed bidirectional converter

The proposed bidirectional converter, depicted in Fig. 1, consists of five switches, three inductors, and three capacitors. In the forward mode, switches S_1 and S_2 are simultaneously triggered while switches S_3 through S_5 remain off. Conversely, in the backward mode, switches S_3 and S_4 are triggered in a similar manner, with S_1 and S_2 turned off. Therefore, a single PWM pulse is sufficient to control the converter in both operating modes. During state 2 of both step-up and step-down modes, the MOSFET body diodes conduct naturally when the corresponding switches are turned off, providing a freewheeling path for the inductor currents and ensuring continuous current flow.

Converter operation

For ease of analyzing the steady-state characteristics of the proposed converter, the following practical assumptions are applied: (a) all power semiconductor devices and energy storage elements are considered ideal, and the converter operates under continuous conduction mode (CCM); (b) the capacitances are sufficiently large such that the voltage across each capacitor remains essentially constant during each switching cycle. In each mode of operation, the converter functions in continuous conduction mode (CCM) and exhibits two separate switching modes. Figure 2 depicts the key waveforms in both the step-up and step-down operating modes. Figures 3 and 4 show the equivalent circuits of the converter in the step-up and step-down modes, respectively.

$$V_{C1} = V_{C2} = V_C \tag{1}$$

$$C_1 = C_2 = C \tag{2}$$

$$\frac{di_{L1}}{dt} = \frac{V_L}{L_1} \tag{3}$$

$$\frac{di_{L2}}{dt} = \frac{V_{C1} + V_{C2}}{L_2} \tag{4}$$

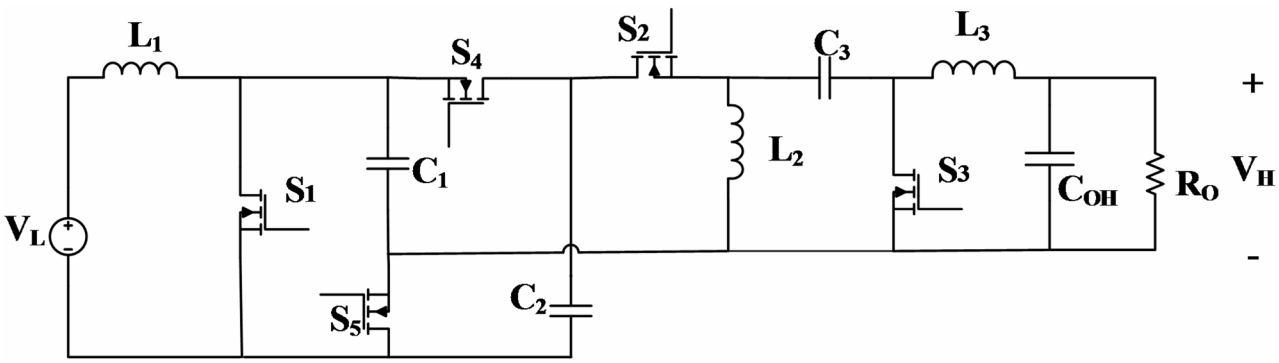


Fig. 1. Circuit schematic of the proposed bidirectional converter.

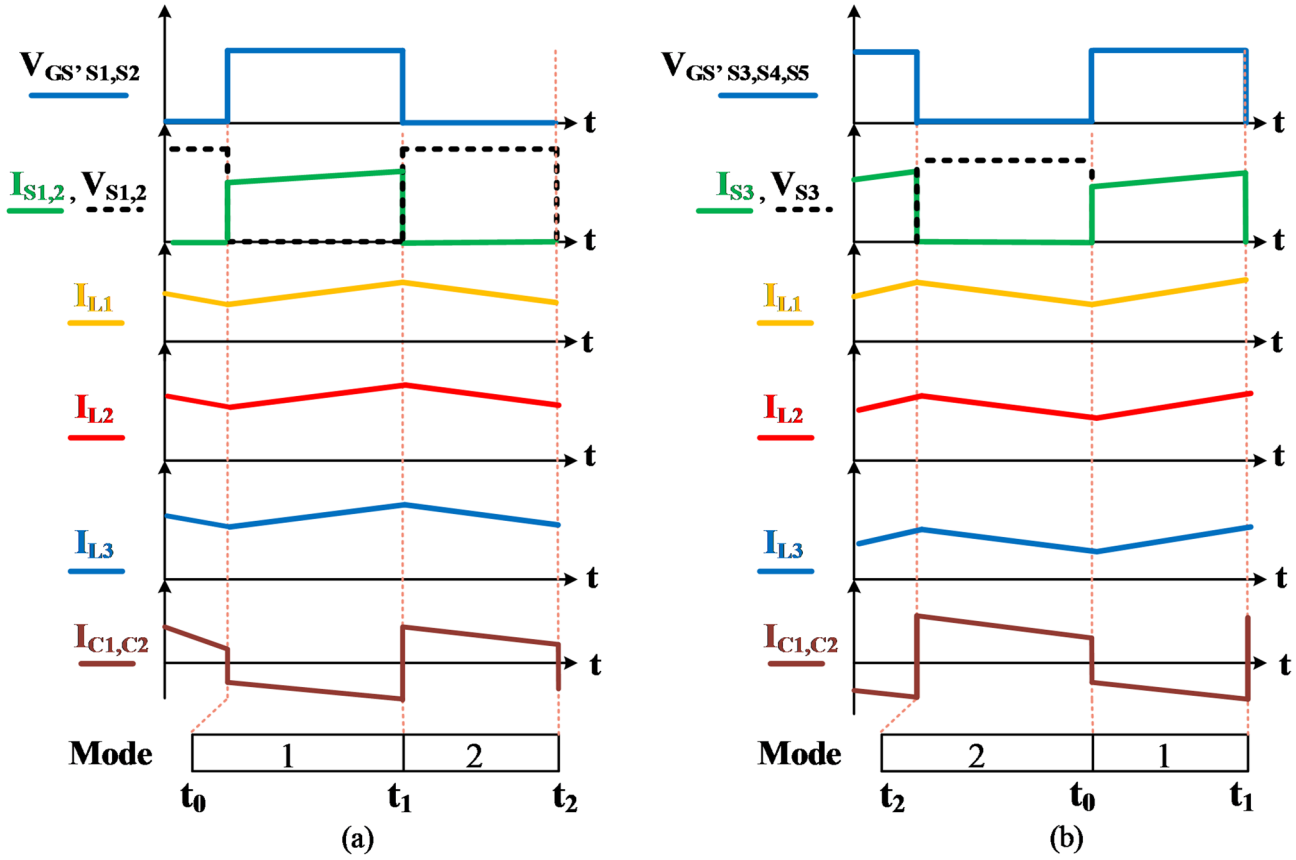


Fig. 2. Representative waveforms of the proposed converter: **(a)** step-up operation; **(b)** step-down operation.

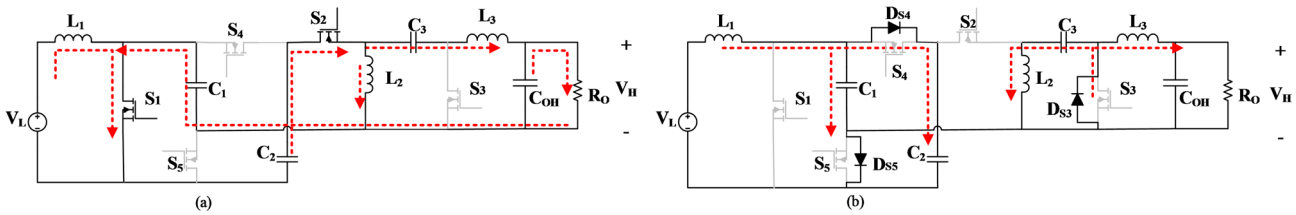


Fig. 3. Equivalent circuit of the converter in step-up mode: **(a)** first state; **(b)** second state.

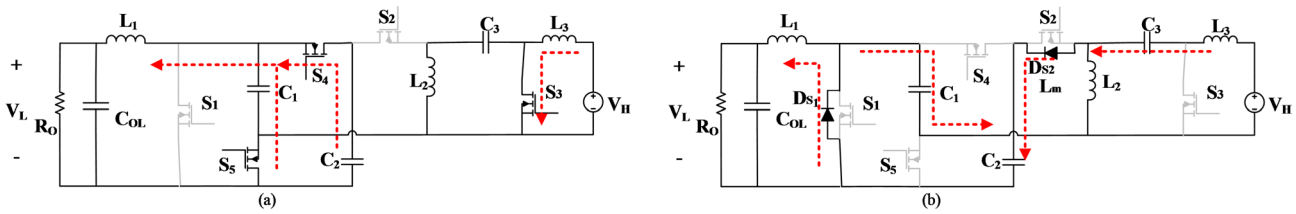


Fig. 4. Equivalent circuit of the converter in step-down mode: **(a)** first state; **(b)** second state.

$$\frac{di_{L3}}{dt} = \frac{V_{C2} + V_{C3} - V_H + V_{C1}}{L_3} \tag{5}$$

$$\frac{dV_C}{dt} = -\frac{i_{L3} + i_{L2}}{C} \tag{6}$$

$$\frac{dV_{C3}}{dt} = \frac{-i_{L3}}{C_3} \tag{7}$$

$$\frac{dV_H}{dt} = \frac{\frac{-V_H}{R_o} + i_{L3}}{C_{oH}} \tag{8}$$

Step-up mode

State 1: switches S_1 and S_2 remain ON, while S_3, S_4, and S_5 are kept OFF. Under these conditions, inductors L_1 and L_3 store energy, whereas capacitors C_1, C_2, and C_3 release their stored charge. During this period, the load is powered entirely by the output capacitor C_{oH}. The corresponding state-space equations for the converter in this operating state are expressed as follows.

$$V_{C1} = V_{C2} = V_C \tag{9}$$

State 2: With switches S_1 and S_2 turned off, the body diodes of S_4, S_5, and S_3 conduct. During this interval, inductors L_1 and L_3 release their stored energy to the output, while capacitors C_1, C_2, and C_3 are being charged. This mode concludes once the switches are turned on again.

$$\frac{di_{L1}}{dt} = \frac{V_L - V_C}{L_1} \tag{10}$$

$$\frac{di_{L2}}{dt} = \frac{-V_{C3}}{L_2} \tag{11}$$

$$\frac{di_{L3}}{dt} = \frac{-V_H}{L_3} \tag{12}$$

$$\frac{dV_C}{dt} = \frac{i_{L1}}{2C} \tag{13}$$

$$\frac{dV_{C3}}{dt} = \frac{i_{L2}}{C_3} \tag{14}$$

$$\frac{dV_H}{dt} = \frac{\frac{-V_H}{R_o} + i_{L3}}{C_{oH}} \tag{15}$$

Step-down mode

State1: In this state, switches S_4, S_5, and S_3 are in the on-state, while S_1 and S_2 remain off. Inductor L_3 is energized, and with S_1 and S_2 turned off, capacitors C_1 and C_2 are effectively paralleled, delivering their stored energy to the output via L_1. Simultaneously, capacitor C_3 supplies energy to magnetize the coupled inductor. During this mode, both L_1 and L_3 undergo a linear charging process. The state-space representation of the converter in this operating mode is expressed as follows.

$$V_{C1} = V_{C2} = V_C \tag{16}$$

$$C_1 = C_2 = C \tag{17}$$

$$\frac{di_{L1}}{dt} = \frac{V_C - V_L}{L_1} \tag{18}$$

$$\frac{di_{L2}}{dt} = \frac{V_{C3}}{L_2} \tag{19}$$

$$\frac{di_{L3}}{dt} = \frac{V_H}{L_3} \tag{20}$$

$$\frac{dV_C}{dt} = -\frac{i_{L1}}{2C} \tag{21}$$

$$\frac{dV_{C3}}{dt} = -\frac{i_{L2}}{C_3} \tag{22}$$

$$\frac{dV_L}{dt} = \frac{-\frac{V_L}{R_o} + i_{L1}}{C_{o1}} \tag{23}$$

State 2: During this stage, switches S_4, S_5, and S_3 are in the off-state, causing the body diodes of S_1 and S_2 to conduct. Consequently, inductors L_1 and L_3 release their stored energy to the output, while capacitors C_1, C_2, and C_3 are being energized.

$$\frac{di_{L1}}{dt} = \frac{-V_L}{L_1} \tag{24}$$

$$\frac{di_{L3}}{dt} = \frac{-2V_C}{L_2} \tag{25}$$

$$\frac{di_{L3}}{dt} = \frac{V_H - 2V_C}{L_3} \tag{26}$$

$$\frac{dV_C}{dt} = \frac{i_{L2} + i_{L3}}{C} \tag{27}$$

$$\frac{dV_{C3}}{dt} = \frac{i_{L3}}{C_3} \tag{28}$$

$$\frac{dV_L}{dt} = \frac{\frac{-V_L}{R_o} + i_{L1}}{C_{o1}} \tag{29}$$

Steady-state analysis of the proposed converter

This section provides a comprehensive analysis of the proposed bidirectional converter, including its voltage gain in both modes of operation, the voltage and current stresses on the components, and the design equations for the passive elements.

Voltage gain

The voltage–second balance principle is applied to all three inductors of the circuit for both step-up and step-down operation modes. Based on these formulations, the expressions for the converter voltage gain in each mode are directly derived as follow.

$$L_1 : \; V_L DT + (V_L - V_C)(1 - D)T = 0 \tag{30}$$

$$V_C = V_{C1} = V_{C2} = \frac{V_L}{(1 - D)} \tag{31}$$

$$L_2 : \; (V_{C1} + V_{C2})DT - V_{C3}(1 - D)T = 0 \tag{32}$$

$$V_{C3} = \frac{2DV_L}{(1 - D)^2} \tag{33}$$

$$L_3 : \; (V_{C1} + V_{C2} + V_{C3} - V_H)DT - V_H(1 - D)T = 0 \tag{34}$$

$$V_H = (V_{C1} + V_{C2} + V_{C3})D = \frac{2DV_L}{(1 - D)^2} \tag{35}$$

$$\frac{V_H}{V_L} = \frac{2D}{(1 - D)^2} \tag{36}$$

For step-down mode:

$$L_1 : \; (V_{C1} - V_L)DT + (-V_L)(1 - D)T = 0 \tag{37}$$

$$V_L = DV_{C1} \tag{38}$$

$$L_2 : \; -V_{C3}DT + (V_{C1} + V_{C2})(1 - D)T = 0 \tag{39}$$

$$V_{C3} = \frac{(V_{C1} + V_{C2})(1 - D)}{D} \tag{40}$$

$$L_3 : \; V_H DT + \left(V_H - (V_{C1} + V_{C2} + V_{C3})\right)(1 - D)T = 0 \tag{41}$$

$$V_H = \frac{V_{C1} + V_{C2} + V_{C3}}{1 - D} \tag{42}$$

$$V_{C1} = V_{C2} = \frac{V_L}{D} \tag{43}$$

$$\frac{V_L}{V_H} = \frac{D^2}{2(1 - D)} \tag{44}$$

Figure 5 depicts the voltage gain profiles of the converter under both step-up (Fig. 5(a) and step-down (Fig. 5(b)) operating modes.

Switch voltage stress

Using Kirchhoff's voltage law for the switch loop when the switches are OFF, the maximum voltage across them can be easily determined from the following Eq.

$$V_{S1} = V_{S4} = V_{S5} = V_C = \frac{V_L}{1-D} \tag{45}$$

$$V_{S2} = V_{C2} + V_{C3} = \frac{(1+D)V_L}{(1-D)^2} \tag{46}$$

$$V_{S3} = V_{C1} + V_{C2} + V_{C3} = \frac{2V_L}{(1-D)^2} \tag{47}$$

Passive component design

Prior to selecting the capacitance values, it is essential to determine the average currents of the capacitors. By applying the ampere–second balance principle to capacitors C_1, C_2, C_3, and C_o, and utilizing Eqs. (2) and (4), the average currents of the inductors are derived as follows:

$$I_{L1} = \frac{2DI_H}{(1-D)^2} \tag{48}$$

$$I_{L2} = \frac{DI_H}{(1-D)} \tag{49}$$

$$I_{L3} = I_H \tag{50}$$

$$L_1 \geq \frac{V_L(1-D_H)^2}{0.4I_H f} \tag{51}$$

$$L_2 \geq \frac{V_{C3}(1-D_H)^2}{0.2DI_H f} \tag{52}$$

$$L_3 \geq \frac{10D_H V_L}{(1-D_H)I_H f} \tag{53}$$

$$C_1 = C_2 \geq \frac{I_H D}{f(1-D)\Delta V_C} \tag{54}$$

$$C_3 \geq \frac{I_H D}{f\Delta V_{C3}} \tag{55}$$

Small-signal analysis and controller design of the converter

By presuming ideal characteristics for all semiconductor and passive elements, the averaged and small-signal representations are formulated using the state-space averaging technique. In the step-up configuration (Fig. 3(b)) as well as in the step-down configuration (Fig. 4(a)), conduction of S_4 and S_5 or their intrinsic diodes places C_1 and C_2 in parallel, thereby enforcing voltage equality between C_1 and C_2.

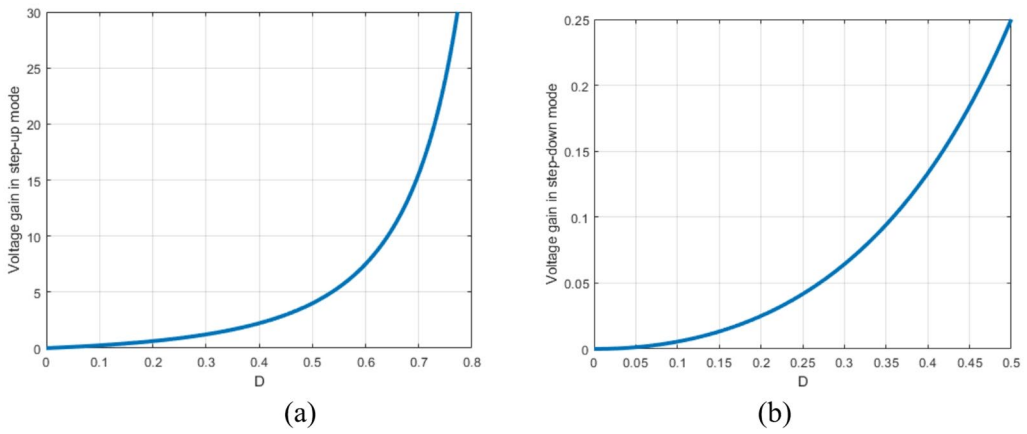


Fig. 5. Voltage gain plot of the converter: **(a)** step-up mode; **(b)** step-down mode.

Modeling of the step-up operating mode

To analyze the dynamic behavior of the proposed bidirectional converter, the state-space averaging technique is employed. Considering ideal semiconductor and passive elements, two subintervals corresponding to switch ON and OFF states are modeled in step-up mode. By averaging these models over a switching cycle with duty ratio D the large-signal model is expressed as below

$$A = \begin{bmatrix} 0 & 0 & 0 & -\frac{1-D}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{D}{L_2} & \frac{D}{L_2} & -\frac{1-D}{L_2} & 0 \\ 0 & 0 & 0 & \frac{D}{L_3} & \frac{D}{L_3} & \frac{D}{L_3} & -\frac{1}{L_3} \\ \frac{1-D}{2C_1} & -\frac{D}{C_1} & -\frac{D}{C_1} & 0 & 0 & 0 & 0 \\ \frac{1-D}{2C_2} & -\frac{D}{C_2} & -\frac{D}{C_2} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-D}{C_3} & -\frac{D}{C_3} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{OH}} & 0 & 0 & 0 & -\frac{1}{R_O C_{OH}} \end{bmatrix} \tag{56}$$

$$B = \begin{bmatrix} \frac{V_L}{L_1(1-D)} \\ \frac{2V_L}{L_2(1-D)^2} \\ \frac{2V_L}{L_3(1-D)^2} \\ \frac{2DV_L}{R_o C_1(1-D)^4} \\ \frac{2DV_L}{R_o C_2(1-D)^4} \\ \frac{2DV_L}{R_o C_3(1-D)^3} \\ 0 \end{bmatrix} \tag{57}$$

$$C = [\ 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1\ ]$$
$$D = [0] \tag{58}$$

$$y + A(D)\, x = \dot{x} \tag{59}$$

$$Cx = B(D)\, V_L \tag{60}$$

$$G_{vd,step-up}(s) = \frac{2.273 * 10^9 s^4 - 2.611 * 10^{12} s^3 + 8.124 * 10^{16} s^2 - 3.704 * 10^{19} s + 5.268 * 10^{23}}{s^6 + 45.45 s^5 + 6.327 * 10^7 s^4 + 2.669 * 10^9 s^3 + 6.767 * 10^{14} s^2 + 2.338 * 10^{16} s + 2.634 * 10^{20}} \tag{61}$$

Modeling of the step-down operating mode

To investigate the dynamic performance of the proposed bidirectional converter in the step-down mode, the state-space averaging method is applied. Assuming ideal components, two switching intervals (ON and OFF states) are formulated, and their combination over a switching cycle with duty ratio D yields the corresponding large-signal model.

$$A = \begin{bmatrix} 0 & 0 & 0 & \frac{D}{L_1} & 0 & -\frac{1}{L_1} \\ 0 & 0 & 0 & -\frac{(1-D)}{L_2} & \frac{D}{L_2} & 0 \\ 0 & 0 & 0 & -\frac{(1-D)}{L_3} & 0 & 0 \\ -\frac{D}{2C} & \frac{(1-D)}{C} & \frac{(1-D)}{C} & 0 & 0 & 0 \\ 0 & -\frac{D}{C_3} & \frac{(1-D)}{C_3} & 0 & 0 & 0 \\ \frac{1}{C_{OL}} & 0 & 0 & 0 & 0 & -\frac{1}{R_O C_{OL}} \end{bmatrix} \tag{62}$$

$$B = \begin{bmatrix} \frac{V_L}{2(1-D)L_1} \\ \frac{V_L}{D(1-D)L_2} \\ \frac{V_L}{(1-D)L_3} \\ \frac{DV_L}{4R_O C_{OL}(1-D)^2} \\ \frac{D^2 V_L}{4R_O C_3(1-D)^2} \\ 0 \end{bmatrix} \tag{63}$$

$$C = [\ 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1\ ] \tag{64}$$

$$D = [0] \tag{65}$$

$$G_{vd}(s) = \frac{1.333e10 s^4 - 2.647e11 s^3 + 3.008e18 s^2 + 3.298e20 s + 2.743e25}{s^6 + 1024 s^5 + 1.546 * 10^8 s^4 + 1.107 * 10^{11} s^3 + 5.271 * 10^{15} s^2 + 9.753 * 10^{17} s + 3.744 * 10^{22}} \tag{66}$$

Dynamic behavior of the converter

Because the converter may exhibit nonminimum-phase behavior in step-up operation due to the presence of a right-half-plane zero, the crossover frequency ω_c must be selected well below the RHP-zero frequency and also remain a small fraction of the switching frequency, i.e., $\omega_c \lesssim 0.2\ \omega_{z,\mathrm{RHP}}$ and $\omega_c \ll 0.1\ \omega_s$. To ensure stable and

well-damped closed-loop performance, a PI controller of the form $C_{PI}(s) = K_p + K_i/s = K_p(1 + \omega_i/s)$ with $\omega_i = K_i/K_p$ is designed using loop-shaping. In the step-down operating mode, a PI controller is also adopted to regulate the output voltage and achieve stable closed-loop performance. Unlike the boost case, the buck configuration does not introduce a right-half-plane zero; therefore, the crossover frequency ω_c can be selected higher, though it still must remain well below one-tenth of the switching frequency to ensure robustness, i.e., $\omega_c \ll 0.1\ \omega_s$. The PI compensator maintains the same structure, $CPI(s) = K_p + K_i/s = Kp(1 + \omega i/s)$ where the zero is placed at $\omega_i \approx \omega_c/10$ to improve phase margin and enhance low-frequency tracking. The proportional gain K_p is again tuned by enforcing unity open-loop gain at the chosen ω_c. This procedure ensures that in the step-down mode the system achieves sufficient phase margin and disturbance rejection, while the integral term guarantees zero steady-state error in output voltage regulation.

Figure 6 depicts the control block diagram of the proposed bidirectional converter, whereas Figs. 7 shows the system's Bode plots for the step-up and step-down modes, respectively, comparing the cases with and without the PI controller.

Comparative assessment with recent advances

Table 1 provides a comparative evaluation of the proposed converter against previously reported topologies in terms of voltage gain in both operating modes, component count, current ripple on both sides, and overall efficiency. Converters[20,24,30,31], and[32] exhibit both lower voltage gain and higher ripple at the high-voltage port, necessitating larger filter capacitors. Although converters[33–35] maintain low current ripple on both sides, their achievable gain remains limited. As illustrated in Fig. 8, the proposed converter demonstrates superior performance in both step-up and step-down operations, reducing the duty ratio in step-up mode while increasing it in step-down mode. Additionally, converter[20] incurs considerable conduction losses due to its diode-based structure, whereas converter[27] is unsuitable for low-voltage applications such as batteries or fuel cells because of its high input-side ripple. Figure 8 illustrates the comparative voltage gain characteristics for both operating modes, where (a) corresponds to the step-up mode and (b) represents the step-down mode. Figure 9 compares the maximum switch voltage stress (Fig. 9(a)) and the maximum switch current stress (Fig. 9(b)) among the converters listed in Table 1. As demonstrated in Fig. 9, the proposed converter achieves superior performance by substantially reducing the normalized switch voltage and current stress, leading to lower conduction losses and component ratings.

Figure 10 presents a comparative analysis of the estimated cost and power density for the proposed converter and several state-of-the-art topologies reported in the literature. Each converter is represented by two adjacent bars corresponding to the cost (in USD) and the power density (in W/cm^3). As illustrated, the proposed design exhibits a balanced performance achieving a significantly higher power density while maintaining a moderate overall cost compared with most reference converters.

Loss analysis of a bidirectional DC-DC converter

This section presents a detailed loss analysis of a bidirectional DC-DC converter operating in step-up and step-down mode. The goal is to calculate the conduction and switching losses of MOSFETs, conduction losses of body

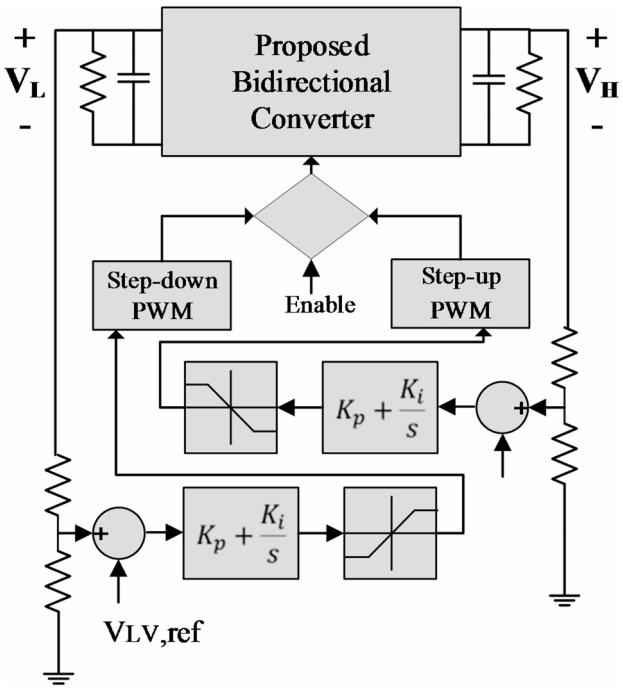


Fig. 6. Schematic diagram of the control circuit of the proposed bidirectional converter.

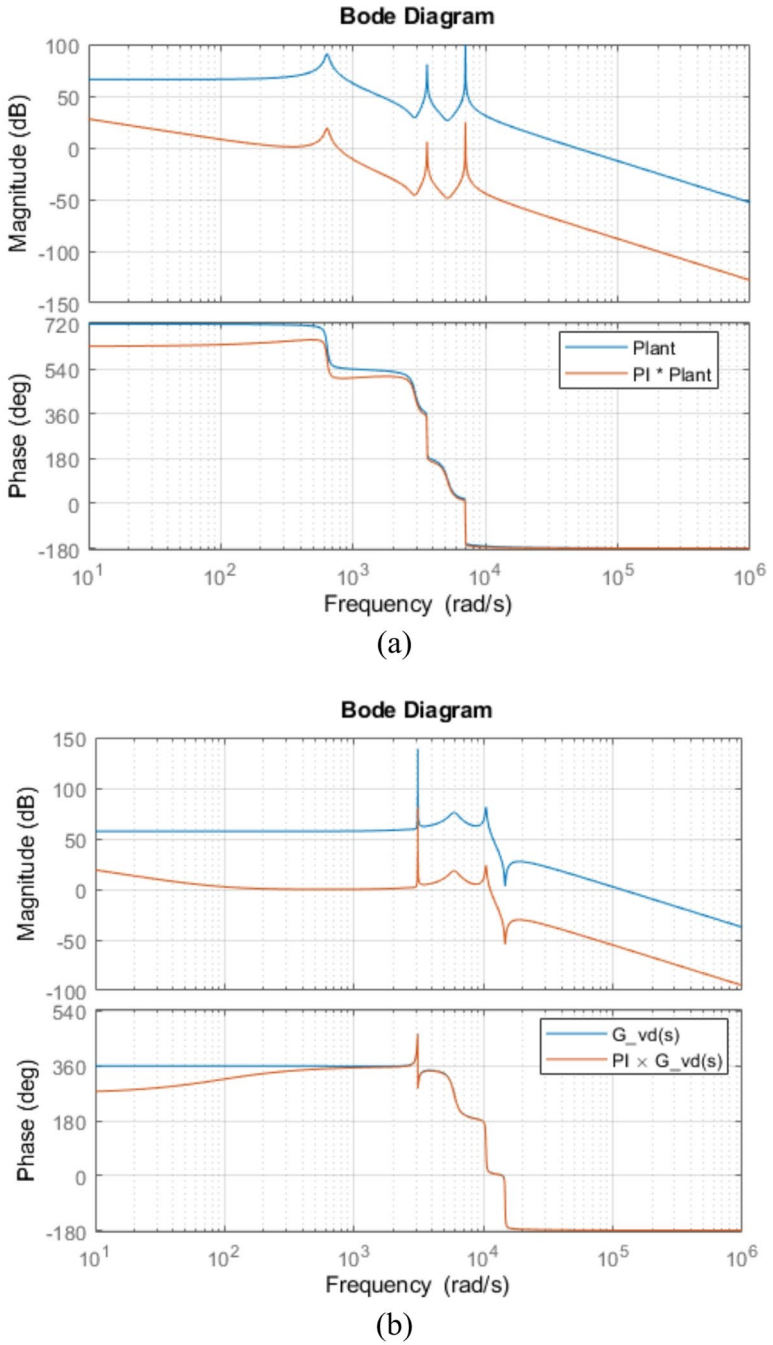


Fig. 7. The Bode diagram of the proposed converter: **(a)** operation in step-up mode, **(b)** operation in step-down mode.

diodes, copper and core losses of the inductors, and losses in the capacitors, as well as to estimate the overall efficiency.

Step-up mode losses

MOSFET Conduction Losses: The conduction loss of each MOSFET is calculated using:

$$P_{Con(Sw)} = \left(\sum_{i=1}^{2} {I_{RMS-Si}}^2 R_{DS-i}\right) = 0.04 * \left(4.36^2 + 2.14^2\right) = 1.085W \tag{67}$$

MOSFET Switching Losses: The switching losses due to turning on and off the MOSFETs are estimated by:

Converter	Voltage gain		Number of elements				Current ripple		Efficiency(%)	
	Step-up	Step-down	L	S	C	T[1]	LV	HV	S.D[2]	S.U[3]
[20]	$\frac{1}{(1-D_H)^2}$	${D_L}^2$	2	3+ 2Diode	4	11	Low	High	95.9	97.2
[24]	$\frac{1}{(1-D_H)^2}$	${D_L}^2$	2	4	3	9	Low	High	96	95.2
[26]	$\frac{1+D_H}{(1-D_H)^2}$	$\frac{{D_L}^2}{2-D_L}$	2	5	4	11	Low	High	97.2	96.8
[27]	$\frac{2-D_H}{(1-D_H)^2}$	$\frac{{D_L}^2}{1+D_L}$	2	5	4	11	High	Low	95	95.2
[30]	$\frac{2}{(1-D_H)}$	$\frac{D_L}{2}$	2	5	4	11	Low	High	95.2	95.3
[31]	$\frac{1-D_H+{D_H}^2}{(1-D_H)^2}$	$\frac{{D_L}^2}{1-D_L+{D_L}^2}$	3	4	4	11	Low	Low	91.8	93
[32]	$\frac{{D_H}^2}{(1-D_H)^2}$	$\frac{{D_L}^2}{(1-D_L)^2}$	3	4	4	11	Low	Low	97	97
[33]	$\frac{{D_H}^2}{(1-D_H)^2}$	$\frac{{D_L}^2}{(1-D_L)^2}$	3	6	4	13	Low	Low	92	91
[34]	$\frac{2-D_H}{(1-D_H)}$	$\frac{{D_L}^2}{1+D_L}$	3	5	5	13	Low	High	95.3	95.7
[35]	$\frac{2+D_H}{(1-D_H)}$	$\frac{D_L}{3-D_L}$	3	5	4	12	Low	High	96.6	92.6
Proposed	$\frac{2D_H}{(1-D_H)^2}$	$\frac{{D_L}^2}{2(1-D_L)}$	3	5	5	13	Low	Low	96.3	96

Table 1. Performance comparison between the proposed converter and other previously developed converters. 1.Total number of components 2. Step-down 3. Step-up.

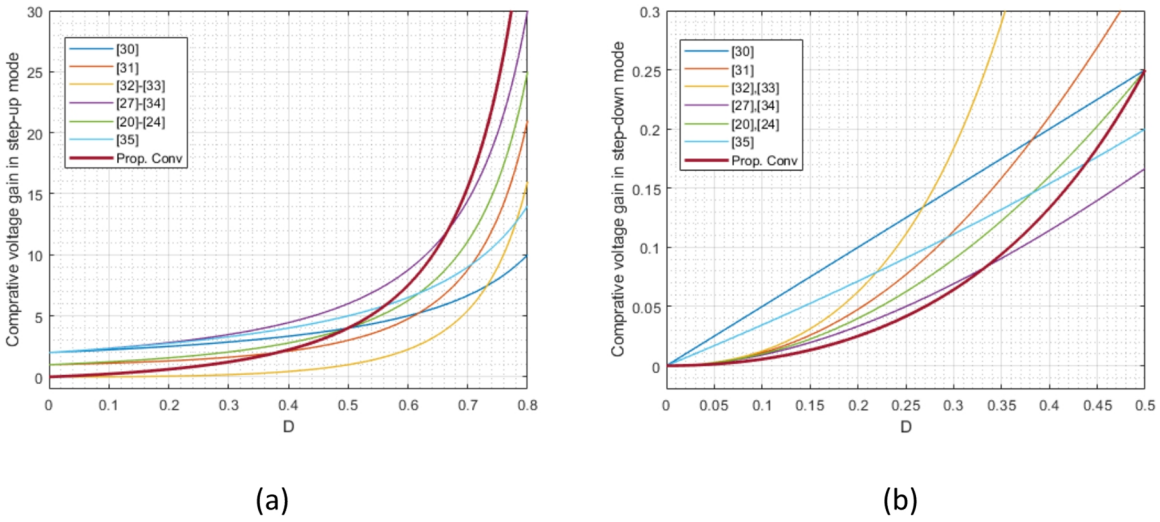
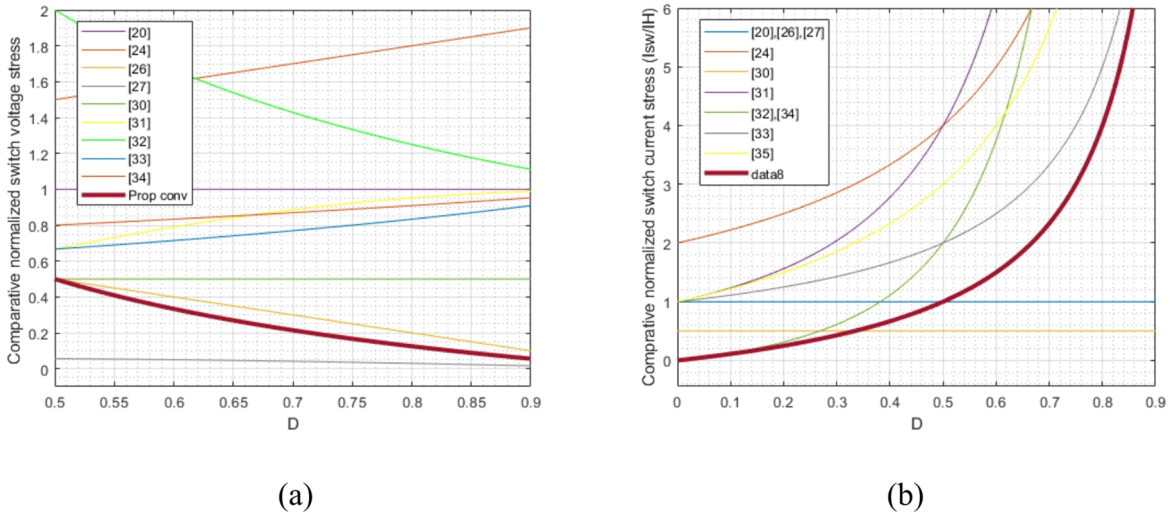


Fig. 8. Comparative plots of the converter: **(a)** voltage gain comparison in step-up mode, **(b)** voltage gain comparison in step-down mode.

$$P_{Switching(Sw)} = \left(\sum_{i=1}^{2} \frac{1}{2} I_{DS-Si} V_{DS-i}(t_r + t_f) f_{sw}\right) = 0.5^*\left(4.36^*120 + 2.14^*345\right)^*180^*10^{-9}{}^*50^*10^3 = 4.5\text{W} \quad (68)$$

MOSFET Capacitive Turn-On Losses: The capacitive turn-on (drain-to-source capacitance) losses are calculated using:

$$P_{Capacitive(Sw)} = \left(\sum_{i=1}^{2} \frac{1}{2}.C_{Oss-Si} V^2{}_{DS-i} f_{sw}\right) = 0.5 * 603 * 10^{-12} * 50 * 10^3 * (120^2 + 345^2) = 3.17W \quad (69)$$



(a) (b)

Fig. 9. Comparative plots of the converter: **(a)** normalized switch voltage stress in step-up mode, **(b)** normalized switch current stress in step-up mode.

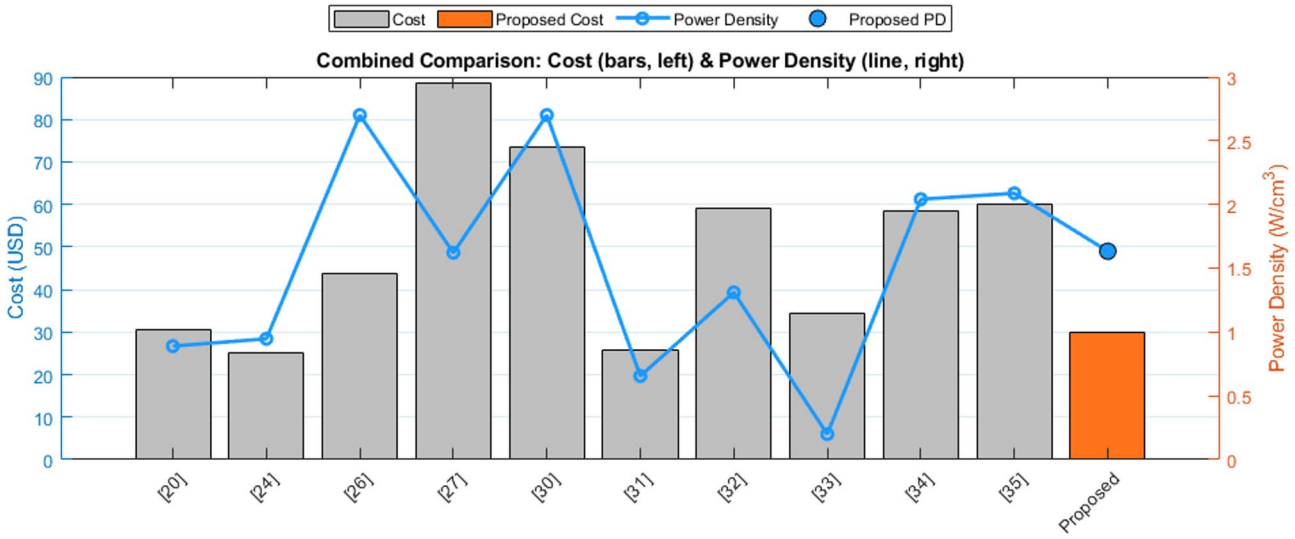


Fig. 10. Comparison of estimated cost and power density among the proposed converter and other reported topologies.

Body Diode Conduction Losses: Conduction losses for the MOSFET body diodes are estimated by:

$$\sum_{i=3}^{5} I_{av-D_{Si}} V_F = (1.2 + 0.99 + 1.011) * 1.3 = 4.29W \tag{70}$$

Inductor Copper Losses: The copper losses in the inductors are computed as:

$$\begin{aligned} P_{Con,Inductors} &= \sum_{i=1}^{3} R_{L1i} {I_{RMS'\,L1i}}^2 \\ &= 0.015 * 8.4^2 + 0.04 * 0.46^2 + 0.2 * 1.11^2 = 1.79W \end{aligned} \tag{71}$$

Inductor Core Losses The core losses are estimated conservatively based on ferrite volume and typical loss density at 50 kHz:

$$P_{Core,Inductors} = \sum_{i=1}^{3} f * k_i * A_e * l_e * {V_{Core}}^b * \Delta B \left(\frac{V_{on}}{N A_e f \Delta B} \right)^{\alpha - 1} = 0.73W \tag{72}$$

The total core loss for the three Ferrite inductors is modeled and verified to be 0.73 W using the comprehensive loss equation at a switching frequency 50 kHz. The calculation incorporates the core's effective area (Ae), set at 0.5 * 10^{-4} m^2, and a peak-to-peak flux density change $\Delta B = 0.1T$. The key loss parameters for the Ferrite material are the frequency coefficient α, approximately 2.5 the volume coefficient (b), approximately 1, and the material coefficient (k), which is determined by the selected material and design to be 4.61 * 10^5.

Capacitor Losses: Capacitor ESR losses are calculated using:

$$\begin{aligned} P_{Cap} &= \sum_{i=1}^{5} R_{Ci} {I_{RMS,Ci}}^2 \\ &= 0.02 * 1.5^2 + 2 * 0.015 * 0.8^2 + 2 * 0.49^2 * 0.05 + 0.015 * 0.574^2 = 0.11W \end{aligned} \tag{73}$$

In this mode, the total converter loss is obtained from theoretical calculations by summing the conduction and switching losses of the semiconductors, the copper and core losses of the inductors, and the ESR losses of the capacitors. The efficiency is then expressed as

$$Eff_{boost} = \frac{P_o}{P_o + P_{loss}} = \frac{400}{400 + 15.67} \approx 96.23\% \tag{74}$$

Step-down mode losses

The same methodology applied for boost mode is also used to analyze the converter in step-down mode at full load. In this configuration, three switches are actively conducting while the body diodes of the remaining two switches carry current. The total losses are calculated by summing the conduction and switching losses of the active MOSFETs, the losses in the body diodes, the copper and core losses of the inductors, and the ESR losses of the capacitors. The efficiency is then determined as the ratio of the output power to the total of output power and losses. The detailed formulas used for each component's loss calculation are presented. The loss analysis, detailing the distribution for both step-up and step-down modes, is summarized in the breakdown shown in Fig. 11.

$$P_{Con(Sw)} = \left(\sum_{i=1}^{3} {I_{RMS-Si}}^2 R_{DS-i} \right) = 0.27 * 1.11^2 + 2 * \ 0.04 * 2.08^2 = 0.68W \tag{75}$$

$$\begin{aligned} P_{Switching(Sw)} &= \left(\sum_{i=1}^{3} \frac{1}{2} I_{DS-Si} V_{DS-i} (t_{ri} + t_{fi}) f_{sw} \right) \\ &= 0.5 * 1.11 * 160 * 245 * 10^{-9} * 50 * 10^3 + 2 * 0.5 * 0.97 * 120 * 180 * 10^{-9} * 50 * 10^3 = 2.1W \end{aligned} \tag{76}$$

$$\begin{aligned} P_{Capacitive(Sw)} &= \left(\sum_{i=1}^{3} \frac{1}{2} . C_{Oss-Si} {V^2}_{DS-i} f_{sw} \right) \\ &= 0.5 * 870{*}10^{-12} * 180^2{*}50{*}10^3 + 2 * 0.5{*}603{*}10^{-12}{*}120^2{*}50{*}10^3 = 1.51W \end{aligned} \tag{77}$$

$$\sum_{i=1}^{2} I_{av-D_{Si}} V_F = (1.11 * 1.3 + 3.32 * 1.3) = 5.76W \tag{78}$$

$$P_{Con,Inductors} = \sum_{i=1}^{3} R_{L1i} {I_{RMS'\ L1i}}^2 = 0.02 * 8.33^2 + 0.07 * 1.26^2 + 0.07 * 1.23^2 = 1.63W \tag{79}$$

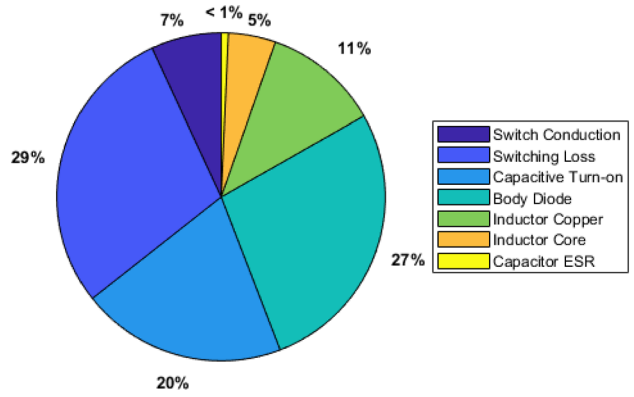
$$P_{Core,Inductors} = \sum_{i=1}^{3} f * k_i * A_e * l_e * {V_{Core}}^b * \Delta B \left(\frac{V_{on}}{N A_e f \Delta B} \right)^{\alpha - 1} = 0.64 \tag{80}$$

$$\begin{aligned} P_{Cap} &= \sum_{i=1}^{4} R_{Ci} {I_{RMS,Ci}}^2 \\ &= 0.02 * 1.11^2 + 0.015 * 1.15^2 + 0.015 * 0.816^2 + 0.015 * 1.02^2 + 0.05 * 0.632^2 = 0.09W \end{aligned} \tag{81}$$

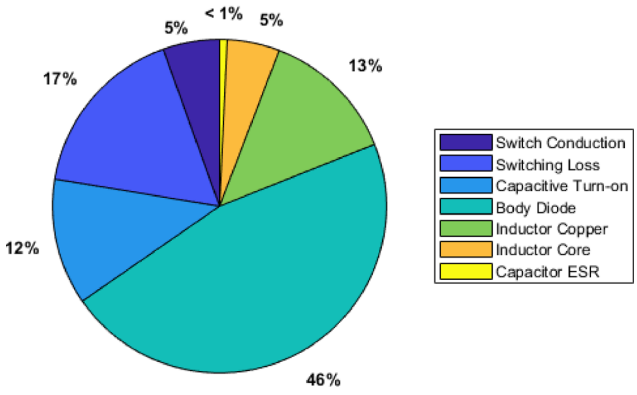
$$Eff_{buck} = \frac{P_o}{P_o + P_{loss}} = \frac{400}{400 + 12.41} \approx 96.99\% \tag{82}$$

Experimental verification

For experimental validation of the theoretical analyses, a laboratory prototype of the proposed converter was built, featuring a 400 W power rating and compact dimensions of 7*10*3.5 cm^3. The detailed parameters of this prototype are listed in Table 2, and a photograph of the hardware implementation is shown in Fig. 12. Experimental results for both step-up and step-down operation modes are provided in Figs. 13 and 14, respectively. Specifically, Fig. 13(a) presents the gate voltage waveforms of switches S_1 and S_2, while Fig. 13(b) illustrates the drain–source voltage and current of S_1. The current waveform of inductor L_1 is presented in Fig. 13(c). The drain–source voltage and current of switch S_2 are illustrated in Fig. 13(d), whereas Fig. 13(e) provides the measured input and output voltage profiles of the converter. The dynamic response of the converter to load variations, confirming the effectiveness of the control loop, is shown in Fig. 13(f). Likewise, for the step-down mode, Fig. 14(a) shows the gate voltage waveforms of switches S_3 and S_4, and Fig. 14(b) depicts their drain–source voltages. The drain-source currents of switches S_3 and S_4 are displayed in Fig. 14(c), and the corresponding current for S_5 is illustrated in Fig. 14(d). Capacitor voltage waveforms (C_1–C_3) are presented in Fig. 14(e), and the dynamic load response is illustrated in Fig. 14(f). The dynamic response characteristics of



a



b

Fig. 11. Loss breakdown for **(a)** step-up operation and **(b)** step-down operation.

Parameter & Component	Values
Rated power	400 W
Low voltage side	48 V
High voltage side	360 V
L_1, L_2	400µH
L_3	800µH
C_1,C_2,C_3	10µF
C_{LV},C_{HV}	220 µF
f	50 kHz
S_3	IRFP460
Other switches	IRFP260N

Table 2. Parameter specifications utilized in the experimental setup.

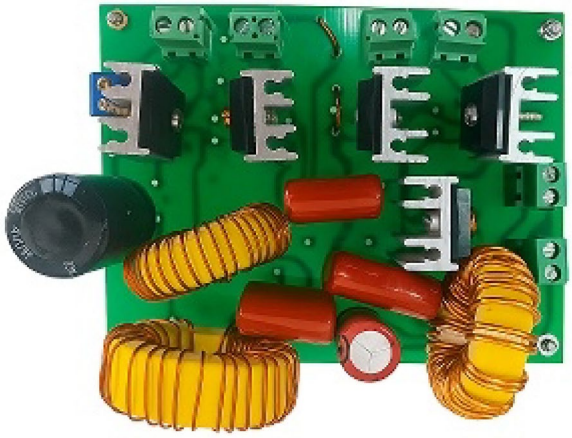


Fig. 12. Laboratory implementation of the proposed converter.

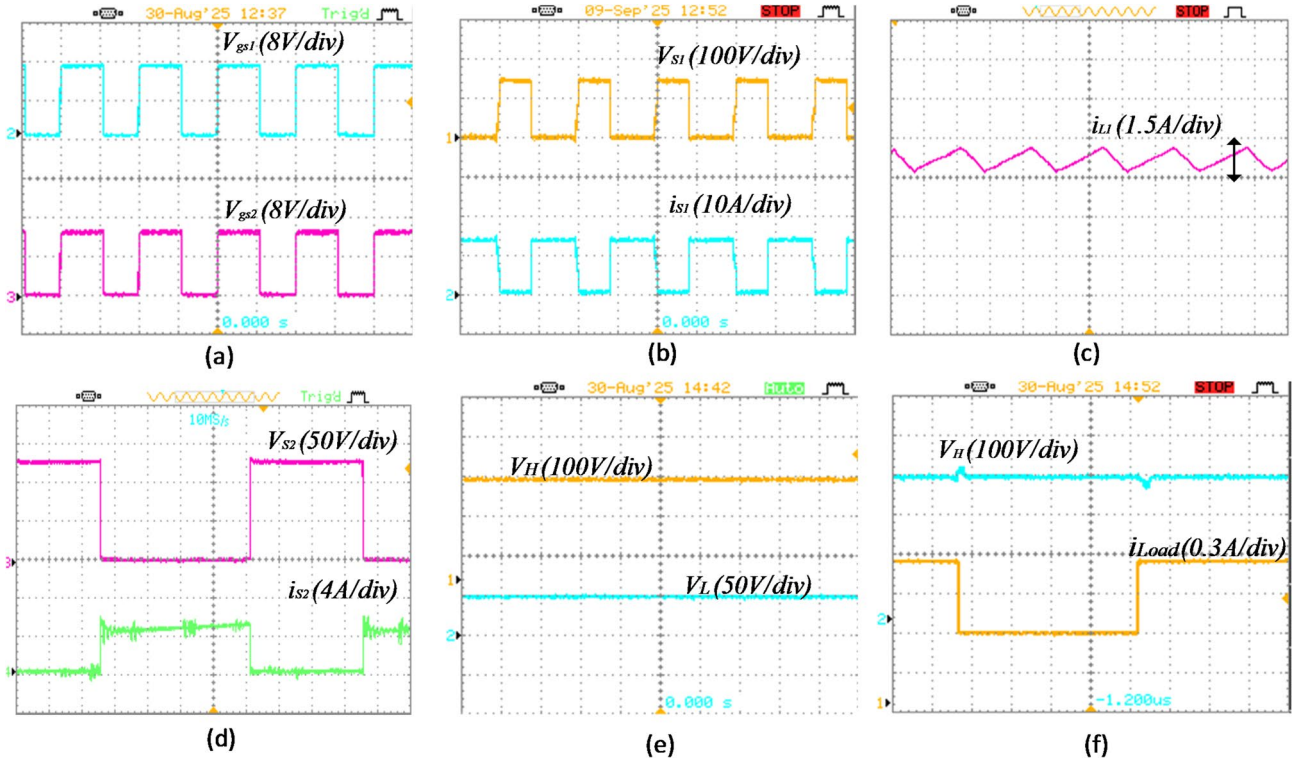


Fig. 13. Step-up mode practical results: **(a)** gate voltage of S_1, S_2 **(b)** drain-source voltage and current of S_1 **(c)** current of L_1 **(d)** drain-source voltage and current of S_2 **(e)** regulated output voltage and input voltage **(f)** dynamic response of the proposed converter.

the converter to input voltage changes are illustrated in Fig. 15, showing transient behavior under both sudden (Figs. 15(a), 15(b)) and linear (Fig. 15(c)) changes in the input voltage. Specifically, Fig. 15(c) depicts step-up operation where the input voltage rises steadily from 40 V to 100 V while the output voltage remains fixed at 360 V. Altogether, these experimental findings corroborate the theoretical analysis.

Converter efficiency

According to Fig. 16, the efficiency of the proposed bidirectional converter improves as the output power increases in both the step-up and step-down modes. At light loads, conduction and switching losses play a more dominant role in lowering efficiency, but their influence becomes less pronounced as the load grows, resulting in higher overall performance. When comparing the two modes, the step-down operation exhibits slightly better efficiency than the step-up operation, mainly due to fewer active switch turn-ons, lower circulating currents, and

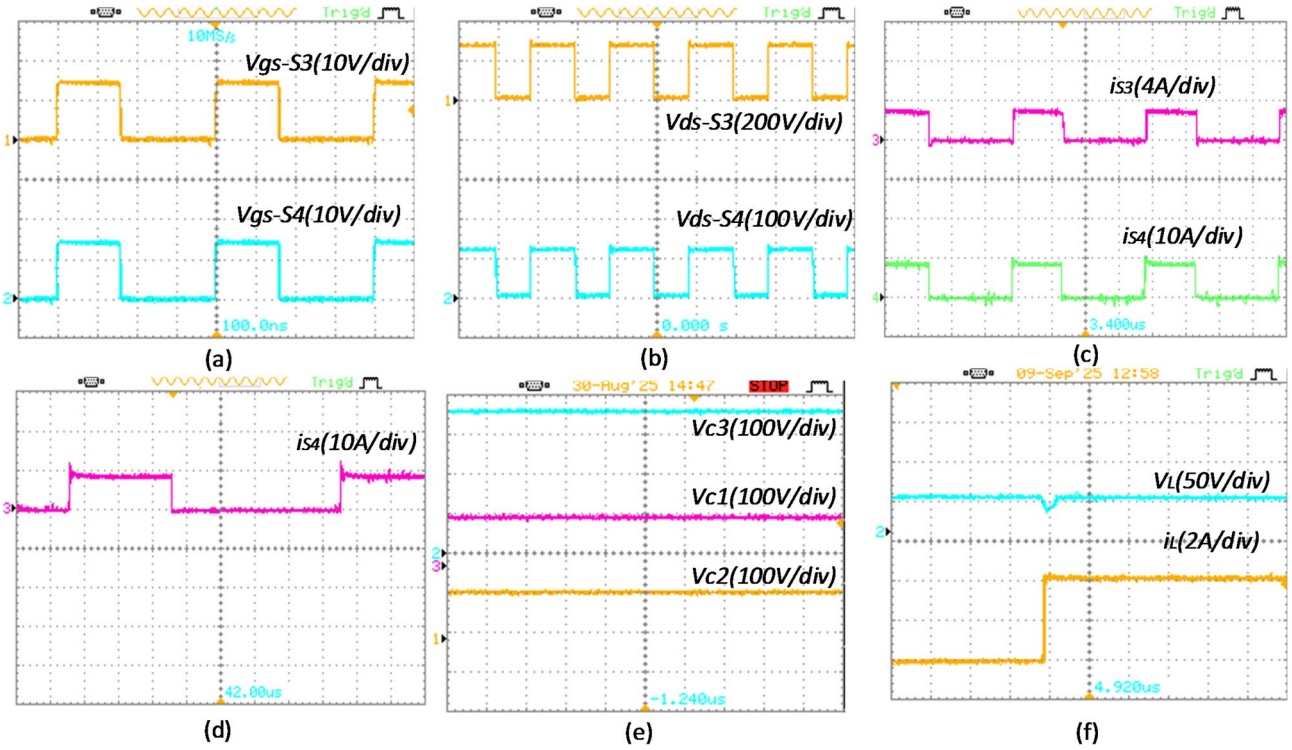


Fig. 14. Step-down mode practical results: **(a)** gate voltage of S_3, S_4 **(b)** the drain-source voltage of S_3 and S_4 **(c)** the drain-source current of S_3 and S_4 **(d)** the drain-source current of S_5 **(e)** voltages across capacitors C_1, C_2, and C_3 **(f)** dynamic response of the proposed converter.

therefore reduced losses. In general, the converter maintains an efficiency 96.3% in step-down mode and 96% in step-up mode at full load, confirming its effectiveness and suitability for practical applications.

Conclusion

This study presents a novel bidirectional DC–DC converter capable of delivering very high voltage gain in the step-up mode and substantially reduced voltage gain in the step-down mode. The design employs only two switches operating concurrently in step-up mode and three switches operating together in step-down mode, which simplifies the control structure. Moreover, the proposed configuration achieves low current ripple on both input and output sides, enabling the use of smaller filter capacitors. Experimental results validate the effectiveness of the converter, showing excellent efficiency of 96% in step-up operation and 96.3% in step-down operation.

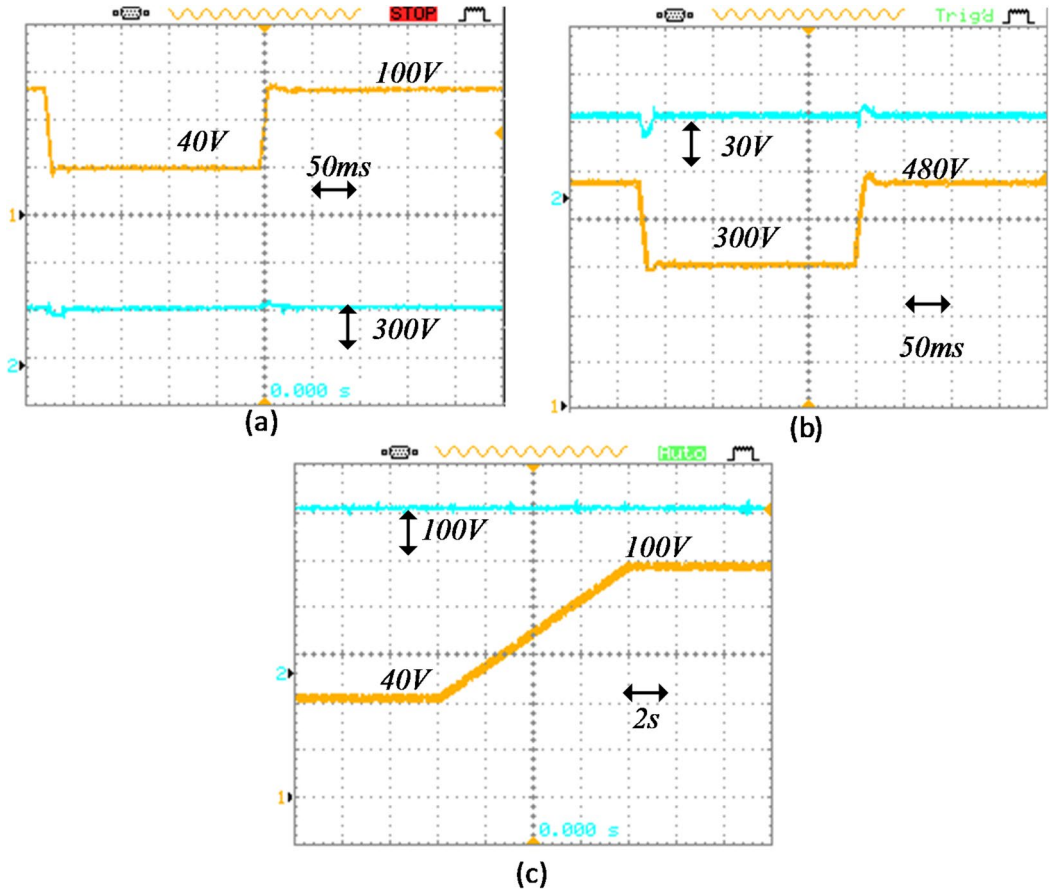


Fig. 15. Dynamic response of the converter to input voltage variations: **(a)** abrupt input voltage change from 40 V to 100 V in step-up mode; **(b)** abrupt high-voltage side change from 480 V to 300 V in step-down mode; and **(c)** linear input voltage change from 40 V to 100 V in step-up mode.

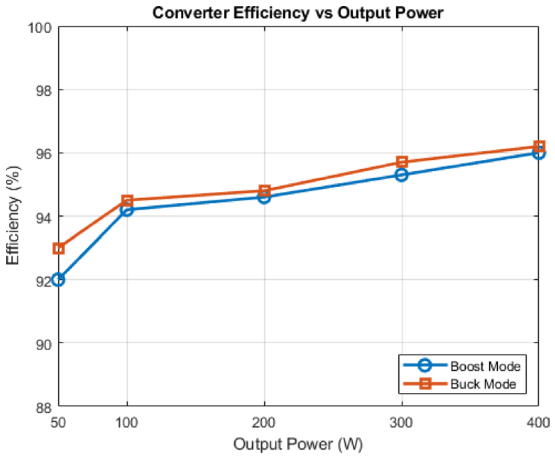


Fig. 16. Efficiency curves of the proposed converter in both step-up and step-down modes under varying output load conditions.

Data availability

All data generated and analyzed during the current study are available from the corresponding author upon reasonable request.

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Author contributions

All authors contributed to the review of the manuscript. S. S was responsible for the design and execution of the experiments, data analysis, documentation, and overall supervision. M. D contributed to data analysis and provided supervision.

Declarations

Competing interests
The authors declare no competing interests.

Additional information
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