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## A novel hierarchical control strategy for enhancing stability of a DC microgrid feeding a constant power load

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In recent years, DC microgrids supplying constant power loads (CPLs) have attracted significant attention due to their impact on overall system stability, which is attributed to their electrical characteristics that exhibit negative incremental impedance. This paper examines a secondary control strategy aimed at ensuring accurate power sharing and voltage restoration within an islanded DC microgrid supplying a constant power load. The droop control function is typically used in the primary control layer to facilitate power sharing among distributed generators (DGs). However, differing load profiles may cause the DC bus voltage to deviate from its nominal value. To restore the DC bus voltage to its nominal value while maintaining accurate power sharing, a primary and secondary control scheme is proposed. This scheme employs an integrated control strategy combining sliding mode control for the primary control level and H-infinity control for secondary control. The approach is based on a two-time-scale stability analysis, i.e., the settling time of the primary control must be faster than that of the secondary control. Additionally, compared to most existing methods, the proposed approach requires no global information and depends exclusively on DC bus voltage feedback, eliminating the need for passive loads in parallel with the CPL. A test system of an islanded DC microgrid feeding a CPL is created using Matlab and PSIM software to assess the proposed method. An experimental prototype comprising two DGs and a tightly voltage-controlled boost converter emulating a CPL is developed to demonstrate the proposed approach and confirm the theoretical results.

**Keywords** DC microgrids, Droop control, Sliding mode control (SMC), H\_infinity control, Secondary control

The growing demand for efficient, reliable, and sustainable energy systems has driven significant interest in innovative power generation and distribution methods. The integration of renewable energy sources, combined with advancements in power electronics and digital controllers, has accelerated the adoption of distributed generation and microgrid (MG) technologies. This shift not only supports a diversified energy mix but also enables localized energy production, enhancing system reliability and reducing transmission losses, making MGs a key component in the development of modern energy infrastructure. MGs integrate distributed generation units (DGs), energy storage systems, and local loads, forming a flexible and resilient power structure. This design enhances energy management and improves system stability, particularly when integrating variable renewable sources such as solar and wind power<sup>1,2</sup>.

MGs are categorized based on the type of coupling bus: alternating current (AC) MGs, direct current (DC) MGs, and hybrid AC/DC MGs. Each configuration is suited to specific applications and operational

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requirements, providing flexibility that enables MGs to play a critical role in advancing renewable integration and enhancing grid reliability within modern power systems<sup>3,4</sup>.

This paper primarily focuses on DC MGs, particularly those supplying constant power loads (CPLs). These systems typically operate in an islanded mode, as shown in Fig. 1. DC MGs are especially well-suited for applications where precise load control and stability are crucial, offering a practical and efficient solution for integrating renewable energy while maintaining system reliability<sup>5-7</sup>.

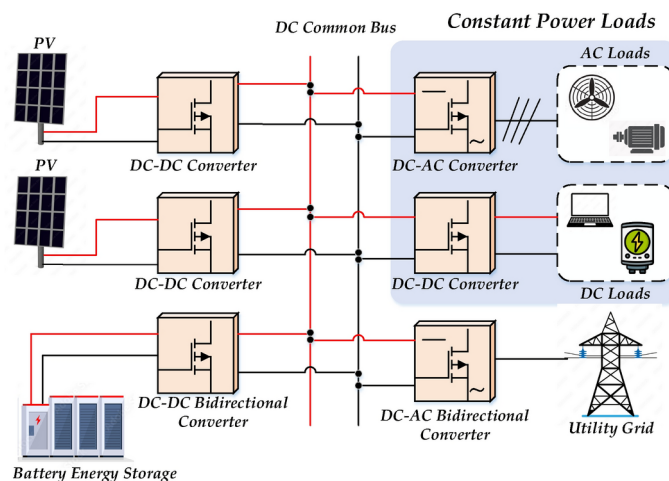
In islanded DC MGs, droop control is commonly used within the local controllers of DGs to achieve balanced power sharing. This decentralized approach allows each DG to produce an equal current output, effectively distributing the load across the system without requiring inter-unit communication. However, the implementation of droop control introduces a trade-off between power-sharing accuracy and voltage regulation. While it improves load sharing, droop control often compromises voltage regulation, causing the DC bus voltage to deviate significantly from its desired reference value. External disturbances and the influence of CPLs exacerbate voltage deviations, making it challenging to maintain the stability of the DC bus at its desired level<sup>8-10</sup>.

To address these limitations, a secondary control strategy is introduced for DC MGs supplying CPLs. This strategy includes a secondary voltage compensation controller specifically designed to enhance voltage regulation and ensure system stability. In this approach, the voltage deviation error is detected and processed by an appropriate controller, which then sends a corrective control signal to all DGs to maintain the desired voltage<sup>11-14</sup>.

Despite these advancements, certain challenges remain. A suitable model must be developed to effectively design the controller and mitigate the destabilizing effects of CPLs, which are known to be a source of instability in DC MGs when the controller is insufficient. In particular, CPLs are nonlinear loads that exhibit incremental negative impedance (INI) characteristics, meaning that a decrease in output voltage leads to an increase in output current, and an increase in voltage causes a reduction in current. This nonlinear behavior complicates control efforts, as it requires a specific strategy to stabilize the common DC bus of the DC MG<sup>15</sup>. CPLs are prevalent in applications such as aircraft, electric vehicles, ships, and telecommunications, highlighting the need for robust control to manage their effects and ensure stability in DC MGs<sup>16,17</sup>.

The presence of CPLs in DC MGs produces instability, irised by the INI effect, destabilizing the system and causing issues with voltage stabilization and power sharing among DGs. The complex dynamics of hierarchical control and CPLs complicate stability analysis, requiring advanced control strategies to maintain stable operation and ensure balanced power distribution. Various solutions have been proposed to address these challenges, and the following literature review investigates these strategies and their effectiveness in enhancing stability and power sharing in DC MGs. In<sup>18</sup>, a comprehensive review of hierarchical control strategies for DC MGs is presented, emphasizing the importance of secondary control in maintaining voltage stability and power balance under varying load conditions. The authors in<sup>19</sup> propose a secondary control method for standalone DC MGs that enhances voltage regulation, load sharing, and reduces line losses, thereby improving overall system performance. In<sup>20</sup>, the challenges posed by CPLs in droop-controlled DC MGs are addressed, suggesting methods to mitigate instability and ensure robust operation. In<sup>21</sup>, the authors introduce a cooperative decentralized tertiary control approach for DC MGs with renewable distributed generation, focusing on coordinated voltage regulation and power sharing among multiple energy sources. In<sup>22</sup>, the authors analyze CPLs in droop-controlled MGs for more electric aircraft applications, highlighting the need for robust control strategies to maintain system stability.

A novel secondary optimal control is developed in<sup>23</sup> for multiple battery energy storage systems in a DC MG, aiming to improve voltage stability and efficient power management. A distributed secondary control method is proposed in<sup>24</sup>, using averaging virtual current derivatives to improve voltage regulation and system resilience against disturbances. An enhanced droop control method, presented in<sup>25</sup>, ensures accurate load sharing and voltage regulation in islanded and interconnected DC MGs, addressing issues related to proportional load distribution. The authors in<sup>26</sup> utilize neural networks to achieve voltage recovery and current sharing in DC



**Fig. 1.** Typical DC microgrid with CPLs.

MGs with uncertain CPLs, demonstrating the potential of artificial intelligence in MG control. In<sup>27</sup>, a review of power sharing, voltage restoration, and stabilization techniques in hierarchical controlled DC MGs is provided, offering insights into various control methodologies and their effectiveness.

In<sup>28</sup>, the authors conduct control and stability analysis of DC MGs with CPLs and source disturbances, proposing strategies to enhance system robustness. The authors in<sup>29</sup> assess the performance of reverse droop control for multi-DER cooperative DC MGs, offering solutions for improved voltage regulation and load sharing. A finite-time synergetic controller is proposed in<sup>30</sup> for DC MGs with CPLs, achieving rapid system stabilization and improved dynamic response. An adaptive damping control is introduced in<sup>31</sup> for load-side converters to mitigate instability in DC MGs caused by CPLs, enhancing system reliability. The authors in<sup>32</sup> focus on the detection and mitigation of false data in cooperative DC MGs with unknown CPLs, ensuring data integrity and reliable operation. In<sup>33</sup>, the authors develop a stable and robust DC power system for more electric aircraft, addressing challenges unique to aviation applications. In<sup>34</sup>, the dynamic response of dual-active-bridge converters with CPLs under extended-phase-shift control is improved, enhancing performance under varying load conditions. In<sup>35</sup>, a deep learning controller is proposed for DC–DC buck–boost converters in wireless power transfer systems feeding CPLs, showcasing the integration of machine learning in power electronics control.

An improved droop control strategy is proposed in<sup>36</sup> for accurate current sharing and DC-bus voltage compensation in DC MGs, addressing common issues in conventional droop control methods. In<sup>37,38</sup>, the authors focus on modeling and control of single-phase dual-active-bridge-based medium-voltage DC shipboard power systems, contributing to the development of reliable maritime MGs. A distributed control method is proposed in<sup>39</sup> to ensure proportional load sharing and improve voltage regulation in low-voltage DC MGs, highlighting the benefits of decentralized control architectures. In<sup>40</sup>, voltage and frequency control of inverter-based weak low-voltage network MGs is explored, providing solutions for maintaining stability in such systems.

A decentralized control method is proposed in<sup>41</sup> for low-voltage DC MGs, facilitating scalable and flexible MG operation. In<sup>42</sup>, the authors offer practical design considerations for current sharing control in parallel voltage regulator module applications, relevant to MG power distribution. A control strategy for islanded MGs with DC-link voltage control is presented in<sup>43</sup>, ensuring stable operation under islanded conditions. The authors in<sup>44</sup> provide a general approach toward standardization in hierarchical control of droop-controlled AC and DC MGs, contributing to the harmonization of control strategies.

In<sup>45</sup>, the authors analyze the stability of DC MGs with CPLs under distributed control methods, offering insights into maintaining stability in the presence of CPLs. Distributed control and optimization in DC MGs are discussed in<sup>46</sup>, presenting methods to achieve optimal performance through decentralized control. A secondary control method for MGs based on distributed cooperative control of multi-agent systems is proposed in<sup>47</sup>, facilitating coordinated control actions among distributed energy resources. In<sup>48</sup>, the authors conduct a small-signal analysis of MG secondary control, considering communication time delays and addressing challenges related to information exchange in control systems. In<sup>49</sup>, a novel decentralized primary and distributed secondary control strategy for DC MGs with CPLs is proposed, providing a comprehensive approach to improving system resilience under the influence of CPLs. However, the stability of DC MGs feeding CPLs under multi-level distributed control remains insufficiently studied due to the complex interactions between hierarchical control systems and CPLs. This challenge leaves the detailed stability analysis of such systems an open problem for further research.

This paper investigates the stability of parallel buck converters in a DC MG supplying local CPLs, addressing their nonlinear behavior under hierarchical control for voltage stabilization and precise power sharing. A decentralized primary droop control is implemented, guided by a sliding mode controller (SMC) with an adjusted droop expression<sup>50,51</sup>. The secondary control employs an H-infinity controller to enhance power sharing and restore voltage<sup>52,53</sup>. A two-time-scale analysis is conducted to evaluate system stability, considering the dynamics of the converters, CPLs, and the controller. The proposed method is validated through simulations and experimental tests, confirming its effectiveness. The key contributions of this study are outlined as follows:

1. Development of a decentralized primary control based on SMC.
2. Design of a secondary H-infinity controller for precise power sharing and voltage stabilization in the DC MG.
3. A two-time-scale stability analysis, considering converter dynamics, CPL behavior, and hierarchical control effects.
4. Validation through simulations and experimental results.

The paper is organized as follows: in “[Discussion and analysis of DC MG feeding a CPL](#)” section examines a DC MG supplying a CPL. In “[Primary control design for a DC microgrid with a CPL](#)” section details the design of a primary SMC-based controller aimed at achieving power sharing between DGs. In “[Secondary control strategy for a DC microgrid feeding a constant power load](#)” section discusses the use of hybrid sliding mode H-infinity control to enhance system stability. Simulation results are presented in “[Simulation results](#)” section, with experimental findings in “[Experimental validation](#)” section. In “[Conclusion](#)” section concludes the paper.

## Discussion and analysis of DC MG feeding a CPL

The dynamic interaction between the CPL and the DC MG can lead to large-signal oscillations, compromising system stability. Addressing this instability is crucial to ensure reliable and robust operation of the DC MG in the presence of a CPL. In continuous conduction mode (CCM), the input impedance behaves as a negative resistance when the frequency is below the voltage loop cut-off frequency of the DC MG. However, when the frequency exceeds the cut-off frequency, the input impedance transitions to behave like an inductance<sup>15</sup>.

The consumed power for a CPL is constant throughout the controller bandwidth, and its relationship is provided by:

$$P_{cpl} = v_{dc\_Bus} \cdot i_{dc\_Bus} = Cte \quad (1)$$

where  $P_{cpl}$  is the power absorbed by the CPL,  $v_{dc\_Bus}$  is the input voltage and  $i_{dc\_Bus}$  stands for the consumed current.

Deriving the current of the CPL with respect to its voltage and inverting the result yields to the expression of the incremental negative impedance of a CPL, as follows:

$$\frac{dv_{dc\_bus}}{di_{dc\_bus}} = -\frac{v_{dc\_bus}}{i_{dc\_bus}} = -\frac{P_{cpl}}{i_{dc\_bus}^2} = -\frac{v_{dc\_bus}^2}{i_{dc\_bus}^3} \quad (2)$$

Thus

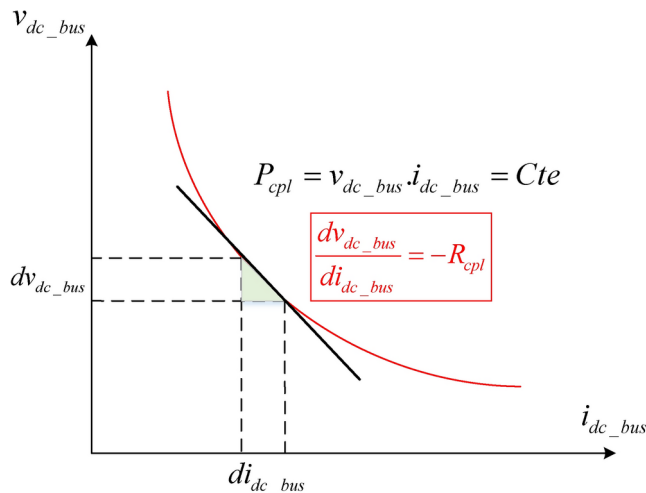
$$\frac{dv_{dc\_bus}}{di_{dc\_bus}} = -R_{cpl} \quad (3)$$

The INI characteristic of the CPL, highlighted in Eq. (3) and depicted in Fig. 2, introduces a  $-180^\circ$  phase lag in the Bode diagram, as shown in Fig. 3. From a control systems perspective, this phase lag causes instability when the output impedance of the source DC MG intersects with the input impedance of the CPL, especially when the cut-off frequency of the source DC MG is lower than that of the CPL. This instability impacts overall system performance and degrades power quality<sup>15</sup>.

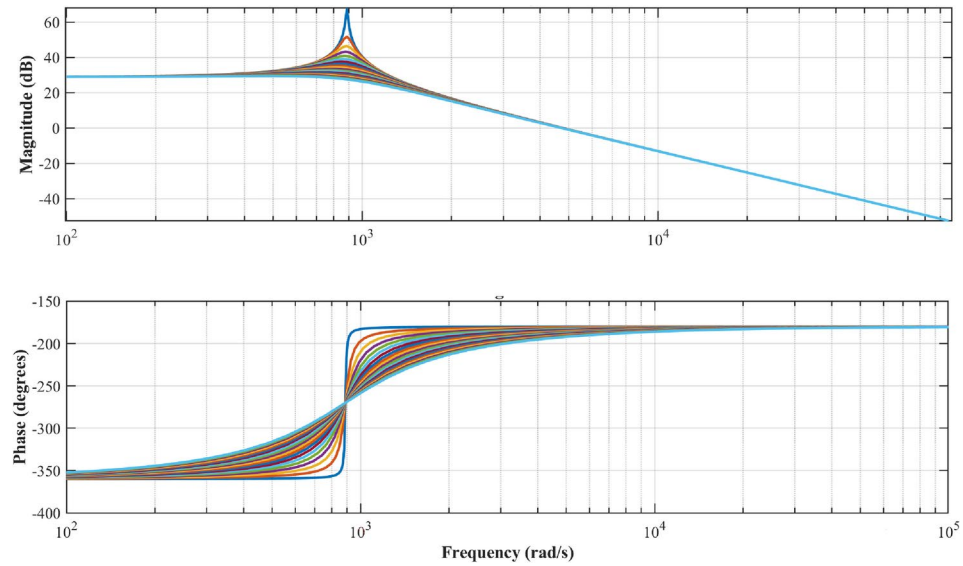
External variations, such as changes in power load demand and input voltage, can significantly impact system performance, particularly settling time and overshoot. To analyse these effects, a Bode analysis is performed on an open-loop DC MG feeding a CPL, where the power load demand is changed 10 times, incrementally increasing from 10 to 100 W. The results show that such variations reduce the system's cut-off frequency and quality factor, leading to increased overshoot and a slower transient response. Based on this example analysis, a more comprehensive control strategy is required to manage power sharing and voltage regulation effectively in a DC MG with CPLs.

To manage power sharing and voltage regulation in a DC MG with CPLs, a two-level control strategy is employed. The primary control, often using droop control, balances power distribution among DG units but may lead to voltage deviations. To address these deviations, a secondary control level is added to enhance stability and performance, as shown in Fig. 4. The proposed approach is based on a two-time-scale stability analysis, where the settling time of the primary control is designed to be faster than that of the secondary control. This hierarchical structure ensures that the primary control layer is responsible for fast stabilization, local regulation of voltage and current, and balancing power among the DGs. Once the primary control achieves stability, the secondary control, operating on a slower time scale, performs higher-level tasks such as restoring the nominal DC bus voltage, achieving system-wide balance, and ensuring proper power sharing. This separation of time scales minimizes dynamic interactions between the control layers, enhancing the overall stability and robustness of the DC MG.

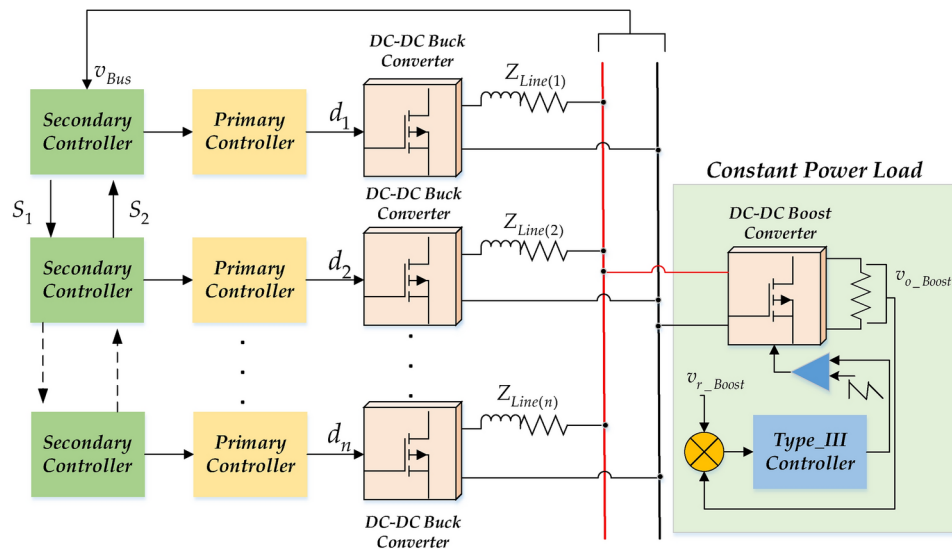
This coordinated control approach is particularly crucial for addressing the challenges posed by CPLs. The behavior of CPLs introduces instability-induced INI, which destabilizes the system by causing oscillations in the LC filters.



**Fig. 2.** Incremental negative-impedance behavior of a CPL.



**Fig. 3.** Bode diagram behaviour of a DC MG feeding a CPL ( $v_{in,1,2} = 28$  V,  $C_{1,2} = 1000$   $\mu$ F,  $L_{o1} = 6$  mH,  $L_{o2} = 2.7$  mH,  $P_{cpl} = 10:10:100$  W,  $d = 0.5$ ,  $R_{Line,1} = 1$   $\Omega$ ,  $R_{Line,2} = 2$   $\Omega$ ).



**Fig. 4.** Parallel configuration of DC–DC converters supplying CPLs.

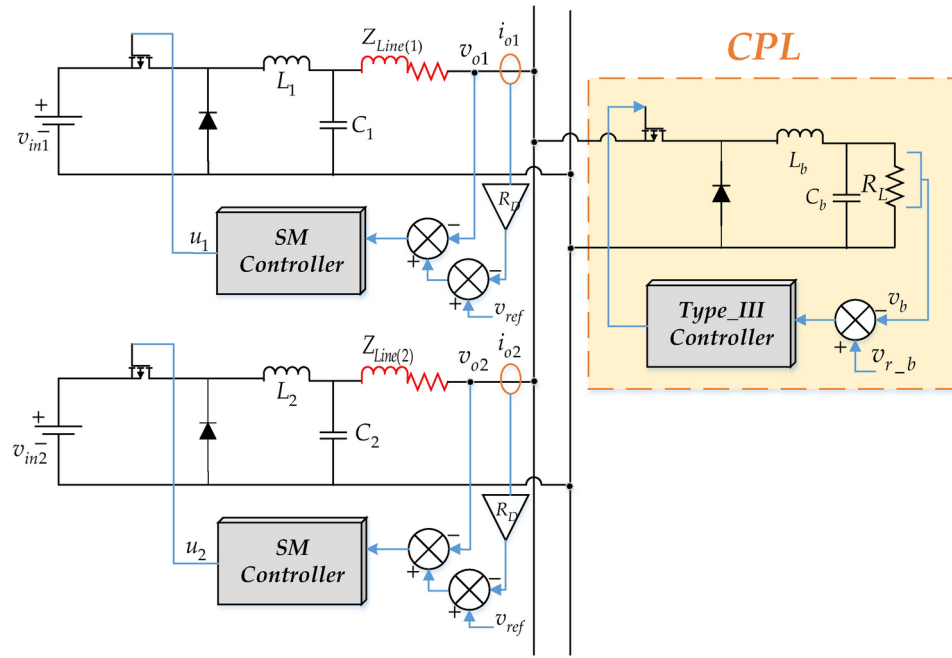
Traditional controllers designed for resistive loads struggle with the complexities introduced by CPLs, necessitating advanced control techniques. To address this, control loops (current and voltage) using an SMC are implemented for dynamic power sharing and voltage regulation in each DC–DC converter forming the MG. A secondary controller, featuring a PI controller enhanced by an H-infinity controller, is then developed to efficiently correct voltage deviations caused by the primary control and improve system stability<sup>50–55</sup>.

**Primary control design for a DC microgrid with a CPL**  
**Design of the inner loops (current–voltage) based on SMC**

This section introduces a nonlinear control strategy to address instability and enhance the performance of the inner loops in each DC–DC converter forming the MG. To achieve this, a robust SMC is applied to the inner current–voltage control loops. Figure 5 illustrates the setup, featuring a DC MG supplying a CPL.

The state-space model for a DG unit powering a CPL is derived and represented as:

$$\begin{cases} \frac{di_{L\_i}}{dt} = \frac{1}{L_i} (v_{in\_i}d_i - v_{o\_i}) \\ \frac{dv_{o\_i}}{dt} = \frac{1}{C_i} \left( i_{L\_i} - \frac{P_{cpl\_i}}{v_{o\_i}} \right) \end{cases} \quad (4)$$



**Fig. 5.** Primary control using SMC in a DC MG feeding a CPL.

where  $v_{in\_i}$  is the input voltage of the DG unit;  $v_{o\_i}$  represents the output voltage of the DG unit;  $L_i, C_i$  are the parameters value of the LC filter of the DG unit;  $i_{L\_i}$  represents the inductor current of the DG unit;  $P_{cpl}$  is the CPL value.

A transformation method is used to reduce the number of state variables by selecting the output voltage and its derivative as the state variables  $x_{1\_i}$  and  $x_{2\_i}$  for each DG unit.

Substituting  $x_{1\_i}$  and  $x_{2\_i}$  into Eq. (4) provides an updated expression for each DG unit supplying a CPL. This transformation simplifies the control process, enhancing model clarity and control efficiency, as shown below:

$$\begin{cases} \dot{x}_{1\_i} = x_{2\_i} \\ \dot{x}_{2\_i} = \frac{v_{in\_i}}{C_i L_i} d_i - \frac{x_{1\_i}}{C_i L_i} - \frac{P_{cpl} x_{2\_i}}{C_i x_{1\_i}^2} \end{cases} \quad (5)$$

where  $x_{1\_i}$  represents  $v_{o\_i}$ , and  $x_{2\_i}$  represents  $\dot{v}_{o\_i}$ .

In typical DC MG systems, the primary control level employs voltage and current controllers based on PI control. This section proposes an alternative approach that combines inner current–voltage loops into a unified control framework using SMC.

The SMC ensures that the output voltage of each DG unit in the DC MG accurately tracks the reference value, maintaining stable operation when connected to a CPL and improving robustness against disturbances<sup>50,51,55</sup>. Additionally, this method offers simplicity and ease of implementation, making it well-suited for control applications.

Therefore, we define the nonlinear switching surface function  $S_i$  as

$$S_i(x_i; t) = \left( \frac{d}{dt} + \lambda_i \right)^{n-1} \tilde{x}_i \quad (6)$$

where  $\lambda_i$  is a positive constant weight coefficient to adjust the convergence speed;  $\tilde{x}_i$  is the tracking error of each DG units representing the DC MG.  $n$ th-order  $S_i$  function.

By setting  $n = 1$  and based on the dynamic model Eq. (5), the tracking error is defined as:

$$\begin{cases} \tilde{x}_i = x_{1\_i} - v_{ref\_i} \\ \dot{\tilde{x}}_i = x_{2\_i} - \dot{v}_{ref\_i} \end{cases} \quad (7)$$

where  $x_{1\_i}$  and  $x_{2\_i}$  represent the output voltage of each DG unit of the DC MG, and its derivative, respectively.

By substituting Eqs. (4) and (7) into Eq. (6), it can be expressed as:

$$S_i = (x_{2\_i} - \dot{v}_{ref\_i}) + \lambda_i (x_{1\_i} - v_{ref\_i}) \quad (8)$$

To derive the control law  $u(t)$  for the SMC, the switching control law is expressed as:

$$u_{sw\_i} = \dot{S}_i = -k_i \text{sign}(S) - q_i S_i = \begin{cases} \dot{S}_i > 0 \text{ if } S_i < 0 \\ \dot{S}_i < 0 \text{ if } S_i > 0 \end{cases} \tag{9}$$

where  $k_i$  and  $q_i$  are positive constant coefficients.

Let us suppose the candidate Lyapunov function as:

$$V_i(S_i) = \frac{1}{2} S_i^2 \tag{10}$$

Thus, based on Eqs. (9), (10), and (5), the derivative of the Lyapunov function must be negative when  $S \neq 0$ .

The time derivative of  $V_i$  is given as:

$$\dot{V}_i(S_i) = S_i \cdot \dot{S}_i < 0 \tag{11}$$

To validate Eq. (9), the time derivative of Eq. (6) for each DG unit is given as:

$$\dot{S}_i = (\dot{x}_{2\_i} - \ddot{v}_{ref\_i}) + \lambda_i (\dot{x}_{1\_i} - \dot{v}_{ref\_i}) \tag{12}$$

By using Eq. (5), Eq. (12) becomes as follows:

$$\dot{S}_i = \frac{v_{in\_i}}{C_i L_i} d_i - \frac{x_{1\_i}}{C_i L_i} - \frac{P_{cpl} x_{2\_i}}{C_i x_{1\_i}^2} - \ddot{v}_{ref\_i} + \lambda_i x_{2\_i} - \lambda_i \dot{v}_{ref\_i} \tag{13}$$

To ensure stability, Eq. (11) is satisfied using Eqs. (5) and (9), verified by substituting Eq. (9) into Eq. (13). Therefore, two conditions are obtained as:

1. If  $S_i > 0$  should be  $S_i < 0$ . Then, the control law equal to 1, which can be written as

$$\dot{S}_i = \frac{v_{in\_i}}{C_i L_i} d_i - \frac{x_{1\_i}}{C_i L_i} - \frac{P_{cpl} x_{2\_i}}{C_i x_{1\_i}^2} - \ddot{v}_{ref\_i} + \lambda_i x_{2\_i} - \lambda_i \dot{v}_{ref\_i} < 0 \tag{14}$$

2. If  $S_i < 0$  should be  $S_i > 0$ . Then, the control law equal to 0, which can be written as

$$\dot{S}_i = \frac{v_{in\_i}}{C_i L_i} d_i - \frac{x_{1\_i}}{C_i L_i} - \frac{P_{cpl} x_{2\_i}}{C_i x_{1\_i}^2} - \ddot{v}_{ref\_i} + \lambda_i x_{2\_i} - \lambda_i \dot{v}_{ref\_i} > 0 \tag{15}$$

To validate Eq. (11), the initial derivative of the Lyapunov candidate function for each DG unit in the DC MG is computed as:

$$\dot{V}_i = S_i \cdot \dot{S}_i = S_i \cdot \left( \frac{v_{in\_i}}{C_i L_i} d_i - \frac{x_{1\_i}}{C_i L_i} - \frac{P_{cpl} x_{2\_i}}{C_i x_{1\_i}^2} - \ddot{v}_{ref\_i} + \lambda_i x_{2\_i} - \lambda_i \dot{v}_{ref\_i} \right) \tag{16}$$

In DC-DC converters forming the DC MG, the control variable is the duty cycle. Thus, based on Eqs. (9) and (13), the control input  $d$  (i.e.,  $u = d$ ) is given as:

$$d_i = u_i = \frac{C_i L_i}{v_{in\_i}} \left( \frac{x_{1\_i}}{C_i L_i} + \frac{P_{cpl} x_{2\_i}}{C_i x_{1\_i}^2} + \ddot{v}_{ref\_i} - \lambda_i x_{2\_i} + \lambda_i \dot{v}_{ref\_i} \right) + \frac{C_i L_i}{v_{in\_i}} (k_i \text{sign}(S_i) + q_i S_i) \tag{17}$$

The equivalent control law is given by:

$$u_{eq\_i} = \frac{C_i L_i}{v_{in\_i}} \left( \frac{x_{1\_i}}{C_i L_i} + \frac{P_{cpl} x_{2\_i}}{C_i x_{1\_i}^2} + \ddot{v}_{ref\_i} - \lambda_i x_{2\_i} + \lambda_i \dot{v}_{ref\_i} \right) \tag{18}$$

The discontinued control law is defined as:

$$u_{dis\_i} = \frac{C_i L_i}{v_{in\_i}} (k_i \text{sign}(S_i) + q_i S_i) \tag{19}$$

Substituting Eq. (17) into Eq. (16) yields:

$$\dot{V}_i = S_i \cdot \dot{S}_i = -S_i (k_i \text{sign}(S_i) + q_i S_i) \tag{20}$$

This denotes

$$\dot{V}_i < -S_i (k_i \text{sign}(S_i) + q_i S_i) < 0 \tag{21}$$

Thus, the mathematical results confirm that the Lyapunov condition has been satisfied.

### Report of conventional droop control

In DC MGs, droop control is a primary strategy for distributing loads among parallel DC–DC converters. It manages current circulation and ensures dynamic power sharing, especially in islanded MG setups<sup>44,54</sup>. This method autonomously balances power distribution among DC–DC converters by using virtual resistive impedance, eliminating the need for data exchange between DG units.

Figure 5 illustrates the conventional droop control method with two parallel DC–DC converters, detailing the configuration as follows:

$$v_{o_{-}(i,j)} = v_{o_{-}(i,j)}^* - (R_{D_{-}(i,j)} + R_{line_{-}(i,j)}) i_{o_{-}(i,j)} \quad (22)$$

where  $v_{o_{-}(i,j)}$  represents the output voltage of each converter;  $v_{o_{-}(i,j)}^*$  is voltage reference value of the DC bus for the DC MG;  $R_{D_{-}(i,j)}$  indicates the droop coefficient value of each converter;  $R_{line_{-}(i,j)}$  represents the value of resistive line for each converter.

The output current of each DC–DC converter is determined by its virtual resistive value, as explained below:

$$\frac{i_{o_{-}i}}{i_{o_{-}j}} = \frac{R_{D_{-}j} + R_{line_{-}j}}{R_{D_{-}i} + R_{line_{-}i}} \approx \frac{R_{D_{-}j}}{R_{D_{-}i}} = \eta_{i,j} \quad (23)$$

where  $\eta_{i,j}$  is the ratio of the rated capacity between the  $i$ -th converter and the  $j$ -th converter.

From Eq. (23), Eq. (22) can be expressed as:

$$v_{o_{-}(i,j)} = v_{o_{-}(i,j)}^* - R_{D_{-}(i,j)} i_{o_{-}(i,j)} \quad (24)$$

Assuming that  $\xi_{v_{-}i}$  is the maximum allowed voltage deviation,  $R_{D_{-}i}$  and  $v_{o_{-}i}^*$  must be designed as follows:

$$v_{o_{-}i}^* = v_{o_{-}i} - \xi_{v_{-}i} / 2 \quad (25)$$

$$R_{D_{-}i} = \xi_{v_{-}i} / i_{o_{-}i_{\max}} \quad (26)$$

The droop control method causes voltage deviations at both the output of each DC–DC converter and the DC bus, which require correction according to the following expression:

$$\Delta v_{o_{-}(i,j)} = v_{o_{-}(i,j)}^* - (R_{D_{-}(i,j)} + R_{line_{-}(i,j)}) i_{o_{-}(i,j)} \quad (27)$$

The novel secondary control corrects voltage deviations and improves current sharing, enhancing the efficiency and reliability of the DC MG.

### Secondary control strategy for a DC microgrid feeding a constant power load

This section proposes an H-infinity-based control method to enhance the secondary control of a DC MG supplying a CPL. The primary objectives are to correct DC bus voltage deviations caused by the primary control, develop a new model for the DC MG with a CPL, and ensure system stability despite disturbances from the CPL load and input voltage<sup>52,53</sup>. The secondary control mechanism is shown in Fig. 6. The main contributions of this section are as follows:

1. Development of a robust H-infinity secondary control to correct voltage deviations from the primary control.
2. Introduction of a new DC MG model incorporating a CPL for effective secondary control application.
3. Assurance of system stability in the presence of CPL loads and external disturbances.

The derivative of the error reported for  $PI_{\infty}(s)$  is written as:

$$\dot{e} = Z (k_{p\infty} \cdot \dot{e} + k_{i\infty}) \quad (28)$$

where

$$Z = - (f \cdot |R_{cpl}| \cdot 1_{n \times 1} \cdot 1_{n \times 1}^T \cdot \hat{A}^{-1} + \beta \cdot L) \quad (29)$$

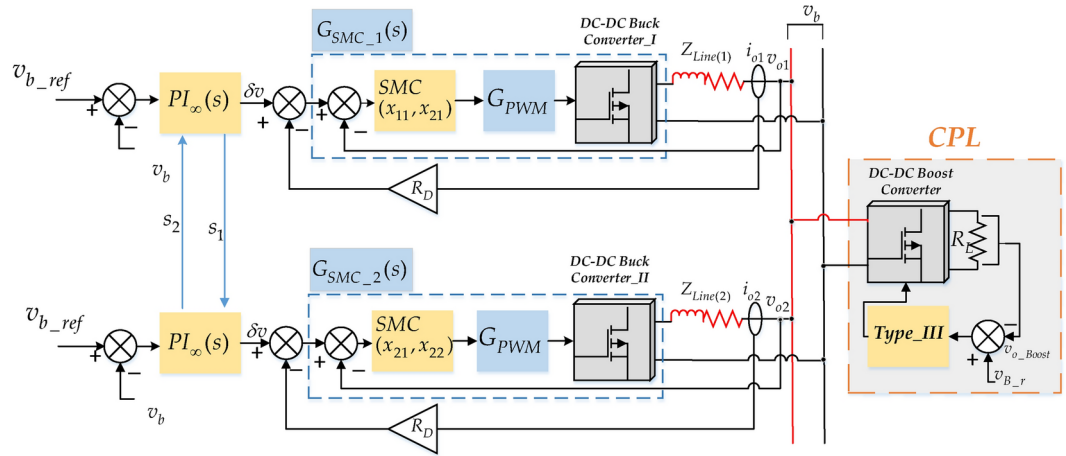
and

$$\hat{A} = Z_{line} + R_D + |R_{cpl}| \cdot 1_{n \times 1} \cdot 1_{n \times 1}^T \quad (30)$$

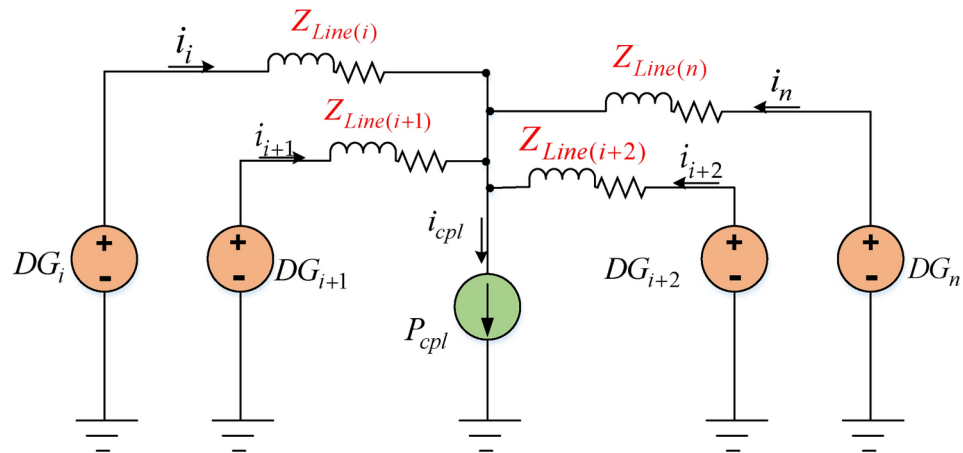
$$f = \text{diag}([f_1 \quad \dots \quad f_i \quad 0_{(i+1) \times n}]), \quad i = 1, \dots, n-1 \quad (31)$$

$$\beta = \text{diag}(\beta_1, \dots, \beta_i, \dots, \beta_n), \quad i = 1, \dots, n \quad (32)$$

$$R_D = \text{diag}(R_{D_{-}1}, \dots, R_{D_{-}i}, \dots, R_{D_{-}n}), \quad i = 1, \dots, n \quad (33)$$



**Fig. 6.** Secondary control diagram for a DC MG with a CPL. Where  $G_{SMC}(s)$  is a robust sliding mode controller intended for the inner loops (current, voltage) of the primary control.  $PI_{\infty}(s)$  is a robust H infinity controller intended for secondary loops.  $G_{PWM}(s)$  is a PWM transfer function.



**Fig. 7.** Electrical interconnection of parallel-connected DGs supplying a CPL.

$$s_i = s_j, \quad \forall j, i \tag{34}$$

$$Z_{Line} = \text{diag} (Z_{Line(1)}, \dots, Z_{Line(i)}, \dots, Z_{Line(n)}) , \quad i = 1, \dots, n \tag{35}$$

The diagonal matrix gains  $f$  and  $\beta$  are carefully chosen to ensure that the matrix  $Z$  satisfies the Hurwitz condition;  $Z_{Line}$  is a line impedance diagonal matrix;  $R_D$  is a diagonal droop resistance gain matrix;  $L$  denotes a Laplacian matrix;  $R_{cpl}$  denotes INI characteristic of the CPL.

**System modeling**

To begin, the relationship between the output voltage of the DG unit and the DC bus voltage must be defined. This relationship is critical for constructing the DC MG model at the primary control level. Figure 7 illustrates a representative circuit of a DC MG supplying a CPL, with multiple DC sources operating simultaneously.

The DC bus voltage  $v_b$  for a DC MG supplying a CPL is expressed as:

$$v_b = v_{o\_i} - Z_{Line(i)} \cdot i_{o\_i} \tag{36}$$

The generated current of each DG unit is stated below using the superposition theorem:

$$i_{o\_i} = I_{DG_i} - \sum_{j=1}^n I_{DG_j}, \quad \{i = j, I_{DG_j} = 0\} \tag{37}$$

where  $1 \leq i \leq n, 1 \leq j \leq n; n$  is the number of DG units used to make the DC MG.  $I_{DG_i}$  denotes the current supplied by the  $i$ th DG unit.

According to Eq. (37),  $I_{DG_i}$  and  $I_{DG_j}$  are given as follows:

$$I_{DG_i} = \frac{v_{o\_i}}{Z_{Line(i)} + \left( \sum_{j=1}^n \frac{1}{Z_{Line(j)}} + \frac{1}{|R_{cpl}|} - \frac{1}{Z_{Line(i)}} \right)^{-1}} \tag{38}$$

$$I_{DG_j} = v_j \cdot \frac{\left( \sum_{T=1}^n \frac{1}{Z_{Line(T)}} + \frac{1}{|R_{cpl}|} - \frac{1}{Z_{Line(j)}} \right)^{-1}}{Z_{Line_j} + \left( \sum_{T=1}^n \frac{1}{Z_{Line(T)}} + \frac{1}{|R_{cpl}|} - \frac{1}{Z_{Line(j)}} \right)^{-1}} \cdot \frac{1}{Z_{Line(i)}} \tag{39}$$

Assume the DG units have the same line impedance, it follows that  $Z_{Line(1)} = \dots = Z_{Line(i)} = Z_{Line(j)} = \dots = Z_{Line(n)} = Z_{Line} = \frac{1}{Y}$ . In the primary control of a DC MG supplying a CPL, it is assumed that  $v_{o\_1} = v_{o\_i} = v_{o\_j} = \dots = v_{o\_n}$ .

Based on the previous assumptions, substituting Eq. (37) into Eq. (36) yields the DC bus voltage.  $v_b$  as follows:

$$v_b = \left( 1 - \frac{\left( (n-1) \cdot Y + \frac{1}{|R_{cpl}|} \right) \cdot Z_{Line} - (n-1)}{\left( (n-1) \cdot Y + \frac{1}{|R_{cpl}|} \right) \cdot Z_{Line}^2 + Z_{Line}} \cdot Z_{Line} \right) \cdot v_{o\_i} \tag{40}$$

As a result, using Fig. 6, the output voltage of each DC converter forming the DC MG can be expressed as:

$$v_{o\_i} = G_{SMC\_i} \cdot v_{ref\_i} \tag{41}$$

where

$$v_{ref\_i} = v_{o\_i}^* - R_{D\_i} \cdot i_{o\_i} \tag{42}$$

$v_{o\_i}^*$  represents the nominal output voltage of the DC converter.

By substituting Eq. (41) into Eq. (40), the DC bus voltage can be rewritten as:

$$v_b = \left( 1 - \frac{\left( (n-1) \cdot Y + \frac{1}{|R_{cpl}|} \right) \cdot Z_{Line} - (n-1)}{\left( (n-1) \cdot Y + \frac{1}{|R_{cpl}|} \right) \cdot Z_{Line}^2 + Z_{Line}} \cdot Z_{Line} \right) \cdot G_{SMC\_i} \cdot v_{ref\_i} \tag{43}$$

Substituting Eq. (17) into Eq. (5), the inner loop  $G_{SMC\_i}$  of the  $i$ th DG unit can be expressed as:

$$\begin{cases} \dot{x}_{1\_i} = x_{2\_i} \\ \dot{x}_{2\_i} = (q_i - \lambda_i) x_{2\_i} + \lambda_i q_i x_{1\_i} + \ddot{v}_{ref} + (\lambda_i - q_i) \dot{v}_{ref} - \lambda_i q_i v_{ref} + k \operatorname{sgn}(S_i) \end{cases} \tag{44}$$

The system in Eq. (41) is linearized using the Jacobian matrix to approximate its behavior near a specific operating point. This linearization simplifies the nonlinear dynamics of Eq. (41), enabling easier analysis and control design for the secondary control. It allows the use of linear control techniques to assess stability, analyze disturbance responses, and achieve desired performance, such as voltage stabilization and power sharing in the DC MG.

$$\dot{X} = A \cdot X + B \cdot u \tag{45}$$

where  $X$  represents the vector  $[x_1 \ x_2]^T$ ;  $\dot{X}$  denotes the vector  $[\dot{x}_1 \ \dot{x}_2]^T$ , and  $u = v_{ref}$ .

The matrices A and B are derived from Eq. (44) using the Jacobian approach, as shown below:

$$A = \begin{bmatrix} 0 & 1 \\ \lambda_i q_i & (q_i - \lambda_i) \end{bmatrix} \tag{46}$$

$$B = \begin{bmatrix} 0 & 0 & 0 \\ -\lambda_i & (\lambda_i - q_i) & 1 \end{bmatrix} \tag{47}$$

Using matrices from Eqs. (46) and (47), the transfer function of the system can be derived as:

$$G_{SMC\_i} = C (SI - A)^{-1} \cdot B = \frac{s}{s^2 - (q_i - \lambda_i) s + \lambda_i q_i} \tag{48}$$

The DC bus voltage transfer function can be expressed by substituting Eq. (48) into Eq. (43), resulting in:

$$v_b = \frac{\theta \cdot Z_{Line} - (n - 1)}{Z_{Line} (\theta \cdot Z_{Line} + 1)} \cdot G_{SMC\_i} \cdot v_{ref\_i} \tag{49}$$

where  $\theta$  defined as  $(n - 1)Y + \frac{1}{|R_{cpl}|}$ .

The uniform mathematical formulation of secondary control across all DG units indicates a consistent control strategy throughout the system. Variations in line impedance among DG units introduce uncertainties, which can affect the performance and stability of the system. This uncertainty in the values of  $Z_{Line}$  and  $Y$  can lead to variations in power sharing and voltage stabilization in the DC MG. It is essential to account for these variations in the control strategy to ensure the system remains stable and responsive to external disturbances. By modeling and representing this uncertainty, more robust control techniques can be designed to minimize its impact and ensure reliable operation of the DC MG, even under varying conditions.

$$Z_{Line} = Z_{Line0} + \delta_{Z_{Line}} Z_{Line0} \tag{50}$$

$$Y = Y_0 + \delta_Y Y_0 \tag{51}$$

By substituting Eqs. (50) and (51) into Eq. (43) and performing the required mathematical operations, the expression for the DC bus voltage  $v_b$  can be derived as:

$$v_b = G_{SMC\_i}(s) B_1(s) (v_{ref\_i} + w_b) \tag{52}$$

where

$$B_1(s) = \frac{Y_0 Z_{Line0} (n - 1) + 1}{n Y_0 Z_{Line0} + \frac{Z_{Line0}}{|R_{cpl}|} + 1} \tag{53}$$

$w_b$  represents the parameter that accounts for disturbances caused by transmission impedance uncertainty, and it is expressed as:

$$w_b = \Delta(s) \begin{pmatrix} v_{ref\_i} \\ v_b \end{pmatrix} = \frac{1}{B_1(s)} \begin{pmatrix} \phi_1 & \phi_2 \end{pmatrix} \begin{pmatrix} v_{ref\_i} \\ v_b \end{pmatrix} \tag{54}$$

where

$$\phi_1 = G_{SMC\_i}(s) (n - 1) \frac{\delta_{Z_{Line}} Z_{Line0} Y_0 + \delta_Y Z_{Line0} Y_0}{n Y_0 Z_{Line0} + \frac{Z_{Line0}}{|R_{cpl}|} + 1} \tag{55}$$

$$\phi_2 = \frac{\delta_{Z_{Line}} \left( n Y_0 Z_{Line0} + \frac{Z_{Line0}}{|R_{cpl}|} \right) + \delta_Y Y_0 Z_{Line0}}{n Y_0 Z_{Line0} + \frac{Z_{Line0}}{|R_{cpl}|} + 1} \tag{56}$$

### Secondary control level control design process for a DC MG feeding a CPL

This study focuses on designing the secondary control process using an H-infinity approach based on a Nonsmooth Optimization Algorithm (NOA), as referenced in<sup>52</sup>. The methodology incorporates an augmented system that captures the mathematical relationships between the signals to be mitigated and the target signals, such as the control variable and error. This augmented system also includes weight functions, which play a crucial role in formulating the secondary control by defining the desired performance criteria. The secondary control block diagram in Fig. 8 illustrates the developed system and highlights the significance of weight functions in the design phase. The weight functions  $W_{S1}(s)$ ,  $W_{S2}(s)$  and  $W_{S3}(s)$  are used to create the secondary controller of the DC MG feeding a CPL (see Fig. 9).

The augmented plant  $P(s)$  required for the design process, as depicted in Fig. 9, is represented by the following expression:

$$\begin{pmatrix} e_1 \\ e_2 \\ y_s \end{pmatrix} = P(s) \begin{bmatrix} V^* \\ W^* \\ s_i \end{bmatrix} = \begin{bmatrix} W_{S1}(s) f_i & -W_{S1}(s) G_{SMC}(s) B_1(s) f_i W_{S3}(s) & -W_{S1}(s) \\ 0 & 0 & W_{S2}(s) \\ 1 & -G_{SMC}(s) B_1(s) W_{S3}(s) & G_{SMC}(s) B_1(s) \end{bmatrix} \begin{bmatrix} V^* \\ W^* \\ s_i \end{bmatrix} \tag{57}$$

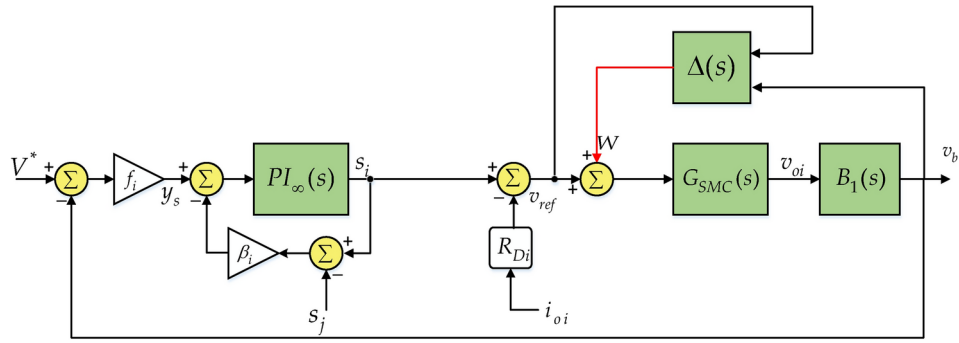
During steady-state operation, all decentralized secondary controllers generate identical compensation voltage signals, such that  $(s_1 = s_2, \dots, s_i, \dots, s_n)$ .

Therefore,  $s_i$  can be approximately expressed as:

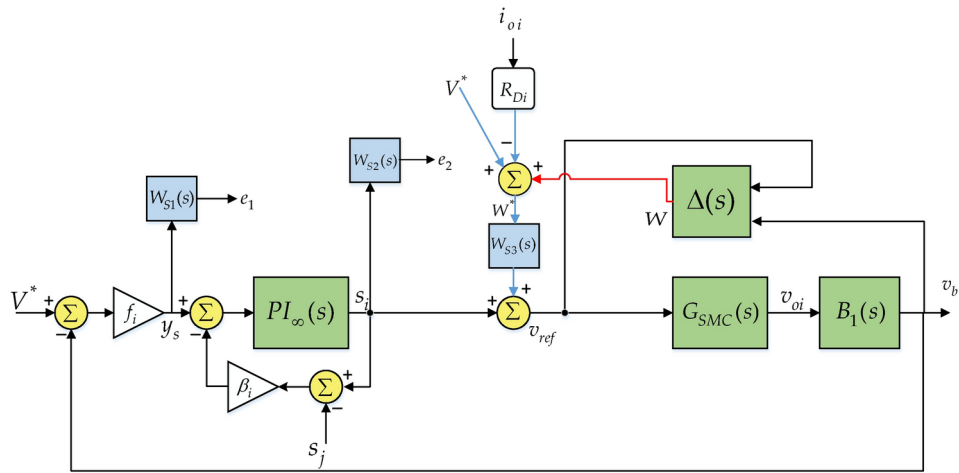
$$s_i = P I_\infty(s) y(s) \tag{58}$$

The linear fractional transformation (LFT) of the system is defined as follows:

$$y = F_L(P(s), P I_\infty(s)) \cdot y_{in} \tag{59}$$



**Fig. 8.** Robust secondary control in a closed-loop system.



**Fig. 9.** Robust secondary control using weight functions.

where

$$F_L(P(s), PI_\infty(s)) = \begin{pmatrix} W_{S1}(s)S_S(s) & W_{S1}(s)S_S(s)G_{SMC}(s)B_1(s)W_{S3}(s) \\ W_{S2}(s)S_S(s)PI_\infty(s) & -W_{S2}(s)\varpi_s(s)W_{S3}(s) \end{pmatrix} \quad (60)$$

where  $y$  and  $y_{in}$  are written as follows:  $y_{in} = \begin{pmatrix} V^* \\ W^* \end{pmatrix}$ ,  $y = \begin{pmatrix} e_1 \\ e_2 \end{pmatrix}$ .

The sensitivity functions, denoted as  $S_S(s)$  and  $\varpi_s$ , can be expressed as follows:

$$S_S(s) = \frac{1}{1 + PI_\infty(s)G_{SMC}(s)B_1(s)} \quad (61)$$

$$\varpi(s) = \frac{PI_\infty(s)G_{SMC}(s)B_1(s)}{1 + PI_\infty(s)G_{SMC}(s)B_1(s)} \quad (62)$$

To ensure that the designed controller  $PI_\infty(s)$  meets the control objectives, it must satisfy the following condition:

$$\|F_L(P(s), PI_\infty(s))\|_\infty \leq \gamma \quad (63)$$

The design must meet Eq. (63) and select suitable weight functions for stability. To validate this condition, it is recommended to examine the norm of the H\_infinity of the gains within the transfer matrix  $\|F_L(P(s), PI_\infty(s))\|_\infty$ , ensuring these values remain below a specified boundary  $\gamma$ . This approach ensures a robust design, confirming the effectiveness and reliability of the introducing controller in achieving the optimal control objectives. This leads to:

$$\begin{cases} \|S_S(s)\|_\infty \leq \frac{\gamma}{\|W_{S1}(s)\|_\infty} \rightarrow \|S_S(s)\|_\infty \leq \frac{\gamma}{|W_{S1}(s)|} \\ \|S_S(s)G_{SMC}(s)B_1(s)\|_\infty \leq \frac{\gamma}{\|W_{S1}(s)W_{S3}(s)\|_\infty} \rightarrow \|S_S(s)G_{SMC}(s)B_1(s)\|_\infty \leq \frac{\gamma}{|W_{S1}(s)W_{S3}(s)|} \\ \|S_S(s)PI_\infty(s)\|_\infty \leq \frac{\gamma}{\|W_{S2}(s)\|_\infty} \rightarrow \|S_S(s)PI_\infty(s)\|_\infty \leq \frac{\gamma}{|W_{S2}(s)|} \\ \|\varpi_s(s)\|_\infty \leq \frac{\gamma}{\|W_{S2}(s)W_{S3}(s)\|_\infty} \rightarrow \|\varpi_s(s)\|_\infty \leq \frac{\gamma}{|W_{S2}(s)W_{S3}(s)|} \end{cases} \quad (64)$$

The mathematical expressions of these weight functions are expressed as:

$$\begin{cases} W_{S1}(s) = \frac{1}{K_{S1}} \cdot \frac{s+w_{cs}K_{S1}}{s+w_{cs}k_{s1}} \\ W_{S2}(s) = \frac{1}{k_{s2}} \cdot \frac{s+\frac{w_{cs}}{k_{s1}}}{s+\frac{w_{cs}}{k_{s1}}} \\ W_{S3}(s) = K'_2 \end{cases} \quad (65)$$

where

$$K_{s1} = K_{s2} = e^{-\frac{\log(10)}{20} \Delta G} \quad (66)$$

and

$$k_{s1} = k_{s2} = \varepsilon \quad (67)$$

In addition,  $K'_2$  have to be chosen less than  $\varepsilon$ .

The parameter  $w_{cs}$  represents the cutoff frequency, which plays a crucial role in shaping the dynamic response of the secondary control system. Since the primary control typically responds faster than the secondary control,  $w_{cs}$  must be selected to operate at a lower frequency than the primary control. This ensures that the secondary control system can effectively complement and stabilize the primary control response, reducing the risk of instabilities or oscillations in the overall control framework.

The parameters  $w_{cs}$  and  $\Delta G$  are key metrics for evaluating system performance, with  $w_{cs}$  representing the steady-state error and  $\Delta G$  indicating the gain margin. The next section provides a detailed overview of the NOA and explains how the NOA process is applied.

### Secondary control for DC microgrid using nonsmooth optimization algorithm

The NOA is used to address a specific optimization problem in secondary control design. Its main goal is to find a structured controller configuration that minimizes the  $H_\infty$  norm of  $F_L(P(s), PI_\infty(s))$ . This optimization aims to reduce the impact of disturbances, especially those represented by  $y_{in}$ , and stabilize  $P(s)$  within the system. By minimizing the  $H_\infty$  norm, the NOA enhances the system's ability to attenuate disturbances and maintain stability, leading to better performance and reliability in practical applications<sup>52</sup>. This optimization problem is formulated as follows:

$$\begin{aligned} & \underset{w \in \mathbb{R}}{\text{Minimize}} \|F_L(P(s), PI_\infty(s))\|_\infty \\ & \text{subject\_to } PI_\infty(s) \text{ stabilizes } P(s) \end{aligned} \quad (68)$$

The variable  $w$  denotes the frequency and is defined within the real interval  $\mathbb{R}$ ; The controller  $PI_\infty(s)$  is designed with a fixed structure similar to that of a PI control configuration.

The NOA relies on the derivative of the Clarke subdifferentiable function, which is defined as follows:

**Definition 1** (Clarke subdifferentiable function). Let consider two functions  $f(x)$  and  $G(x)$ , where  $f(x)$  is equal to the  $H_\infty$  norm of  $G(x)$ .  $f(x)$  can be written as follows:

$$f(x) = \|G(x)\|_\infty \quad (69)$$

The Clarke subdifferentiable function derived from  $f(x) = \|G(x)\|_\infty$  is written as follows:

$$\delta f(x) = \varphi'(x) \cdot \min(\phi(\varphi(x))) \quad (70)$$

where  $\varphi(x)$  is the smooth operator, mapping  $R^n$  on the space  $H_\infty$  of the  $G(x)$ ,  $\varphi'(x)$  is the adjoint of  $\varphi(x)$  and  $\phi(\varphi(x))$  is the subgradient  $\phi(x)$  of at  $G(x)$ .

**Definition 2** (Smooth operator). Let consider a function  $G(x)$  that links the outputs vector  $y$  to the inputs vector  $u$ . This mathematical relationship between  $u$  and  $y$  is expressed as follows:

$$y = G(x)u \quad (71)$$

where  $u$  and  $y$  can be written as:

$$y = \begin{pmatrix} y_1 \\ y_2 \\ \vdots \\ y_n \end{pmatrix} \tag{72}$$

$$u = \begin{pmatrix} u_1 \\ u_2 \\ \vdots \\ u_n \end{pmatrix} \tag{73}$$

$G(x)$  can be divided into smooth operators, where each operator is a subfunction derived from  $G(x)$ . Linking a single input to a single output, as expressed by the following equation:

$$y_j = \underset{u_i \rightarrow y_i}{G} (x) \cdot u_i \tag{74}$$

$G_{u_i \rightarrow y_j}(x)$  denotes the smooth operator.

**Definition 3 (Smooth operator subgradient).** Let's consider a function  $G(x)$ , and  $G_{u_i \rightarrow y_i}(x)$  is a smooth operator derived from  $G(x)$ . The subgradient of  $G_{u_i \rightarrow y_i}(x)$  at  $G(x)$  is given as

$$\phi \left( \underset{u_i \rightarrow y_i}{G} (x) \right) = \|G(x)\|_{\infty}^{-1} \operatorname{Re} \left( \operatorname{Tr} \left( G(x)^* \underset{u_i \rightarrow y_i}{u} \cdot \underset{u_i \rightarrow y_i}{u}^* \underset{u_i \rightarrow y_i}{G} (x) \right) \right) \tag{75}$$

Based on Definition 2, the smooth operators derived from  $F_L(P(s), PI_{\infty}(s))$  are given as follows:

$$e_1 = \underset{V^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s)) \cdot V^* \tag{76}$$

$$e_1 = \underset{W^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s)) \cdot W^* \tag{77}$$

$$e_2 = \underset{V^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s)) \cdot V^* \tag{78}$$

$$e_2 = \underset{W^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s)) \cdot W^* \tag{79}$$

As per Definition 3, subgradients can be determined using the smooth operators at  $F_L(P(s), PI_{\infty}(s))$  outlined in Eqs. (76), (77), (78), and (79). These equations can be expressed as follows after rewriting them accordingly.

$$\phi \left( \underset{V^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s)) \right) = \|F_L(P(s), PI_{\infty}(s))\|_{\infty}^{-1} \operatorname{Re} \left( \operatorname{Tr} \left( F_L(P(s), PI_{\infty}(s))^* \cdot \underset{V^* \rightarrow e_1}{u_1} \cdot \underset{V^* \rightarrow e_1}{u_1}^* \cdot \underset{V^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s)) \right) \right) \tag{80}$$

$$\phi \left( \underset{W^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s)) \right) = \|F_L(P(s), PI_{\infty}(s))\|_{\infty}^{-1} \operatorname{Re} \left( \operatorname{Tr} \left( F_L(P(s), PI_{\infty}(s))^* \cdot \underset{W^* \rightarrow e_1}{u_1} \cdot \underset{W^* \rightarrow e_1}{u_1}^* \cdot \underset{W^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s)) \right) \right) \tag{81}$$

$$\phi \left( \underset{V^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s)) \right) = \|F_L(P(s), PI_{\infty}(s))\|_{\infty}^{-1} \operatorname{Re} \left( \operatorname{Tr} \left( F_L(P(s), PI_{\infty}(s))^* \cdot \underset{V^* \rightarrow e_2}{u_1} \cdot \underset{V^* \rightarrow e_2}{u_1}^* \cdot \underset{V^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s)) \right) \right) \tag{82}$$

$$\phi \left( \underset{W^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s)) \right) = \|F_L(P(s), PI_{\infty}(s))\|_{\infty}^{-1} \operatorname{Re} \left( \operatorname{Tr} \left( F_L(P(s), PI_{\infty}(s))^* \cdot \underset{W^* \rightarrow e_2}{u_1} \cdot \underset{W^* \rightarrow e_2}{u_1}^* \cdot \underset{W^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s)) \right) \right) \tag{83}$$

According to Definition 1, Clarke subdifferentiable functions derived from Eqs. (80), (81), (82), and (83) can be expressed as follows:

$$\delta f_1(x) = \underset{V^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s))^* (x) \cdot \min_{w \in R} \left( \phi \left( \underset{V^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s)) (x) \right) \right) \tag{84}$$

$$\delta f_1(x) = \underset{W^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s))^* (x) \cdot \min_{w \in R} \left( \phi \left( \underset{W^* \rightarrow e_1}{F_L} (P(s), PI_{\infty}(s)) (x) \right) \right) \tag{85}$$

$$\delta f_1(x) = \underset{V^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s))^* (x) \cdot \min_{w \in R} \left( \phi \left( \underset{V^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s)) (x) \right) \right) \tag{86}$$

$$\delta f_1(x) = \underset{W^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s))^* (x) \cdot \min_{w \in R} \left( \phi \left( \underset{W^* \rightarrow e_2}{F_L} (P(s), PI_{\infty}(s)) (x) \right) \right) \tag{87}$$

The data of the controller  $PI_{\infty}(s)$ , represented by  $x$ , can be expressed as follows:

$$x = (k_{p\infty} \quad k_{i\infty}) \tag{88}$$

The NOA operates using subgradients and Clarke subdifferentiable functions. The NOA process involves the following steps.

- *Step 1* start the variable  $x$  with a large initial value, denoted as  $x = x^+$
- *Step 2* Minimize Eqs. (80) to (83) as part of solving a convex optimization problem.
- *Step 3* Insert the minimal values from Eqs. (80) to (83) into Eqs. (84) to (87). If all results are non-zero, decrease  $x$  by  $\Delta x$  ( $x = x^+ - \Delta x$ ) (where  $\Delta x = (\Delta k_p \frac{\Delta k_p}{\|d\|})$ ). Choose  $\Delta k_p$  as small as possible, and let  $d$  should be the subgradients vector from Eqs. (84) to (87). Update  $x^+$  with the new  $x$  and go back to Step 2. If any Equation equals zero, check the condition in Eq. (64). If satisfied, stop and use the controller as the solution from Eq. (68). If the condition is met, go to Step 4 to calculate  $\gamma$ .
- *Step 4* Update the weight functions and restart at Step 1. The process concludes when the weight functions have effectively optimized the controller.

The steps of the NOA Algorithm are illustrated in the flowchart shown in Fig. 10.

**Stability analysis**

The stability analysis of the system under investigation necessitates the verification of the condition in Eq. (64) for varying system parameters, including DC bus voltage thresholds of  $v_b - 40\% < v_b < v_b + 40\%$ , using the singular value plot. In this context, the singular value evolutions of the sensitivity and complementary sensitivity functions are presented in Fig. 11. The system parameters employed for the stability study are provided in Table 1.

Where the controller that have been used for the secondary controller is defined as follows:

$$PI_{\infty}(s) = 0.0017 \cdot \frac{1 + 1.5455 \cdot s}{1.5455 \cdot s} \tag{89}$$

According to the generated algorithm, the weight functions applied to the secondary controller are specified as follows:

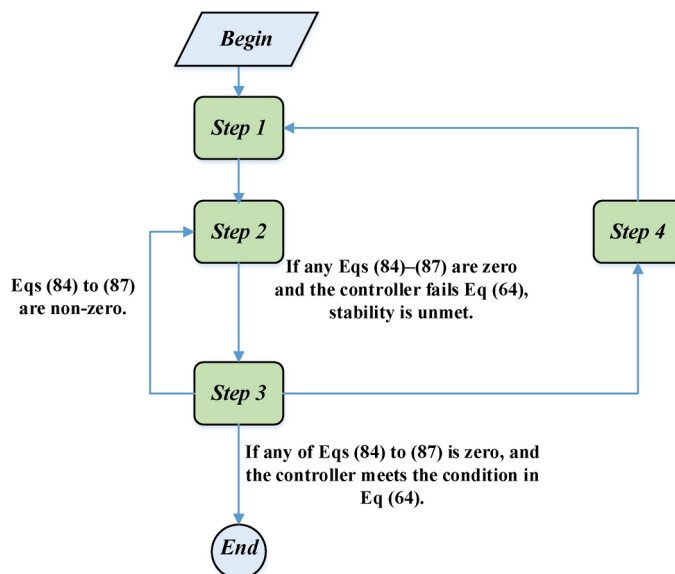
$$\begin{cases} W_{S1}(s) = \frac{0.5 \cdot s + 321.5}{s + 0.3120} \\ W_{S2}(s) = \frac{10^3 \cdot s + 15.6250 \cdot 10^4}{s + 3152 \cdot 10^6} \\ W_{S3}(s) = 3 \cdot 10^{-4} \end{cases} \tag{90}$$

$\gamma$  is given as follows:

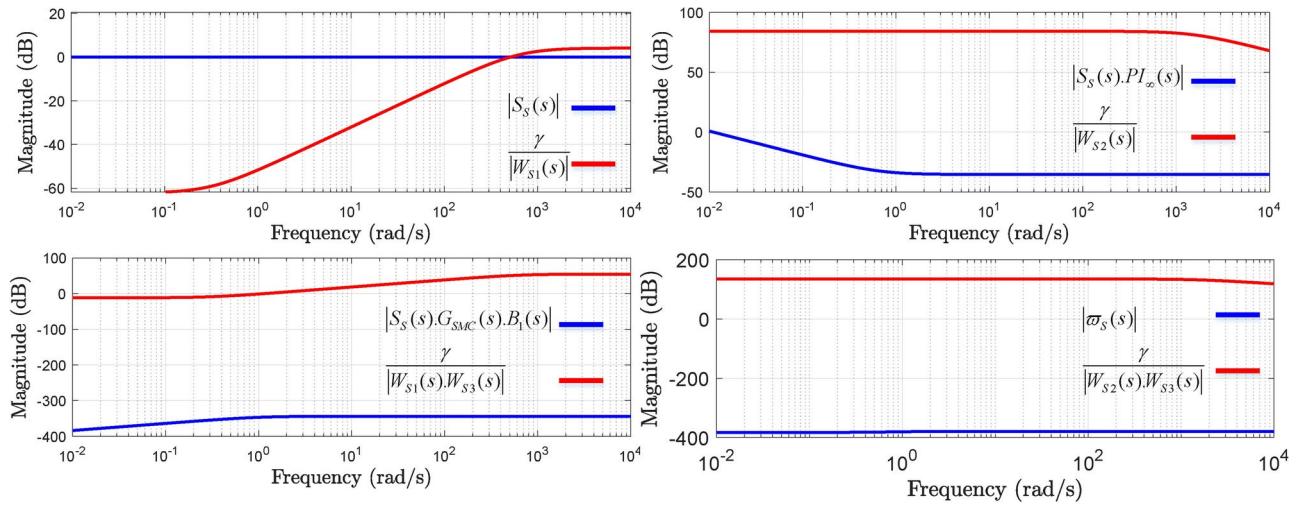
$$\gamma = 0.80 \tag{91}$$

$f_i$  and  $\beta_i$  are selected for each DC-DC buck converter as follows:

$$\begin{cases} f_i = 1 \\ \beta_i = 1 \end{cases} \tag{92}$$



**Fig. 10.** Nonsmooth optimization algorithm flowchart.



**Fig. 11.** Frequency response analysis based on the evolution of Eq. (64).

Variables	Description	Values
$V_{ref}$	Reference bus voltage	16 V
$V_{in}$	DC power supply voltage	32 V
$L_{o1}$	Inductance nominal value of converter_1	6 m
$L_{o2}$	Inductance nominal value of converter_2	2.7 mH
$C_o$	Capacitance nominal value	1000 $\mu$ F
$f_s$	Switching frequency	25 kHz
$P_{cpl}$	CPL power	10 W
$Z_{Line}$	Transmission line impedance	10(mH) + 30( $\mu$ F)

**Table 1.** DC microgrid parameters values.

As shown in Fig. 11, the condition specified in Eq. (64) is verified, indicating that the stability criteria for the proposed  $H_\infty$  control design are met. This confirms the ability of the proposed control strategy to effectively attenuate all disturbances in the DC bus. The performance of the  $PI_\infty(s)$  control scheme is further demonstrated as follows:

Based on Fig. 9 and neglecting the influence of the weight functions in the proposed control loop, the error  $y$  ( $y = V^* - v_b$ ) and the voltage compensation signal  $s_i$  can be expressed as follows:

$$\begin{cases} y = S_S(s)V^* + S_S(s)G_{SMC}(s)W^* \\ s_i = S_S(s)PI_\infty(s) \cdot V^* - \varpi_S(s)W^* \end{cases} \quad (93)$$

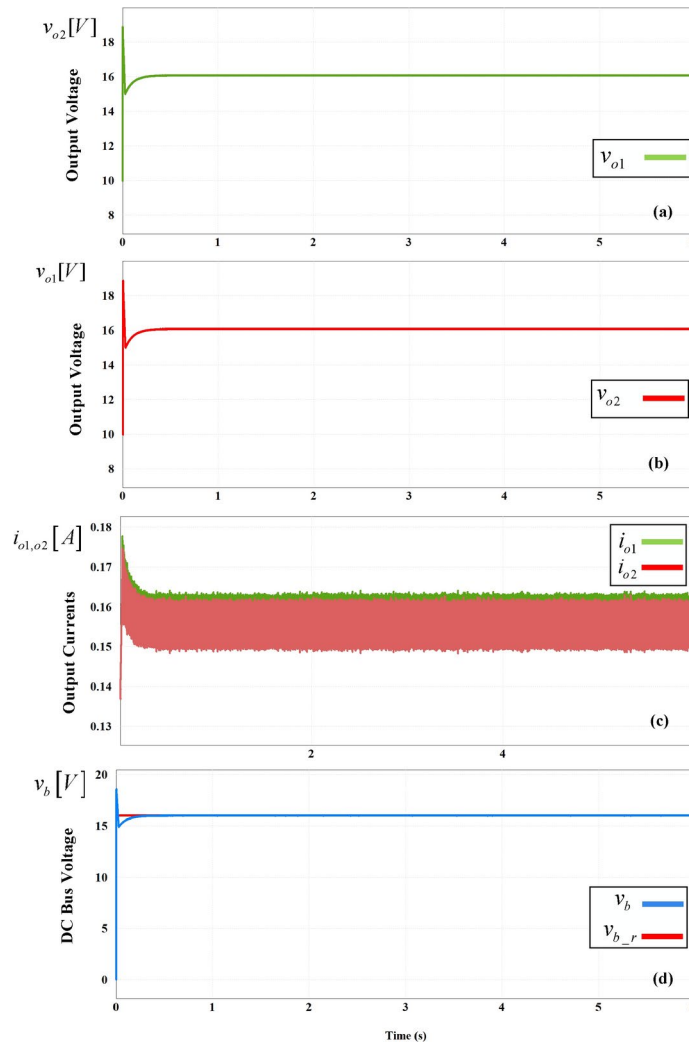
Based on the obtained singular plots, the magnitude of all expressions in Eq. (64) is less than 1, where ( $|S_S(s)G_{SMC}(s)| \ll 1$ ,  $|S_S(s)G_{SMC}(s)| \ll 1$ ,  $|\varpi_S(s)| \ll 1$ ,  $|S_S(s)G_{SMC}(s)B_1(s)| \ll 1$ ).

This implies that the influence of the disturbance variables  $V^*$  and  $W^*$  on the  $y$  and  $s_i$  is neglected. Therefore, based on Eq. (58),  $y$  depends exclusively on  $s_i$ .

### Simulation results

A simulation using PSIM software was conducted to test the developed controller, modeling a DC MG as illustrated in Fig. 4, and operating under the proposed approach. This MG consists of two parallel-connected buck converters supplying a CPL. These two DC–DC converters have differing LC filter parameters. The input voltage for the converters is supplied by DC sources, serving as an equivalent model of RESS. Various scenarios were tested throughout the simulation. Due to an external disturbance in the MG, fluctuations in the load and input voltage are taken into account in this simulation. The parameters of the DC–DC buck converters are given in Table 1.

Figure 12 illustrates the performance of the DC MG with the proposed secondary controller, highlighting quick settling times (0.2 s), minimal overshoot, and accurate tracking of the output voltages, achieving a stable zero steady-state error. Furthermore, proportional load current sharing is achieved among the DGs, ensuring the restoration and stability of the DC bus voltage.



**Fig. 12.** Closed-loop response of the DC MG with the proposed secondary controller: (a)  $v_{o1}$ , (b)  $v_{o2}$ , (c) output currents, (d) DC bus voltage.

### Case 1: activated of the proposed controller test

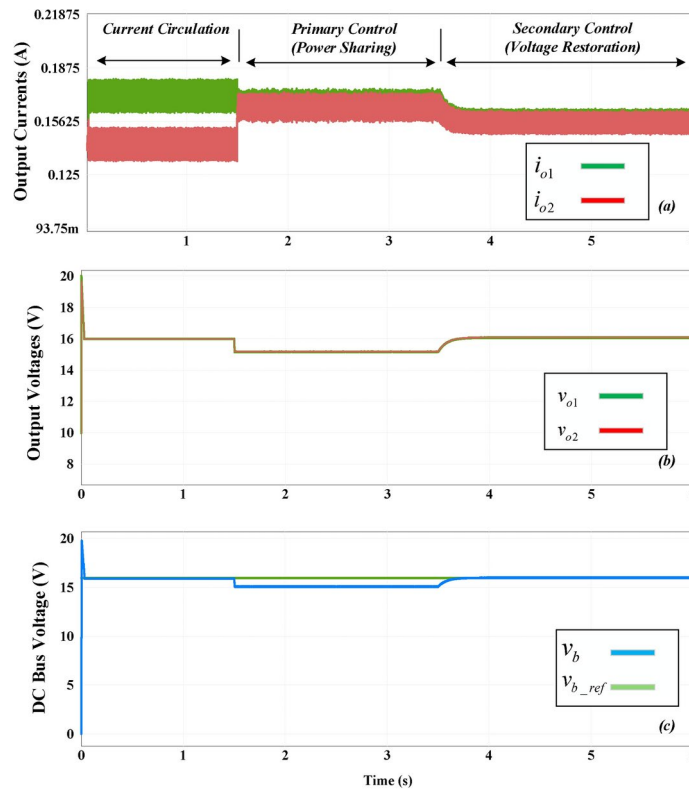
Initially, the stability of the DC MG with the proposed secondary controller is evaluated. Prior to  $t = 1.5$  s, the two DGs operate in parallel, each regulating its respective output voltage. The terminal voltage is maintained at a reference value of 16 V (see to Fig. 13). Due to variations in load, the output currents of the DGs differ (see Fig. 13b). At  $t = 3.5$  s, DG-1 and DG-2 are synchronized using primary controllers (see Fig. 13c), with the virtual impedance in the droop controls set to 5  $\Omega$ . Subsequently, the secondary controller is activated at  $t = 3.5$  s to correct the voltage deviation caused by the primary control, which draws 10 W.

As illustrated in Fig. 13b, proportional load current sharing is achieved by automatically adjusting the DG voltages (see Fig. 13a) to their nominal values using the proposed secondary controller.

### Case 2: power demand variation test

The simulation results validate the effectiveness of the proposed controller in stabilizing the DC MG system under dynamic and challenging conditions. Specifically, the controller successfully mitigates fluctuations caused by abrupt changes in the power demand of a CPL, as shown in Fig. 14. Initially, the system operates at a steady state with a power demand of 10 W. Between  $t = 1$  s and  $t = 3.5$  s, the CPL power demand increases rapidly to 25 W. Despite this significant demand increase, the controller ensures system stability, effectively preventing oscillations or sudden transient disturbances. A further increase in power demand to 35 W between  $t = 3.5$  s and  $t = 4.5$  s, with the controller once again demonstrating its robustness by promptly adjusting to the new load while maintaining stable operation. Finally, an additional sudden increase of 15 W is applied from  $t = 4.5$  s to the end of the simulation, further complicating the power demand profile. The controller continues to stabilize the system, as evidenced by the absence of fluctuations in Fig. 14.

These simulation results show that the controller is strong and flexible in handling sudden large changes in power demand from the load of the DC MG. Its ability to reduce quick fluctuations and prevent instability makes it valuable for keeping DC MG systems reliable, especially in environments where power needs change randomly.



**Fig. 13.** Response to secondary control activation: (a) output currents, (b) output voltages, (c) DC bus voltage.

This capability is vital for applications with fluctuating power demands, as it allows for consistent performance and reliable operation under a variety of scenarios.

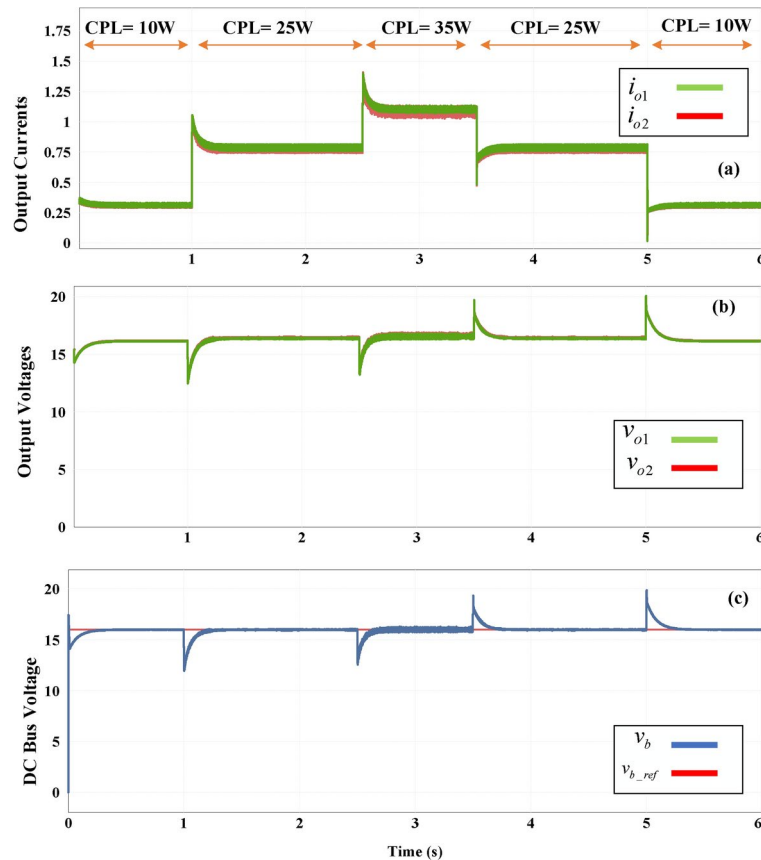
### Case 3: input voltage variation test

To thoroughly evaluate the robustness and effectiveness of the proposed secondary controller under challenging conditions, a set of tests was conducted simulating significant input voltage fluctuations. These tests involved voltage drops of up to 45%, as illustrated in Fig. 15, where the input voltage initially decreased from 32 to 17 V before returning to the nominal level. The simulation results indicate that the controller successfully maintained the output voltages of both DGs and the DC bus close to their reference values, despite the large variations in input voltage. This performance demonstrates the fast response capabilities of the controller, as it minimized the risk of overshoot or instability, a common issue during abrupt voltage changes.

Additionally, the secondary controller effectively balanced current sharing among the DGs, which is essential for stable and efficient MG operation. The ability to keep inductor current variations low further indicates that the controller can stabilize internal currents under non-ideal input conditions. This balanced current distribution not only helps protect the DGs from overloading but also extends their durability by ensuring a more even load distribution. Such robust control over fluctuating input voltages is crucial in practical applications where voltage conditions are not always stable, highlighting the value of the controller for reliable and consistent DC MG operation in real-world settings.

### Case 4: DC bus reference variation test

This test aims to evaluate the stability and robustness of the system by introducing a step change in the DC bus reference voltage within the DC MG, as illustrated in Fig. 16. Initially, the DC bus voltage stabilizes at 16 V, reflecting a rapid response to the set reference. At  $t = 1.5$  s, the reference voltage is increased to 19 V, and at  $t = 3.5$  s, it reverts to the original value (see Fig. 16a). During these transitions, the system effectively adapts by adjusting the output currents of both DC-DC converters, ensuring stable power-sharing and mitigating instability (see Fig. 16b). The test results reveal that the DC bus voltage tracks the target profile accurately, showing minimal settling time, no overshoot, and a high degree of stability, even with significant step variations in the reference value. Furthermore, the proposed secondary compensation control ensures the DC bus voltage adjusts closely to the desired reference value, highlighting its effectiveness in high-performance applications (see Fig. 16d). This control approach enhances system stability, demonstrating robustness against voltage variations while maintaining balanced load sharing across the DC-DC converters. Consequently, the developed control technique proves to be robust, showing that the system can manage sudden changes in the DC bus voltage reference without compromising power distribution or operational stability.



**Fig. 14.** System response to changing CPL power demand: (a) output currents, (b) output voltages, (c) DC bus voltage.

### Case 5: DG plug-and-play

This study investigates the plug-and-play capabilities of the suggested secondary control for DG units in a DC MG, as shown in Fig. 17. The setup involves DG-2, initially integrated with the DC bus and operating under the primary and secondary controllers, which ensure a stable output voltage of 16 V. At  $t = 1.5$  s, DG-2 is intentionally unplugged from the DC bus, creating a test scenario for the response of the suggested controller. Following the disconnection, the DC bus voltage remains steady at 16 V, suggesting the capacity of the system to maintain voltage levels in the absence of DG-2. The unplugged period continues until  $t = 3$  s, after which DG-2 is restored to the DC bus. This reconnection promptly restores stability across the DC bus, illustrating the capability of the controller to seamlessly reintegrate DG units without causing transient disturbances. This response highlights the effectiveness of the controller in maintaining system stability and managing dynamic changes in network configuration.

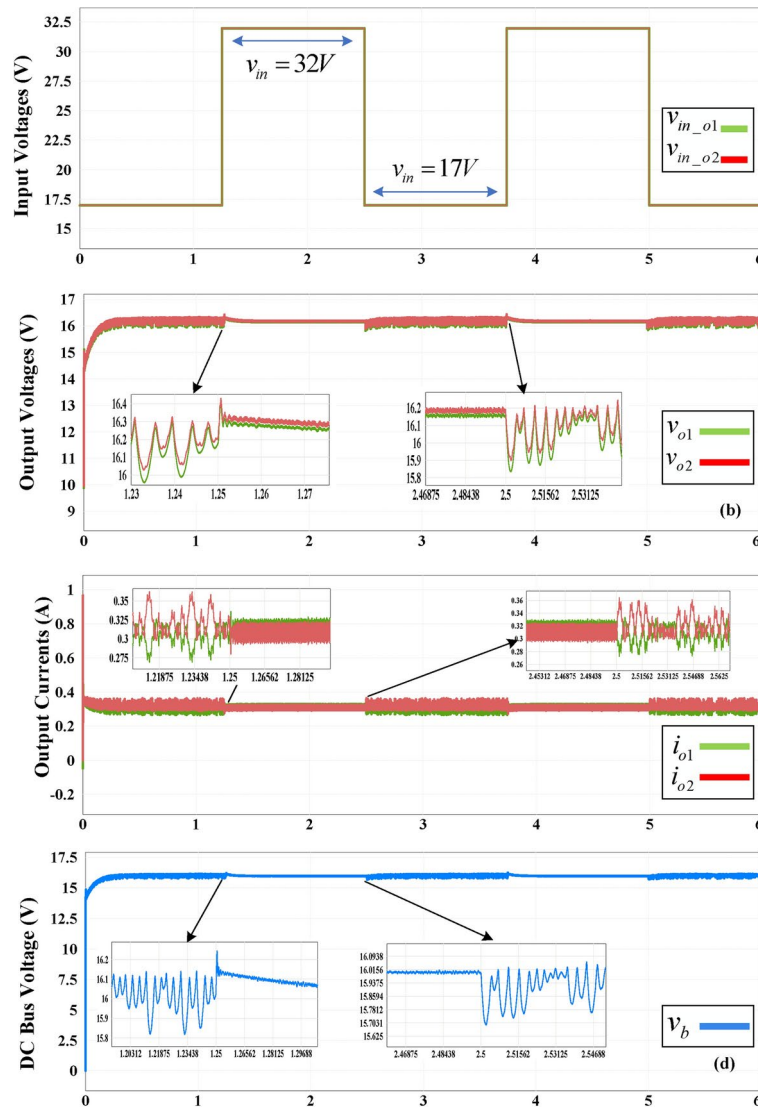
The results, as illustrated in the accompanying Fig. 17, highlight the effectiveness of the proposed controller in regulating voltage and ensuring system stability despite the plug-and-play behavior of DG units. By eliminating voltage deviation and maintaining a steady-state condition, the controller proves to be a robust solution for ensuring power quality within dynamic and flexible distributed energy systems. This functionality is essential for MGs, where the intermittent nature of DG units and varying load demands necessitate a control strategy capable of rapid adaptation. Consequently, this study affirms the suitability of the secondary controller for applications requiring high levels of reliability and resilience, thereby supporting the integration of distributed generation in sustainable and efficient power networks.

### Comparative performance assessment:

This subsection presents a comparative performance analysis of the proposed hybrid sliding mode  $H_\infty$  control for primary and secondary control, compared to well-known existing methods in the literature, as shown in Table 2. From Table 2, it can be inferred that the proposed control outperforms all other algorithms, making it an effective solution for handling power sharing and voltage regulation, even under external disturbances such as input voltage variation, power load demand fluctuations, plug-and-play scenarios, and uncertainties.

### Experimental validation

A scaled-down laboratory prototype of a DC MG with two DGs was implemented to experimentally validate the proposed controller. The experimental setup was carried out based on the generated C code from PSIM software. In this experiment, a voltage-controlled boost converter, acting as a CPL, was supplied by two parallel buck



**Fig. 15.** System response under input voltage fluctuations: (a) input voltage variation test, (b) output voltages, (c) output currents, (d) DC bus voltage.

converters, forming the DC MG. To simulate line impedance effects, resistors were placed between each output of the converters and the main DC bus, replicating real MG conditions.

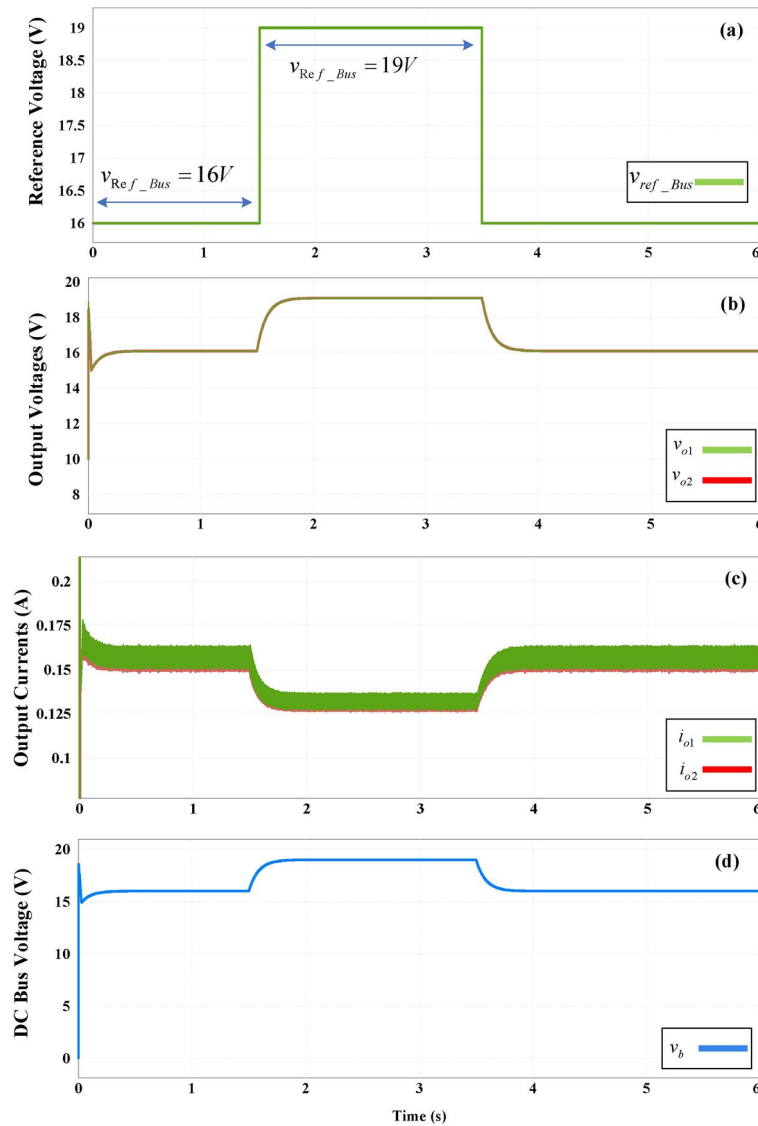
The experimental setup, depicted in Fig. 18, models each DG as an ideal voltage source ( $V_{DC} = 36\text{ V}$ ) paired with a buck converter, representing the power generation units in the DC MG. The setup was built using a voltage sensor (LA25-NP, 717087) and a current sensor (LV25-P, 714227). Control algorithms for the system were implemented on a DSP28335 microcontroller, which generates pulse-width modulation (PWM) signals for both buck converters and the boost converter acting as the CPL. Data acquisition and PWM frequencies were both set at 25 kHz for synchronized control.

The effectiveness of the proposed controller was tested under four scenarios:

- Test 1: Secondary control activation.
- Test 2: Power load demand variation.
- Test 3: DC bus voltage reference variation.
- Test 4: Plug and play.

This experimental setup allowed for testing voltage regulation, stability, and the robustness of the secondary control approach under dynamic conditions. It is worth noting that, despite the parameters listed in Table 1 not being identical to those used in the implementation, all experimental results demonstrated excellent tracking performance and disturbance rejection in all scenarios.

Figures 19, 20, 21, 22, 23, 24, 25, 26 and 27 illustrate the experimental results. Detailed configuration parameters, including component values and system settings, are provided in Table 3.



**Fig. 16.** System response under reference DC bus voltage changes: (a) reference DC bus voltage variation test; (b) output voltages; (c) output currents; (d) DC bus voltage.

The parameters of the boost converter are:  $v_{in\_boost} = 18$  V,  $v_{o\_boost} = 22$  V,  $C_{o\_boost} = 470$   $\mu$ F,  $L_{o\_boost} = 0.52$  mH,  $R_{L\_boost} = 33$   $\Omega$ ,  $f_{sw\_boost} = 25$  kHz.

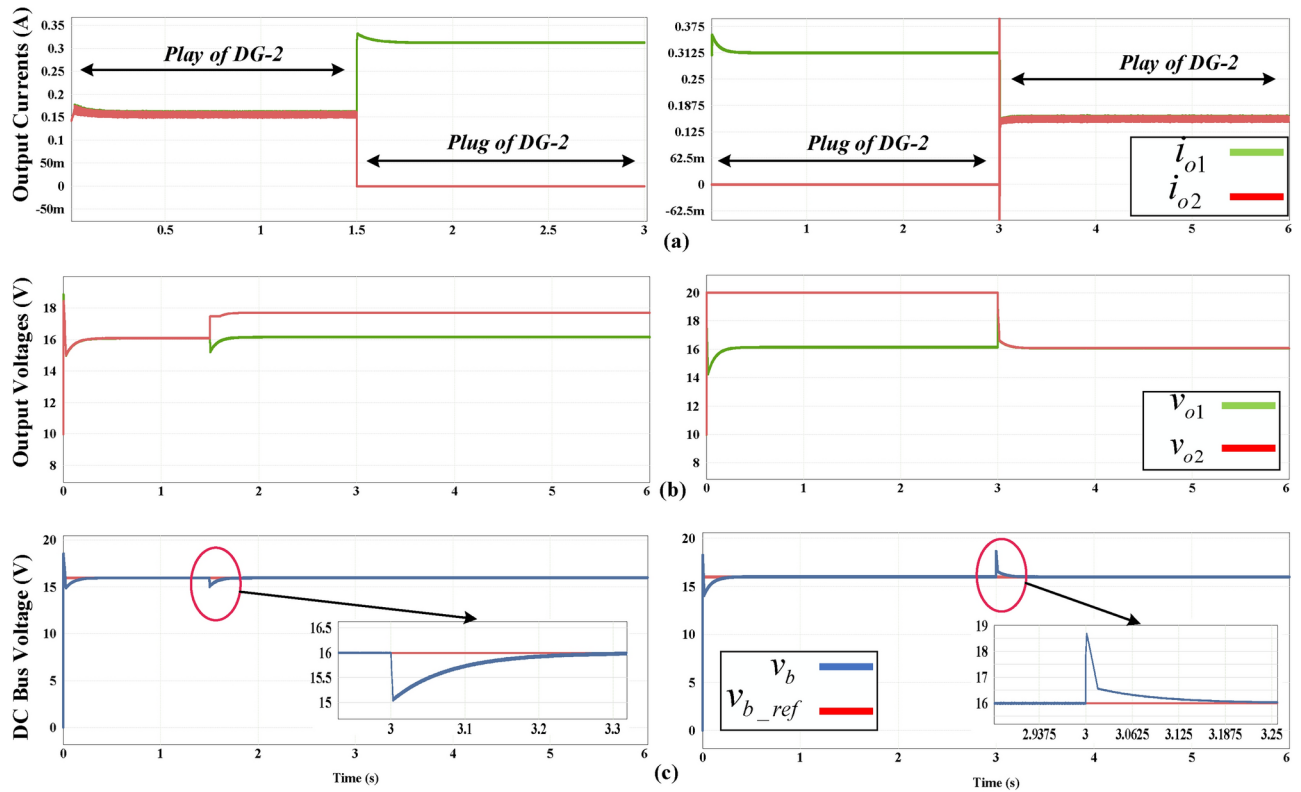
### Experimental results with the secondary control activation

In this sub-section, the proposed secondary control technique is evaluated under a scenario that includes secondary control activation. The experimental results in real time, presented in Figs. 19, 20, and 21, show the systems behavior before and after control activation. Initially, neither primary nor secondary control is active, resulting in output voltage drops for  $v_{o1}$  and  $v_{o2}$  to 16.5 V and 17 V, respectively, and a DC bus voltage of 17.2 V. This deviation from the reference voltage  $v_b = 18$  V is attributed to the issue of current circulation within the system.

Upon activation of the primary control, output voltages  $v_{o1}$  and  $v_{o2}$  further drop to 13.4 V and 13.5 V, with the DC bus voltage decreasing to 13.4 V, creating a substantial deviation from the required reference values. However, under primary control, a balanced power-sharing ratio is achieved between DGs with a fast-settling time around of 0.2 s, although overshoot is not observed. These observations emphasize the need for secondary control to maintain stable output and bus voltages while ensuring accurate power-sharing.

Upon activation of the proposed secondary control, the DC bus voltage is restored to the desired reference value with a fast response within 0.75 s, and no overshoot is noted. The control strategy effectively stabilizes voltage and maintains a consistent power-sharing ratio among the distributed generators, ensuring balanced load distribution.

The experimental evaluation demonstrates that the proposed secondary control strategy effectively stabilizes the DC bus voltage at the desired reference value and maintains a balanced power-sharing ratio between the



**Fig. 17.** Response to plug and play: (a) output currents; (b) output voltages; (c) DC bus voltage.

Refs.	Objectives	Voltage regulation	Power sharing	Disturbance rejection	Stability under CPL	Implementation complexity	Tracking speed	Power efficiency
Proposed	Optimize voltage, power, disturbance, and stability	Very high	High	Very high	High	Low	Fast	Very high
18	Review of hierarchical control strategies	Good	Good	Moderate	Moderate	Moderate	Moderate	Moderate
19	Secondary control for voltage and load sharing	Good	Good	High	Good	Moderate	High	High
20	Challenges in CPLs in droop-controlled DC MGs	Moderate	Moderate	High	Low	High	Low	Low
23	Novel secondary optimal control for storage	High	High	High	High	Moderate	Moderate	High
24	Distributed secondary control via current derivatives	High	High	High	High	High	High	High
25	Enhanced droop control method	Moderate	High	High	Moderate	Moderate	High	Moderate
49	Decentralized primary and secondary control for DC MGs	High	High	High	High	Moderate	High	High

**Table 2.** Comparison of the proposed hybrid sliding mode  $H^\infty$  control with other techniques on a qualitative basis.

DGs. Without any control activation, voltage deviations occur due to current circulation, leading to significant drops in both output voltages and DC bus voltage. While primary control achieves power-sharing, it does not adequately address voltage stability. The activation of secondary control successfully resolves these issues, highlighting its essential role in achieving both voltage regulation and balanced current-sharing distribution within the DC MG.

**Experimental results with constant power load fluctuation**

In this sub-section, we evaluate the proposed controller under conditions where the CPL fluctuates. To test the response of the system, the CPL power is varied from 10 to 20 W before returning to its nominal value. The experimental results, displayed in Figs. 22, 23, and 24, indicate that despite these fluctuations, whether the power load demand steps up or down, the DC bus voltage remains stable at  $v_b = 18$  V.

The two DGs exhibit effective current-sharing, producing nearly equal output while maintaining stable output voltages unaffected by fluctuations. The performance conforms to the droop control method and the functionality of local controllers, demonstrating the robustness of the proposed control strategy.

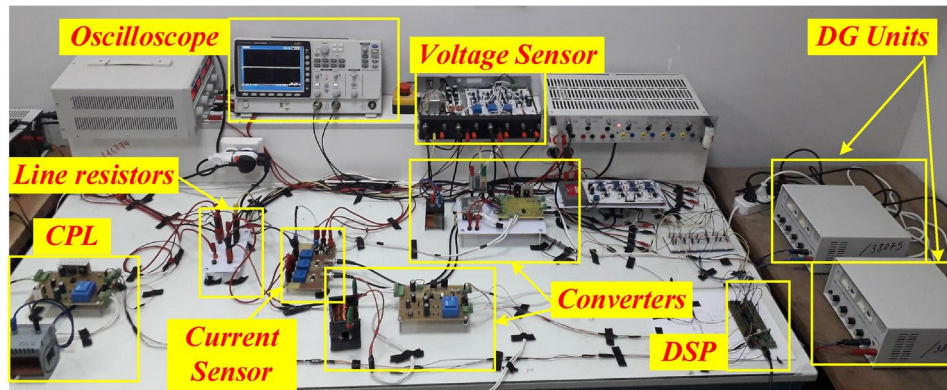


Fig. 18. Experiment setup.

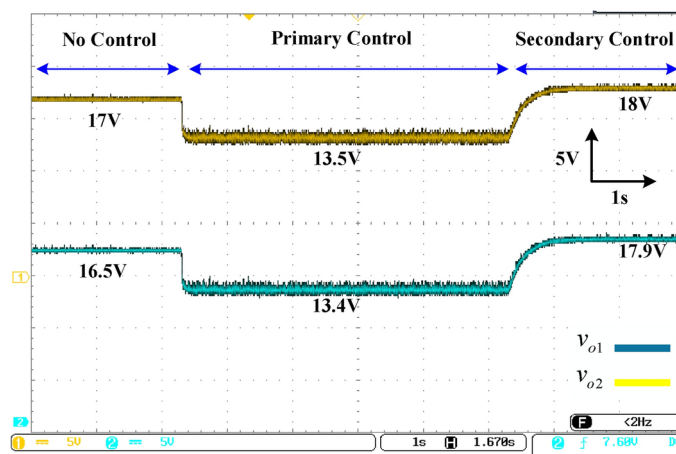


Fig. 19. Experimental results: time evolution of DG output voltages during secondary control activation.

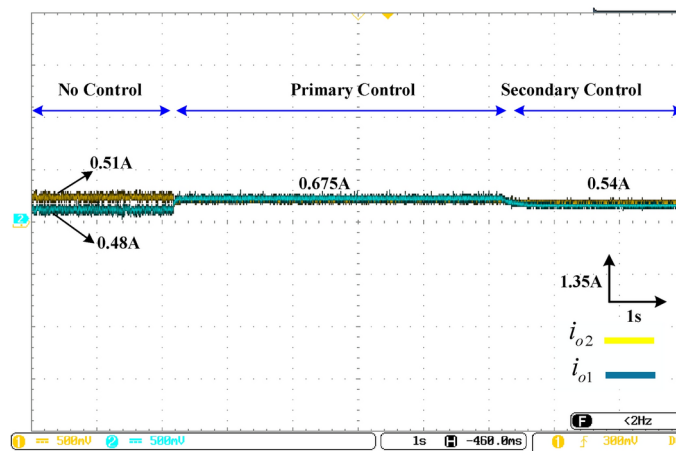


Fig. 20. Experimental result: time evolution of the output currents of each DG under secondary control activation.

The proposed control maintains DC bus voltage stability at the reference value of  $v_b = 18$  V, rejecting all fluctuations with a good response time of around 0.7 s and negligible overshoot. The experimental results confirm that the DC bus voltage remains stable despite variations in the CPL, while the DGs efficiently share the current output and maintain stable voltages across the buck converters. This finding, consistent with the droop

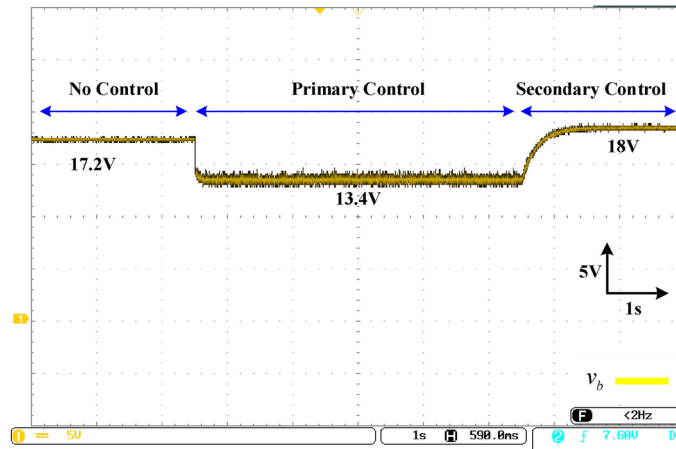


Fig. 21. Experimental result: time evolution of the DC bus voltage under secondary control activation.

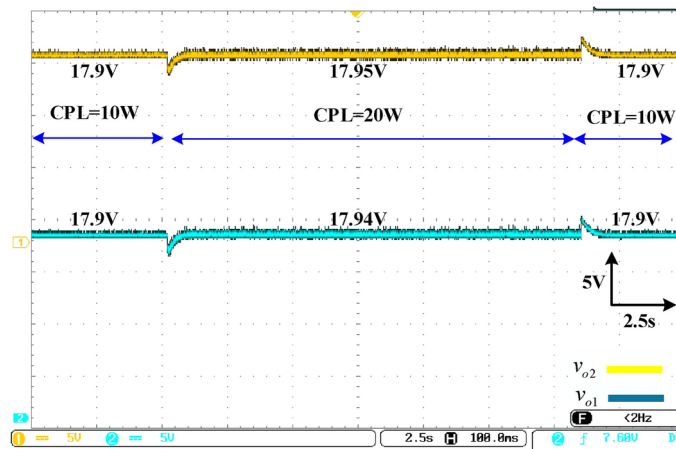


Fig. 22. Experimental results: time evolution of the output voltages of each DG under CPL variation.

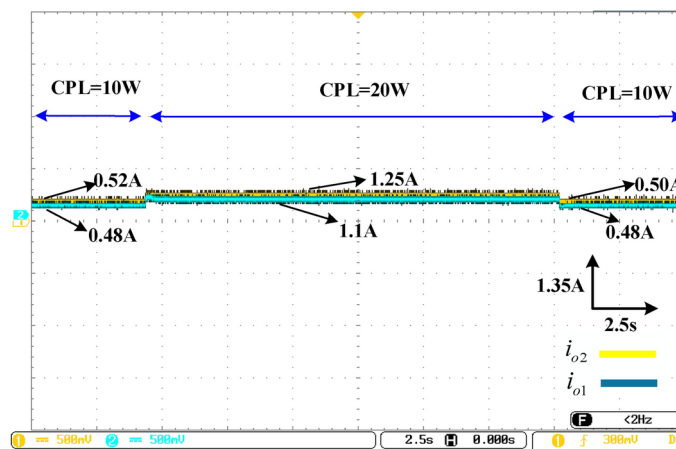


Fig. 23. Experimental results: time evolution of DG output currents during CPL variation.

control design, highlights the effectiveness of the control strategy in achieving reliable voltage regulation and balanced load distribution within the system, even under dynamic operating conditions.

These results highlight the system ability to maintain voltage stability and ensure balanced load distribution among DGs, even under fluctuations in the CPL.

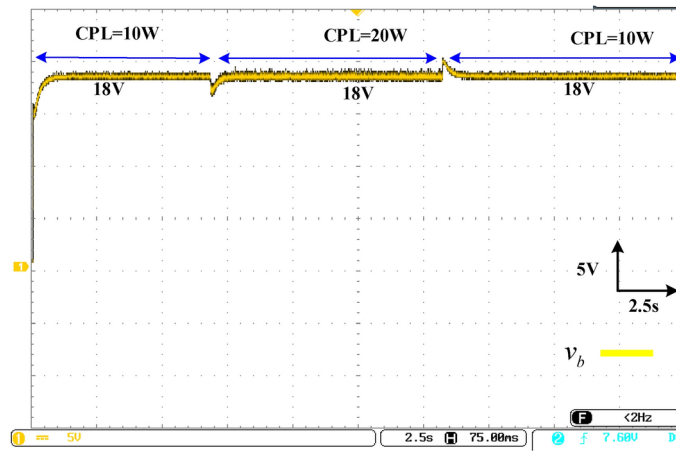


Fig. 24. Experimental result: time evolution of the DC bus voltage under CPL variation.

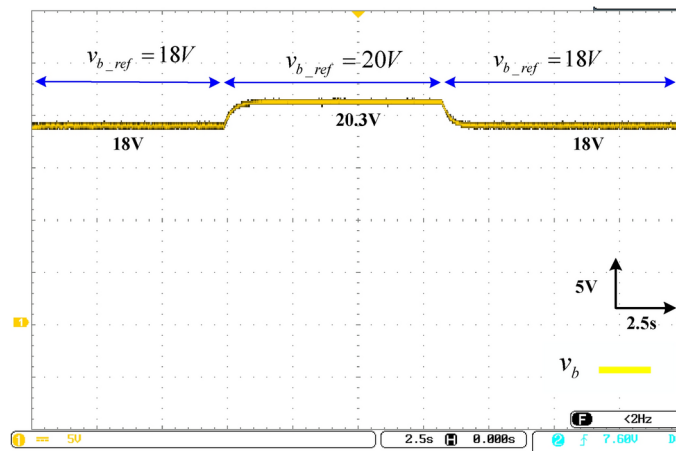


Fig. 25. Experimental result: time evolution of the DC bus voltage response to reference value changes.

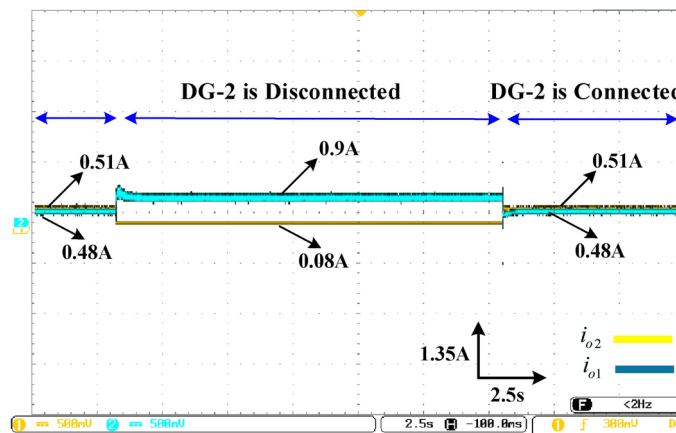
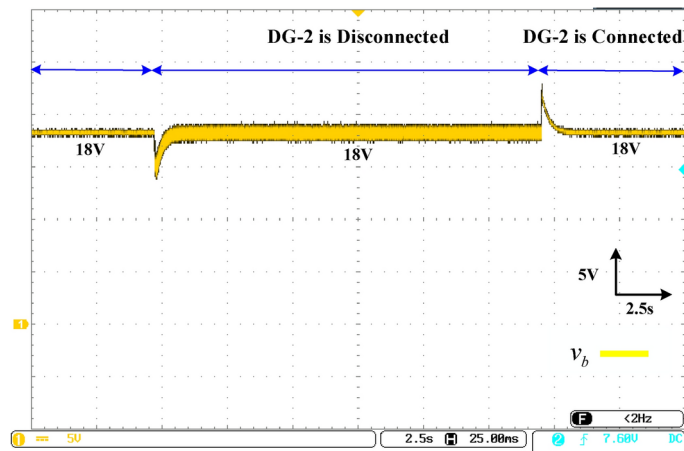


Fig. 26. Experimental results: time evolution of DG output currents during plug-and-play scenario.

### Experimental results with DC bus voltage reference variation

This sub-section evaluates the performance of the proposed controller under varying DC bus voltage reference conditions. The DC bus reference voltage is adjusted from 18 to 20 V and then returned to its nominal value. This scenario was used to assess the response of the DC bus under the proposed secondary control strategy with a



**Fig. 27.** Experimental result: time evolution of the DC bus voltage under the scenario of plug-and-play.

	DG-1		DG-2	
DG	$v_{in-1}$	36 V	$v_{in-2}$	36 V
	$f_s$	25 kHz	$f_s$	25 kHz
LC filter	$L_1$	6 mH	$L_2$	2.7 mH
	$C_1$	470 $\mu$ F	$C_2$	470 $\mu$ F
Line resistance	$R_{line\_1}$	1 $\Omega$	$R_{line\_2}$	2 $\Omega$
Primary control (SMC parameters)	$\lambda$	10 e16	$\lambda$	10 e16
	$k$	10 e20	$k$	10 e20
	$q$	10 e16	$q$	10 e16
Droop gain	$R_D$	5 $\Omega$	$R_D$	5 $\Omega$
Secondary control	$K$	0.0017	$K$	0.0017
	$T$	1.5455	$T$	1.5455
DC bus reference	$v_{b\_ref} = 18$ V			
CPL power	10 W			

**Table 3.** Parameters of the MG system and controller.

variable reference voltage. The experimental results show that the DC bus voltage tracks the reference value with a fast-settling time of approximately 0.8 s, even when the reference voltage fluctuates.

Experimental results, displayed in Fig. 25, demonstrate that the DC bus voltage remains stable regardless of fluctuations in the reference, whether it increases or decreases.

### Experimental results with plug-and-play

This sub-section examines the systems performance during the plug-and-play integration of DG-2 into the DC MG. DG-2 is sequentially disconnected and reconnected to the DC bus to assess the systems response. The experimental results, shown in Figs. 26 and 27, demonstrate that the proposed secondary control method effectively rejects fluctuations, maintaining the DC bus voltage at the reference value throughout the operation. Additionally, DG-1 adjusts its current output, nearly doubling it, to share the load almost equally in response to DG-2s disconnection.

The results confirm that the control strategy maintains DC bus voltage stability during DG-2s plug-and-play operation. Despite DG-2s disconnection and reconnection, the control method eliminates fluctuations, ensuring the DC bus voltage remains at the reference value with a fast response time of approximately 0.4 s. Furthermore, DG-1 increases its current output, ensuring balanced load sharing when DG-2 is disconnected. These findings underscore the robustness of the secondary control in enhancing voltage stability and adaptive load distribution in a plug-and-play scenario.

### Comparison between simulation and experimental results

To validate the proposed control strategy, this subsection presents a comparison of key performance metrics obtained from simulation and experimental results, as shown in Table 4. This table includes overshoot, efficiency, and time response, providing insights into the practical applicability of the control approach under real-time conditions. The comparison shows strong agreement between simulation and experimental results, with minor

Experiment	Metric	Simulation results	Experimental results	Improvement
CPL fluctuation experiment	Efficiency (%)	94	88	6
	Overshoot (%)	2.8	3.1	-0.3
	Response time (s)	0.25	0.7	-0.45
	Waveform comparison	Figure 14c	Figure 24	
Secondary control activation experiment	Efficiency (%)	96.8	89.5	7.3
	Overshoot (%)	0	0	0
	Response time (s)	0.35	0.75	-0.4
	Waveform comparison	Figure 13d	Figure 19	
DC bus voltage reference experiment	Efficiency (%)	96.5	92.5	4
	Overshoot (%)	0	0	0
	Response time (s)	0.7	0.8	-0.1
	Waveform comparison	Figure 16d	Figure 25	
Plug and play experiment	Efficiency (%)	94.8	90.5	4.3
	Overshoot (%)	15.625	16.666	-1.041
	Response time (s)	0.25	0.4	-0.15
	Waveform comparison	Figure 17c	Figure 27	

**Table 4.** Comparison of simulation and experimental results for key performance metrics.

discrepancies attributed to hardware limitations and unmodeled parasitic effects. These findings confirm the robustness and practical feasibility of the proposed method.

## Conclusion

In this paper, a hybrid sliding mode and H-infinity control strategy is proposed for enhanced primary and secondary regulation in a DC microgrid feeding a tightly voltage-regulated boost converter that acts as a constant power load (CPL). CPLs are characterized as loads that behave like negative impedances, which introduce stability challenges to the microgrid. To adapt this nonlinear control technique to this specific case, the circulating current problem, a key limitation of the primary control, is first addressed by suggesting a sliding mode controller (SMC). This approach effectively achieves voltage regulation and ensures balanced power distribution.

The system model for each DC–DC converter in the microgrid, including the CPL, was transformed to adapt to the sliding mode controller design. This method successfully eliminates the need for passive loads with CPLs, which are commonly used in previous works. In the second step, voltage deviation, a primary control issue, is addressed through a secondary control strategy using H-infinity control. This approach combines inner SMC loops, droop control, and the CPL of each DC–DC buck converter, with model linearization achieved through the Jacobian technique.

The effectiveness of the proposed controller has been validated through simulations and experiments, involving five case studies. These tests included secondary control activation, responses to CPL fluctuations, input voltage variations, reference value changes, and sudden plug-and-play scenarios—typical situations in DC or AC microgrids. As a result, the system demonstrated effective performance in tracking, power sharing, voltage restoration, and disturbance rejection. The experimental results also validated these capabilities of the proposed controller. As a future perspective, the authors plan to extend the proposed method to handle diverse load types including motor drives. Furthermore, integrating hybrid AC–DC MGs represents a promising avenue for further investigation. These efforts aim to enhance the method's robustness and scalability in complex and diverse MG configurations.

## Data availability

The datasets used and/or analyzed during the current study are available from the corresponding author on reasonable request.

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## Author contributions

K.L., J.M.G., M.B., A.C., B.K., A.C. and M.Z.Y. wrote the main manuscript text. K.L., J.M.G., M.B., A.C., B.K., A.C. and M.Z.Y. prepared figures. All authors reviewed the manuscript.

## Declarations

### Competing interests

The authors declare no competing interests.

### Additional information

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