



OPEN Energy-efficient neuromorphic system using novel tunnel FET based LIF neuron design for adaptable threshold logic and image analysis applications

Faisal Bashir¹✉, Furqan Zahoor¹, Ali Alzahrani¹ & Haider Abbas²

In this study, a novel tunable dopingless band-to-band tunneling mechanism based Leaky Integrate and Fire (LIF) neuron is proposed with a notable improvement in integration density and energy consumption. The forward transfer characteristics of Tunnel FET with sharp sub-threshold swing have been utilised to simulate the neural activity. The simulations performed using Atlas 2D software confirm that the proposed TFET can effectively replicate the spiking behavior of a biological neuron, eliminating the need for additional circuitry, in addition to offering tunable features. The proposed LIF neuron demonstrates significantly lower energy consumption, operating at just 144 aJ per spike. This energy efficiency is at least 10^6 times lower than the single MOSFET-based neuron and 10^3 times lower than TFET-based 1-transistor neurons reported in prior literature. This remarkable improvement is attributed to the underlying mechanism, which leverages tunneling and material engineering techniques. The proposed neuron has also been successfully investigated for the implementation of adaptable threshold logic functions (NOT, OR and AND). This offers a solution for the design of highly scalable and energy efficient threshold logic circuits for future neuromorphic computing systems. Lastly, we implement a multilayer SNN that confirms the image recognition ability of the proposed neuron with 92.1% accuracy.

Neuromorphic computing uses the human brain as a model to develop energy-efficient information processing technology that can do extremely complex jobs. By emulating the brain's distributed topology, systems constructed using common electronics can enhance speed and energy efficiency. Significant hardware technical advancements are needed to scale up such systems and improve their speed, energy consumption, and performance by several orders of magnitude. Artificial neural network (ANN) has emerged as the potential choice to minimize the effect of Von Neumann bottlenecks paradigms in computing systems¹⁻⁶. Inspired by high-parallelism biological brain networks, the bio-inspired computing architecture has emerged as a practical way to manage challenging artificial intelligence tasks without requiring frequent data shuttles in the von Neumann design. For intelligence tasks, bio-mimetic spiking neural networks (SNNs) exhibit a great deal of promise for excellent energy efficiency⁷. The third generation of ANNs, known as SNNs, were first created with inspiration from the brain⁸. The research community has been drawn to the efficiency of computers in resolving categorization and recognition issues as well as the laws guiding how the human brain functions. In order to create a neuromorphic computing system—a viable choice for a quicker and more energy-efficient computer system—researchers are working to create hardware with computational capabilities like to those of the human brain. The neuronal cell is a key component of a neural network and is necessary for its correct operation. The leaky-integrate-and-fire (LIF) model⁹⁻¹³ is an effective method of formalizing a neuron's dynamics and closely resembles the behavior of biological neurons. Using the outputs of other neurons, the synapses assist in activating a neuron. Through the use of ion channels, the neurotransmitter chemical compounds transfer the stored charged carrier in the potential well of the neuron cell. Ion channels are activated to produce an action potential once the accumulated charge carriers in the cell potential well reach their critical value. This causes an axon to spike and the neuron to return to its resting posture.

¹Department of Computer Engineering, College of Computer Science and Information Technology, King Faisal University, Al-Ahsa 31982, Kingdom of Saudi Arabia. ²Department of Nanotechnology and Advanced Materials Engineering, Sejong University, Seoul 143-747, Republic of Korea. ✉email: famed@kfu.edu.sa

A major problem for large-scale integrated neuromorphic computing systems is that artificial neurons are still primarily CMOS-implemented and still have high energy consumption and high hardware costs. In contrast, SNN has used a variety of emerging memory devices, to develop the artificial synapses for significantly improved energy and area efficiency^{14,15}. Compact and energy-efficient neurons will always play a part in large-scale neuromorphic computing. Consequently, a great deal of research has been conducted to design and implement such devices. In this regard, two terminal structures include NIPIN diodes¹⁶ and biristors¹⁷. However, since these devices lack a control terminal, neuron inhibition is not possible. Field effect transistor (FET) based neurons have been described in the literature as a solution to these issues. Utilizing innovative beyond-CMOS devices is one potential remedy^{18,19}. Tunnel FET (TFET), has emerged as a promising promising energy-efficient device having steep subthreshold swing which is beneficial for low-power neuromorphic computing applications^{20–24}. A significant obstacle that TFETs must overcome is their low ON current value, which results from the inefficiency of their ambipolar current, doping related issues and band-to-band tunneling (BTBT) functioning. The use of strain, high-k gate insulators, low bandgap materials, and heterostructures fully addresses these issues^{25–27}. Based on literature, FET based neurons are broadly classified as: (1) impact ionization based devices and (2) tunneling based devices. Partially depleted silicon on insulator (PDSOI)⁹ and 1-T neurons²⁸ are examples of impact ionization-based devices. However, because of their slow body charging behaviour, these devices are energy inefficient and behave sluggishly²⁹. It should be noted that impact ionization is a high current process, and that the creation of electron-hole pairs (EHPs) uses a very small portion of the drain current (0.1%), leading to energy-inefficient devices. Additionally, one of the biggest problems with impact ionization-based devices is their hot carrier dependability issue³⁰. However, tunneling-based devices^{31,32} use less energy because the charge carriers in these devices integrate into the body to raise the body potential by tunneling through drain-channel junctions. These devices use more external circuitry, which increases the circuit's complexity and energy consumption even while they use less energy when used alone.

Recently, spiking neurons have been implemented in hardware using heterojunction TFETs based on direct bandgap III-V materials^{33,34}. The steep subthreshold swing of TFETs can lower the supply voltage for neurons, but they have a high-static-energy-consumption problem because of the high OFF-state leakage current of III-V heterojunction TFETs. This problem can be even more severe for event-driven brain-inspired neuromorphic systems. Since the circuit topology remains the same as with a traditional MOSFET-based neuron, the hardware cost for implementing a III-V-TFET-based neuron is still significant.

In this work, a spiking neuron based on novel TFET is proposed, achieving higher energy efficiency, tunability and lower hardware cost than CMOS implementation. The proposed device consists of dual semiconductor material (InGaAs and Silicon), Floating gates and does not require the conventional doping for the realization of Source and Drain regions, as these regions are created using metal work-function engineering: a charge plasma concept (CP)³⁵. Due to the utilization of CP, material and oxide engineering, the proposed device is named the Dopingless Material-Engineered Floating Gate Tunnel FET (DI-FG-ME-TFET). To obtain the neuron LIF behavior, the TFET transfer characteristics have been utilised. The main reason for employing DI-ME-FG-TFET structure for LIF neuron design is its lower supply voltage, steep sub-threshold swing (SS), desired threshold voltage and improved driving capability.

The rest of the manuscript is arranged as follows: The description of the device parameters and schematics is presented in “Structural description and simulation parameters”. The analysis of the results is detailed in “Results”. Lastly, “Conclusion” describes the conclusion of the paper.

Structural description and simulation parameters

The proposed doping-less floating gate-based Indium Gallium Arsenide (InGaAs) and Silicon (Si) double gate tunnel FET (DI-FG-ME TFET) is shown in Fig. 1a. The proposed device is constructed using ternary compound semiconductor material (InGaAs) and elemental semiconductor (Silicon). The different dimensional parameters of the proposed TFET are summarized in Table 1. The Source and Drain of the proposed TFET have been realized using the charge plasma concept^{36,37}. Atlas TCAD³⁸ has been used to simulate LIF neuron and adaptable threshold logic using the FG-InGaAs/Si TFET. The various models incorporated in the atlas device simulator are drift diffusion, Lombardi, fermi, conmob, FLDMOB, and PRPMOB are utilized in the simulations. The PRPMOB and FLDMOB mobility models account for the perpendicular and parallel components of the electric field. Additionally, the Shockley–Read–Hall (SRH) recombination model is employed. The non-local band-to-band tunneling (BTBT) model is also used to capture the BTBT phenomenon in TFETs.

Results

Device and neuron characteristics

The energy band diagram of the proposed TFET under different bias conditions is shown in Fig. 1b. The three different energy band plots represent: (1) the equilibrium state ($V_{DS}=0.5$ and $V_{GS}=0$) (2) the ON state ($V_{DS}=0.5$ and $V_{GS}=0.5$) and (3) operation with Gate 1 and Gate 2 terminals ($V_{DS}=0.5$ and $V_{GS1}=0.5$ $V_{GS2} = -0.4$ V) controlled separately. The energy band diagrams clearly show that the channel barrier is controlled by the gate voltage, while the floating gates (FGs) regulate the modulation of the bands between the source and the channel to enhance tunneling. The two gates in the proposed double gate TFET can used separately to control the TFET characteristics and realize the Excitatory and Inhibitory functions of the neuron. The dc transfer characteristics of the proposed TFET shows the characteristics for the two gates (G1,G2) connected together (normal operation) and G1, G2 connected separately (for controlling). It is clear from the energy band diagram that as long as G1 and G2 are connected together, the device can be operated normally with sub-threshold swing of 1.6 mV/dec, $I_{OFF}=2\times 10^{-14}$ A, and $I_{ON}=18\times 10^{-6}$ A as shown in Fig. 1d, however when the G2 is connected to -0.5 V supply the device remains in the OFF state as can be seen from the Fig. 1b.

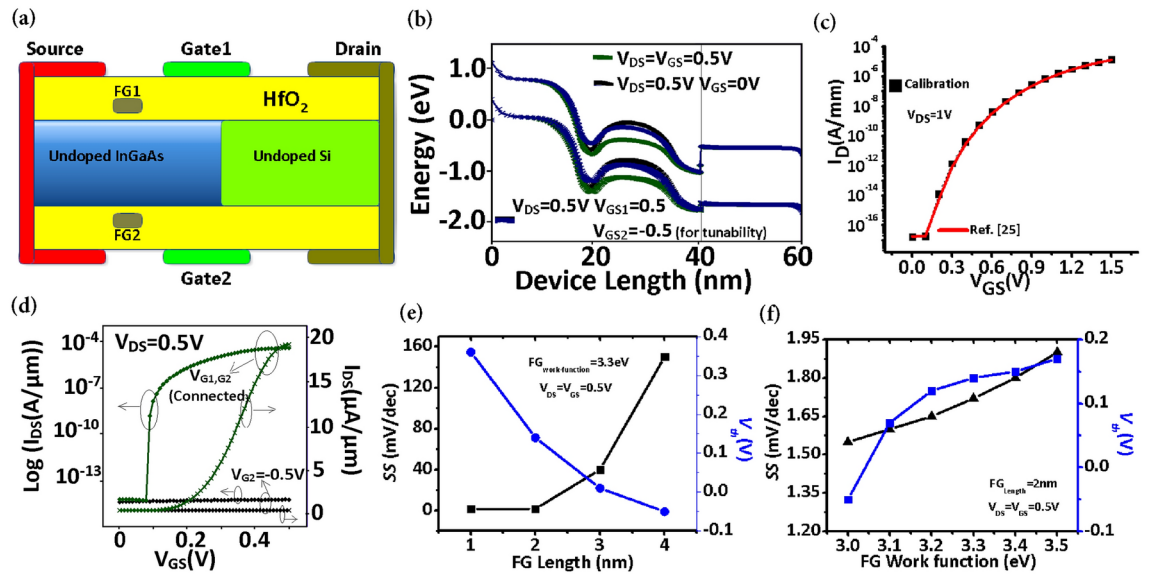


Fig. 1. DI-FG-ME-TFET (a) proposed device structure, (b) energy band diagram (ON, OFF state and with gate2(G2) connected to -0.5 V), (c) calibrated transfer characteristics, (d) proposed devices transfer characteristics, (e) impact of floating gate (FG) length, (f) impact of floating gate (FG) workfunction.

S. no.	Parameter	Specifications
1	Gate length (L_G)	20 nm
2	S/D length 2	18 nm
3	Floating gate length	2 nm
4	InGaAs and silicon thickness	8 nm
5	HfO_2 thickness	2 nm
6	Source work-function	5.9 eV
7	Drain work-function	3.9 eV
8	Gate work-function	4.9 eV
9	Floating gates work-function	3.4 eV

Table 1. Structural description of the proposed DI-FG-ME-TFET.

The two gates in the proposed double-gate TFET can be used independently to control the TFET characteristics and implement the excitatory and inhibitory functions of a neuron. The DC transfer characteristics of the proposed TFET illustrate its behavior in two configurations: when both gates (G1, G2) are connected together (normal operation) and when they are controlled separately shown in Fig. 1d. The energy band diagram clearly shows that when G1 and G2 are connected together, the device operates normally with a sub-threshold swing, threshold voltage, leakage current and ON current of $SS=1.6\text{mV/dec}$, $V_{th} = 0.14\text{ V}$, $I_{OFF}=2 \times 10^{-14}\text{ A}$, and $I_{ON} = 18 \times 10^{-6}\text{ A}$ respectively. However, when G1 is varied from 0 to 0.5 V and G2 is connected to a -0.5V supply, the device remains in the OFF state, as shown in energy band diagram of Fig. 1b. To validate the accuracy and practicality of our simulations, we calibrated the simulation model using an earlier work on TFET^{36,39,40} for silicon materials, as depicted in Fig. 1c. Figure 1e shows the impact of the FGs length and work-function on the performance of the proposed device. It has been observed that for FG length up to 2nm, the device has very sharp SS and desirable V_{th} , both of which are important parameters for realizing the energy efficient neuron. However, as the FG length increase beyond 2nm, the SS and V_{th} both gets degrade causing the device to lose its desired characteristics. This degradation occurs because a longer FG induces more electrons in the channel, leading to increased leakage and a deterioration of SS. Thus floating gates in the proposed device plays a crucial role for controlling the sub-threshold swing, threshold voltage, and ON current, which are essential parameters for design a energy efficient LIF neuron.

The work function of the floating gate (FG) plays a crucial role in determining the characteristics of the proposed device as shown in Fig. 1f. It has been observed that a lower work function is beneficial for achieving optimal device performance in terms of subthreshold swing (SS) and on-current (I_{ON}). However, when the work function of the FG falls below 3.1 eV, the device loses control, and its characteristics become undesirable for both device operation and neuron functionality.

Figure 2 shows the actual neuron, proposed neuron circuit, input current and LIF action of the neuron. The transfer characteristics of the DI-FG-ME-TFET are illustrated in Fig. 1c. The device's low subthreshold swing

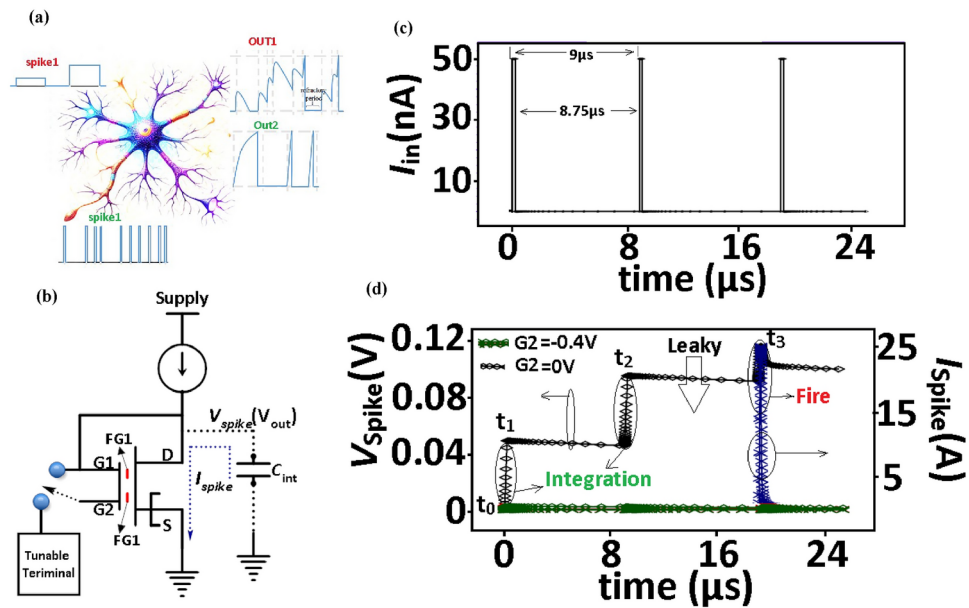


Fig. 2. Neuron (a) biological, (b) circuit design, (c) input current to neuron circuit, (d) voltage and current spiking characteristics.

(1.7 mV/decade) and a gate length of 20nm makes it highly suitable for implementing energy efficient and compact design of spiking neural networks (SNNs).

The operation of the neuron circuit for LIF action can be explained using the circuit configuration depicted in Fig. 2. The current I_{in} from the presynaptic neuron serves as the input to the TFET, which is connected between the drain and gate. Initially, the device is presumed to be in the equilibrium t_0 . When I_{in} is applied, charge integration occurs, causing the voltage to gradually build up (at time t_1 , t_2 and t_3), . The amount of voltage accumulated per step is expressed as:

$$V_{step}(t) = \frac{I_{in} \times T_{on}}{C_{int}} \quad (1)$$

Here, T_{ON} represents the ON time of the input current, and C_{int} is the internal drain capacitance of the device. An input current of 50 nA, with an ON time of 0.25 μs and a frequency of 100 KHz, is applied. As a result, a voltage of 0.05 V is generated per pulse. When this voltage surpasses the spiking voltage (V_{spike} of the device at time t_3 , a current spike (I_{spike}) is observed, as illustrated in Fig. 2d. Once the device switches to the ON state, all accumulated charges discharge to the ground, resetting the device to its initial OFF state t_0 . No external circuitry is required for this process. Due to the sharp transition in the device's transfer characteristics, the resulting current manifests as a sharp spike. Besides this, if the G2 ($V_{G2}=-0.5V$) is connected separately with the tunable terminal, then both inhibitory and excitatory functions can be realized using the proposed neuron circuit as shown in Fig. 2c.

When the Gates (G1,G2) and Drain terminals are shorted, the transistor operates in a diode-connected configuration. This configuration ensures that the voltage across the Gate and Source (V_{GS}) is equal to the voltage across the drain and source (V_{DS}). As a result, the transistor is biased in such a way that it remains in saturation, creating a nonlinear relationship between the input current and the output voltage. This behavior is critical for the proper functioning of the LIF neuron. The transistor in this configuration acts as a voltage-controlled switch. When V_{GS} exceeds V_{th} the transistor allows current to flow, triggering the discharge of the capacitor (C_{int}). The steep transition from OFF to ON states ensures that the spike generation is sharp and well-defined, which is essential for accurate neuromorphic computation. The double gate (G1,G2) configuration of the proposed device provides additional feature tunability for the neuron. If the gate (G1) is connected to drain terminal and gate (G2) to tunable terminal (i.e -0.5V supply), the neuron circuit remains in the inhibition mode.

Figure 3a shows the device profile, position of energy band diagram and tunneling rate of the proposed neuron for different time instants. At the time instant t_0 , the neuron is in an equilibrium state where the energy barriers in the channel are elevated, preventing the tunneling process as shown in the Fig. 3a. However, at the subsequent time instants t_1 and t_2 , the integration process occurs (limited tunneling (Fig. 3b, c)), causing the output voltage to gradually increase, reaching 0.1 V, as shown in Fig. 2d. Finally, at t_3 , the output voltage attains the spiking threshold of 0.12 V, resulting in the generation of a spike, where energy band is lowered and the tunneling rate is high as shown in Fig. 3d. A current spike of 25 nA is detected once the accumulated voltage surpasses 0.12 V. The energy consumed per spike by the neuron is determined using the following relationship:

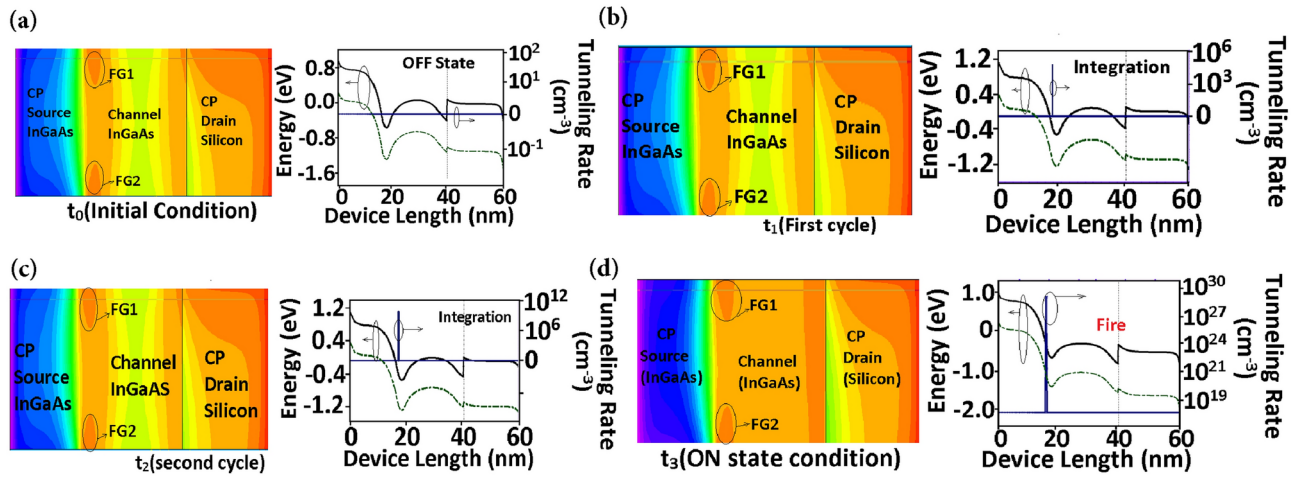


Fig. 3. Electron CP device profile with tunneling rate and respective energy band diagrams of DI-FG-ME-TFET (a) t_0 without input, (b) t_1 with first pulse, (c) t_2 with second pulse, (d) t_3 with third pulse.

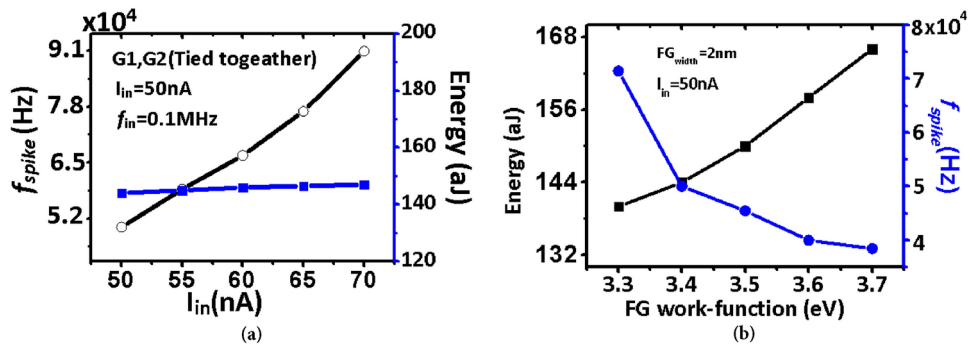


Fig. 4. (a) Spiking frequency and spiking energy versus input current. (b) Spiking frequency and spiking energy versus floating gate work-function.

$$E_{spike} = V_{spike} \times I_{spike} \times t_{width-spike} \tag{2}$$

As shown in Fig. 2d, the device’s threshold voltage or spiking voltage (V_{spike}) is 0.12 V, the current spike magnitude (I_{spike}) is 25 nA, and the spike duration ($t_{width-spike}$) is 0.5 ns. Consequently, the energy usage of the DI-FG-ME-TFET neuron is calculated to be approximately 144 aJ per spike.

Figure 4a illustrates the relationship between energy consumption per spike (E_{Spike}), spiking frequency (f_{Spike}), and input current (I_{in}). It is evident that the energy per spike remains nearly constant regardless of the input current magnitude. However, the spiking frequency increases linearly with the input current. This occurs because a higher input current reduces the time required to reach the spiking voltage, thereby increasing the spiking frequency. This behavior is a desirable trait for neuronal functionality and can be leveraged to implement various Boolean functions, as discussed in the next section. A slight non-linearity in the characteristics is attributed to the neuron’s leaky behavior, which causes a minor deviation.

Figure 4b shows the impact of workfunction of FGs on the neuron characteristic parameters like E_{Spike} , and f_{Spike} . It has been observed as the workfunction increases, the electrons induced by FGs are reduced, which decreases the tunneling width and thereby decreases driving capability of the device. Due to low driving capability f_{Spike} will increase, as it will take more time for the spike to occur, however energy per spike remains more or less constant.

A comprehensive comparison between the proposed neuron and state-of-the-art LIF neurons is presented in Table 2. As demonstrated in the table, the proposed TFET-based neuron achieves low energy consumption without requiring any external circuitry. This makes it an energy-efficient and straightforward solution for implementing LIF neurons.

Threshold logic design

To design a Boolean logic functions using neural networks, Logic Gates (LGs) are employed⁴⁷. By processing binary inputs through a predefined hard-limiting activation function, the LG generates the binary output $P(V)$ as follows:

Ref	Device type	L_G	E_{spike}	EC	ToC	V_{spike} (V)	f_{spike}
2	GaSb/Si V-DGTFET	50 nm	0.748 aJ	Yes	OC	0.2	534 GHz
9	SOI-MOSFET	32 nm	35 pJ	Yes	OC	2.8	1 MHz
12	JL-FET	20 nm	1.4 pJ	Yes	OC	0.4	1 MHz
13	$In_{0.95}Ga_{0.05}As$ MOSFET	1000 nm	7.1 pJ	No	OC	1.06	0.26 MHz
16	Si nipin diode	10 nm	0.02 fJ	Yes	—	0.6	1 MHz
17	Biristor neuron	20 nm	5.6 pJ	No	—	2.5	1.5 kHz
28	MOSFET	800 nm	45 pJ	No	OC	3	400 Hz
31	SiGe TFET	50 nm	210 fJ	No	TF	0.9	50 Hz
41	SB-MOSFET	180 nm	4 pJ	No	OC	4.5	50 Hz
42	SiGe MOSFET	400 nm	3.8 pJ	No	OC	2.5	50 Hz
43	Ge-MOSFET	800 nm	8 pJ	No	OC	1.8	70 Hz
44	Positive feedback FET	1000 nm	8.83 pJ	Yes	TF	1.4	1 MHz
45	BTBT Si neuron	40 nm	2.74 fJ	Yes	OC	0.2	150 kHz
46	Si-TFET	50 nm	750 fJ	No	TF	1.2	MHz
This work	DI-FG-ME-TFET	20 nm	144 aJ	No	TF	0.12	0.1 MHz

Table 2. Comparison table of the state-of-the-art LIF works. EC external circuit, ToC type of characteristics.

$$P(V) = f \left(\sum_{i=1}^K [w_i V_i] + w_0 I_{BIAS} \right) \quad (3)$$

Where V_i is the neuron input, w_i is weight to assigned to V_i , w_0 is weight assigned to input bias current, K is number of synaptic inputs, f is a hard-limiting activation function

Figure 5 shows the study conducted on the threshold logic gates design based on proposed TFET based neuron to achieve basic Boolean functions, aiming to validate its practical applicability. As illustrated in Fig. 5a, the NOT function is implemented by applying inputs I_1 and I_{BIAS} , where I_1 and I_{BIAS} have same magnitude but opposite polarity.

By giving the input current a weight w_1 of -1, the negative sign has been corrected. Since $I_{BIAS} + I_1 = 0$ when I_1 is applied, there is no spike and the net current to drain (I_{in}) is zero. On the other hand, a current spike is seen when $I_1 = 0$ and $I_{BIAS} = I_1$. This is shown in Fig. 5a.

As illustrated in Fig. 5b, the AND function is implemented by applying inputs I_1 and I_2 in addition to I_{BIAS} , where $I_{BIAS} = -50$ nA. The input has been set to 0 nA for logic 0 and 50 nA for logic 1 for the investigation. There is no charge accumulation when none or either of the inputs are applied, as a result no spike is observed. As seen in Fig. 5b, a current spike occurs when both of the inputs is at logic 1. The charge accumulation take place only when both I_1 and I_2 are at logic 1.

Figure 5c illustrated the OR function is implemented by applying inputs I_1 and I_2 in addition to I_{BIAS} , where $I_{BIAS} = 0$ nA. There is no charge accumulation and, as a result, no spike when both inputs are at logic 0. As seen in Fig. 5b, a current spike occurs when any of the inputs is at logic 1. However, as shown in Fig. 4, the linear relationship between the spiking frequency and the input current magnitude causes the spiking frequency to double when both inputs are at logic 1. The values of I_{BIAS} , w_1 and w_2 for implementing various logic functions are presented in Table 3.

Image identification

Lastly, we evaluate the performance of the TFET based design for AI-based-data analysis using the simulation approach wherein the SNNs is employed for identification of the MNIST dataset images. The electrical characteristics of the device, such as the threshold voltage, OFF-state resistance, reset voltage, and capacitance, are simulated and analyzed using Atlas TCAD. These parameters are validated to confirm the proposed neuron's capability for effective pattern recognition. An analogous model of the TFET neuron is created using these features on a Python-based platform. The three-layer SNN was constructed with 784 (28×28) neurons in the input layer, 100 neurons in the hidden layer, and 10 neurons in the output layer, as seen in Figure 6(a). The SNNs makes use of backpropagation method for calculating and updating the synaptic weight change in the network. The network is made to identify large set of 60,000 images to achieve higher recognition accuracy for the handwritten digits of the MNIST data set. Fig. 6(b) shows the recognition accuracy of the SNN, as is evident the maximum recognition accuracy for the handwritten digits reaches a maximum value of 92.1% for training cycle of 100 epochs which confirms the successful deployment for image identification tasks.

Conclusion

In this article, a novel structure of a dopingless floating gate material-engineered TFET (DI-FG-ME-TFET) is utilized to design a Leaky Integrate-and-Fire (LIF) neuron without the need for any external circuitry. The proposed neuron architecture employs a single transistor and consumes only 144 aJ per spike, which is six and three orders of magnitude lower than previously reported silicon-based MOSFET and TFET LIF neurons, respectively. The proposed LIF neuron demonstrates exceptional performance in terms of simplicity, scalability,

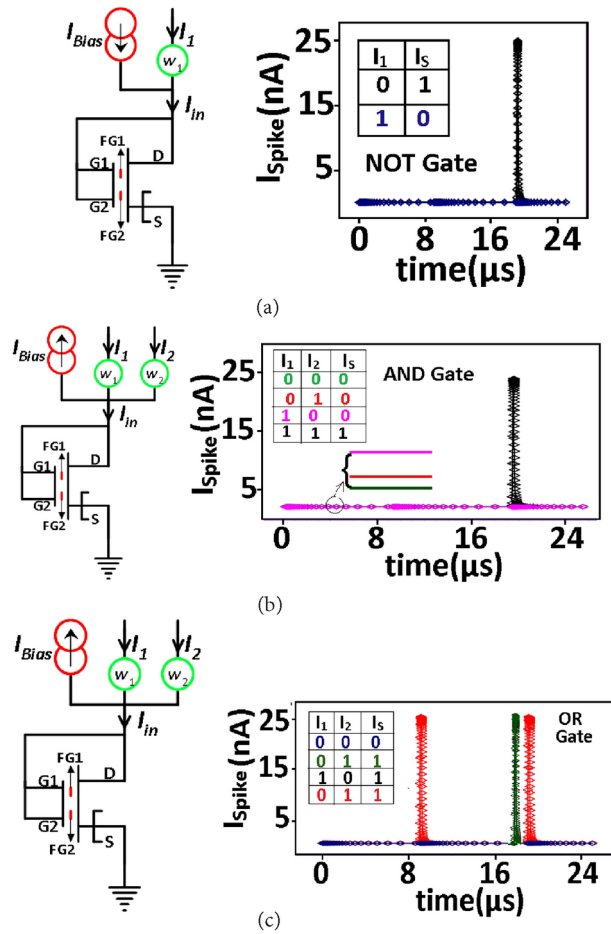


Fig. 5. Configuration for NOT, AND and OR (a) NOT gate, (b) AND gate, (c) OR gate.

Logical function	Biasing current (I_{Bias})	w_1	w_2
NOT operation	50 nA	-1	Not required
AND operation	-50 nA	1	1
OR operation	0	1	1

Table 3. Parameters of circuits for various logic functions.

adaptability, and energy efficiency. The DI-FG-ME-TFET exhibits a steep subthreshold swing (SS) and a reduced threshold voltage (V_{th}), which contribute to the design of an energy-efficient LIF neuron. To evaluate the applicability of the proposed neuron in logic design, threshold logic circuits were developed, and their functionality as linearly separable logic gates was confirmed. Additionally, a multilayer SNN was constructed, achieving a 92.1% accuracy in image recognition, thereby validating the neuron’s effectiveness. The proposed neuron holds significant potential for highly scalable logical designs in the field of neuromorphic computing. Furthermore, the dopingless nature of the device eliminates doping-related issues, offering additional advantages in design and performance.

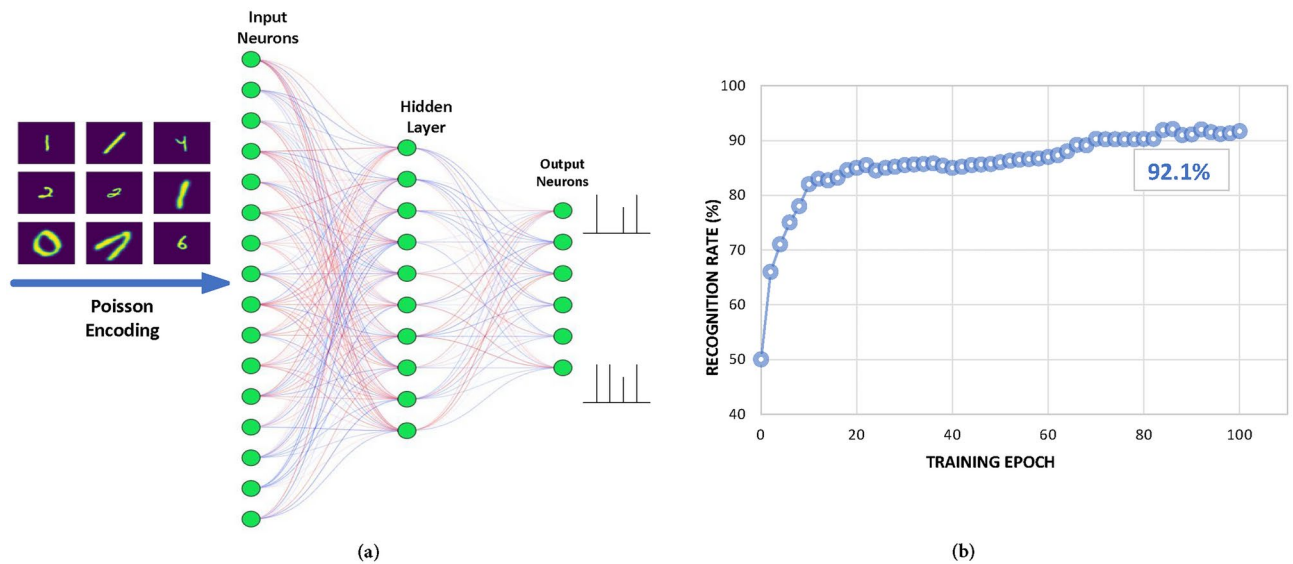


Fig. 6. (a) Schematics of the proposed SNN for image classification. (b) Accuracy graph with maximum accuracy of 91.21%.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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References

- Schwartz, J. H., Kandel, E. R., Jessell, T. M., Siegelbaum, S. A. & Hudspeth, A. *Principles of Neural Science* (Elsevier, 1991).
- Singh, S. et al. Emulation of neuro-mimetic dynamics via GASB/SI heterojunction v-DGTFET leaky-integrate-fire silicon neuron. *Micro Nanostruct.* **185**, 207709 (2024).
- Bashir, F. et al. Toward cognitive machines: evaluating single device based spiking neural networks for brain-inspired computing. *ACS Appl. Electron. Mater.* **7**, 4 (2025).
- Grollier, J. et al. Neuromorphic spintronics. *Nat. Electron.* **3**, 360–70 (2020).
- Upadhyay, N. K. et al. Emerging memory devices for neuromorphic computing. *Adv. Mater. Technol.* **4**, 1800589 (2019).
- Zahoor, F. et al. An overview of critical applications of resistive random access memory. *Nanoscale Adv.* (2024).
- Luo, J., Chen, C., Huang, Q. & Huang, R. A biomimetic tunnel FET-based spiking neuron for energy-efficient neuromorphic computing with reduced hardware cost. *IEEE Trans. Electron. Dev.* **69**, 882–886 (2021).
- Maass, W. Networks of spiking neurons: The third generation of neural network models. *Neural Netw.* **10**, 1659–1671 (1997).
- Dutta, S., Kumar, V., Shukla, A., Mohapatra, N. R. & Ganguly, U. Leaky integrate and fire neuron by charge-discharge dynamics in floating-body MOSFET. *Sci. Rep.* **7**, 8257 (2017).
- Chatterjee, D. & Kottantharayil, A. A CMOS compatible bulk Finfet-based ultra low energy leaky integrate and fire neuron for spiking neural networks. *IEEE Electron Dev. Lett.* **40**, 1301–1304 (2019).
- Singh, S. et al. Dopingless-TFET leaky-integrated-fire (LIF) neuron for high-speed energy efficient applications. *IEEE Trans. Nanotechnol.* **21**, 110–117 (2022).
- Kamal, N. & Singh, J. A highly scalable junctionless FET leaky integrate-and-fire neuron for spiking neural networks. *IEEE Trans. Electron Dev.* **68**, 1633–1638 (2021).
- Faizan, Mohd, Loan, Sajad A. & Alkhamash, Hend I. Highly scalable In_{0.95}Ga_{0.05}As based controllable leaky-integrate-fire neuron for high performance spiking neural network and applications. *Phys. Scr.* **100**, 025934 (2025).
- Zhang, X. et al. Fully memristive SNNs with temporal coding for fast and low-power edge computing. In *2020 IEEE International Electron Devices Meeting (IEDM)*, 29–6 (IEEE, 2020).
- Wan, W. et al. 33.1 a 74 TMACS/w CMOS-RRAM neurosynaptic core with dynamically reconfigurable dataflow and in-situ transposable weights for probabilistic graphical models. In *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*, 498–500 (IEEE, 2020).
- Das, B., Schulze, J. & Ganguly, U. Ultra-low energy LIF neuron using Si NIPIN diode for spiking neural networks. *IEEE Electron Dev. Lett.* **39**, 1832–1835 (2018).
- Han, J.-W. & Meyyappan, M. Leaky integrate-and-fire biristor neuron. *IEEE Electron Dev. Lett.* **39**, 1457–1460 (2018).
- Chen, C. et al. Bio-inspired neurons based on novel leaky-fetfet with ultra-low hardware cost and advanced functionality for all-ferroelectric neural network. In *2019 Symposium on VLSI Technology*, T136–T137 (IEEE, 2019).
- Luo, J. et al. Capacitor-less stochastic leaky-fetfet neuron of both excitatory and inhibitory connections for snn with reduced hardware cost. In *2019 IEEE International Electron Devices Meeting (IEDM)*, 6–4 (IEEE, 2019).
- Bokka, Jagadeesh Babu, D., & Jagannadham, B.V. Line-tunneling based GaP/Si heterostructure vertical gate-all-around tunnel FET for enhanced electrical performance. *Mater. Sci. Eng. B* **312**, 117875 (2025).
- Huang, Q. et al. Self-depleted t-gate Schottky barrier tunneling FET with low average subthreshold slope and high i on/i off by gate configuration and barrier modulation. In *2011 International Electron Devices Meeting*, 16–2 (IEEE, 2011).
- Zhao, Y., Huang, Q. & Huang, R. A novel tunnel FET design through hybrid modulation with optimized subthreshold characteristics and high drive capability. *Sci. China Inf. Sci.* **63**, 129402 (2020).

23. Pal, Arnab et al. An ultra energy-efficient hardware platform for neuromorphic computing enabled by 2D-TMD tunnel-FETs. *Nat. Commun.* **15**, 3392 (2024).
24. Cherik, Iman Chahardah, Mohammadi, Saeed, Hurley, Paul K., Ansari, Lida & Gity, Farzan. Investigating vertical charge plasma tunnel field effect transistors beyond semiclassical assumptions. *Sci. Rep.* **15**, 4682 (2025).
25. Ionescu, Adrian M. & Riel, Heike. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **479**, 329–337 (2011).
26. Saravanan, M. & Parthasarathy, Eswaran. A review of III-V tunnel field effect transistors for future ultra low power digital/analog applications. *Microelectron. J.* **114**, 105102 (2021).
27. Kanungo, Sayan, Ahmad, Gufran, Sahatiya, Parikshit, Mukhopadhyay, Arnab & Chattopadhyay, Sanatan. 2D materials-based nanoscale tunneling field effect transistors: Current developments and future prospects. *npj 2D Mater. Appl.* **6**, 83 (2022).
28. Han, J.-K. et al. Mimicry of excitatory and inhibitory artificial neuron with leaky integrate-and-fire function by a single Mosfet. *IEEE Electron Dev. Lett.* **41**, 208–211 (2019).
29. Wei, A., Sherony, M. J. & Antoniadis, D. A. Transient behavior of the kink effect in partially-depleted SOI Mosfet's. *IEEE Electron Dev. Lett.* **16**, 494–496 (1995).
30. Gopalakrishnan, K., Woo, R., Jungemann, C., Griffin, P. B. & Plummer, J. D. Impact ionization MOS (I-MOS)-part II: Experimental results. *IEEE Trans. Electron Dev.* **52**, 77–84 (2004).
31. Bashir, F., Zahoor, F. & Alzahrani, A. S. Utilizing forward characteristics of pocket doped SIGE tunnel FET for designing LIF neuron model. *Silicon* 1–8 (2024).
32. Bashir, F., Zahoor, F., Abbas, H., Alzahrani, A. & Hanif, M. Dielectrically modulated single Schottky barrier and electrostatically doped drain based FET for biosensing applications. *IEEE Access* (2024).
33. Rajasekharan, D., Dutta, T., Trivedi, A. R. & Chauhan, Y. S. Energy-efficient spiking neural networks based on tunnel FET. In *2016 3rd International Conference on Emerging Electronics (ICEE)*. 1–4 (IEEE, 2016).
34. Rajasekharan, D., Chauhan, S. S., Trivedi, A. R. & Chauhan, Y. S. Energy and area efficient tunnel FET-based spiking neural networks. In *2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)*. 59–61 (IEEE, 2018).
35. Rajasekharan, B. et al. Fabrication and characterization of the charge-plasma diode. *IEEE Electron Dev. Lett.* **31**, 528–530 (2010).
36. Kumar, M. J. & Janardhanan, S. Doping-less tunnel field effect transistor: Design and investigation. *IEEE Trans. Electron Dev.* **60**, 3285–3290 (2013).
37. Bashir, F. et al. A novel high performance nanoscaled dopingless lateral pnp transistor on silicon on insulator. In *Proceedings of the IMECS* (2014).
38. Atlas Device Simulation Software. (Silvaco International, 2019).
39. Boucart, K. & Ionescu, A. M. Double-gate tunnel FET with high k gate dielectric. *IEEE Trans. Electron Dev.* **54**, 1725–1733 (2007).
40. Bashir, F., Loan, S. A., Rafat, M., Alamoud, A. R. M. & Abbasi, S. A. A high performance gate engineered charge plasma based tunnel field effect transistor. *J. Comput. Electron.* **14**, 477–485 (2015).
41. Bashir, F., Zahoor, F., Alzahrani, A. S. & Khan, A. R. A single Schottky barrier Mosfet-based leaky integrate and fire neuron for neuromorphic computing. *IEEE Trans. Circuits Syst. II Exp. Briefs* **70**, 4018–4022 (2023).
42. Khanday, M. A., Khanday, F. A. & Bashir, F. Single SiGe transistor based energy-efficient leaky integrate-and-fire neuron for neuromorphic computing. *Neural Process. Lett.* **55**, 6997–7007 (2023).
43. Khanday, M. A., Bashir, F. & Khanday, F. A. Single germanium Mosfet-based low energy and controllable leaky integrate-and-fire neuron for spiking neural networks. *IEEE Trans. Electron Dev.* **69**, 4265–4270 (2022).
44. Kwon, M.-W. et al. Integrate-and-fire neuron circuit using positive feedback field effect transistor for low power operation. *J. Appl. Phys.* **124** (2018).
45. Chavan, T., Dutta, S., Mohapatra, N. R. & Ganguly, U. Band-to-band tunneling based ultra-energy-efficient silicon neuron. *IEEE Trans. Electron Dev.* **67**, 2614–2620 (2020).
46. Khanday, M. A., Khanday, F. A., Bashir, F. & Zahoor, F. Exploiting steep sub-threshold swing of tunnel FET for energy-efficient leaky integrate-and-fire neuron model. *IEEE Trans. Nanotechnol.* **22**, 430–435 (2023).
47. Han, J.-K., Lee, M.-W., Yu, J.-M. & Choi, Y.-K. A single transistor-based threshold switch for a bio-inspired reconfigurable threshold logic. *Adv. Electron. Mater.* **7**, 2100117 (2021).

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Author contributions

FB and FZ discussed the idea of the LIF implementation. FB performed the simulations and verified the concept with the help of HA. FB, FZ, HA and AZ drafted the manuscript and actively participated in the discussions during the preparation of the manuscript. All the authors contributed to the revision of the manuscript, and they approved it for publication.

Declarations

Competing interests

The authors declare no competing interests.

Additional information

Correspondence and requests for materials should be addressed to F.B.

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