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A Novel Three-Phase Switched Capacitor Multilevel Inverter for PV Applications

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Abstract

This article introduces a new, compact 3 - ∅, 5-level (line-to-line) switched-capacitor multilevel inverter (5L-SCMLI) design. This design can automatically balance its capacitor voltages and offers a way to increase its voltage gain. There is no extra magnetic circuit or DC-DC boost converter needed to accomplish a voltage gain of two in the proposed topology (PT). The PT is more efficient and cost-effective since it synthesizes 5-levels (line-to-line) using only five switches, two capacitors and one diode. A detailed comparison with current SCMLI structures shows the PT benefits. The extensive simulation and experimental studies have been conducted to validate the PT effectiveness and assess the efficacy of the proposed technique. The PT stands out as the most cost-effective design at only 54.59 USD with an efficiency 97.81%. This work aligns with SDG 7 (Affordable and Clean Energy) and SDG 9 (Industry, Innovation and Infrastructure) by proposing a cost-

effective, high-efficiency multilevel inverter that enhances energy conversion and supports sustainable power electronics systems.

Keywords: Cost function, Multilevel Inverter, Switched Capacitors, LS-PWM, Switch Count, total Voltage Stress, SDG 7, SDG 9.

I. Introduction

Renewable energy has emerged as the most promising alternative to fossil fuels amid their depletion. Nonetheless, although most renewable sources are DC, alternating current (AC) is necessary for domestic and industrial applications. Power electrical devices, such as inverters, are utilised to facilitate efficient DC-to-AC conversion, thereby bridging this gap[1]. Conventional two-level inverters are widely used but face significant drawbacks, including high switching losses and inferior harmonic performance. Multilevel inverters (MLIs) have attained considerable prominence in the power electronics domain owing to their benefits over traditional inverters, such as reduced $^{dv}/_{dt}$, enhanced power quality, and reduced total harmonic distortion (THD), minimizing voltage stress on power devices. Due to these advantages, MLIs are widely utilised in diverse applications, including flexible AC transmission systems (FACTS), active power filters, and renewable energy generation (REG) [2]. However, incorporating an inductor in a boost converter increases the system's size and complicates its control architecture. A feasible design for medium- and high-power applications is the SCMLI. It can boost voltage, reduce the number of devices, and naturally balance capacitor voltage without the need for extra sensors or controllers. Several five-level inverter configurations employing switched-capacitor (SC) technology have been presented in the literature, each offering distinct advantages and limitations. A dual-T-type 5-level SCMLI that uses a half bridge to twice the voltage. It deals with the impulse charging currents and uneven operation that are frequent in SCMLI [3]. Using only eight switches and two capacitors, this five-level common ground inverter efficiently boosts voltage twice. It minimises leakage current, balances capacitor voltages, and achieves high efficiency (~96.5%). [4]. A common ground type inverter that uses SC to boost voltage while cutting down the energy those capacitors need to store. Unlike older designs where capacitors had to handle peak output voltage, this one uses capacitors rated just for half that voltage. It balances voltage on its own, keeps voltage change rates low, and doesn't need sensors to operate [5]. It introduces an H-9 topology with nine switches for output voltage control. Uses virtual grounding to cut down leakage current and keeps the capacitor ripple balanced [6]. A new five-level inverter design focuses on a common ground design to minimise leakage current. The inverter uses just two SC, each rated for half the output voltage, which cuts down the size, cost, and complexity [7]. An improved five-level ANPC inverter, unlike the conventional version that utilises only half of the DC-link voltage, achieves doubled DC voltage utilisation by employing an SC charged to half of the input voltage [8]. A single-phase five-level SC boost inverter is proposed to achieve higher voltage gain compared to conventional impedance-source inverters. The SC configuration effectively doubles the boosting capability while ensuring self-balancing of capacitor voltages [9-11]. A novel dual-mode, transformerless five-level inverter with a common-ground architecture for PV grid-connected systems. The topology provides efficient voltage boosting and self-balancing, significantly reduces leakage current, and ensures stable power injection with simple control strategies, thereby improving reliability, power quality, and adaptability to input voltage variations [12-14]. A five-level inverter that

addresses the problem of current spikes by employing a soft-charging technique using a dedicated inductor–switch circuit. The topology enhances voltage gain and achieves improved utilisation of the dc-link voltage compared to conventional designs [15-17]. A single-phase five-level converter design using SCs. The key point is that it boosts voltage without the usual H-bridge for reversing polarity, which reduces switching losses and voltage stress on parts [18-19]. A new single-phase five-level SC boost inverter with improved voltage gain over traditional impedance-source inverters. It uses an SC structure that doubles the boost factor while keeping capacitor voltages balanced [20-21].

The main benefits of the suggested topology are as follows:

(i) Increasing boosting ability, i.e, 2X
(ii) Natural balancing of the capacitor voltage
(iii) Lower total standing voltage(TSV)
(iv) Lower cost
(v) Only half of the switches operate for any voltage level.
(vi) Low losses
(vii) Operate for a wide range of power factors

The remaining details of the section are as follows: Part II specifies the SCMLI design's concept and operation. In Section III, discuss the PT control techniques. The idea of power loss of the proposed **5L-SCMLI** is explained in detail in Section IV. Section V covered a comparison study to establish the effectiveness of the suggested topology. In part VI, explore the analysis of results. The last section, VII, provides a summary of the work.

II. Proposed 5L-SC-MLI Topology

(a) Proposed Three-Phase 5L-SC-MLI Topology

Figure 1(a) illustrates a three-phase 5L-SCMLI configuration that employs a single input source and comprises five switches, two capacitors, and two diodes. The PT generates five different voltage levels (line to line)as an output: $2V_{DC}$, $1V_{DC}$, 0, $-1V_{DC}$, and $-2V_{DC}$. The PT doesn't need any sensor or any other circuit to keep the capacitor voltage balanced. The capacitors naturally keep themselves balanced because they are connected to the input source in both series and parallel[18][19][26]. Table 1 shows the order in which the proposed topology operated for each state of the pole voltage v_{RO} for phase R (refer to Fig. 1(b). Voltage stress for different voltages is noted in Table 2.

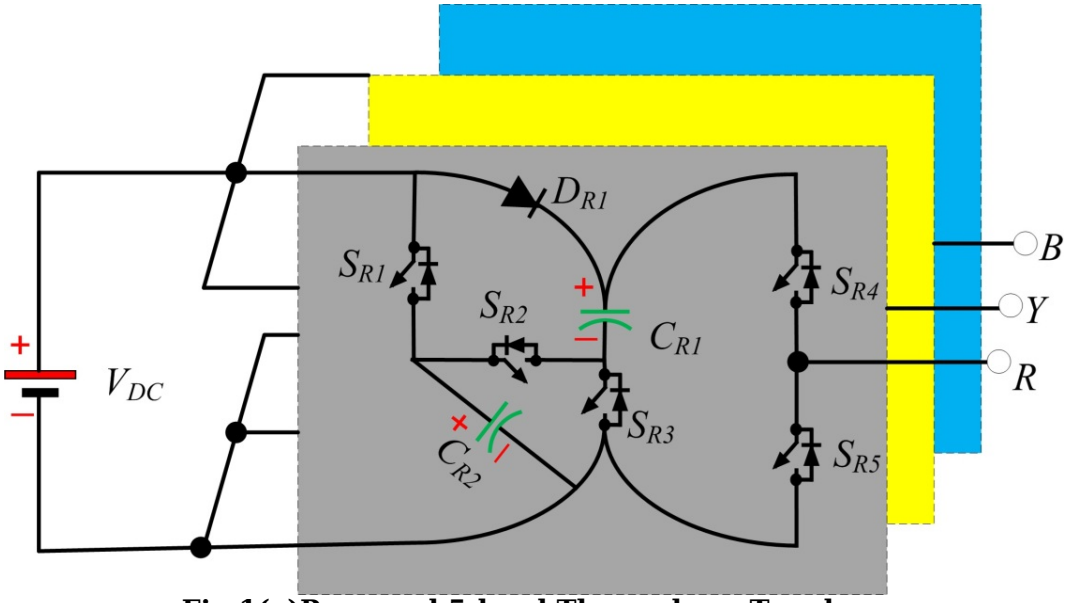


Fig.1(a)Proposed 5-level Three phase Topology

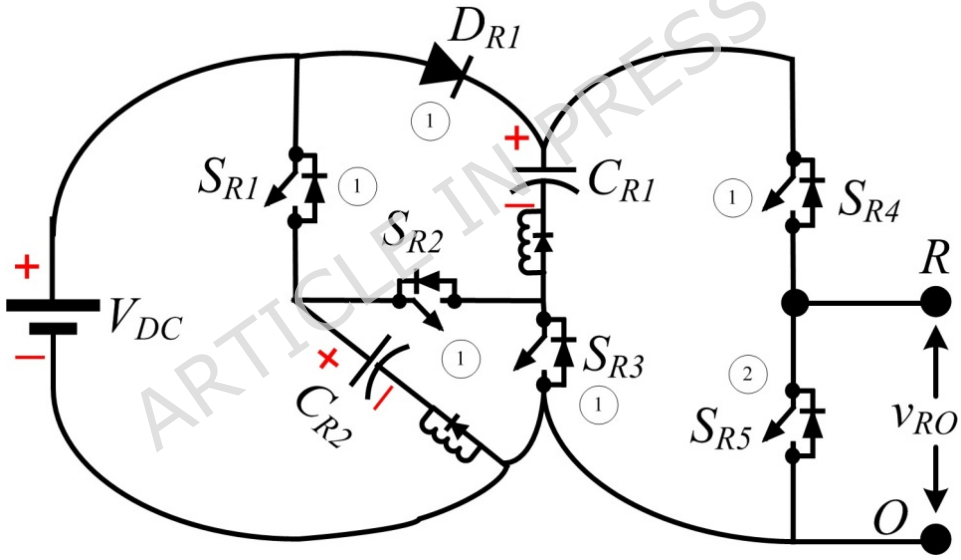


Fig.1 (b) R-Phase

Table 1:Switching patern of 5L-SC-MLI

Mode	S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{R5}	C_{R1}	C_{R2}	v_{RO}
β_1	1	-	-	-	1	-	C	0
β_2	-	-	1	1	-	C	-	$1V_{DC}$
β_3	-	1	-	1	-	D	D	$2V_{DC}$

A:state, "1": Active-state,"-": inactive state, C: charging,D: discharging, v_{RO}: output

Table 2:Voltage stress of 5L-SC-MLI

Mode	S_{R1}	S_{R2}	S_{R3}	S_{R4}	S_{R5}	v_{RO}
β_1	0	$1V_{DC}$	$1V_{DC}$	$1V_{DC}$	0	0
β_2	$1V_{DC}$	$1V_{DC}$	0	0	$1V_{DC}$	$1V_{DC}$
β_3	$1V_{DC}$	0	$1V_{DC}$	0	$2V_{DC}$	$2V_{DC}$

(b) Proposed Three Phase 5L-SC-MLI Topology operation

Mode -p_1: v_{RO}=0

v_{RO}=0 can be generated by activating S_{R5} simultaneously S_{R1} activated to charge C_{R2} to V_{dc}as illustrated in Fig. 2(a). The pole voltage and the capacitor charging path are indicated by blue and red dotted lines, respectively.

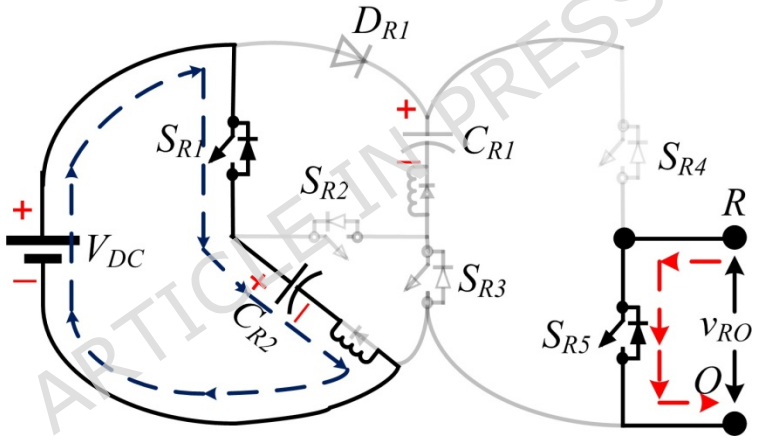


Fig.2(a) v_{RO} = 0

Mode -p_2: v_{RO}=V_{dc}

v_{RO}=V_{dc} can be generated by activating S_{R4} simultaneously S_{R3} activated to charge C_{R1} to V_{dc}as illustrated in Fig. 2(b).

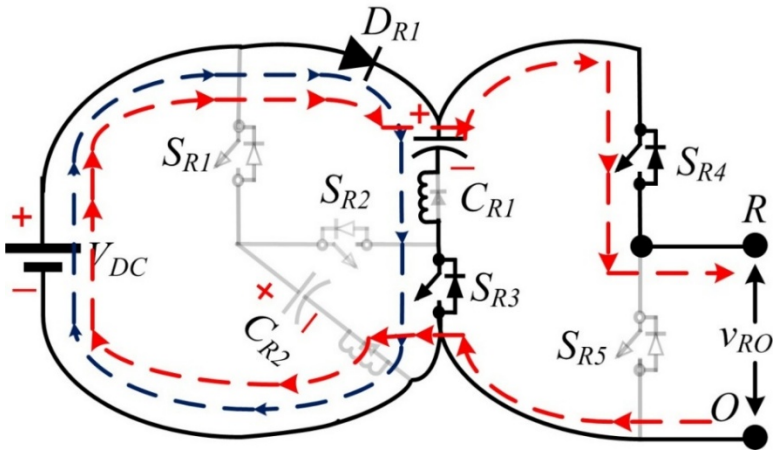


Fig.2 (b) $v_{RO} = V_{dc}$

Mode -p_2: $v_{RO}=2V_{dc}$

$v_{RO}=2V_{dc}$ can be generated by activating S_{R4} and S_{R2}, here both C_{R1} and C_{R2} discharges through load as illustrated in Fig. 2(c).

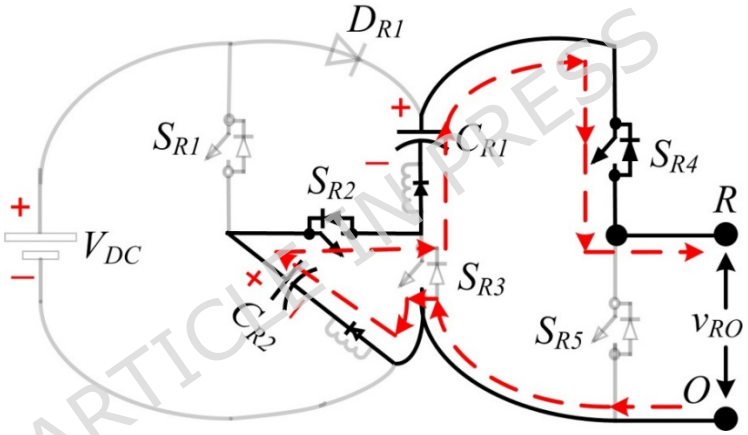


Fig.2 (c) $v_{RO} = 2V_{dc}$

Fig.2 (a) $v_{RO} = 0$ (b) $v_{RO} = V_{dc}$ (c) $v_{RO} = 2V_{dc}$

(c) Modular Structure of the PT

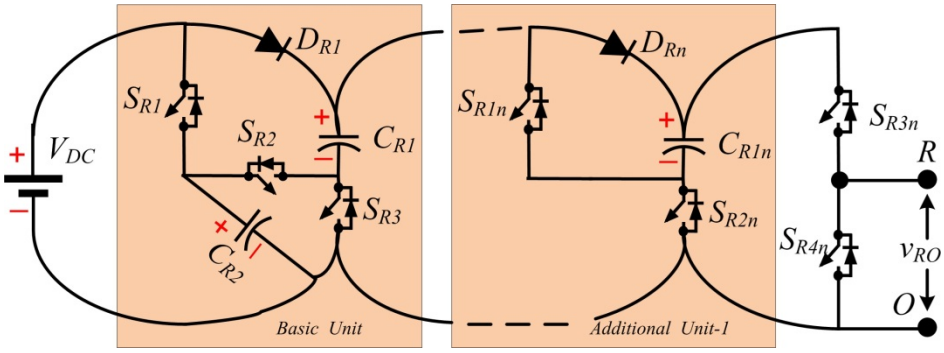


Fig 2(d) Modular structure of the PT

The modular structure for the PT are as shown in the Fig.2(d). For the basic unit it generates 3-level ploe voltage and 5-level line voltage. For "n" additional unit

pole voltage level = n + 3

$$\text{line voltage} = 7 + (n - 1)2$$
$$N_{sw} = 7 + (n - 1)2$$
$$N_c = 2 + n$$
$$N_d = 1 + n$$

III. Control Method

The PT has been designed to produce 3-Level output waveforms using a Level-Shifted pulse width modulation (LSPWM) technique to create gate pulses[18][22][26]. The control technique of the PT is depicted in Fig. 3. In this proposed PWM scheme, two carrier signals (A_c) $C_1(t)$ and $C_2(t)$, per phase at the desired switching frequency is compared with a modulating signal *(Ua)* for the R-Phase. The outputs of the comparators are added to get the aggregated signals ***a(t)***. This aggregated signal ***a(t)*** is mapped to the output level, as shown in Table 1, to obtain the switching pulse for Phase R. Similarly, the switching pulses for Phase -Y and Phase -B can be obtained.

$$M = \frac{U_r}{2A_c}$$

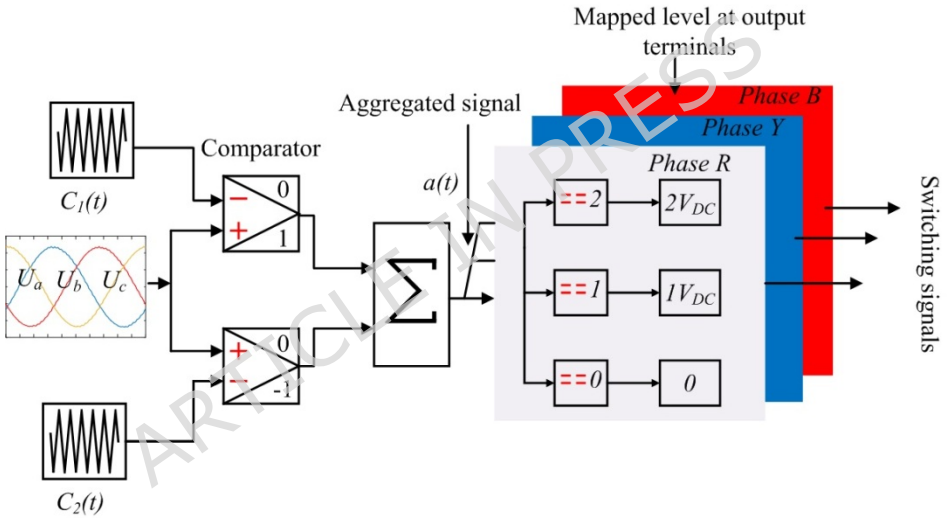


Fig.3 Modulation Scheme

Selection of capacitance

The typical relationship between voltage ripple (δV) across a capacitor and capacitance is inversely proportional. The values of t_1 ,t_2, can be calculated from Fig.4 as[26]

$$t_1 = \frac{\sin(\frac{1}{2})}{2\pi f} \quad (1)$$

$$t_2 = \frac{\pi - \sin(\frac{1}{2})}{2\pi f} \quad (2)$$

Capacitance values are derived from the maximum load current and the longest discharge period of the capacitor. Therefore, the maximum discharge of a capacitor can be represented as follows:

$$Q_{C,i} = \int_x^{t_y} I_m \sin(\omega t - \varnothing)\, dt \quad (3)$$

Hence, the optimum capacitance values can be determined by:

$$C_i > \frac{Q_{C,i}}{\delta V \times V_{dc}} \tag{4}$$

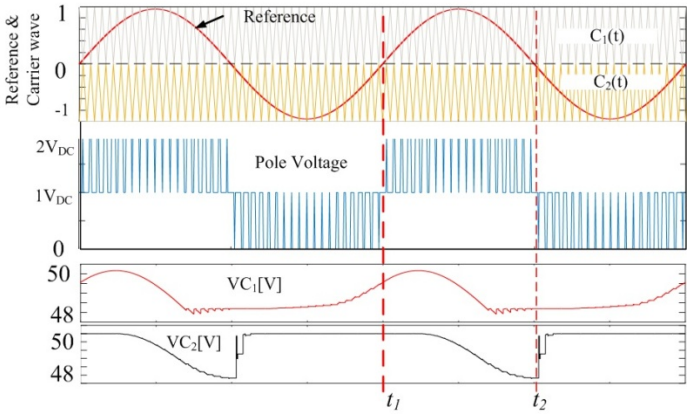
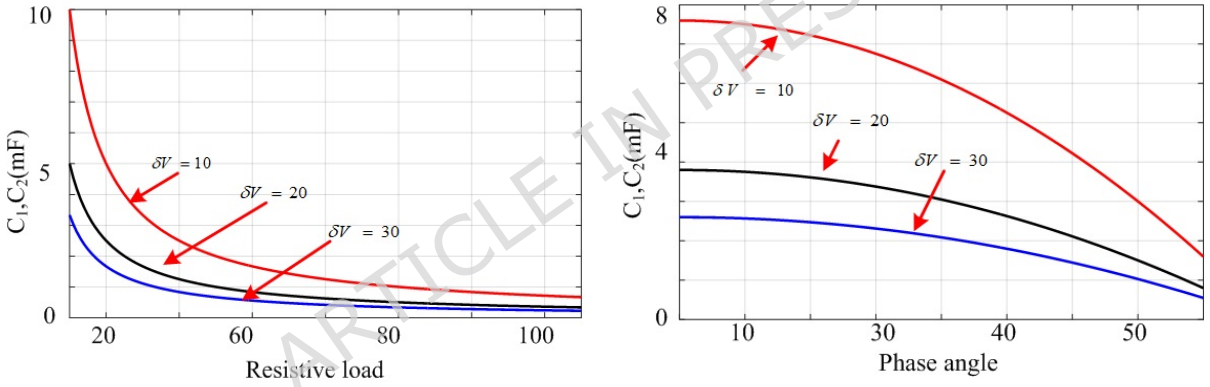


Fig. 4: Capacitor discharging Instant

Figure 5(a) and (b) show the least amount of capacitance C_1 and C_2 needed for resistive and inductive loads. It is noted that the capacitance required for a resistive load exceeds that for an inductive load when the voltage ripples are equal.



(a) (b)

Fig.5 (a) Resistive load, (b) Inductive load with different p.f

IV. Losses analysis of the proposed SCMLI

There are a total of three kinds of losses in an SCMLI: switching losses (P_S), capacitor losses (P_r), and conduction losses (P_C). Power switches and diodes are the sources of conduction and switching losses, whereas capacitors are the sources of ripple losses.

Conduction losses (P_C):

The on-state of semiconductor devices causes these losses [12].

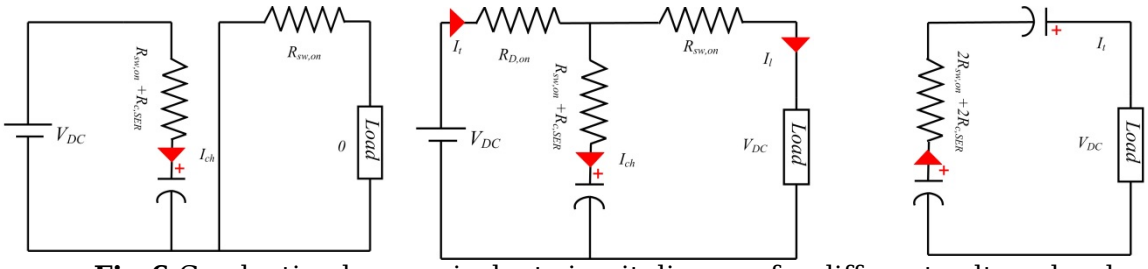


Fig.6 Conduction loss equivalent circuit diagram for different voltage levels

Fig. 6 demonstrates the way to express the instantaneous conduction losses for a resistive load as follows[27]:

$$P_{i,1} = I_{ch}^2(R_{sw,on} + R_{c,SER}) \quad (4)$$

$$P_{i,2} = I_{ch}^2(R_{sw,on} + R_{c,SER} + R_{D,on}) + I_l^2(R_{sw,on}) + I_t^2(R_{D,on}) \quad (5)$$

$$P_{i,2} = I_{ch}^2(R_{sw,on} + R_{c,SER} + R_{D,on}) + I_l^2(R_{sw,on}) \quad (6)$$

Where $I_t = I_l + I_{ch}$

$$P_{avg,1} = \frac{t_1}{T} P_{i,1} \quad (7)$$

$$P_{avg,2} = \frac{2(t_2 - t_1)}{T} P_{i,2} \quad (8)$$

The conduction losses can be calculated as

$$P_C = \sum_{i=1}^{3} P_{avg,i} \quad (9)$$

Switching losses (P_S):

These losses arise during the switching transitions of semiconductor devices. The corresponding loss can be expressed as[12][15]

$$P_S = \frac{1}{2} V_{off} f_{sw}(t) [t_{on} + t_{off}] \quad (10)$$

V_{off}: off-state voltage, t_{on} and t_{off} : on and off time durations of the switch.

Capacitor losses (P_{rip}):

The variation in capacitor voltage during the discharging process leads to ripple losses.

$$\delta V = \frac{1}{C_i} \int_{t_x}^{t_y} i_{C,i} dt \quad (11)$$

$$P_{rip} = \frac{f}{2} C_i \delta V^2 \quad (12)$$

δV: Ripple voltage, (t_x,t_y): discharging time span, $i_{C,i}$: Current flowing through the capacitor

The total power loss can be expressed as:

$$P_{total} = \sum P_C + \sum P_S + \sum P_{rip} \quad (13)$$

V. Comparative study

The comparative cost analysis of various SCMLI topologies underscores the economic feasibility of the proposed design. **Table 3** shows how much switches, diodes, capacitors, and driver circuits cost in different topologies. The number and kind of switches have a big effect on both the cost and the complexity of the circuit. For example, the designs in [10] and [11] use many more IXTP36N30T switches (six and twelve, respectively), making them much more expensive. The PT, on the other hand, uses six IXTP36N30T and two IRFP460PBF devices, which makes it work reliably at a lower cost. When it comes to diodes, topologies like [13] use up to four devices, which raises the cost. The PT, on the other hand, only needs two SBR40U300CTB diodes, which keeps efficiency high with little extra hardware. Capacitors are one of the most expensive parts, so they also affect the total cost. Most topologies, like [9], [10], [11], [13], and [PT], use two 300 V capacitors. However, the design [16] uses a single 500 V capacitor, which costs much more and raises the total cost significantly. The proposed inverter cuts the number of drivers needed from twelve to eight, making the setup easier and cheaper. When looking at the total costs, [PT] stands out as the most cost-effective design at only 54.59 USD. So, the PT successfully reduces the number of devices and drivers needed, saving money while maintaining high performance, reliability, and practicality for medium-power use. **Table 4** compares the current topologies and the PT with respect to several parameters, including total standing voltage (TSV), voltage gain, and the number of capacitors, diodes, and switches. In contrast to inverters [10], [11], and [18], which require more switches, the proposed inverter PT uses only five, reducing switching losses and the number of gate drivers needed. Unlike [13], which needs four diodes, this one utilises just two, and it matches most topologies with two capacitors, thus it naturally balances itself. PT achieves a voltage gain of 2, which is higher than [20][19], which delivers just 1.5, and 1 . Notably, the suggested design reduces device stress and expense by achieving a lower TSV of 7, which is lower than[3-4][10][6][13][17][15]. Hence, the proposed topology offers an optimal balance of lower TSV and reliable performance. **Table 5** presents a comparative evaluation of various inverter topologies referenced from studies [19]-[25] along with the PT. Each topology is assessed based on its merits, limitations, and key features, including the number of components, maximum capacitor voltage, *TSV*, voltage gain, and energy storage requirements. *TSV* is defined as the sum of the maximum voltage across switches and diodes of the inverter. This TSV is calculated as:

$$\mathrm{TSV} = \sum(\text{voltage stress across switch} + \mathrm{PIV}) \tag{14}$$

This $\mathrm{TSV_{pu}}$ is calculated as:

$$\mathrm{TSV_{pu}} = \sum \mathrm{TSV}/v_{max} \tag{15}$$

Table 3: Per phase Cost comparision of the PT

Part/ Description	Cost($)	[9]	[10]	[11]	[13]	[15]	[16]	[17]	[PT]

Switch	IXTP36N30T(TO220), 300V, 36A	2.65	3	6	12	3	5	1	10	3
	IRFP460PBF (TO247), 500V, 20A	4.11	4	3	-	4	4	7	2	2
Diode	SBR40U300CTB, 300V, 40A	2.11	3	1	2	4	-	1	-	1
	RURU5050(TO-218), 500V, 50V	3.1	-	1	-	-		-	-	-
Capacitor	871-B43415C3218A000, 2100 µF, 300V	13.83	2	2	2	2	2	1	2	2
	ALF70G222KP500, 2200µF, 500V	26.17	-	1	-	-	-	2		-
Drive	TLP250, 25kHz	2.18	7	9	12	7	9	8	12	5
Total cost($)@700W			75.7	128	89.8	75.7	77.9	177	88.5	54.59

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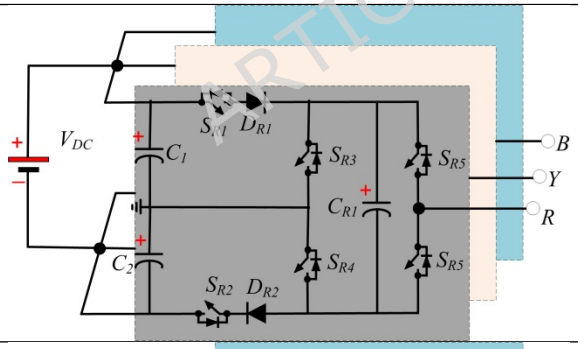
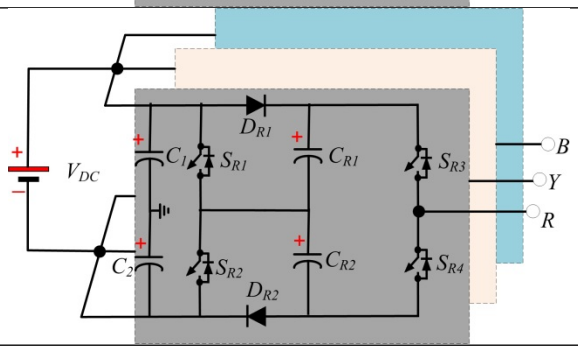
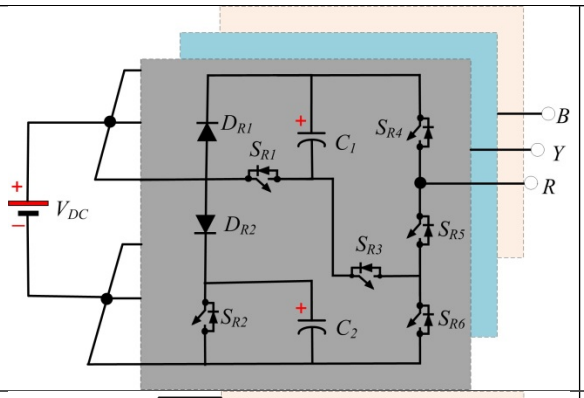
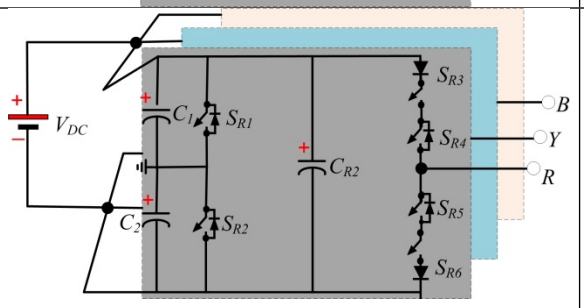
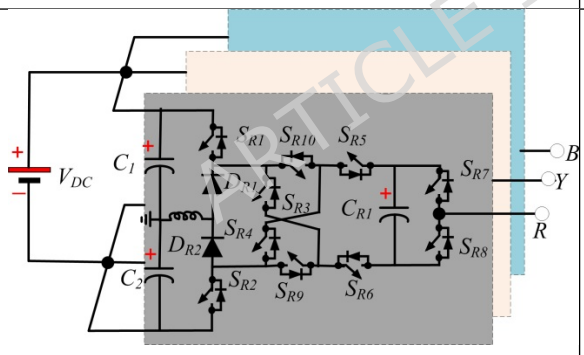
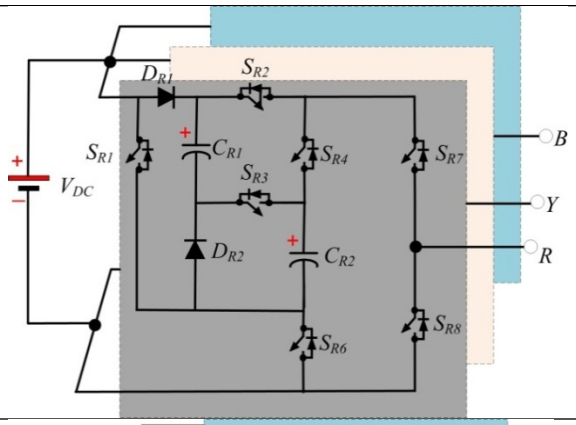
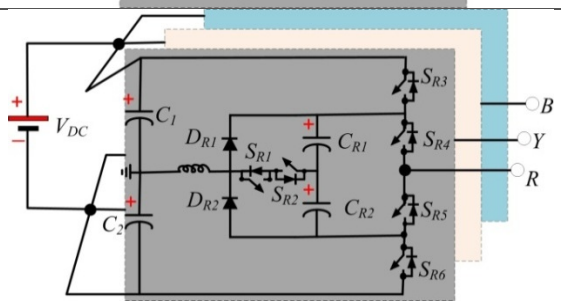
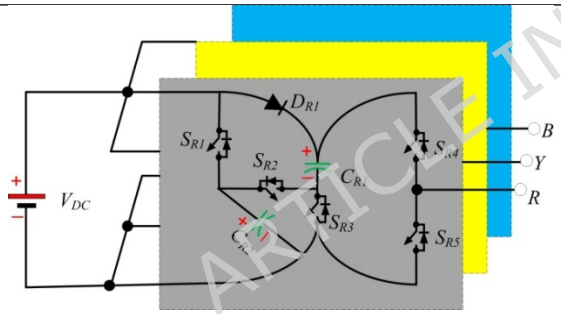
Table 4: Comparative analysis with the existing Topologies

Parameter	[3]	[4]	[10]	[6]	[13]	[17]	[11]	[14]	[15]	[20]	[19]	[18]	[PT]
a	10	4	9	9	7	8	12	7	9	4	6	7	5
b	1	1	2	1	4	1	2	3	-	2	2	-	1
c	1	1	3	2	2	2	2	2	2	4	3	1	2
d	2	2	2	2	2	2	1.5	2	2	2	1	2	2
e	14	5	15	14	16	15	11	14	9	6	5	7	7
f	2	2	2	2	2	2	2	2	2	1.5	1	2	2
g	10	4	9	9	7	8	12	7	9	4	6	7	5
a. No of switches, b. No. of diodes/inductor, c. No. of capacitors, d. MBV, e. TSV, f. Gain,g=No.driver													

Table 5. Merist and Key Features of the 3 Phase SCMLI Topologies

Ref.	Topologies	Metiers	Key features and Remarks
[25]		N_{comp} = 11 TSV_{pu}/leve = 2 gain = 1 $T_{SC,M}$ = 1 η=96.8%@700 W	▯ Can not generate any level operation under open-circuit fault condition of the capacitor. ▯ larger energy storage requirement.
[20]		N_{comp} = 14 TSV_{pu}/leve = 2 gain = 1,5 $T_{SC,M}$ = 1 η=96.2%@700 W	▯ Can not generate any level operation under open-circuit fault condition of the capacitor. ▯ larger energy storage requirement.

[23]		N_{comp} = 10 TSV_{pu}/leve = 4 gain = 2 $T_{SC,M}$ = 1 ɳ=97.2%@700 W	▯ Can not generate any level operation under open-circuit fault condition of capacitor. ▯ low energy storage requirement.
[19]		N_{comp} = 11 TSV_{pu}/level = 2 gain = 1 $T_{SC,M}$ = 1 ɳ=97.5%@700 W	▯ Can not generate any level operation under open-circuit fault condition of capacitor. ▯ Incapable of handling the C_{R2} failure. ▯ Lower energy storage requirement. ▯ Capable of handling the inductive load.
[24]		N_{comp} = 14 TSV_{pu} = 2 gain = 2 $T_{SC,M}$ = 1 ɳ=96%@700W	▯ Can not generate any level operation under open-circuit fault condition of capacitor. ▯ Incapable of handling the C_{R1} failure. ▯ Lower energy storage requirement.

[22]		N_{comp} = 11 TSV_{pu} = 1.6 gain = 2 $T_{SC,M}$ = 0.5 η=94.23%@700W	▯ Can not generate any level operation under open-circuit fault condition of capacitor. ▯ Lower energy storage requirement.
[21]		N_{comp} = 13 TSV_{pu}/level = 1.66 gain = 1 $T_{SC,M}$ = 0.5 η=97.6%@700W	▯ Can not generate any level operation under open-circuit fault condition of capacitor. ▯ Incapable of handling the C_3 failure. ▯ Lower energy storage requirement.
[P]		N_{comp} = 6 TSV_{pu}/level = 0.7 gain = 2 $T_{SC,M}$ = 1 η=97.81%@70W	▯ Can create a three-level when capacitor C_1 and C_2 are open-circuit. ▯ Lower energy storage requirement. ▯ Capable of handling the inductive load.

VI. Results Analysis

(a) Results of the Simulation:

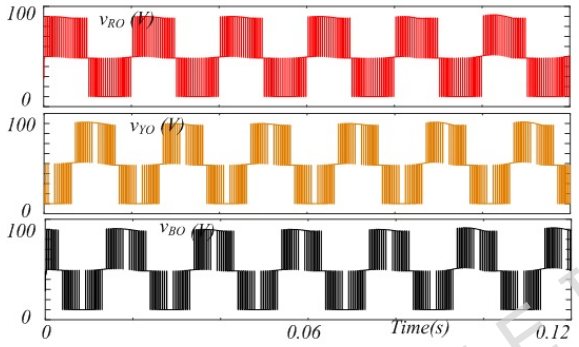
Table 6: Parameters for Validation of Simulation and Experimentation

Item	Specification
V_{DC}	50
C_1, C_2	2100μF
f_{sw}	2000Hz
f	50 Hz
Diode	SBR40U300CTB, 300V, 40A
MOSFETs	IXTP36N30T(TO220), 300V, 36A
Driver	TLP250, 25kHz

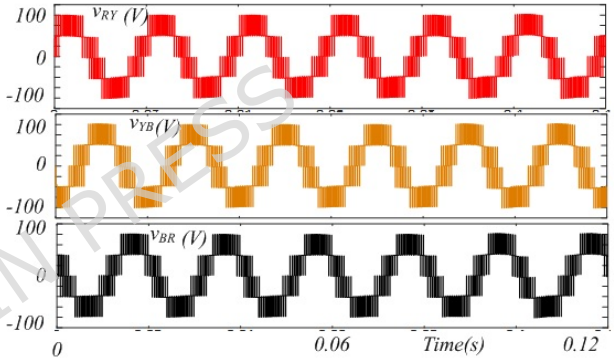
load	R=50, L=80mH

*www.mouser.in

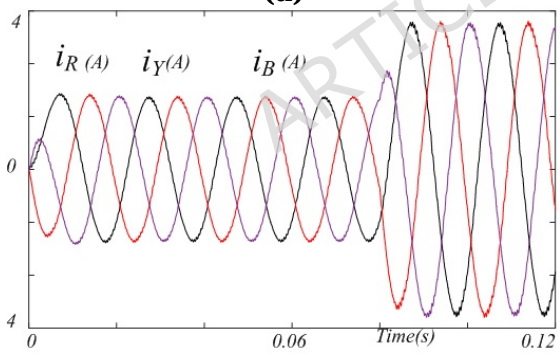
A detailed time-domain simulation of the PT supplying an RL load has been performed to analyse its transient response. The system parameters are listed in Table 6. As illustrated in Fig. 7(a), the pole voltage waveform consistently exhibits three distinct levels of magnitude 50 V without distortion, even under varying load conditions. The corresponding line voltage waveforms of the PT are presented in Fig. 7(b), showing that a stable five-level (line to-line)output is maintained for each phase regardless of load variation. During transient states, the PT effectively adapts and maintains capacitor-voltage self-balancing under load variations, as demonstrated in Figs. 7(c). Fig. 7(d) illustrates the per-phase voltage, current, and capacitor voltage waveforms, providing a clearer understanding of the capacitor voltage balancing mechanism. Fig. 7(e) shows the current in capacitors. Fig.7 (f) shows the voltage stress of various switches. Fig.7 (g-h) shows the transient response of the input voltage and the modulation index. Fig. 7(i) and (j) show the total harmonic distortion (THD) of the voltage and current, respectively.



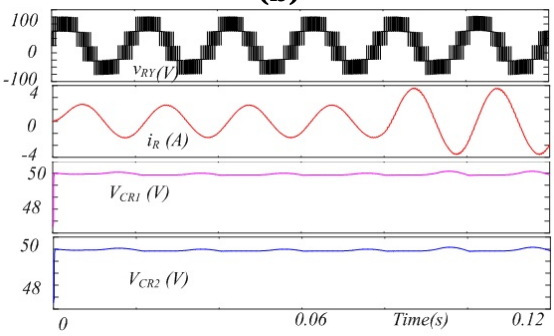
(a)



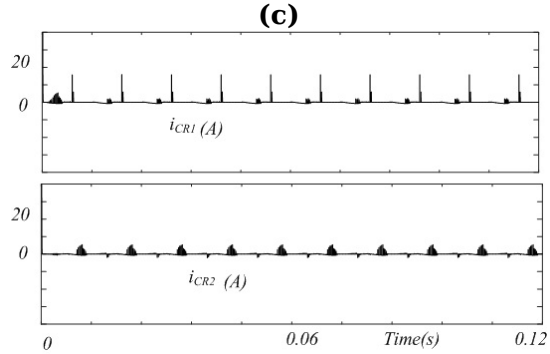
(b)



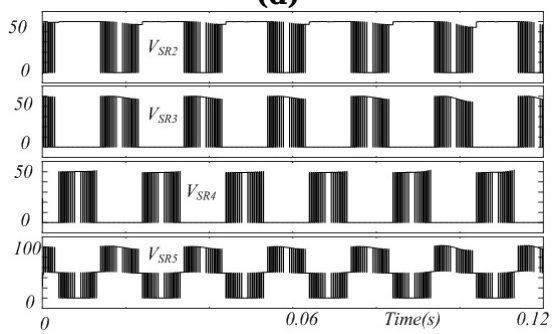
(c)



(d)



(e)



(f)

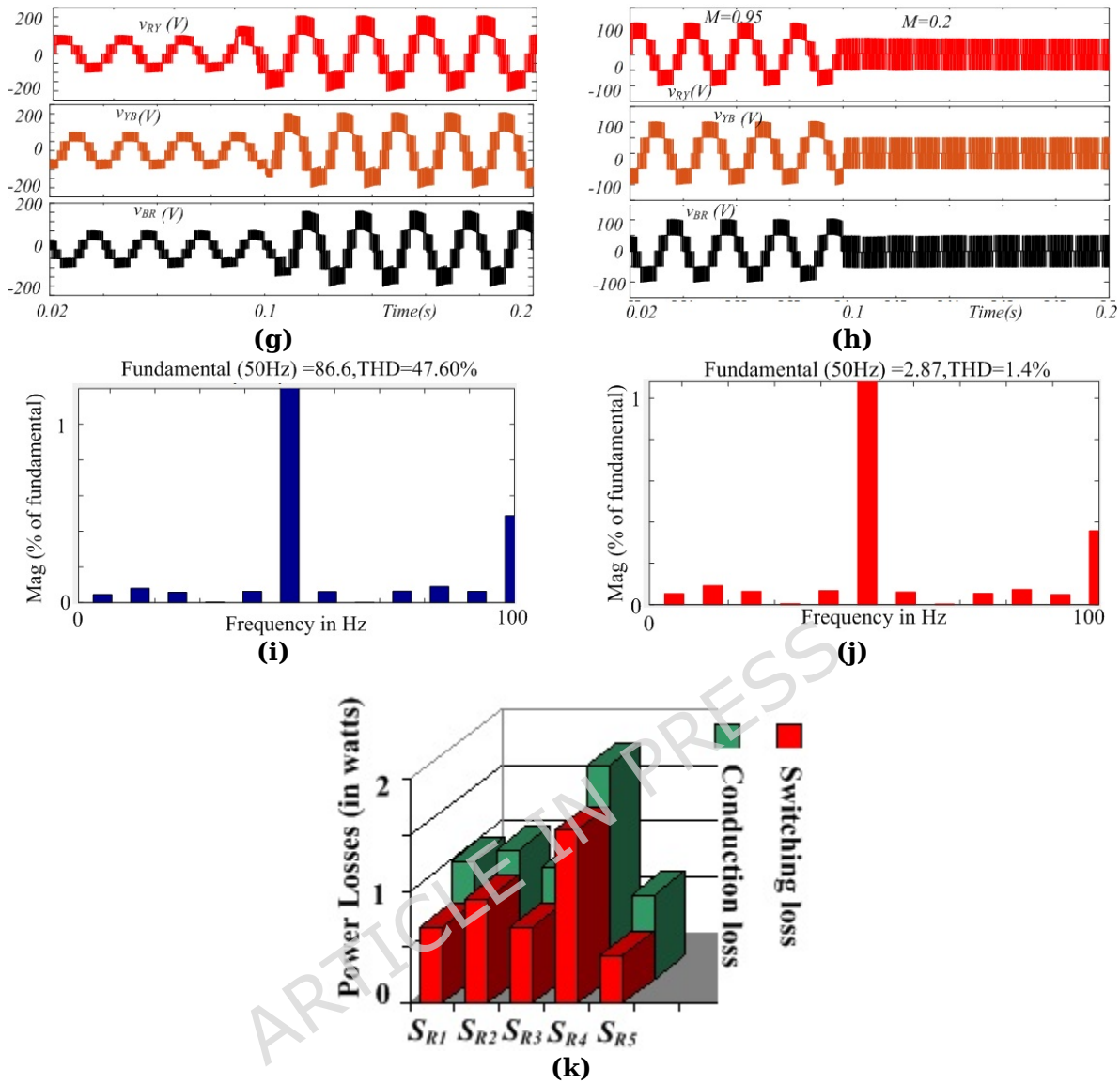


Fig. 7 displays simulation results (a), v_{RO}, v_{YO}, v_{BO} (b) v_{RY}, v_{YB}, v_{BR}, (c) li_R, i_Y,i_B (d) (d) Per Phase, v_{RY},i_R,V_{CR1},V_{CR2} (e) capacitor charging current (f) voltage stress of the switches (g) step change in voltage (h) step change in modulation index (i) voltage THD (j) Current THD (k) loss distribution graph

(b) Results of the experiment:

To confirm the efficacy of the PT, experimental testing was performed in the laboratory. Table 6 shows the parameters used for the experimental setup, and Fig. 8 shows the laboratory prototype module. The corresponding experimental results are presented in Fig. 9. The PT makes a three-level pole voltage (v_{RO}, v_{YO}, v_{BO}) and each level has the same amount of 50V, as shown in Fig. 9(a). Figure 9(b–c) shows the PT line voltages (v_{RY}, v_{YB}, v_{BR}) and the line currents (i_R, i_Y,i_B). It has been noted that the PT setup successfully creates a 5-level line-to-line voltage when the load is stepped in increments. Figure 9(d) shows the phase voltage and current waveforms during transient conditions, making it

easier to understand how the capacitor maintains its voltage. Fig. 9(e) displays the power and efficiency behaviors for both simulation and experimentation under different loading circumstances. Changes in voltage and modulation index are shown in Fig.9 (f-g), respectively. Voltage stress and capacitor current are shown in Fig.9(h-i). Approximately zero leakage current of the proposed structure is shown in Fig. 9(j), making it suitable for PV applications. Fig.9(k-l) shows the THD analysis of the proposed SCMLI.

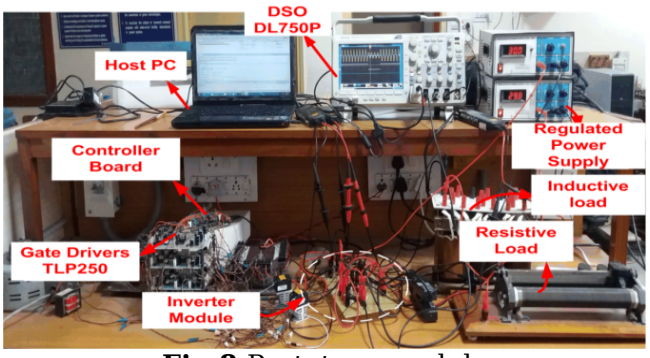
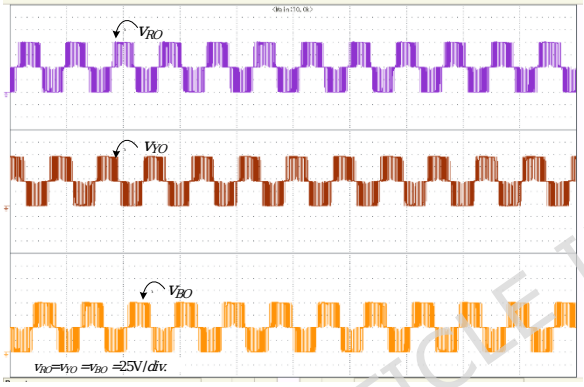
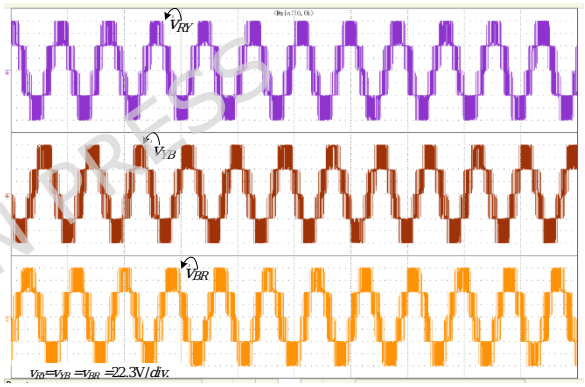


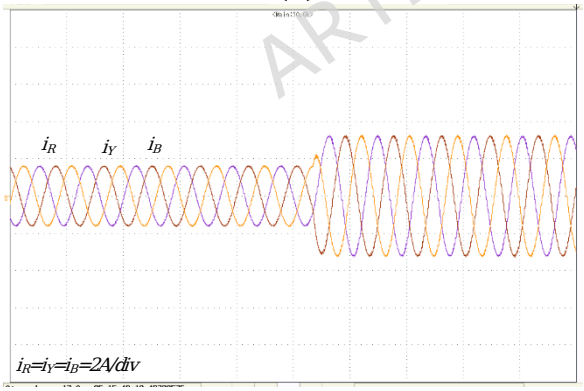
Fig.8 Prototype module



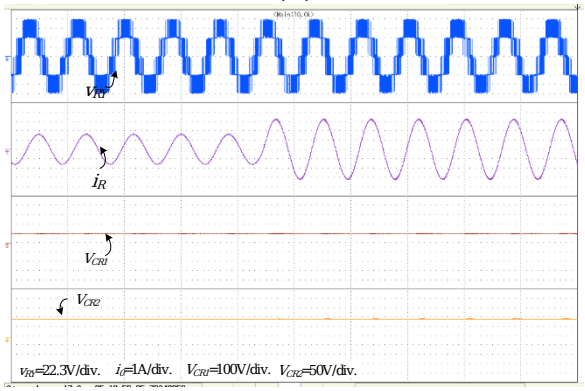
(a)



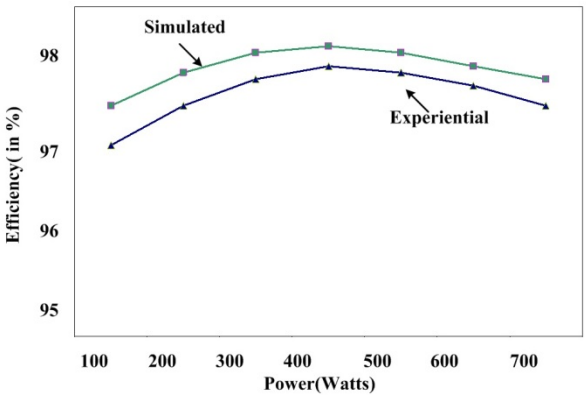
(b)



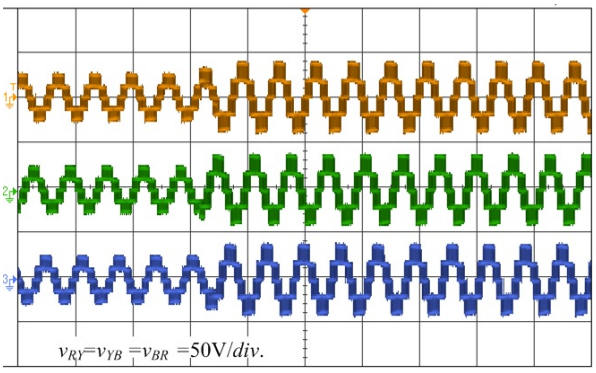
(c)



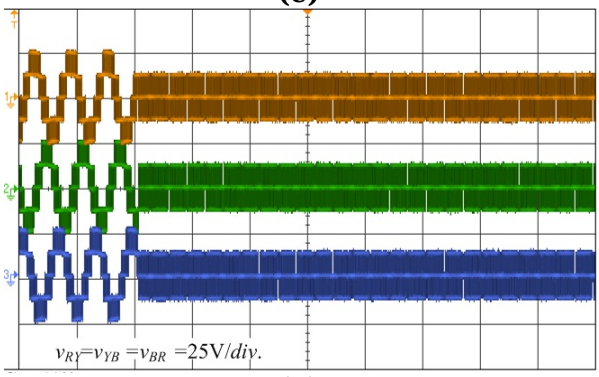
(d)



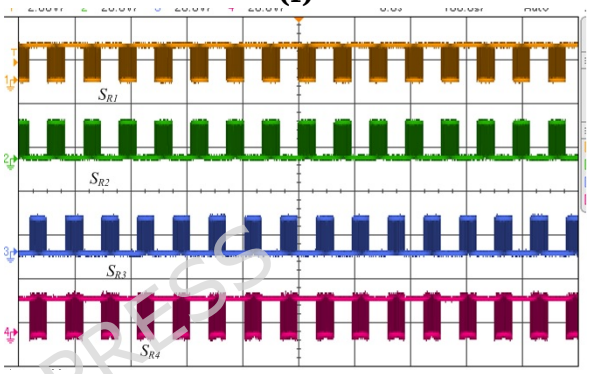
(e)



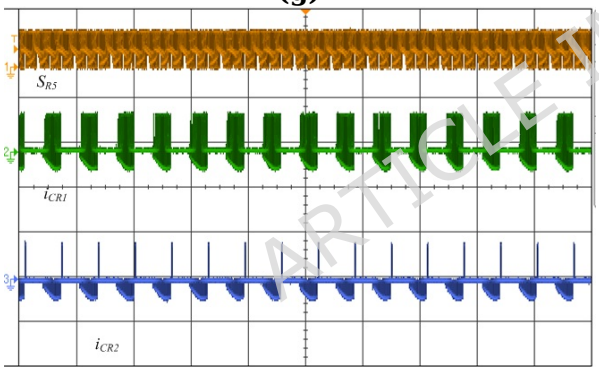
(f)



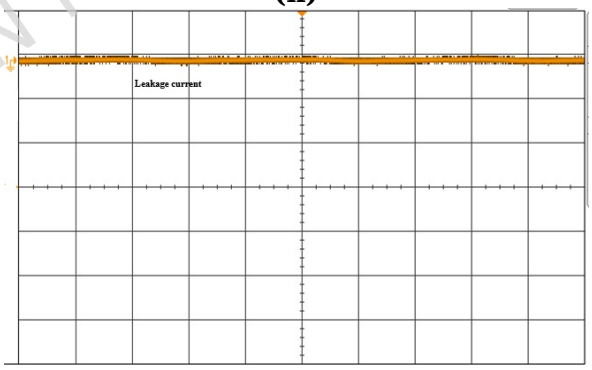
(g)



(h)

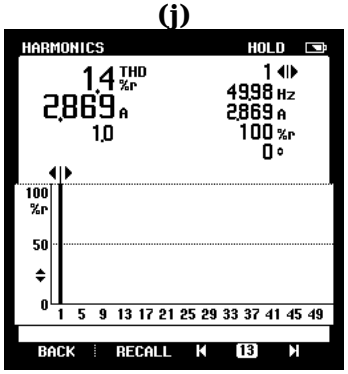


(i)



(j)

(k)



(l)

Fig.8 Experimental Results (a), v_{RO}, v_{YO}, v_{BO} (b) v_{RY}, v_{YB}, v_{BR}, (c) li_R, i_Y,i_B (d) Per Phase, v_{RY},i_R,V_{CR1},V_{CR2} (e) Power Vs Efficiency curve (f) change in input voltage (g) change in Modulation index (h) voltage stress (i) capacitor current stress (j) leakage

current (k)Voltage THD (l) Current THD

VII. Conclusion

A novel three-phase five-level SCMLI for RE applications is presented in this article. Additionally, the suggested inverter achieves capacitor self-balancing by eliminating the need for voltage sensors. It attains a voltage gain of two and a noteworthy least TSV of 7. Due to its boosting capability, the proposed SCMLI is suitable for applications in PV, EV, and UPS. A thorough comparison analysis demonstrates this topology superiority over current designs. A prototype module is used to experimentally validate the PT, confirming reliable operation across different operational modes. Moreover, the maximum efficiency of the PT is around 97.81% at 400 W and the cost is $54.59.

Declarations:

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Authors' Contribution: NN, KJ: Conceptualization, Methodology, Data Analysis, Writing-original draft. KJ, KKG: Visualization, Supervision, Validation. AMK, DK, NKD: Visualization, Analysis, Writing – review & editing.

Data availability: The datasets used and/or analyzed during the current study are available from the corresponding author upon reasonable request.

Conflict of Interest declaration: The authors declare that they have NO affiliations with or involvement in any organization or entity with any financial interest in the subject matter or materials discussed in this manuscript.

Competing interest: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Ethical Approval: Ethical and professional standards have been met. No animals or humans are used in this study.

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