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Van der Waals junction field effect transistors with both n- and p-channel transition metal dichalcogenides

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Two-dimensional (2D) transition metal dichalcogenides (TMDs)-based van der Waals (vdW) PN junctions have been used for heterojunction diodes, which basically utilize out-of-plane current across the junction interface. In fact, the same vdW PN junction structure can be utilized for another important device application, junction field effect transistors (JFETs), where in-plane current is possible along with 2D–2D heterojunction interface. Moreover, the 2D TMD-based JFET can use both p- and n-channel for low voltage operation, which might be its unique feature. Here we report vdW JFETs as an in-plane current device with heterojunction between semiconducting p- and n-TMDs. Since this vdW JFET would have low-density traps at the vdW interface unlike 2D TMD-based metal insulator semiconductor field effect transistors (MISFETs), little hysteresis of 0.0–0.1 V and best subthreshold swing of ~100 mV/dec were achieved. Easy saturation was observed either from n-channel or p-channel JFET as another advantage over 2D MISFETs, exhibiting early pinch-off at ~1 V. Operational gate voltage for threshold was near 0 V and our highest mobility reaches to ~>500 $cm^2/V{\cdot}s$ for n-channel JFET with MoS_2 channel. For 1 V JFET operation, our best ON/OFF current ratio was observed to be ~10^4.

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INTRODUCTION

Two-dimensional (2D) transition metal dichalcogenides (TMDs) have been extensively studied in both aspects of materials and devices for the past decade, since those are regarded to have great potentials for future nanoelectronics.[1–11] Main focus has been on 2D TMD semiconductor devices, which are probably the most important for existing or future technologies.[3,8–12] Many of metal insulator semiconductor field effect transistors (MISFETs) using 2D TMD channels have thus been reported,[8,10,13–22] along with their use for complementary metal-oxide-semiconductor transistor inverters.[23–28] Heterojunction 2D TMD p–n (PN) diodes with van der Waals (vdW) interface have also received much attention from researchers.[29–44] These vdW PN junction interfaces basically experience out-of-plane or vertical current across the junction during device operation. In fact, the same vdW PN junction structure can be utilized for another important device application, junction field effect transistors (JFETs), where in-plane current is possible along with 2D–2D heterojunction interface. However, the vdW JFET application seems not reported yet, although some possibilities have just been casted in black phosphorous/ZnO nanowire junction systems.[45]

In the present work, we have fabricated vdW JFETs as an in-plane current device with heterojunction between semiconducting p-$MoTe_2$ (or p-WSe_2) and n-MoS_2 TMDs. Since this vdW JFET would have low-density traps at the heterojunction interface when p-type material plays as a gate for n-channel and vice versa, little hysteresis of 0.05–0.1 V and good subthreshold swing (SS) of ~100 mV/dec were achieved. In addition, vdW JFET always exhibited easy saturation at a low drain voltage of ~1 V and reproducibly showed low operational gate voltages for threshold near 0 V (+0.2 V for p-JFET and −0.2 V for n-JFET). Above-mentioned properties have rarely been realized all together from general vdW 2D MISFETs.[20,22] The highest mobility reaches to ~>500 $cm^2/V{\cdot}s$ for n-channel JFET with MoS_2 channel while p-channel JFET with $MoTe_2$ appears much lower by more than an order of magnitude (~13 $cm^2/V{\cdot}s$). These values are comparable or approaches to previous results from 2D FETs.[12,25,46] For our low-voltage JFET devices, ON/OFF current ratios were observed to be ~>10^4. The operation of both channel JFETs with ultrathin vdW 2D TMDs is regarded unique and different from that of general three-dimensional (3D) JFETs and MISFETs, and in principle two opposite (p and n) channels can be used as gate for each other. We again confirmed the principle through another p-TMD/n-TMD JFET (p-WSe_2/n-MoS_2 junction).

RESULTS AND DISCUSSION

Figure 1a displays an optical microscopic (OM) image of our p-$MoTe_2$/n-MoS_2 channel JFET device fabricated on 285-nm-thick SiO_2/p-Si wafer. Pt and Au are used as source/drain ohmic electrodes, respectively, for $MoTe_2$ and MoS_2 channel. As shown in a 3D schematic device view in Fig. 1c, hexagonal 2H-MoS_2 channel overlies on 2H-$MoTe_2$ when the two channels cross each other. The two semiconducting TMDs are simultaneously and clearly identified by micro Raman spectroscopy as shown in Fig. 1b, for which a central spot of the overlapped region is probed (see the red spot in Fig. 1a). Since the p- and n-channel materials are crossing, four different PN diodes are possibly formed using Pt and Au electrode and such diode behavior was confirmed (see

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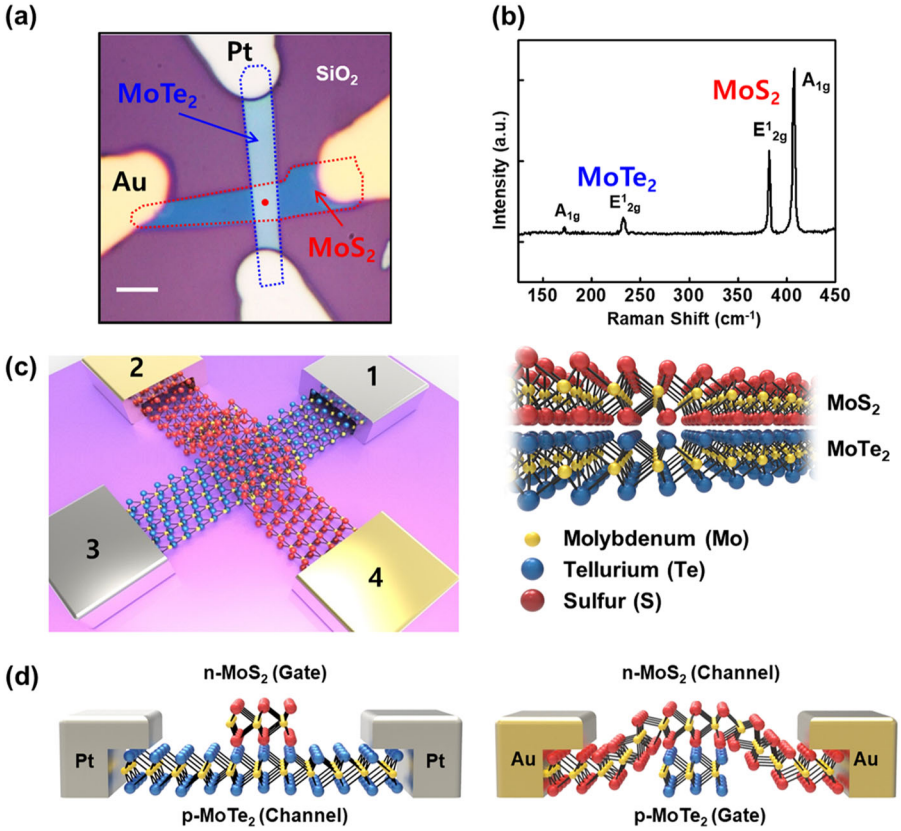

Fig. 1 Materials characteristics and device schematic views. **a** Optical microscopic (OM) image of our JFET device fabricated on 285-nm-thick SiO_2/p-Si wafer. Red and blue dashed lines outline MoS_2 and $MoTe_2$ flake area, respectively. Scale bar = 5 μm. **b** Raman spectra obtained from red dot point of the overlapped region. **c** 3D schematic view of our MoS_2 and $MoTe_2$ junction device. Four heterojunction PN diode pairs can basically be formed (supporting information, Fig. S1) **d** 3D cross sectional views of p-MoTe2 channel (n-MoS2 gate) and n-MoS2 channel (p-MoTe2 gate) JFET devices

supporting information in Figure S1). In addition, from the same structure, p- and n-type MISFET behavior was also confirmed along with large hysteresis in the transfer curve characteristics (Figure S2a).

Following the OM for the JFET structure (Figs. 1a and 2a inset), atomic force microscopy (AFM; Fig. 2a, b) and scanning kelvin probe microscopy (SKPM, Fig. 2c) were conducted probing a rectangular region of the same device, which contains four respective surfaces as shown in Fig. 2a: SiO_2 substrate, $MoTe_2$, MoS_2, and overlay MoS_2 on $MoTe_2$. According to AFM results (image contrast), the thickness of $MoTe_2$ and MoS_2 channel appears to be ~16 and 6 nm, respectively. According to SKPM results, the work functions of individual $MoTe_2$ and MoS_2 are quite the same, to be 4.54 eV, while that of MoS_2 overlay on $MoTe_2$ is slightly higher to be 4.56 eV. Slightly higher value is probably because MoS_2 on $MoTe_2$ is exempted from the effects of trap charges on SiO_2 surface[47,48] and also because of some electron charge transfer between the two TMDs. Based on SKPM data, we could expect and construct the band diagrams of $MoTe_2/MoS_2$ PN junction, MoS_2 n-channel, and $MoTe_2$ p-channel as seen in Fig. 2d–f, respectively. The PN junction should contain ~0.3 nm vdW gap between $MoTe_2$ and MoS_2. Without gate bias, channel has almost no energy barrier but built-in potential energy ($q\Phi_i$ = 0.02 eV for n-channel). When a reverse bias is applied to the p-type gate of n-channel, the MoS_2 channel should have energy barrier at the p-gated (overlapped) region (Fig. 2e), where the Fermi energy becomes located in the middle of the band gap indicating charge carrier depletion (for OFF state). Similarly, the $MoTe_2$ channel has the energy barrier at the n-gate region (Fig. 2f) under a reverse bias applied on p-channel. Without drain bias voltage, the band diagram with the barrier must be symmetric; however, it should become asymmetric under drain bias.

As expected from the in-plane direction band diagram (Fig. 2e, f), n-channel JFET was experimentally demonstrated in Fig. 3a–f. Figure 3a shows an OM image of another JFET that is different from that of Fig. 1a but has a comparable channel thickness dimension: ~12 and 7 nm, respectively, for MoS_2 and $MoTe_2$ channels. Output characteristics (drain current–drain voltage; I_D–V_{DS}) of the device in Fig. 3d display three stages for typical transistors: linear (i), pinch-off (ii), and saturation-to-early effect (iii). Those three stages are well explained with schematic JFET cross-sections under, respectively, different V_{DS} in Fig. 3c, while each material component of the device is identified by color in the schematic 3D view of Fig. 3b. Cross-section (i) in Fig. 3c shows a conducting channel under small V_{DS} for linear regime I_D. As V_{DS} increases toward more positive voltage, drain side experiences reverse bias with respect to the p-gate and asymmetric channel depletion (crosshatched area) takes place while source side maintains forward bias and channel opening. As V_{DS} increases further, the n-channel reaches to pinch-off state (ii) and even channel length (L) modulation (iii). Such channel length modulation causes shorter length (L') and elevated current (deviated from saturation; early effect). This channel modulation was quite general in our JFET devices as observed from another JFET (supporting information Figure S3a). Figure 3e shows transfer characteristics (drain current–gate voltage; I_D–V_{GS}), where a good ON/OFF I_D ratio of 5×10^4 and SS of ~100 mV/dec were observed. The gate leakage current (I_G) appears to increase with applied gate voltage (V_{GS}) in Fig. 3e, and it is certainly understandable as

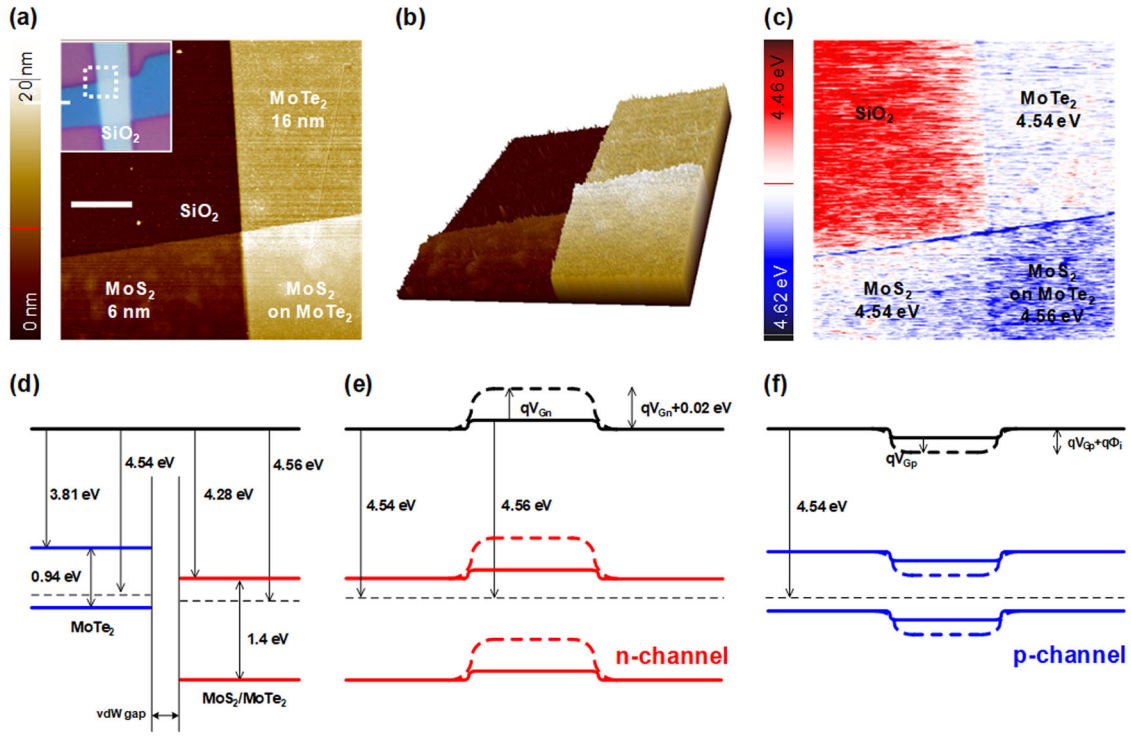

Fig. 2 Device band diagram by AFM and SKPM. **a** 2D and **b** 3D AFM images of the JFET structure. Scale bar = 1 μm. **c** SKPM image of the JFET. White dashed box in the inset of **a** indicates the scanning region for AFM and SKPM (**a**–**c**). Energy band diagrams of **d** $MoTe_2/MoS_2$, **e** MoS_2 n-channel, and **f** $MoTe_2$ p-channel, respectively. V_{Gn} and V_{Gp} means the gate biases, respectively, applied on n- and p-channels

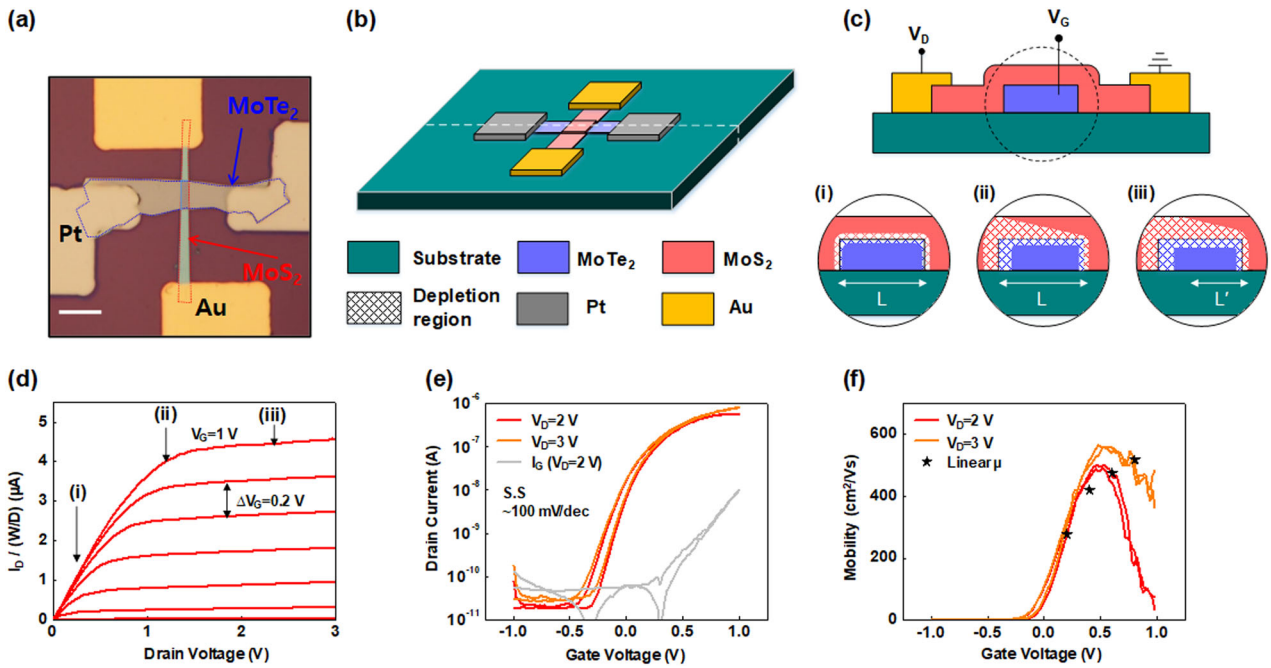

Fig. 3 n-channel of p-$MoTe_2$/n-MoS_2 JFET. **a** OM image of n-channel JFET. Scale bar = 10 μm. **b** Simple 3D schematic of our n-channel JFET. **c** 2D cross-section device views according to (i) small, (ii) pinch-off, and (iii) large V_{DS} as sectioned along with the white dashed line in **b** of our n-channel device. **d** I_D–V_{DS} output characteristics of n-channel JFET. **e** I_D–V_{GS} transfer characteristics of n-channel JFET. **f** Mobility of our n-channel JFET. Red and orange lines indicate the saturation mobility and black stars indicate the linear mobility at different V_{GS} (0.2, 0.4, 0.6, 0.8 V, respectively)

forward bias-induced leakage that originates from the PN junction between n-MoS_2 and p-$MoTe_2$.

The saturation mobility of our JFET is also extracted from the same figure. Threshold voltage and peak saturation mobility appear to be −0.2 V and 500–600 $cm^2/V{\cdot}s$, respectively, according to Fig. 3e, f. The saturation mobility was driven from the following Eq. (1), which needs the information on carrier concentration, N_d, and transconductance, g_m, in MoS_2 n-channel. We extract g_m plots

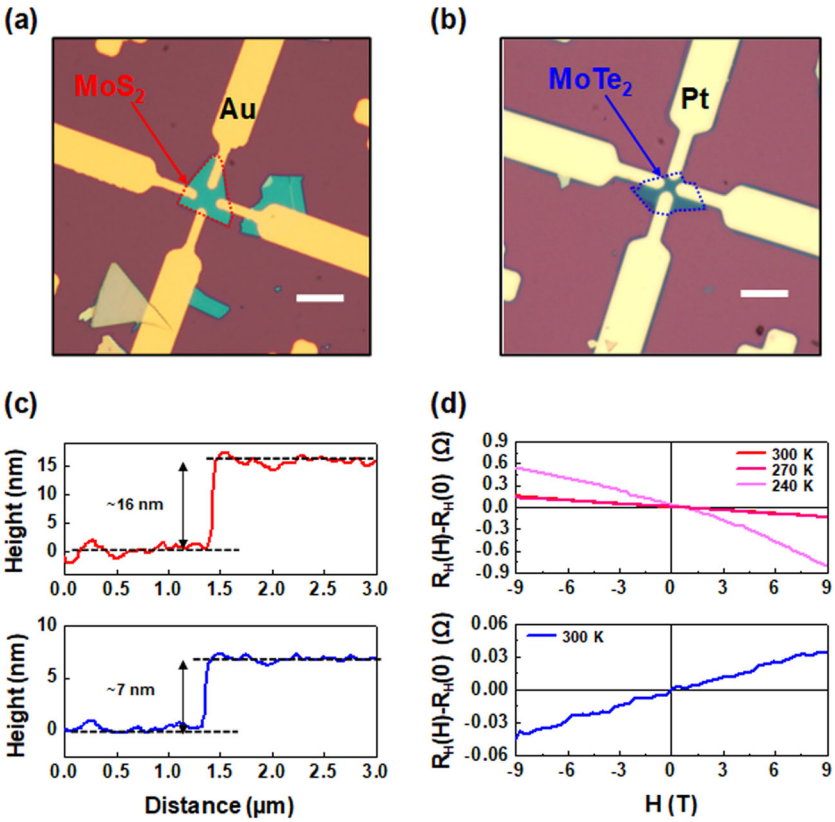

Fig. 4 Hall measurement of MoS_2 and $MoTe_2$. OM image of **a** n-MoS_2 and **b** p-$MoTe_2$ for four-probe Hall measurement. **c** Flake thickness profiles of MoS_2 (red) and $MoTe_2$ (blue) as obtained from AFM scanning, and **d** $R_H(H)$–$R_H(0)$ data under the magnetic field (H) for MoS_2 (top negative slopes) and $MoTe_2$ (positive slope). Scale bar of **a**, **b** = 10 μm

from transfer curves as a function of V_{GS} in Fig. 3e.

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{qN_d\mu tW}{L} \quad (1)$$

So the mobility can be calculated as follows,

$$\mu = \frac{Lg_m}{qN_d tW} \quad (2)$$

where N_d is carrier density as number per cm^3; q is an electronic charge; and t, W, and L are the thickness, width, and length of the channel, respectively. Linear mobility can also be extracted out of the output characteristics at different V_{GS} in Fig. 3d, using the following simple Eq. (3) at small V_{DS}.

$$\mu = \frac{Lg_d}{qN_d tW}, \qquad \left(g_d = \frac{dI_D}{dV_{DS}}\right) \quad (3)$$

The maximum linear mobility appears quite comparable to that of saturation regime.

For both estimations of saturation and linear mobilities, N_d value would be the most important information. In order to obtain N_d value at room temperature, we have actually attempted four-point van der Pauw Hall measurements with Au-contacting 16-nm-thin MoS_2 and Pt-contacting 7-nm-thin $MoTe_2$. Figure 4a, b show two OM images of our samples on SiO_2/p-Si substrate, while each thickness of the samples was measured by AFM scan as shown with the results of Fig. 4c. Although the sample shapes were not ideal symmetric in Fig. 4a, b, $MoTe_2$ and MoS_2 samples displayed positive and negative slopes, respectively, under magnetic field (H) sweep for relative magnetic resistance [$R_H(H)$–$R_H(0)$] vs. H field plot in Fig. 4d. Those slopes clearly identify or distinguish p- and n-type conduction. According to the slope, hole and electron concentrations (N_a and N_d) were calculated to be 2.43×10^{17} and $2.5 \times 10^{16}/cm^3$ at 300 K, respectively. Calculation details are in supporting information section.

All of our JFET devices displayed only a little hysteresis unlike MISFET (Figure S2a) because of small density charge traps at the vdW PN junction interface. Mobility plots in Fig. 3f and transfer curves of Figure S2b exhibit a small hysteresis of 0.05–0.1 V whether the device is n- or p-channel JFET (which is actually a single device working with both channels). Figure 5a shows our third JFET with p-channel, and in fact, this JFET has similar channel thickness of ~10 nm, which is comparable to that of n-channel JFET in Fig. 3a. Output curve characteristics in Fig. 5d show the three I_D regimes: linear (i), pinch-off (ii), and saturation (iii). At first glance, the p-channel I_D output curves are comparable to those of n-channel ones in Fig. 3d; however, it is recognized on detail observation that pinch-off stage appears slower in $MoTe_2$ p-channel; saturation voltages ($V_{SAT} = -1.5$ V for $V_{GS} = -1$ V) of p-channel are larger than those of MoS_2 n-channel ($V_{SAT} =$ ~0.8 V for $V_{GS} = 1$ V). It is related to the hole carrier density of p-channel, which is an order of magnitude larger than that of n-channel; the charge depletion of p-channel is more difficult under the same V_{GD} ($V_{GS}-V_{DS}$) than that of n-channel. Figure 5b, c present schematic 3D and cross-section views of the p-channel JFET. As shown in Fig. 5c, under a positive V_{GD} MoS_2 gate (reverse bias) is more readily depleted than $MoTe_2$ p-channel, which needs further V_{DS} for reaching to pinch-off. In Fig. 5e, our p-channel JFET shows an order of magnitude lower I_D than that of n-channel one, along with inferior SS (200 mV/dec) and ON/OFF I_D ratio (5×10^3) to those of n-channel device. Difficult channel depletion or channel closing might be closely related to such inferiorities. According to Fig. 5f, the saturation (13–14 cm^2/V·s as the peak mobility) and

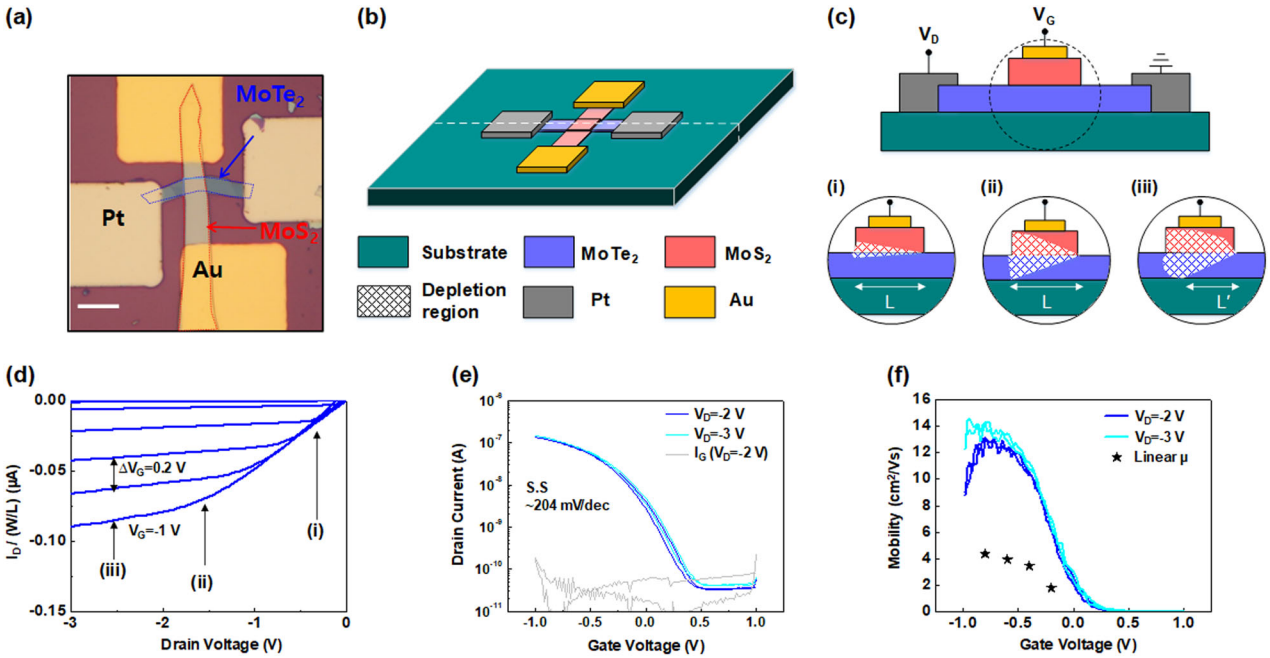

Fig. 5 p-channel of p-$MoTe_2$/n-MoS_2 JFET. **a** OM image of p-channel JFET. Scale bar = 10 μm. **b** Simple 3D schematic of our p-channel JFET. **c** 2D cross-section device views according to (i) small, (ii) pinch-off, and (iii) large V_{DS} as sectioned along with the white dashed line in **b** of our p-channel device. **d** I_D–V_{DS} output characteristics of p-channel JFET. **e** I_D–V_{GS} transfer characteristics of p-channel JFET. **f** Mobility of our p-channel JFET. Blue and skyblue lines indicate the saturation mobility and black stars indicate the linear mobility at different V_{GS} (−0.2, −0.4, −0.6, −0.8 V, respectively)

linear mobilities (4 cm^2/V·s) of p-channel JFET appear comparable to the previous reports from p-$MoTe_2$ MISFETs[25] but much inferior to the values from MoS_2 JFET. Impurity scattering due to an order of magnitude higher carrier concentration in the p-channel would be a main reason for the low mobility along with the intrinsic band structure of $MoTe_2$.[49,50] Besides, we could also suspect the many traps at the $MoTe_2$ channel/SiO_2 interface as another reason of such low mobility in respect of device geometry.

As our final device, p-WSe_2/n-MoS_2 JFET was fabricated on purpose to confirm that any p-TMD/n-TMD JFET generally works in principle; p-TMD works as gate for n-TMD channel while n-TMD does as gate for p-TMD channel. Figure 6a, b, respectively, show the OM and schematic 3D view of the JFET, where Au contact was used in common for both p-WSe_2 and n-MoS_2 channel FETs. Figure 6c displays Raman spectra from both flakes as obtained at once by probing the overlaid position (red dot in Fig. 6a). According to output curve characteristics of Fig. 6d, p- and n-channel JFETs operate well again, although the contact resistance between Au and p-WSe_2 appears serious. Owing to such shortcoming in contact resistance, p-WSe_2 JFET shows its inferior I–V characteristics with a few nA of ON state, and the inferior conductance of p-channel WSe_2 results in its insufficient gating for n-MoS_2 JFET. Hence, n-MoS_2 JFET in p-WSe_2/n-MoS_2 system displays an order of magnitude lower ON state I_D than that of p-$MoTe_2$/n-MoS_2 JFET case, as seen in the output and transfer characteristics of Fig. 6d, e. However, this demonstration of p-WSe_2/n-MoS_2 JFET device still supports that any p-TMD/n-TMD JFET generally works in principle using both channels. (Figure S4 shows AFM thickness profile of p-WSe_2 and n-MoS_2 flakes in JFET.)

In summary, we have fabricated vdW JFETs as an in-plane current device with heterojunction between semiconducting p-$MoTe_2$ and n-MoS_2 TMDs. Since this vdW JFET would have low-density traps at the vdW interface when p-type material plays as a gate for n-channel and vice versa, little hysteresis of 0.05–0.1 V and good SS of ~100 mV/dec were achieved. Easy saturation was observed as another advantage over 2D MISFETs, exhibiting early pinch-off at ~1 V. Operational gate voltage for threshold was near 0 V and the highest mobility reaches to ~>500 cm^2/V·s for n-channel JFET with MoS_2 channel while p-channel JFET with $MoTe_2$ appears much lower by more than an order of magnitude (~13 cm^2/V·s). For 1 V JFET operation, our highest ON/OFF current ratio was observed to be ~10^4. The operation of both channel JFETs with ultrathin vdW 2D TMDs is regarded unique and different from that of general 3D JFETs and MISFETs in the principle that two opposite (p- and n-) channels can be used as gate for each other. We again confirmed the principle through another p-TMD/n-TMD JFET (p-WSe_2/n-MoS_2 junction). We thus conclude that our 2D-like ultrathin channel JFET is fresh enough in its operating principle, structure, and fabrication simplicity to influence the future of 2D semiconductor-based nanoelectronics.

METHODS

Device fabrication

SiO_2/p-Si wafer (285-nm thick) was chosen as JFET device substrate. The substrates were cleaned in acetone and methyl alcohol by ultrasonicator. For p-$MoTe_2$/n-MoS_2 JFETs, α-$MoTe_2$ nanosheet (mechanically exfoliated from bulk crystals using polydimethylsiloxane) was transferred onto the substrate. Fifty-nm (Pt) ohmic electrodes for $MoTe_2$ were patterned by photolithography process and deposited by direct current (DC) magnetron sputtering system. In the next step, MoS_2 nanoflake was transferred onto the $MoTe_2$ flake forming vdW junction. Fifty-nm (Au) ohmic electrodes for MoS_2 were also patterned in the same way. For p-WSe_2/n-MoS_2 JFETs, WSe_2 nanosheet was transferred onto the substrate and then MoS_2 nanoflake was crossed over contacting WSe_2 flake. Au ohmic electrodes for both WSe_2 and MoS_2 were patterned by photolithography process and DC magnetron sputter deposition.

Characterization

All nanoflakes were measured for thickness information with AFM (Nanowizard I, JPK Instrument). SKPM measurements were performed

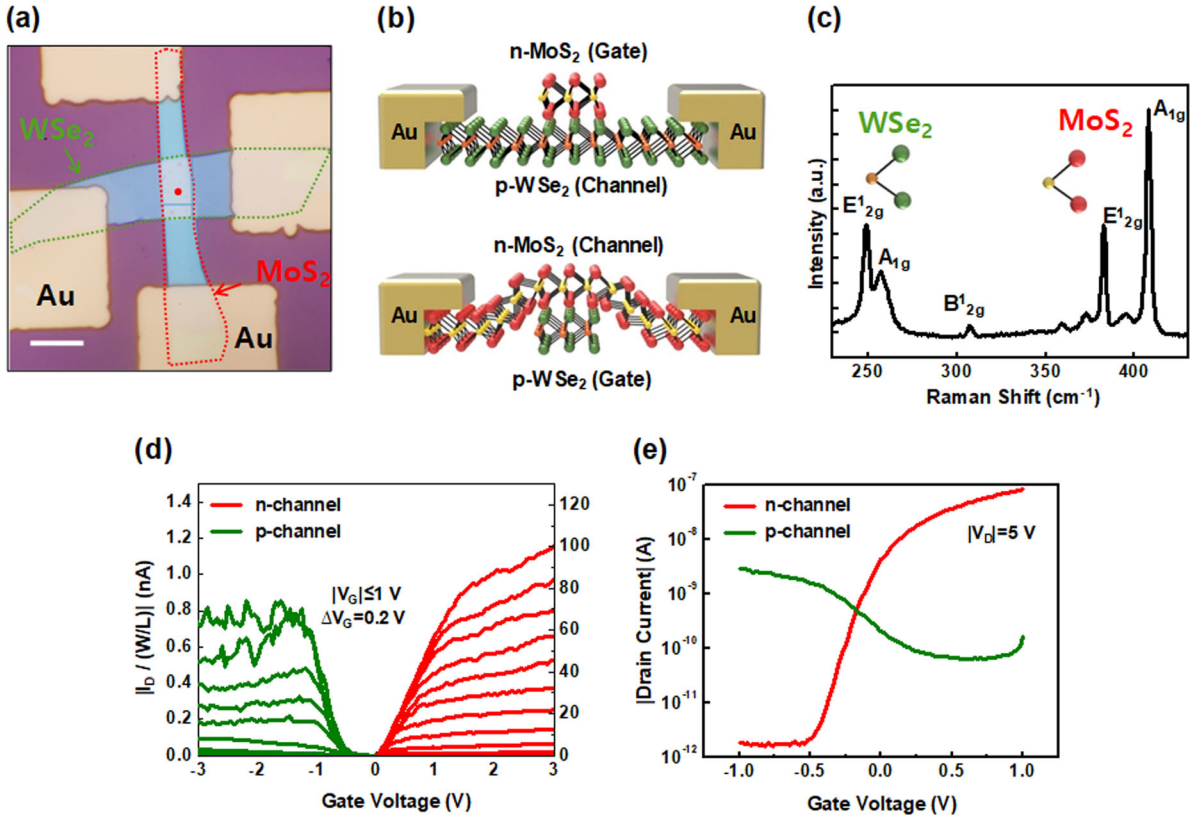

Fig. 6 p-WSe_2/n-MoS_2 JFET. **a** OM image of p-WSe_2/n-MoS_2 JFET on SiO_2/p-Si. Scale bar = 10 μm. **b** 3D schematic cross-sections of p-WSe_2 and n-MoS_2 channel JFET. Au was used as contact metal for both channels. **c** Raman spectra of WSe_2 and MoS_2 as obtained by probing the red spot in **a**. **d** I_D–V_{DS} output characteristics of p-WSe_2 and n-MoS_2 channel JFET. **e** I_D–V_{GS} transfer characteristics of p-WSe_2 and n-MoS_2 channel JFET

using Park Systems XE7 with non-contact mode. In SKPM imaging, we applied an alternating current (AC) bias voltage of 1.5 V with a frequency of 17 kHz to Au-coated tip (PPP-NCSTAu, nanosensors). Device electrical characteristics (I–*V* curve of diodes and transfer and output characteristics of transistors) were performed in the dark at room temperature using a semiconductor parameter analyzer (HP4155C, Agilent Technologies). The Hall measurement for carrier density estimation of MoS_2 and $MoTe_2$ nanoflakes on SiO_2/p^+-Si substrate were conducted by applying an AC current of 0.4 Hz and 0.1 mA as input signal frequency and amplitude, respectively, under the magnetic field (*H*) sweep from −9 to 9 T using physical property measurement system.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article and its supplementary materials.

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AUTHOR CONTRIBUTIONS

J.Y.L. conducted all the experiments and analysis; M.K., Y.Y., and T.K. supported the SKPM measurement; Y.J. and H.G.S. helped device fabrications; K.R.K., J.Y.M., and Y.J.C. helped Hall measurement; S.Y. helped with 3D figure scheme techniques; S.I. designed whole-device experiments.

ADDITIONAL INFORMATION

Supplementary information accompanies the paper on the *npj 2D Materials and Applications* website (https://doi.org/10.1038/s41699-018-0082-2).

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