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# Cross-field optoelectronic modulation via inter-coupled ferroelectricity in 2D $\text{In}_2\text{Se}_3$

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The ability to couple the in-plane (IP) and out-of-plane (OOP) dipole polarizations in ferroelectric  $\text{In}_2\text{Se}_3$  makes it a promising material for multimodal memory and optoelectronic applications. Herein, we experimentally demonstrate the cross-field optoelectronic modulation in  $\text{In}_2\text{Se}_3$  based field-effect devices. Surface potential measurements of  $\text{In}_2\text{Se}_3$  based devices directly reveal the bidirectional dipole locking following high gate voltage pulses. The experimental evidence of hysteretic change in the IP electrical field facilitating a nonvolatile memory switch, was further explored by performing photocurrent measurements. Fabricated photodetectors presented multilevel photocurrent characteristics showing promise for nonvolatile memory and electro-optical applications.

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## INTRODUCTION

Since the successful isolation of graphene<sup>1</sup> and subsequent discovery of its exceptional mechanical, thermal, and electrical properties, substantial research interest has been enthroned on various two-dimensional (2D) materials<sup>2,3</sup> placing them in the forefront of modern science. Among the properties under scrutiny is room temperature ferroelectricity, due to its potential application in a wide range of fields such as nonvolatile phase change memory<sup>4,5</sup>, energy harvesting<sup>6</sup>, strain tuned electronics<sup>7</sup>, artificial brain<sup>8</sup>, neuromorphic sensors<sup>9</sup>, etc. Although the traditional ferroelectric materials, e.g.,  $\text{BaTiO}_3$ <sup>10</sup>,  $\text{BiFeO}_3$ <sup>11</sup>, and  $\text{PbTiO}_3$ <sup>12</sup> have been used for decades, the presence of surface dangling bonds, high leakage current in thinner form, and their complex fabrication process limit their potential integration for nanoelectronics. This emphasizes the need for 2D counterparts that are free from such constraints along with having superior ferroelectric properties to realize sub-10-nm ferroelectric devices, applicable for high-density storage and low power consumption. The list of 2D ferroelectric materials that were isolated so far includes 1T- $\text{MoS}_2$ <sup>13</sup>,  $(\text{M})_{\text{Mo}_2\text{WTe}_2}$ <sup>14,15</sup>,  $\text{CuInP}_2\text{S}_6$ <sup>16</sup>,  $\text{SnTe}$ <sup>17</sup>, and 2H  $\alpha\text{-In}_2\text{Se}_3$ <sup>18</sup>. Among these, 2H  $\alpha\text{-In}_2\text{Se}_3$  exhibits stable ferroelectricity at room temperature, which is essential for practical ferroelectric-based devices<sup>19</sup>. Although the current levels in typical  $\text{In}_2\text{Se}_3$  based electronic devices are relatively low ( $\sim\text{nA}$ ), recently  $\text{In}_2\text{Se}_3$  based electronic devices have utilized ferroelectric effect to replicate neuromorphic devices by realizing artificial synapse<sup>20</sup>. Moreover, its predicted<sup>21</sup> stable intercoupled in-plane (IP) and out-of-plane (OOP) ferroelectricity paves the way for controlling the device functionality in nonconventional ways.  $\alpha\text{-In}_2\text{Se}_3$  is a III–VI compound semiconductor comprising of five atomic layers of Se–In–Se–In–Se with a direct bandgap of  $\sim 1.4\text{ eV}$ <sup>22</sup>, making it a prime candidate for low-power electronics. Among all the polytypes of  $\text{In}_2\text{Se}_3$  ( $\alpha$ ,  $\beta$ ,  $\gamma$ ,  $\delta$ , and  $\kappa$ ), the  $\alpha$ -phase is recognized to have the most stable crystal structure at room temperature along with prominent ferroelectricity<sup>23</sup>. The emergence of the ferroelectricity in  $\alpha$ -phase arises from the different interatomic layer spacing between the central Se layer and the adjacent In layers resulting in the centrosymmetry breaking<sup>21</sup>. Recently,

researchers have reported experimental evidence of both IP<sup>24</sup> and OOP<sup>18</sup> ferroelectricity in  $\alpha\text{-In}_2\text{Se}_3$  using piezoelectric force microscopy (PFM). Although the existence of intercoupled IP and OOP ferroelectricity has been reported by few groups<sup>25,26</sup> for  $\alpha\text{-In}_2\text{Se}_3$  nanoflakes, many open questions regarding the nature of the dipole switching, dipole locking after removal of an external field, and their influence in modulating the optoelectronic properties in this material still remain unanswered.

Recently, Kelvin probe force microscopy (KPFM) has come to the forefront for 2D materials characterization and has been widely used to accurately determine mobility<sup>27</sup>, dopant distribution<sup>28–30</sup>, evaluation of charge carrier distribution<sup>31</sup>, etc. Several groups have used KPFM to resolve pinch-off formation<sup>32</sup> and determine potential profiles across semiconductor channels in field-effect transistors (FETs)<sup>27,33</sup>. Its capability to probe the local surface potential and to provide quantitative information about the remnant polarization in ferroelectric thin films<sup>34,35</sup> open the door towards the exploration of intercoupled ferroelectric behavior in 2D semiconductors.

In this study, we demonstrate the cross-field optoelectronic modulation of ferroelectric  $\text{In}_2\text{Se}_3$  based FET devices. IP variations of the electric field along the device channel were realized by gate electrode actuation of the OOP electric field at room temperature. Our observations based on detailed surface potential measurements using KPFM shed light on the dynamics of the intercoupled dipole modulation. Moreover, at higher OOP field strengths, the modulated dipoles maintained the state even after the withdrawal of bias voltage, essentially leading to dipole locking. Nonvolatile multilevel photoresponse of  $\alpha\text{-In}_2\text{Se}_3$  based phototransistors was demonstrated following different withdrawn gate voltages, which correspond to different OOP fields. Remarkably, the photocurrent showed significant modulation ranging from  $19.38 \pm 0.32\text{ nA}$  for an unpoled device to that of  $10.84 \pm 0.31$  and  $28.15 \pm 0.62\text{ nA}$  for poled devices (negative and positive gate pulses, respectively). The herein presented electronic dipole coupling and its modulation can be utilized to fabricate functional multimodal memory devices based on FET architectures with far-reaching potential for logic, memory, and optoelectronic applications.

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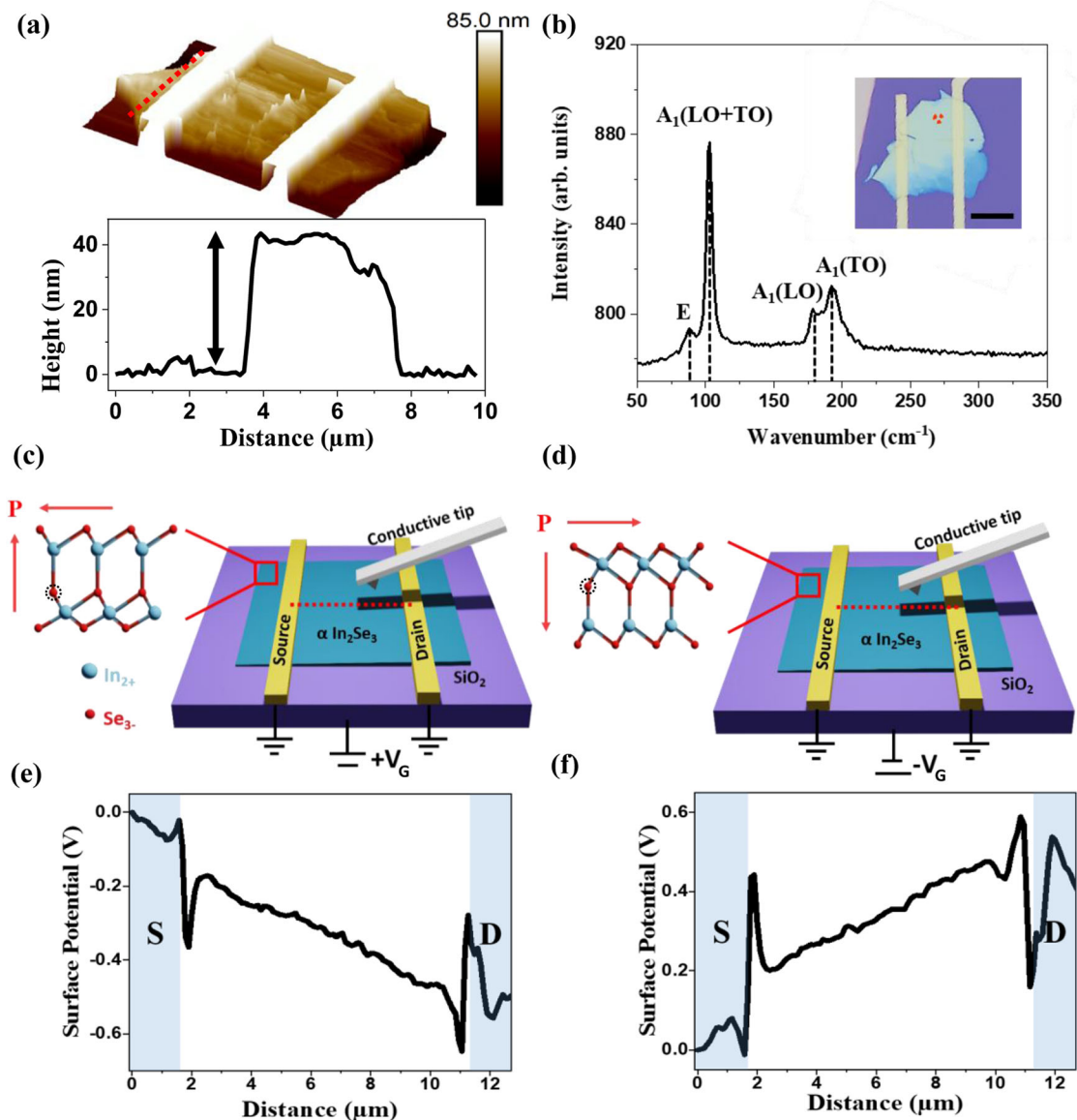
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## RESULTS AND DISCUSSIONS

### Material characterization

Few layers of  $\text{In}_2\text{Se}_3$  flakes were exfoliated onto a conductive-Si wafer covered by 300 nm thermal oxide (Supplementary Fig. 1). Figure 1a shows the AFM topography of a typical flake comprising a height of  $\sim 40$  nm and lateral dimensions of  $\sim 10$   $\mu\text{m}$  (inset of Fig. 1b). Additional AFM topography images for other measured flakes (Supplementary Fig. 2a, b) in addition to optical images (Supplementary Fig. 2c) and Raman maps (Supplementary Fig. 2d–f) show no significant unevenness or contamination on the surface. Figure 1b presents the Raman spectrum of the  $\text{In}_2\text{Se}_3$  flake exhibiting prominent peaks at 89, 104, 178, and 192  $\text{cm}^{-1}$ , which are the signature peaks for the  $\alpha$  phase<sup>26,36,37</sup>. The characteristic peak at 104  $\text{cm}^{-1}$  can be attributed to  $A_1(\text{LO} + \text{TO})$  phonon modes and the peaks at 178 and 192  $\text{cm}^{-1}$  can be attributed to  $A_1(\text{LO})$

and  $A_1(\text{TO})$  phonon modes, respectively. In addition, the peak at 89  $\text{cm}^{-1}$  confirms it to be 2H  $\alpha\text{-In}_2\text{Se}_3$  with hexagonal symmetry<sup>38</sup>. The presence of the  $A_1(\text{LO})$  and  $A_1(\text{TO})$  modes at 178 and 192  $\text{cm}^{-1}$  caused by the LO–TO splitting indicates a lack of inversion symmetry in the structure, thus proving the material to be ferroelectric. The emergence of the intercoupled IP and OOP polarizations<sup>25</sup> is a consequence of the lack of centrosymmetry in the quintuple layered van der Waals structure. Insets in Fig. 1c, d show the 2D structure of  $\alpha\text{-In}_2\text{Se}_3$  crystal arrangement with In atom as blue circles and Se atom as red circles. The relative displacement of the central Se atom, marked by a dotted black circle, with respect to the In atoms, breaks the centrosymmetry providing two energetically degenerate states with opposite OOP electric polarization and IP asymmetry with reverse second-order nonlinear polarization<sup>39</sup>.

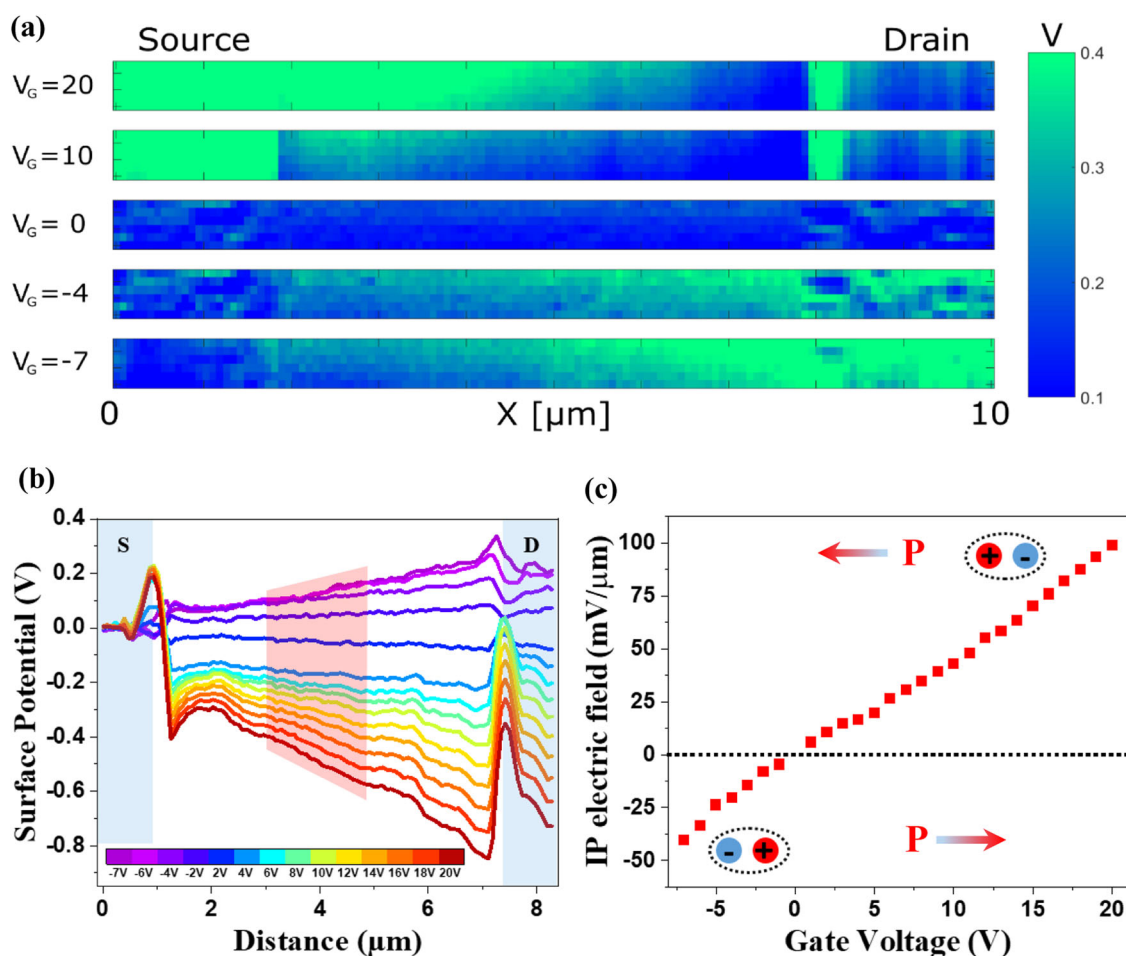


**Fig. 1** Characterization of  $\alpha\text{-In}_2\text{Se}_3$  based field-effect transistors. **a** top—AFM topography of  $\alpha\text{-In}_2\text{Se}_3$  flake on a Si/SiO<sub>2</sub> substrate with Cr/Au electrodes deposited by e-beam lithography, bottom—Height profile of the flake along the red dotted line shows the height to be  $\sim 40$  nm, **b** Raman spectra of  $\alpha\text{-In}_2\text{Se}_3$  flake with prominent peaks at 89, 104, 178, and 192  $\text{cm}^{-1}$ ; inset shows the optical image of the flake and the red dot denotes the point of the Raman measurement. Scale bar is 10  $\mu\text{m}$ . Schematic of the KPFM experimental setup for positive (**c**) and negative (**d**) applied back gate voltage bias with source and drain grounded. The insets illustrate the respective crystal structures for the alternating bias conditions with intercoupled IP and OOP polarizations in the sample (the directions of which are marked by the red arrows). Measured surface potential along the  $\alpha\text{-In}_2\text{Se}_3$  channel for (**e**) positive and (**f**) negative applied gate bias.

## Surface potential properties of electronically polarized $\alpha$ - $\text{In}_2\text{Se}_3$

For device testing, back gated FETs were fabricated based on exfoliated  $\alpha$ - $\text{In}_2\text{Se}_3$  flakes on  $\text{SiO}_2/\text{Si}$  substrate (see Methods). The surface potential measurement of an individual FET device, marked as D1, is schematically shown in Fig. 1c, d. Figure 1e, f present the measured surface potential across the device channel for positive and negative gate polarities, respectively. Both source and drain contacts were grounded throughout the measurement. The nonequivalence of the drain potentials in the figure can be attributed to a convolution effect<sup>33</sup> that the metal electrode of  $\sim 1\ \mu\text{m}$  in width footprint encounters. Such a strong effect was previously demonstrated for silicon nanowire-based field-effect devices<sup>31,33</sup>. Thus, even though the real drain potential should be similar to the source electrode, its measured potential eventually increases. In addition, the metal contact height  $\sim 50\ \text{nm}$ , can potentially result in an incomplete screening of the potential below the electrodes<sup>40</sup> which might strongly arise due to induced dipoles below the metal. The distinct alternating slopes of the surface potential manifest the modulation of the IP dipoles as a result of different polarities of the OOP gate-induced electrical fields<sup>35,41</sup>. Figure 2a, b present the surface potential distributions of  $\alpha$ - $\text{In}_2\text{Se}_3$  FET marked as D2 for various selected applied back gate voltages and the individual cross-sectional potential profiles

across the device channel, respectively. We note that the potential variations across the channel for different applied gate potentials in Fig. 2a are vertically shifted to fall within the range of 0.1–0.4 V for better visualization. The corresponding electric fields across the device channel  $E(x)$  are extracted by taking the potential slope  $\frac{d(\text{Surface Potential})}{dx}$  for each back-gate voltage, where  $x$  is the distance along the semiconductor channel (Fig. 2c). The observed potential variations at the metal-semiconductor interface are attributed to the Schottky barrier formation at the interface<sup>27</sup>. Due to the distinct Schottky barrier at the metal-semiconductor interface, only the surface potential away from the junctions (marked with a semitransparent red box in Fig. 2b) is taken into consideration to have an accurate estimation of the electric field in the channel independent of the effect of metal contacts. We note, that while for most measured devices the potential across the channel was virtually zero for zero applied back-gate voltage, few devices showed an asymmetric potential dependence with an initial nonzero potential slope. The emergence of a distinct slope of the surface potential due to variable OOP gate voltages is indicative of an induced electric field in the IP direction. We observed a gradual increase in  $E(x)$  arising from the increasing OOP applied bias, which eventually modulates the IP dipoles. For an ideal monolayer system, when a positive (negative) voltage is applied on the gate, the central Se atoms in the van der Waals structure are attracted

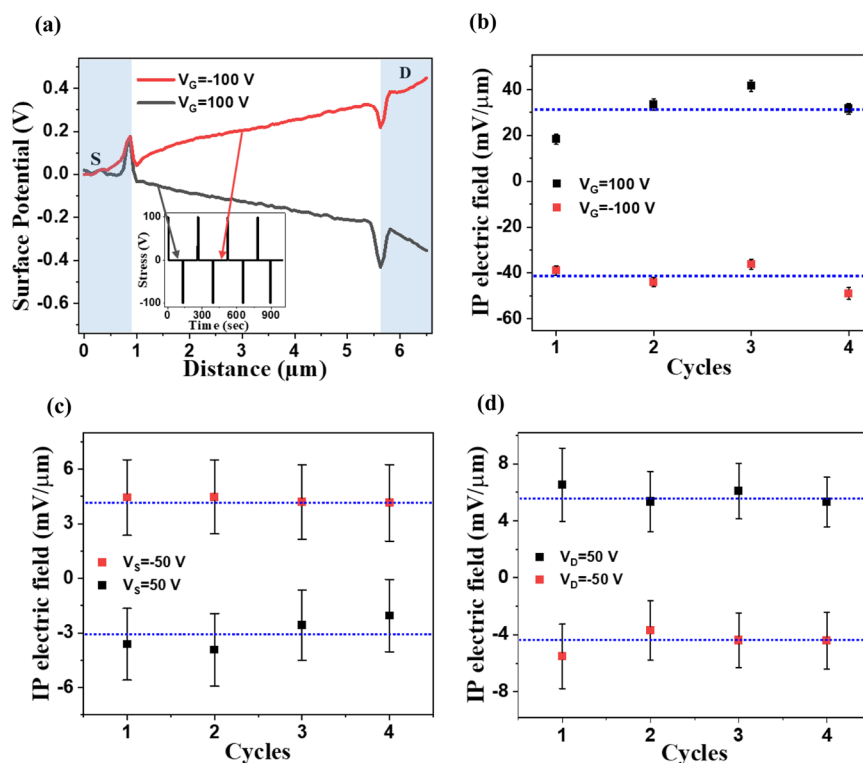


**Fig. 2** Surface potential and electric field distribution across the operating device. **a** Surface potential maps across the  $\alpha$ - $\text{In}_2\text{Se}_3$  channel for different gate bias conditions. **b** Surface potential profiles across the channel for various gate biases ranging from  $V_G = -7\ \text{V}$  to  $V_G = 20\ \text{V}$ . The semi-transparent blue boxes indicate the source and the drain positions. **c** Effective IP electric field calculated from a section of the line profiles away from electrodes (marked by semi-transparent red quadrilateral) in Fig. 2b as a function of applied gate voltage. The orientation of the electric field is attributed to the orientation of the IP dipoles (indicated by the inset images).

(repelled) towards the bottom (top) In atom, leading to the crystal configuration in the inset of Fig. 1c, (d). This creates a net dipole in the system with effective negative (positive) charges accumulating near the interface of  $\alpha$ -In<sub>2</sub>Se<sub>3</sub>/SiO<sub>2</sub> and results in an OOP dipole polarization, the directions of which are exhibited in the inset of Fig. 1c, (d). Due to the intercoupled IP and OOP dipoles nature<sup>25</sup>, the IP dipoles are also reconfigured (Supplementary Fig. 3). Although our system contains tens of layers, the same phenomenon stands true for all individual layers giving rise to similar modifications generating a significant net dipole moment.

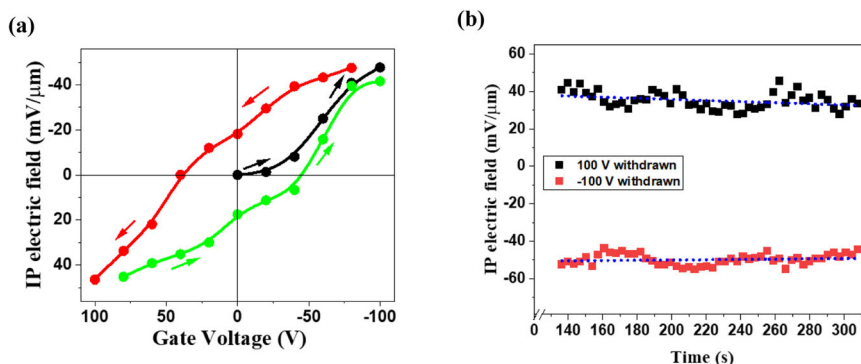
In order to establish a framework for the interpretation of the experimental results and to relate it to polarization, TCAD Sentaurus modeling has been used to solve the potential variations as a consequence of the induced polarization in the In<sub>2</sub>Se<sub>3</sub> field-effect device. The model (details in supplementary) is based on transforming the strain-field distribution of  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> to polarization as a function of the applied field on the basis of the symmetry group of  $\alpha$ -In<sub>2</sub>Se<sub>3</sub>, which has an important role on the intercoupling piezoelectric response. The intercorrelation between IP and OOP polarization under different applied back gate potentials and the corresponding surface potential across the In<sub>2</sub>Se<sub>3</sub> channel has been simulated for different piezoelectric coefficient values of  $e_{13}$  and  $e_{33}$ , all of which are shown in Supplementary Fig. 12. The simulated surface potentials are in excellent agreement with our experimental results. To test the bidirectional hysteretic modulation and repeatability of the phenomenon, surface potentials following high gate pulses of alternating polarities were measured in another  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> FET marked as D3. Figure 3a shows two potential profiles measured at zero gate voltage following  $V_G = 100$  V and  $V_G = -100$  V pulses

marked with gray and red colors, respectively. Due to experimental limitations, surface potentials at live gate voltages were limited to  $\sim \pm 20$  V. Repeated switching of the gate bias demonstrated the repeatability of the induced electric fields across the device (Fig. 3b). The average IP field strength following applied gate bias of  $+100$  V was found to be  $\sim 32$  mV/ $\mu$ m, while that for  $-100$  V gate bias was  $\sim -42$  mV/ $\mu$ m (dotted blue lines mark the average field). The consistent IP field modulation profoundly establishes both bidirectionality and repeatability of the dipoles switching using applied gate bias and is attributed to polarization locking imposed by the unique covalent bond configuration of  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> crystal<sup>39</sup>. Most studied ferroelectrics usually show very low ionic conductivity at room temperature<sup>42</sup>, however, the observed IP dipole locking rules out any contribution of ionic conductivity in  $\alpha$ -In<sub>2</sub>Se<sub>3</sub><sup>43</sup>. Therefore, the observed cross-field electronic switching can be attributed to the intercoupled polarizability of  $\alpha$ -In<sub>2</sub>Se<sub>3</sub>. To support our study, PFM measurements were performed on both pristine and field-effect devices based on In<sub>2</sub>Se<sub>3</sub> to demonstrate the polarization change as a consequence of the applied gate potential (Supplementary Figs. 8 and 9). To study the dipole variations as a function of applied IP electrical field, a voltage was applied to the source and drain electrodes one at a time respectively, while keeping the back-gate contact grounded. Figure 3c, d show the induced IP electrical field measured at zero source-drain voltage after the removal of a bias voltage of  $+50$  V (black squares) and  $-50$  V (red squares), at the source and the drain electrodes, respectively. It is evident from the figures that although an IP field is induced in the material, its magnitude is lower compared to the values for OOP applied voltages. This can be attributed to the significantly stronger IP polarization in  $\alpha$ -



**Fig. 3 Bidirectional switching of the IP field.** **a** Potential profiles across  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> channel following withdrawn  $+100$  V (gray) and  $-100$  V (red) gate potential. Inset shows the pulse profile of the applied electrical bias, with the arrows denoting the point of measurement after withdrawal of pulse (pulse duration was 6 s). **b** Extracted IP electric field across the channel following four cycles of applying alternating gate bias of  $+100$  V (black squares) and  $-100$  V (red squares). **c** Extracted IP electric field across the channel following four cycles of applying a bias of  $+50$  V (black squares) and  $-50$  V (red squares) on the left electrode (Source) with all other terminals grounded. **d** Extracted IP electric field across the channel following four cycles of applying a bias of  $+50$  V (black squares) and  $-50$  V (red squares) on the right electrode (Drain) with all other terminals grounded. Error bars comprise the standard deviation (STD) analyzed from the full measured profile.





**Fig. 4 Polarization hysteresis.** **a** IP electric field across the  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> channel as a function of withdrawn gate voltage. The connected black dots denote electric fields for withdrawn gate voltage from 0 to  $-100$  V, the connected red dots denote electric fields for withdrawn gate voltage from  $-80$  to  $100$  V and the connected green dots indicate electric fields for withdrawn gate voltage from  $80$  to  $-100$  V. The direction of the arrows indicates the direction of progression of the scan. **b** Temporal remanence of the IP electric field after the withdrawal of gate bias. The dotted blue lines show the general trend of the evolution of the electric field with time.

In<sub>2</sub>Se<sub>3</sub> with respect to its OOP polarization<sup>25</sup>. Moreover, the IP field due to a lateral bias ( $V_{DS}$ ) is spread out across the  $\sim \mu\text{m}$  length of the semiconductor, whereas, for the OOP direction, the bias potential ( $V_G$ ) falls across the height of the In<sub>2</sub>Se<sub>3</sub> flake, which is typically  $\sim 50$  nm for our experiments. Since, we apply a similar range of bias voltages for both the gate and drain terminals, the effective electric field in IP and OOP directions is effectively different. The opposite trends of the IP lateral electric fields for bias on each electrode rules out any instrument-based error of the measured surface potential.

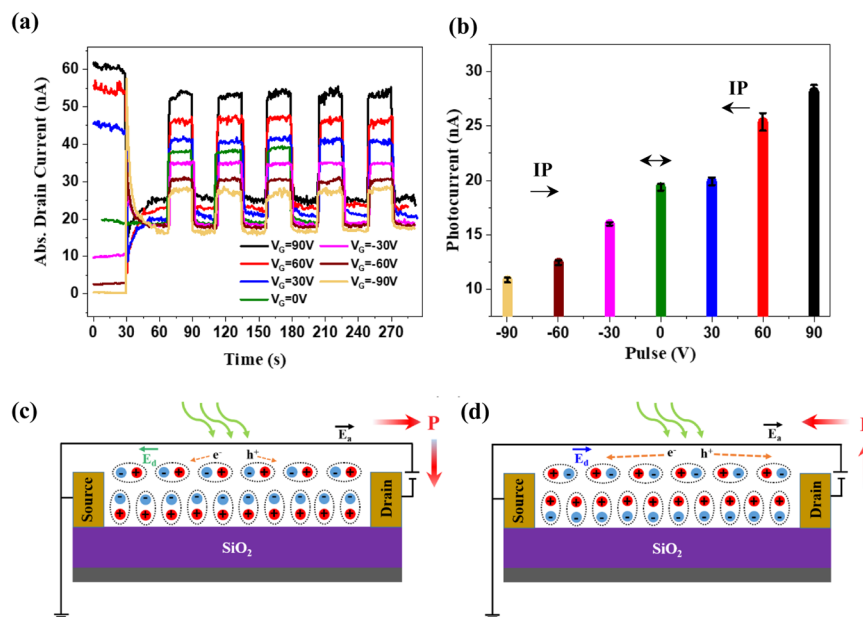
To further understand the hysteretic nature of the gate induced dipole modulation, the IP electric field across the channel in a device marked as D4 was measured as a function of withdrawn gate voltage cyclically from 0 to  $-100$  V (connected black dots),  $-80$  to  $100$  V (connected red dots), and  $80$  to  $-100$  V (connected green dots) (Fig. 4a). The results clearly indicate a significant hysteresis effect following higher withdrawn gate voltages. The hysteresis of the IP field generated by varying the gate strongly adheres to the phenomenon of ferroelectricity<sup>44</sup>. For lower gate pulses, the dipoles did present IP modulation but relaxed upon withdrawal of the gate bias (Supplementary Fig. 4). Figure 4b shows the temporal variations of the IP field after the withdrawal of gate bias of  $+100$  V (black squares) and  $-100$  V (red squares); the blue dotted lines act as a guide to the eye to display the average trend of the evolution of the IP field with time. It is evident from the figure that the remanence of induced electric fields following the withdrawal of gate voltage for both polarities remain almost constant during the test. In addition, to verify the OOP ferroelectric property, surface potential values after withdrawal of different gate voltages were measured and the results are shown in Supplementary Fig. 7. The hysteretic nature of the resultant plot is indicative of the remnant OOP ferroelectric polarization in the material.

### Electronic transport and photoresponse

Following the KPFM measurements, the electrical transport characteristics were examined for the fabricated FET. The output characteristics of the fabricated back-gated FET under dark and illumination are shown in Supplementary Fig. 5a. The output characteristics for varying gate voltages are shown in the supplementary section (Supplementary Fig. 5b). The transfer characteristics of the same device when subjected to different gate sweep voltages show a clockwise hysteresis. Similar clockwise hysteresis has been reported<sup>45</sup> as a manifestation of dipole switching in ferroelectric semiconductor field-effect transistors. Interestingly, the hysteresis visibly increases with a greater gate

sweep range as can be seen in Supplementary Fig. 5c, which is commensurate with our findings from Kelvin probe measurements. The fact that  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> exhibits both semiconducting and insulating ferroelectric properties simultaneously, have already been shown before, which is supported by I-V from one side and surface probe measurements from the other side<sup>19,26,46</sup>. A possible reason for this could be that the I-V, which acts as an indication to its *n*-type semiconducting nature is affected significantly by the charge accumulation at the interface between the SiO<sub>2</sub> dielectric and the  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> channel, whereas, scanning probe measurements are conducted away from this interface i.e., on the surface of the  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> which is more insulating.

Next, we employ the gate-based electronic control over the IP and OOP to modulate the photoelectrical characteristics of  $\alpha$ -In<sub>2</sub>Se<sub>3</sub>. Photoresponse of the fabricated FET was measured immediately after withdrawal of various gate biases ranging from  $+90$  V to  $-90$  V with an interval of  $30$  V. Figure 5a shows the current through the FET with and without white light illumination (details in the Methods section) before and after withdrawal of various gate voltages. A distinct change in photocurrent was observed following negative and positive gate pulses (Fig. 5b). The photocurrent gradually increases (decreases) for positive (negative) gate pulses due to partial modulation of dipoles. Schematic illustrations explaining the origin of the photoresponse modulations for different conditions following the withdrawal of gate bias are shown in Fig. 5c, d. Under illumination with energy higher than that of the bandgap, generated *e*-*h* pairs are separated by the applied drain voltage of  $-2$  V. For the  $0$  V gate bias condition under illumination, the applied potential across the channel leads to drift of the photogenerated electrons and holes towards opposite electrodes resulting in a net increase in the output current, which accounts for a photocurrent of  $19.38 \pm 0.32$  nA. For illumination following the withdrawal of high gate bias of  $+90$  V and  $-90$  V, as demonstrated previously, the dipoles are locked in a particular orientation with respect to the polarity of the applied bias depending on the intercoupling of the IP and OOP polarizations. Thus, following the withdrawal of  $+90$  V gate bias, IP dipoles line up such that they add an effective electric field between the source and drain electrodes. This facilitates an improved charge collection, resulting in a higher magnitude of photocurrent with respect to the dark current and accounts for a photocurrent of  $28.15 \pm 0.62$  nA. In contrary, for the scenario following the withdrawal of  $-90$  V gate bias, the dipoles align in such a way to reduce the effective field between the electrodes and result in a reduced photocurrent of  $10.84 \pm 0.31$  nA. The rise and fall times of the phototransistor are calculated and shown in



**Fig. 5 Photoresponse modulation.** **a** Temporal response of photocurrent in  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> for various gate pulses. Gate pulses were applied for 30 s after which the gate was withdrawn. The measurements were performed with zero applied gate potential and drain voltage of  $-2$  V thereafter. **b** Photocurrent as a function of the withdrawn gate voltage pulse. Error bars comprise the standard deviation (STD) for each current level measured over time of light exposure. **c, d** Schematic illustrations describing the origin for the variable photoresponsivity following the application of negative and positive gate bias, respectively.

Supplementary Fig. 6. Additionally, simulations of photocurrent variations following different gate pulses were carried out using TCAD Sentaurus, the results of which are shown in Supplementary Fig. 12. The change in photocurrent post withdrawal of different gate pulses is in accordance with the results achieved experimentally. Although the photocurrent modulation may be attributed to the photovoltaic effect, in particular since there is an effective field due to dipole modulation, our experiments do not exhibit any switch in the sign of photocurrent with the reversal of polarization as seen in other asymmetric systems<sup>47</sup>. Thus, the presence of a significant photovoltaic effect that can potentially influence the experiment can be ruled out.

In summary, we demonstrated the bidirectional cross-field electronic switching of IP and OOP dipole polarizations in  $\alpha$ -In<sub>2</sub>Se<sub>3</sub>. Surface potential and piezoelectric force measurements of  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> based FET devices directly reveal the dipole modulation and the bidirectional dipole locking following high gate voltages. Furthermore, multilevel photoresponse characteristics are effectively realized by the intrinsic IP field showing great promise for nonvolatile memory and electro-optical applications.

## METHODS

### Sample preparation

$\alpha$ -In<sub>2</sub>Se<sub>3</sub> crystals with 4–6 mm diameter (2D Semiconductors, 99.9999% purity) were used as the source material for mechanical exfoliation. The first few layers of the bulk crystal were mechanically cleaved to eradicate any native oxide layers on the surface. The pristine  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> bulk was consequently cleaved again to exfoliate flakes, which were then transferred onto a pre-patterned degenerately p-doped silicon substrate encapsulated with 300 nm Si oxide.

### Device fabrication

Standard e-beam lithography [Raith-eLine] followed by electron beam evaporation [Evatec BAK 501 A] were used to fabricate the contact electrodes of 5 nm of Cr and 50 nm of Au. Before metal deposition, the sample was subjected to a mild oxygen plasma [Low-Pressure Plasma

System—Diener PCCE] for  $\sim 5$  s to remove unwanted resist residues. The deposition rate was minimized to  $\sim 0.5$  Å/s for Cr and  $\sim 1$  Å/s for Au at the base pressure of  $\sim 7 \times 10^{-7}$  torr to facilitate proper adhesion.

### Surface and electrical characterization

Atomic force microscopy (AFM) was conducted to study topography and flake thickness in an N<sub>2</sub> filled glovebox (H<sub>2</sub>O and O<sub>2</sub> content <1 ppm) in tapping mode (Dimension-Scanassist, Bruker Inc.). KPFM was conducted in amplitude modulation (AM-KPFM) mode in a two-pass procedure, where surface topography was obtained by standard tapping mode AFM in the first pass followed by an interleaved surface potential measurement in the second pass in the same system. Conductive Pt/Ir-coated cantilever [PPP-EFM-50, NANOSensors™] with  $\sim 25$  nm tip radius was used for KPFM measurements. Prior to KPFM, the devices were mounted onto a chip carrier and wire bonded to a prototype PCB board. For the gate-dependent KPFM studies, bias was applied (Keysight B1500A) through back-side conducting ( $p^{++}$ ) Si and the 300-nm-thick SiO<sub>2</sub> layer served as the gate dielectric. PFM measurements were conducted on Dimension-Scanassist, Bruker Inc. system in near-contact resonance mode (frequency of  $\sim 400$  kHz) with conductive Pt/Ir-coated cantilever [PPP-EFM-50, NANOSensors™] tips. For mapping of pristine  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> flakes were exfoliated onto a conducting substrate (5 nm Cr/50 nm Au on Si/SiO<sub>2</sub>) to eliminate electrical charging effects. For mapping devices, the chips were mounted onto a prototype PCB board similar to the process mentioned for KPFM. The electrical measurements of FET devices were carried out using a semiconductor parameter analyzer (Keysight B1500A) and a probe station equipped with an optical microscope. Photoresponse measurements were carried out by illumination with a broadband white light source of spectral range 420–720 nm and an intensity of  $\sim 332$   $\mu$ W/cm<sup>2</sup>.

### Spectroscopic characterization

Raman spectroscopy was used to characterize the flakes and identify the phase of the material. The spectra were recorded using a WITec Alpha300R Raman Microscope in confocal mode comprising of 532 nm laser. A 100x objective (NA = 0.9;  $\Delta\lambda \sim 360$  nm) was used to focus the laser beam, while keeping the laser power typically at  $\sim 1$  mW to avoid degradation of the material.

## Sentaurus modeling

Sentaurus TCAD, which is a general-purpose finite element numerical device simulation tool, was used to simulate the surface potential and the corresponding photoresponse variations as a consequence of the induced polarization in the  $\text{In}_2\text{Se}_3$  field-effect device across the semiconductor channel.

## DATA AVAILABILITY

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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## AUTHOR CONTRIBUTIONS

D.D. performed the experimental work, S.M. provided experimental support, M.U. performed numerical modeling, E.K. supervised the work. All authors participated in manuscript writing.

## COMPETING INTERESTS

The authors declare no competing interests.

## ADDITIONAL INFORMATION

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