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Growth of high-quality semiconducting tellurium films for high-performance p-channel field-effect transistors with wafer-scale uniformity

Taikyu Kim[1], Cheol Hee Choi[1], Pilgyu Byeon[2], Miso Lee[3], Aeran Song[4], Kwun-Bum Chung[4], Seungwu Han[3], Sung-Yoon Chung[2], Kwon-Shik Park[5] and Jae Kyeong Jeong[1]✉

Achieving high-performance p-type semiconductors has been considered one of the most challenging tasks for three-dimensional vertically integrated nanoelectronics. Although many candidates have been presented to date, the facile and scalable realization of high-mobility p-channel field-effect transistors (FETs) is still elusive. Here, we report a high-performance p-channel tellurium (Te) FET fabricated through physical vapor deposition at room temperature. A growth route involving Te deposition by sputtering, oxidation and subsequent reduction to an elemental Te film through alumina encapsulation allows the resulting p-channel FET to exhibit a high field-effect mobility of 30.9 $cm^2 V^{-1} s^{-1}$ and an $I_{ON/OFF}$ ratio of 5.8×10^5 with 4-inch wafer-scale integrity on a SiO_2/Si substrate. Complementary metal-oxide semiconductor (CMOS) inverters using In-Ga-Zn-O and 4-nm-thick Te channels show a remarkably high gain of ~75.2 and great noise margins at small supply voltage of 3 V. We believe that this low-cost and high-performance Te layer can pave the way for future CMOS technology enabling monolithic three-dimensional integration.

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INTRODUCTION

The classical two-dimensional (2D) downscaling of Si semiconductors on the basis of Dennard's design principle is reaching the fundamental physical limits. Geometrical scaling has been replaced by equivalent scaling since 2000, where advances, such as strained Si/SiGe, high-κ/metal-gate stacks and fin field-effect transistor (FET) structures, continue to meet the stringent scaling rule represented by Moore's law. The ever-increasing demands on the performance, power consumption and bandwidth of electronic systems now call for monolithic three-dimensional (M3D) integration as a promising pathway to extend the semiconductor roadmap beyond complementary metal oxide semiconductor (CMOS) technology[1]. The direct vertical integration of data storage and computing devices on a single chip enables ground-breaking improvements in terms of speed, power and performance[2]. However, the constraint of a low-temperature process (≤300 °C) must be considered to realize versatile M3D heterogeneous systems because the performance of underlying CMOS logic devices is seriously degraded by a conventional high-temperature process such as epitaxy, doping and activation.

An amorphous indium-gallium-zinc oxide can be a promising alternative for the channel layer of the upper layer transistor because of its low-temperature processability, reasonable mobility, good uniformity and extremely low leakage current characteristics[3]. Indeed, the application of IGZO to large-scale integration devices, including static random access memory, dynamic random access memory, central processing units, and CMOS image sensors, has been investigated[4]. However, n-channel IGZO FETs have been limited to the niche application of low power/frequency electronics, such as display technology, due to the lack of p-type dopability arising from the strong oxygen *2p* orbital localization. Without a p-type inversion layer and a controllable p-type doping mechanism, these accumulation-mode transistors fail to exhibit the scalability and energy efficiency of traditional CMOS devices. Therefore, p-channel inorganic transistors with low-temperature processability remain a fundamental and technological challenge.

2D materials, such as graphene, transition metal dichalcogenides, and black phosphorous, have been widely studied for use as a channel layer in next-generation nanoelectronics owing to their dangling bond-free nature, single nanometer thickness and superb mobility[5–14]. However, their fabrication method, such as chemical vapor deposition or exfoliation, requires a high growth temperature (~900 °C) for high-quality films and/or poses challenges in achieving thickness uniformity over a large area[11–14], hampering their application in M3D-based integrated circuits. Recently, group VI tellurium (Te), another fascinating 2D material, has been intensively studied owing to its low-temperature processability as well as several promising characteristics including the semiconducting, piezoelectric, photoconductive, and thermoelectric characteristics, etc.[15–26]. Te atoms are covalently bonded with the two nearest atoms, leading to one-dimensional (1D) helical chains along [001] direction. Each 1D helical chain is bonded by the van der Waals interaction, which forms hexagonal crystal arrays. The FETs using the hexagonal Te film showed the extremely promising device performances including the very high hole mobility and great immunity to the air exposure, etc.[15,16], which attracted the broad attention to implement the high-performance p-channel FET applications[17–24]. However, a simple and scalable route compatible with Si CMOS technology is still elusive because these materials were synthesized through a complicated solution process or evaporation requiring cryogenic

[1]Department of Electronic Engineering, Hanyang University, Seoul 04763, Republic of Korea. [2]Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology, Daejeon 34141, Republic of Korea. [3]Department of Materials Science and Engineering and Research Institute of Advanced Materials, Seoul National University, Seoul 08826, Republic of Korea. [4]Division of Physics and Semiconductor Science, Dongguk University, Seoul 04620, Republic of Korea. [5]R&D Center, LG Display Company, Paju-Si, Gyeonggi-Do 413-791, Republic of Korea. ✉email: jkjeong1@hanyang.ac.kr

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temperature (−80 °C) to enlarge grain sizes in most of the previous studies[16–23].

Here, we report a cost-effective and mass-production method involving an encapsulation layer to fabricate wafer-scale high-performance p-type ultrathin hexagonal tellurium (Te) films at a low temperature of 150 °C. An alumina (Al_2O_3) encapsulation layer significantly assists the growth of the underlying hexagonal Te crystal through interfacial energy stabilization and enlarges the crystal size in the sputtered Te film, leading to a very large enhancement in the performance of FETs. The resulting CMOS inverter based on this encapsulated p-channel crystalline Te and an n-channel IGZO layer exhibits great rail-to-rail swing with high gain and noise margins.

RESULTS

Te film characterization

The hexagonal crystalline structure was confirmed by X-ray diffraction (XRD) analysis of polycrystalline Te films deposited by magnetron sputtering at room temperature (see "Methods", Supplementary Figs. 5 and 6). The hexagonal structure is maintained in the Te films with increasing post-deposition annealing (PDA) temperature (T_A) up to 250 °C. However, the crystalline structure abruptly changes to orthorhombic TeO_2 at 300 °C (Supplementary Figs. 5 and 6). Partial volatilization of elemental Te occurs near 250 °C because of its high vapor pressure[22,27] and becomes severe at 300 °C, where the silicon signal from the substrate is detected in some areas of the Te film ($T_A = 300$ °C) by X-ray photoelectron spectroscopy (XPS) (Supplementary Fig. 7). It also causes an abrupt increase in surface roughness from 0.19 to 1.48 nm (root-mean-square value), rendering the roughness of these unstable films easily seen with the naked eye (Supplementary Fig. 8). The evolution of the crystal domains with T_A was observed through polarized light microscopy (PLM) (Fig. 1a, b). While the crystal domains are not discernible in the as-sputtered films, their enlargement is clearly observed for the films annealed at 150 °C. To further examine the nanoscale difference in the crystalline structure at different T_A, the cross-sections of the as-deposited and 150 °C-annealed Te films were compared by high-resolution transmission electron microscopy (HRTEM) (Fig. 1d, e). Although both films have several hexagonal Te crystal domains, the overall crystallinity is enhanced at 150 °C. Additionally, some portions of the amorphous phase consist of tellurium suboxide (TeO) and/or tellurium dioxide (TeO_2) in both films (Supplementary Fig. 9). Encapsulation of the oxygen-containing Te film with Al_2O_3 is a quite important process (see "Methods"). During the growth of Al_2O_3 by atomic layer deposition (ALD), both the crystallinity and crystal size of the hexagonal Te layer are considerably improved compared to those without the encapsulation layer (Fig. 1c, f). In addition, the amorphous TeO and TeO_2 phases observed in the films without the encapsulation layer completely disappear in the encapsulated Te film (Supplementary Fig. 10), which will be discussed later. This enhanced crystal growth of the Te film can be explained from the viewpoint of interfacial energy stabilization through encapsulation (see Supplementary Note 1 and Supplementary Fig. 1)[28].

The chemical states of the Te films depending on T_A were examined by XPS (Supplementary Figs. 11 and 12). The neutral Te (Te^0) state is gradually converted to the Te^{4+} state with increasing T_A, indicating oxidation to TeO_2 during the PDA (Supplementary Fig. 12). Above $T_A > 150$ °C, the dominant chemical state in the Te film changes from the Te^0 state to the Te^{4+} state, leading to the almost complete disappearance of the Te^0 state (~3.6%) at 300 °C. The predominance of the Te^{4+} state with increasing T_A suggests the enhanced formation of TeO_2, which is consistent with the evolution of the crystalline structure seen in the XRD results. As mentioned earlier, the Te^{4+} state in the Te film disappears after the encapsulation of the 150 °C-annealed Te film with Al_2O_3 film (Fig. 2a). This deoxidization progresses during the growth of Al_2O_3 by the ALD method, where trimethylaluminum (TMA) as an Al precursor may act as a strong reducing agent to remove the oxygen in the underlying Te film[29]. As an alternative explanation, the Gibbs formation energy for Al_2O_3 is far lower than that for TeO_2[30], suggesting conversion from a mixture of Te and TeO_2 to homogeneous polycrystalline Te.

The effect of T_A on the optical characteristics of the Te film was investigated through UV/visible spectroscopy. The optical transmittance of the Te film increases with T_A (Supplementary Figs. 13 and 14), where the average transmittance in the visible range (400–700 nm) increases from 58.8% (as-sputtered film) to 98.7 % (300 °C-annealed film). Simultaneously, this increase is accompanied by a decrease in the absorbance (Supplementary Fig. 13). Note that the absorption peak at approximately 2.2 eV completely disappears at 300 °C, which is the intrinsic absorption peak of Te assignable to the transition from the valence band of the lone pair p-orbital to the conduction band of the antibonding p-orbital[31–33]. This is corroborated by the disappearance of the Te^0 state at 300 °C, as discussed regarding the XPS data. The optical bandgap (E_g^{opt}) values were extracted by extrapolating the best fit line in the plot of $(ahv)^{1/2}$ versus hv to the intercept (at $a = 0$) (Supplementary Fig. 13), showing a monotonic increase in E_g^{opt} from 0.9 eV (as-sputtered film) to 1.6 eV (250 °C-annealed film) due to the increased portion of oxidized states of Te in the films. The E_g^{opt} value of the as-sputtered film is similar to a previous calculation and experimental studies[16,34]. Additionally, the extracted E_g^{opt} (2.7 eV) of the film annealed at 300 °C is consistent with the identification of TeO_2[35].

The phonon structure and wafer-scale uniformity of the Te films depending on T_A were characterized by Raman spectra. Three primary Raman modes of E_1 (103 cm^{-1}), A_1 (129 cm^{-1}), and E_2 (145 cm^{-1}) can be assigned to a-axis rotation, chain expansion in the basal plane and asymmetric stretching along the c-axis (Fig. 2b), respectively, which agrees with previous studies (Supplementary Fig. 15)[16,36–39]. While the effect of T_A on the Raman shift for the given modes is negligible up to 200 °C, all the phonon vibrations are significantly suppressed at 250 °C, with their complete disappearance at 300 °C. The decreased Raman intensity ($T_A \geq 250$ °C) can be attributed to the predominance of the Te^{4+} state in the film (Supplementary Fig. 11). Note that the Raman scattering is significantly enhanced through encapsulation (Fig. 2c), which comes from the improved crystallinity[40,41]. In addition, a redshift in the Raman spectra occurs after encapsulation. This may originate from the tensile strain on the polycrystalline Te film due to the thermal expansion coefficient (TEC) difference because the TEC of Al_2O_3 is smaller than that of Te[38,42,43]. The tensile strain elongates the Te–Te bond length, which attenuates the interatomic interactions and thus causes a redshift in the vibration frequency of the E_2 modes[38]. Furthermore, the equilateral triangle projection of the Te chain in the basal plane is reduced under tensile strain, indicated by the decrease in the frequency of the A_1 modes[38]. It is interesting to note that the E_g^{opt} value of 150 °C-annealed Te film with the encapsulation layer was slightly reduced from ~0.94 eV (for the 150 °C-annealed Te film without the encapsulation layer) to ~0.89 eV (see Supplementary Fig. 16). It can be partially originated for the reduction process by the TMA adsorption during the deposition of Al_2O_3 on top of the Te film, as confirmed in the XPS result. Tensile strain-induced bandgap lowering effect, however, cannot be excluded as the origin for the redshift of the 150 °C-annealed film with the encapsulation layer compared to the encapsulation-free Te film as shown in Raman data. To evaluate the uniformity of the as-sputtered film, moreover, the Raman spectra were also observed for 16 locations of the sputtered film on the 4-inch wafer, showing great uniformity without any red/blueshift of the primary peaks (Supplementary Fig. 17).

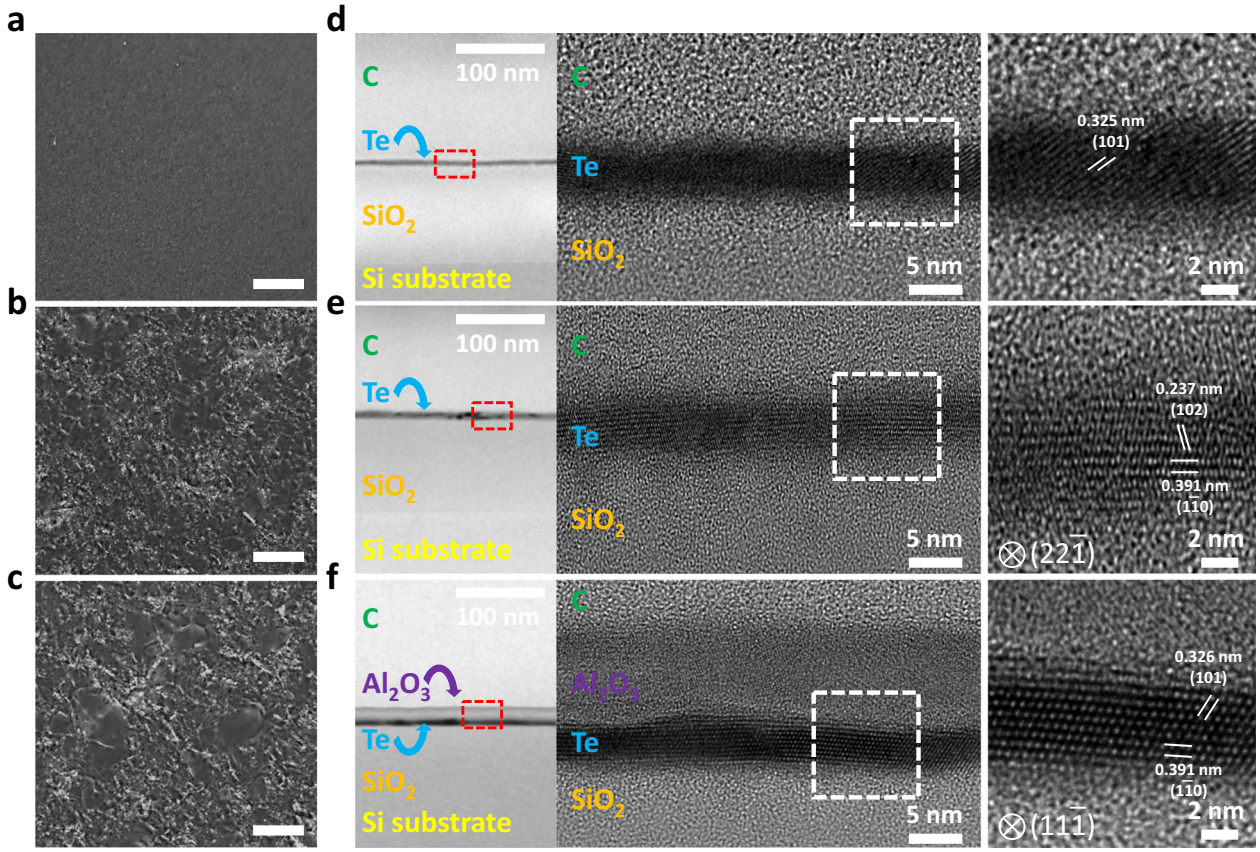

Fig. 1 PLM and HRTEM images. a–c PLM and **d–f** TEM. **a**, **d** As-sputtered Te film. **b**, **e** 150 °C-annealed Te film. **c**, **f** Encapsulated Te film with an Al_2O_3 layer after 150 °C PDA. Scale bars in the PLM images are 20 μm.

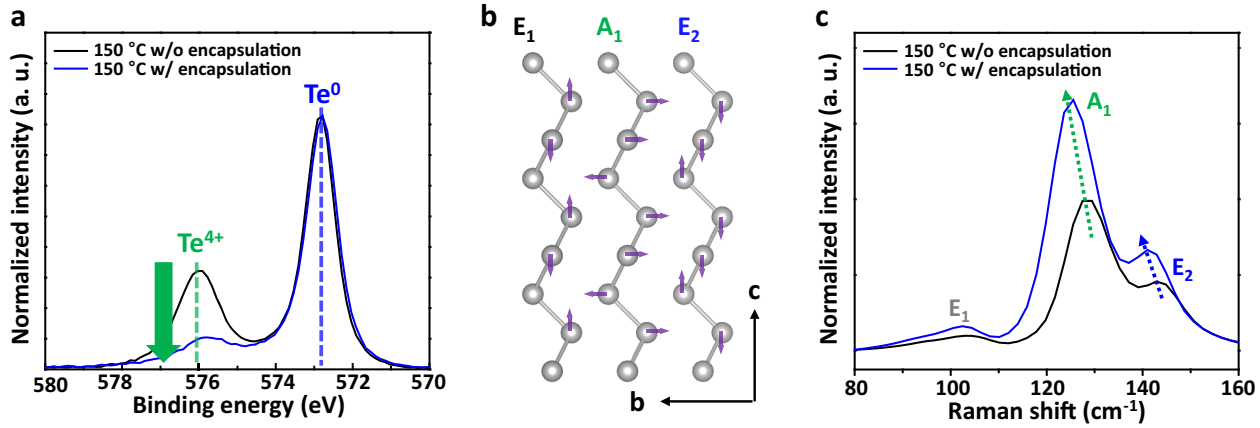

Fig. 2 XPS and Raman spectra. a Te $3d_{5/2}$ XPS spectra of the 150 °C-annealed Te films without and with the Al_2O_3 encapsulation layer. **b** Atomic displacement configurations corresponding to the different lattice vibration modes. **c** Raman spectroscopy of the 150 °C-annealed Te films without and with the Al_2O_3 encapsulation layer.

Device characterization of Te thin-film transistors

We demonstrated FETs using 4-nm-thick Te channel layers with different T_A (see "Methods"). As T_A increases to 150 °C, the device performance is enhanced up to a μ_{FE} of 52.5 $cm^2 V^{-1} s^{-1}$ and an on/off current ratio ($I_{ON/OFF}$) of 1.0×10^4 (Supplementary Fig. 18 and Supplementary Table 1). Even if the reduced Te^0 state in the active layer can slightly localize the valence band (*VB*) edge, the efficient intercalation of the Te *5p* orbital from the Te^0 state near the *VB* edge is sufficient to compensate for the localization, which provides a low hole effective mass. This picture is confirmed through density functional theory (DFT) calculations (see "Methods", Supplementary Note 2 and Supplementary Figs. 2–4, 19, 20). Furthermore, the enhanced crystallinity in the Te layer with increasing T_A partially contributes to the high carrier mobility of the resulting FETs, whereas the off-state leakage current is reduced due to the widening of E_g and the existence of oxidized

states in the Te film lowering the off current. The device performance also showed the great air stability up to 8 weeks (Supplementary Fig. 21), which is in good agreement with the previous result[16]. At $T_A = 200$ °C, however, μ_{FE} begins to be degraded by the predominant Te^{4+} states. The FETs with the Te channel layer of $T_A = 250$ °C largely lose the switching capability, which is attributed to the partial volatilization of Te due to its high vapor pressure[35]. The devices with the Te film of $T_A = 300$ °C exhibit simple resistive behavior, which is consistent with a previous study. Notably, this complete disappearance of the p-type characteristics derives from not only the localized *VB* edge but also the absence of the hexagonal Te array. It is also worth mentioning that the Te FETs annealed at $T_A = 150$ °C under vacuum ambience show the poor electrical characteristics (see "Methods", Supplementary Fig. 22). It can be attributed to the volatilization of Te substance accelerated under the pressure lower than the atmospheric, inducing a number of pinholes on the film surface (Supplementary Fig. 23). This implies that the intentionally introduced oxygen into Te films help maintain the coating uniformity during the PDA[44].

Remarkably, a significant improvement in terms of the $I_{ON/OFF}$ ratio is observed for the 150 °C-annealed FETs through Al_2O_3 encapsulation (Fig. 3a–c). The off current (I_{OFF}) of the encapsulated Te FET decreases by more than 70-fold compared to that of the unencapsulated device, leading to an enhancement in $I_{ON/OFF}$ from 9.3×10^3 (unencapsulated) to 5.8×10^5. Concurrently, major improvements in both the threshold voltage (V_{TH}) from 17.5 to 1.4 V and subthreshold swing (*SS*) from an average of 10.6 to 6.5 Vdecade^{-1} below $I_{DS} = 10^{-8}$ A are accompanied due to the reduced trap density coming from the enhanced crystallinity. Note that severe interfacial traps between the gate insulator and active layer pin the Fermi level and hinder the gate voltage from depleting the active layer[45]. Thus, the reduced trap density can alleviate the Fermi level pinning, enabling the gate to efficiently modulate the accumulation/depletion, which can be further confirmed by the reduction in the operational hysteresis from 28.7 to 9.4 V through the encapsulation[46]. In case of the on-current (I_{ON}), it is slightly reduced after the Al_2O_3 encapsulation, which can be originated from the V_{TH} shift, leading to the significant difference of electrical field (*E*) applied on the channel layer at the same voltage. The negative shift of V_{TH} decreases the effective *E* applied to the channel layer in the on-state despite the same V_{GS} (Fig. 3a), which can reduce transconductance (g_m) and accompany the decrease in the μ_{FE} from 52.5 (unencapsulated) to 30.9 cm^2 V^{-1} s^{-1} (encapsulated) at $V_{GS} = -50$ V (see "Methods"). Finally, notably, the encapsulated FETs reveal exceptional positive/negative bias reliability with a negligible V_{TH} shift (Fig. 3d, e).

Scalability and feasibility for logic application

We fabricated a wafer-scale FET array on a 4-inch Si/SiO_2 wafer to verify the uniformity of the sputtered Te layer, where 70 individual FETs were randomly measured (Fig. 4a). Excellent uniformity was obtained including a μ_{FE} of 29.6 ± 5.0 cm^2 V^{-1} s^{-1}, an *SS* of 7.4 ± 0.4 Vdec^{-1}, a V_{TH} of 2.6 ± 0.6 V, and an $I_{ON/OFF}$ ratio of $5.6 \pm 2.0 \times 10^5$ (Fig. 4b). To test their feasibility in logic circuit applications, a CMOS inverter was fabricated by integrating p-channel encapsulated Te and n-channel IGZO FETs (see "Methods"), where the control n-channel IGZO FET exhibits good electrical characteristics with a μ_{FE} of 25.4 cm^2 V^{-1} s^{-1}, an $I_{ON/OFF}$ of ~10^6, an *SS* of 0.6 Vdec^{-1}, and a V_{TH} of 0.4 V (Supplementary Fig. 24). Supplementary Fig. 25 shows a representative butterfly-shaped rail-to-rail swing with a remarkably high voltage gain of 87.7 at a midpoint voltage of 18.2 V, which is close to the ideal value ($V_{DD}/2$) of 20 V at $V_{DD} = 40$ V. The fabricated CMOS inverter also exhibits outstanding noise margins, with input low level (NM_L) of 15.4 and high level (NM_H) of 20.2 V. This indicates that the resulting CMOS inverter is highly durable against inevitable electrical noise: the inverter can tolerate up to 15.4 and 20.2 V of noise at high and low output, respectively. Furthermore, encapsulated FETs with an 11-nm-thick HfO_2 gate dielectric were fabricated (see "Methods") to demonstrate the low driving voltage for practical applications (Fig. 4c). The driving voltage is successfully reduced from 100 to 6.5 V with a significant improvement in the *SS* from 6.5 to 0.4 V dec^{-1}. Simultaneously, the hysteresis decrease from 9.4 to 2.4 V.

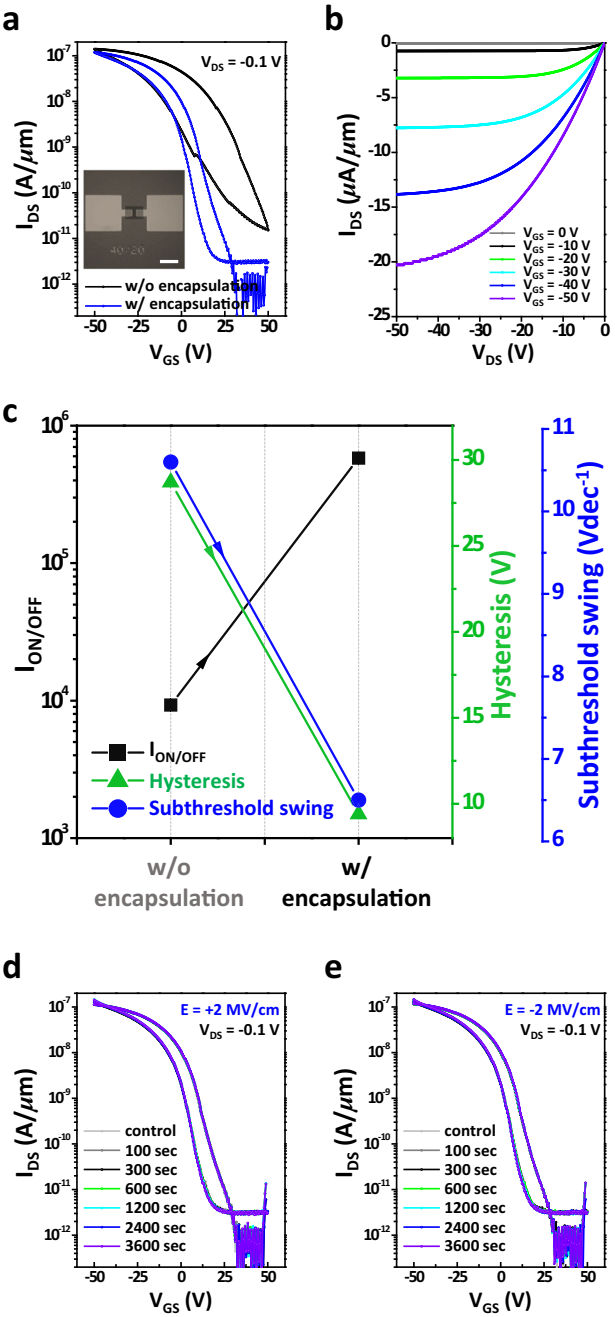

Fig. 3 Change of device performances depending on the encapsulation. a Transfer characteristics of the Te FETs with and without the Al_2O_3 encapsulation layer. Inset shows a top view image of a Te FET, and the scale bar is 100 μm. **b** Output characteristics of the encapsulated Te FETs. **c** $I_{ON/OFF}$, *SS* and hysteresis for the Te FETs with and without the Al_2O_3 encapsulation layer. Bias stress stability test for the encapsulated 150 °C-annealed Te FET under (**d**) positive and (**e**) negative gate bias stress.

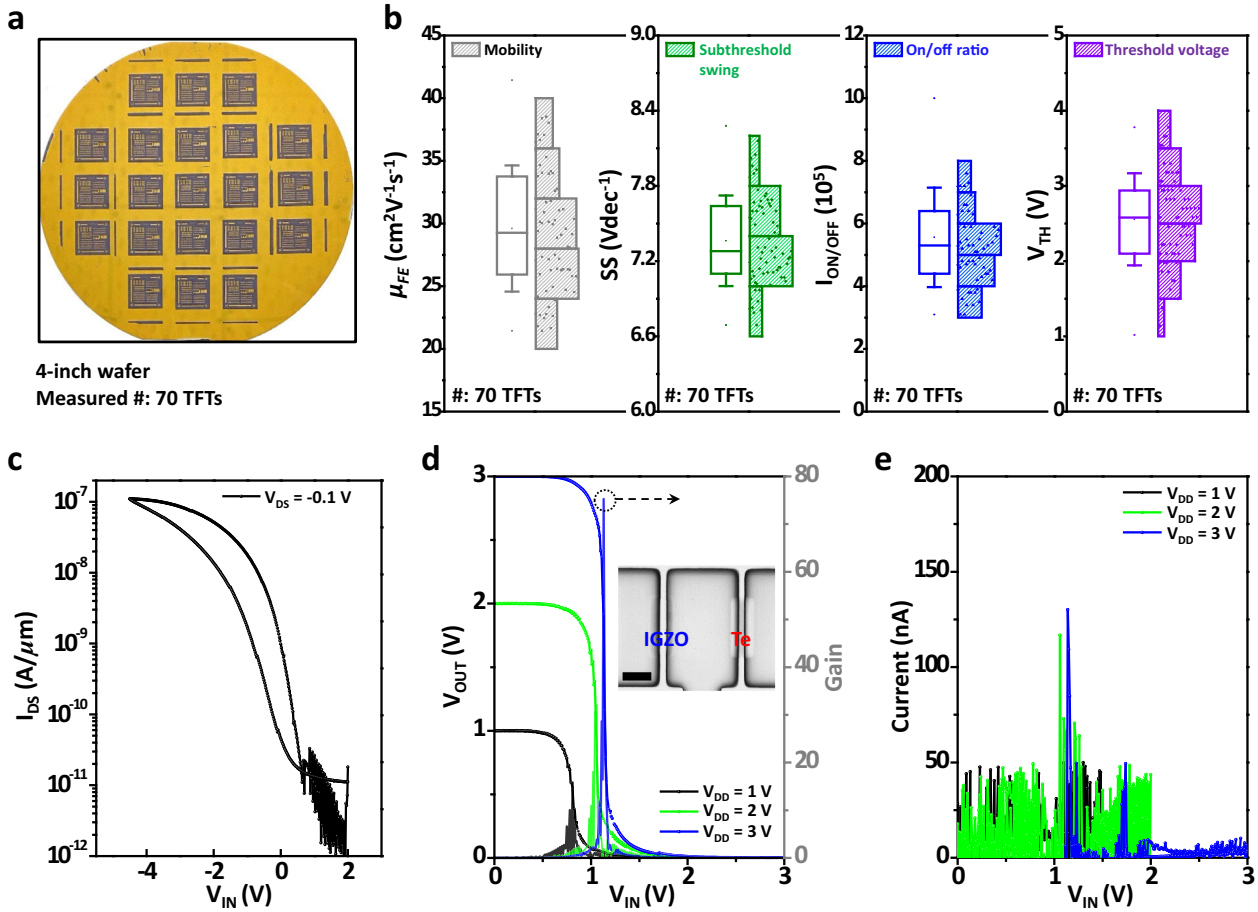

Fig. 4 Scalability and logic applications. a Photograph of the encapsulated Te FET array on a 4-inch Si/SiO_2 (100 nm) wafer. **b** Statistical distribution of the μ_{FE}, *SS*, $I_{ON/OFF}$ and V_{TH} (left to right) for 70 individual transistors in the wafer-scale FET array. Error bars represent standard deviation for each electrical parameter. **c** Transfer characteristics of the encapsulated Te FETs fabricated on a 11-nm-thick HfO_2 gate dielectric ($V_{DS} = -0.1$ V). **d** Voltage transfer characteristics and extracted voltage gain of CMOS inverter using n-channel IGZO and p-channel Te film using the 15-nm-thick HfO_2/Al_2O_3 gate dielectric. Inset shows a top view image of a CMOS inverter. Scale bar is 1 mm. **e** Current characteristics of a CMOS inverter.

Both μ_{FE} and $I_{ON/OFF}$ are maintained at 25.8 $cm^2 V^{-1} s^{-1}$ and 1.7×10^5, which are included within the normal distribution, as shown in Fig. 4b. These results signify the considerable potential of sputtered Te material for high-performance p-channel FETs because these metrics, such as μ_{FE} and *SS*, are comparable to those of n-channel IGZO FETs. Finally, the CMOS inverter using the 15-nm-thick HfO_2/Al_2O_3 gate dielectric was demonstrated (Fig. 4d), which exhibited the outstanding device performance including the voltage gain, NH_L and NH_H of 75.2, 1.0 V and 1.3 V, respectively, at small V_{DD} of 3 V. Static currents in this inverter were as low as 10 nA, which guarantees its low static power consumption (Fig. 4e). A direct current (DC) which flows from V_{DD} to ground during the transition state also showed a very low peak value of 130 nA, indicating the great power consumption of this CMOS inverter. These highly promising electrical characteristics show the strong potential of p-type Te films fabricated through our approach for back-end-of-line (BEOL) compatible CMOS circuits.

DISCUSSIONS

We have proposed a cost-effective and mass-production method of a Te layer as a p-type channel material at a low temperature. The sputtering of the Te film at room temperature and annealing ($T_A \leq 150$ °C) under ambient air allows the resulting film to be uniform, where the introduced oxygen in the Te film may hinder the uncontrolled sublimation of Te substance. The encapsulation of the Te film with Al_2O_3 assists the deoxidation of the local amorphous oxidized phase and conversion to the hexagonal Te phase as well as the grain growth of the pre-existing Te phase, leading to promising p-channel FETs with wafer-scale uniformity. However, there still remains room to be improved for practical implementation in terms of the hysteresis and *SS*. Therefore, various studies must be further conducted, such as source/drain (S/D) contact engineering and trap density control via interface and film optimization (e.g., adopting other encapsulation layers, such as HfO_2, ZrO_2, and SiO_2). In particular, the origin of hysteresis effect in p-channel Te FETs should be identified for minimizing and eliminating the operational hysteresis. Dynamics on a charge carrier trapping/detrapping mechanism at border and interface traps between the gate insulator and channel layer, which is frequently attributed to the rationale for this hysteresis, should be studied using diverse gate dielectric layer. Kinetics of hysteresis depending on the sweeping voltage range and rate for the Te FETs would be also helpful to clarify the origin of hysteretic behavior. Although previous works have demonstrated the feasibility of promising p-channel Te FETs, they have very definite limitations in the deposition process using a solution process or evaporation at cryogenic temperature for realization of high-quality Te films. However, this study provides a facile fabrication method for wafer-scale high-quality Te films using CMOS-compatible methods at low

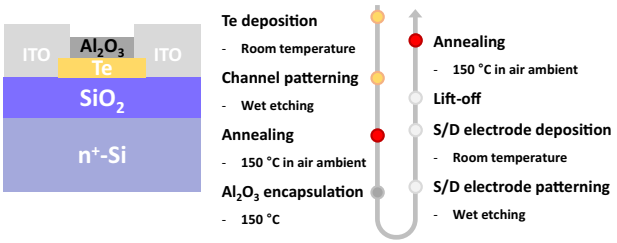

Fig. 5 Device fabrication. Cross-sectional device schematic (left) and its fabrication procedure (right).

temperature of 150 °C. Moreover, the device performances of this 4-nm-thick Te FET are quite competitive compared to other studies regarding the p-channel FETs using not only other p-type inorganic semiconductors but also Te as a channel layer (Supplementary Table 2). Therefore, it is strongly believed that this approach has great potential for implementing high-performance p-channel FETs into industrial-relevant scalable applications such as M3D integration and BEOL electronics because of its significant advantage in the room temperature fabrication and low-temperature annealing (150 °C) as well as the outstanding electrical characteristics.

METHODS

Film fabrication

Te films were deposited by the reactive magnetron sputtering method using a Te target (99.99%, VTM) at room temperature. The chamber base and working pressures were set to 3.0×10^{-6} Torr and 2 mTorr, respectively. The DC sputtering power was fixed to 20 W. The sputtering was conducted for 28 (70) s to deposit the 4 (10)-nm-thick Te films, respectively. The sputtered Te films were thermally annealed at various temperatures for 1 h in ambient air, except for the as-sputtered sample. The temperature increased with the speed of 5 °C/min during the PDA. Furthermore, the vacuum annealing was carried out at 150 °C for 1 h, and it was held below 1×10^{-3} Torr using a rotary pump. An Al_2O_3 film was deposited by plasma-enhanced ALD (PEALD) using the TMA and oxygen plasma as the Al precursor and oxidant, respectively, at 150 °C under 1 Torr. Partial oxygen pressure (P_O) and plasma power during the PEALD process were 10% and 50 W, respectively. A HfO_2 film was grown using the PEALD at 150 °C under 1 Torr using the tetrakis(ethylmethylamido)hafnium precursor. The P_O and plasma power for the HfO_2 deposition were 10% and 100 W, respectively. IGZO films were prepared by the magnetron sputtering method using an IGZO target (99.999%, iTASCO) at room temperature under a radio-frequency sputtering power of 50 W. The base and working pressures were identical to those in the process for the Te films. The deposited IGZO films were subjected to PDA at 400 °C for 1 h in ambient air.

Device fabrication

Bottom-gate top-contact FETs were fabricated on a thermally oxidized SiO_2 (100 nm)/conductive Si substrate where SiO_2 and Si act as a gate insulator and an electrode, respectively. A 100-nm-thick ITO S/D electrode was deposited by sputtering. Both the channel and electrode regions were patterned using a standard photolithography, and the channel width (W) and length (L) were 40 and 20 μm, respectively. Figure 5 shows a schematic illustration of a cross-sectional device structure and an overall procedure of its fabrication. CMOS inverters were patterned using the metal shadow mask.

Film characterization

The thickness of the films was determined by a spectroscopic ellipsometer (Elli-SE, Ellipso Technology) and confirmed by TEM. Basically, all the characterizations were conducted on 4-nm-thick films, except for the XRD and XPS analyses (10-nm-thick Te films were used in these analyses). The crystalline structure was examined by X-ray diffractometer (SmartLab, Rigaku) and HRTEM (Talos F200x, FEI) at 200 kV. Optical images were taken by optical light microscopy (BX51M, Olympus). The surface roughness was analyzed by atomic force microscopy (NX20, Parksystems). The evolution of the crystal domain was observed by PLM (Leica DM4P, Leica). The chemical states were analyzed by XPS (Veresprobe II, Ulvac-phi) after an in situ etching process of the film surface to remove unintentional artifacts such as contamination and oxidation due to exposure to ambient air. The transmittance and absorbance of the prepared Te films were observed by UV/visible spectroscopy (V-770, JASCO). Raman spectra (DXR2xi, Thermo) of the films were obtained using a He-Ne laser (wavelength = 532 nm) at room temperature. The device performances of the FETs and CMOS inverters were measured by an I-V meter (Keithley 4300, Keithley) at room temperature in ambient air.

Statistical analysis

All the electrical characteristics of the FETs and CMOS inverters were measured by an I-V meter (Keithley 4300, Keithley) at room temperature in ambient air. The data plotted in the figures are all raw data. No denoise, smooth, or similar methods were taken. The field-effect mobility was calculated using $\mu_{FE} = g_m L/WC_{OX}V_{DS}$, where g_m, L, W, C_{OX}, and V_{DS} are the transconductance, channel length, channel width, gate oxide capacitance and drain voltage, respectively. Note that the hysteresis which might be originated from interface/border traps between the channel and gate insulator can cause a disparity in the μ_{FE}[47]. Depending on the V_{GS} sweep direction, thus, the μ_{FE} extracted from the maximum value of g_m has different values as shown in Supplementary Fig. 26. When the back-gate sweeps from 50 to −50 V, all the bulk and interface traps are slowly filled and then holes are accumulated in the Te film. When the back-gate sweeps from −50 to 50 V, however, the accumulated holes are fast depleted at first. For this reason, the μ_{FE} extracted from the fast depletion region (−50 to 50 V) is more associated with the channel mobility[48]. The threshold voltage (V_{TH}) was extracted using the linear extrapolation method. The SS was calculated using $SS = dV_{GS}/dlog(I_{DS})$. The voltage gain of CMOS inverters was calculated using dV_{OUT}/dV_{IN}, and noise margins were extracted at $dV_{OUT}/dV_{IN} = -1$.

Density functional calculation

We performed DFT calculations using the Vienna Ab initio Simulation Package[49,50]. The generalized gradient approximation with the Perdew-Burke-Ernzerhof functional was employed for the exchange-correlation energy of electrons[51]. We used 400 eV for the energy cutoff of the plane-wave basis and the Γ point for k-point sampling. The amorphous structures of TeO_x ($1 \le x \le 2$) were modeled using the melt-quenching process. The initial atomic positions were randomized by premelting at 5000 K for 1 ps. We then performed melting for 10 ps at 1500 K and quenching to 300 K with a cooling rate of -100 K ps^{-1}. Finally, we obtained the final configurations by relaxing the cell parameters and atomic positions until atomic forces became less than 0.02 eV/Å. For statistical averaging, we generated three amorphous samples using the same melt-quenching procedure.

DATA AVAILABILITY

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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AUTHOR CONTRIBUTIONS

T.K. and J.K.J. conceived and designed this study. T.K. and C.H.C. conducted the film and device fabrication/analysis under the supervision of J.K.J. A.S. and K.-B.C. performed the XPS analysis. M.L. and S.H. contributed to the DFT calculation. P.B. and S.-Y.C. contributed to the TEM analysis. T.K. and J.K.J. wrote the manuscript. All authors discussed the results and commented on the manuscript.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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Correspondence and requests for materials should be addressed to Jae Kyeong Jeong.

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