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Article

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Interface trap states induced underestimation of Schottky barrier height in metal-MX_2 junctions

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Understanding the interfaces between a contact metal and a two-dimensional (2D) semiconductor, as well as the dielectric gate stack and the same 2D material in transition metal dichalcogenide (TMD) based transistors, is a crucial step towards the introduction of TMD materials into advanced logic nodes. In particular, for the contact metal/2D interface, one of the key parameters is the Schottky barrier height (SBH), which is frequently extracted based on temperature-dependent subthreshold characteristics of TMD field-effect transistors (FETs). However, recently, using this methodology has resulted in rather low extracted SBH values for TMD-based transistors, which seems inconsistent with the low on-current levels in said devices. Here, we therefore connect measured device characteristics on monolayer (ML) MoS_2 transistors with technology computer-aided design (TCAD) simulations. In particular, our analysis shows that low SBHs can be incorrectly extracted when the interface trap density D_{it} is substantial and exhibits, at the same time, a significant temperature dependence, as is the case for TMDs. In fact, TCAD simulations and comparison with the obtained electrical data reveal that the actual SBH is substantially larger than what is extracted when ignoring the above mentioned details of D_{it}.

Frequently, field-effect transistors based on novel semiconducting channel materials are built without mimicking the n/p/n or p/n/p doping profile of a conventional silicon-based metal oxide semiconductor field-effect transistor (MOSFET). In fact, the most common way of building prototype FETs is to employ metal source/drain contacts in conjunction with a gating scheme that controls the entire semiconducting channel. In most instances, a Si/SiO_2 substrate with a thick dielectric layer is used as a global back gate, allowing for quick access to some basic device characteristics. For devices of this type, the contact resistance is dominated by the Schottky barrier at the source/drain-to-channel interfaces. In 2004[1], we discussed a novel approach to extract information, in particular the Schottky barrier height (SBH), using carbon nanotubes as an example. The idea was that the ultra-thin body of the channel material impacts, i.e., reduces the Schottky barrier thickness (SBT) in the gated channel region. This change, in turn, allows for substantial thermal-assisted tunneling between the contacts and the channel, impacting the inverse subthreshold slope (SS) of the device in its off-state. In fact, for gate voltages in the device off-state close to threshold, SS cannot reach the thermal limit, e.g., ~60 mV/dec at room temperature, irrespective of the chosen gate oxide thickness, since this regime is impacted by the gate voltage response of the Schottky barrier thickness (SBT). Through a careful analysis of the "effective barrier height" ϕ_B, the one that can be extracted from an Arrhenius plot of device current versus inverse temperature T for different gate voltages V_{GS}, the actual Schottky barrier height can be identified[1]. Our method has since been used frequently, including for ultra-thin body devices from transition metal dichalcogenides (TMDs).

In a number of instances very small extracted Schottky barrier heights of 12.5, 64, and 16 meV were reported[2–4]. As we discussed in our original paper, there are a couple of signatures that need to be present to ensure that the extracted SBH is indeed the one that actually determines the current transport. For example, (1) SS needs to be proportional to T in the thermal regime—i.e., in the deep off-state of the device—for our analysis to be applicable. Another sanity check is (2) the expected correlation between $\log(I_{DS})$ vs. V_{GS} and ϕ_B vs. V_{GS} in the thermal regime. In fact, for fully depleted devices ($C_D = 0$), SS in the thermal regime should be $(k_BT/q) * \ln(10) * m$ with $m = 1 + C_{it}/C_{ox}$ for constant C_{it} and C_{ox} and $-(d\phi_B/dV_{GS})^{-1} = m$. In case of ref. 4, condition (1) does not apply, as apparent from figure 9b in ref. 4. Condition (2) is clearly violated in refs. 2–4 as evident from Fig. 3 if compared to Fig. 4b in ref. 2, from the absence of any ϕ_B-dependence in figure S3 in ref. 3, and from figure 9b, if compared to figure 9d in ref. 4, where "m" is labeled as "γ^{-1}", respectively.

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In the following, we will elucidate why the above articles presumably vastly underestimated the actual SBH by comparing our own data with those previously published. In particular, we will identify a strong temperature dependence of C_{it} as the culprit for why our previously proposed SBH extraction method[1] cannot be applied. To do that, we fabricated monolayer MoS_2 transistors and electrically characterized the devices at different temperatures to extract the SBH and to understand the effect of the interface traps on the transfer characteristics, especially in the subthreshold regime. Additionally, TCAD simulations are employed to model the distribution of interface traps, which explain the change in subthreshold slope with temperature and underestimation of extracted SBH.

Results

Device fabrication and electrical characteristics

Figure 1a shows the schematic of the as-fabricated MoS_2 transistor. The local bottom gates (LBGs) were first fabricated on a Si/SiO_2 substrate by lithography (100 kV JEOL system) and metallization (e-beam evaporator—3 nm Cr/12 nm Au), followed by the deposition of 5.5 nm ALD HfO_2 (200 °C thermal deposition, 50 cycles) and 3.6 nm amorphous boron nitride (a-BN), serving as the bottom gate dielectric. Next, a monolayer MoS_2 film was wet transferred onto the LBG substrate and etched by reactive ion etching with Cl_2/O_2 (15 sccm/5 sccm) at a RF power of 40 W for 15 s. Finally, Ni source/drain (S/D) contacts were patterned using e-beam lithography and e-beam evaporation. Figure 1b, c show the transfer and output characteristics of an exemplary MoS_2 transistor with a channel length of 200 nm. The device shows good off-state behavior, such as negligible drain-induced barrier lowering (DIBL) and low inverse subthreshold slope (SS ~100 mV/decade, extracted between 1e-3 to 1e-4 μA/μm), and a high on-state current of ~180 μA/μm at $V_{DS} = 1$ V.

To study the impact of the interface trap density on the SBH extraction, we measured the transfer characteristics of ML MoS_2 transistors at different temperatures for $V_D = 0.1$ V as shown in Fig. 1d. At gate biases below flatband voltage ($V_{GS} \leq V_{FB}$, here at current values of around 1e-3 μA/μm) the thermionic current determines the current through the device, with I_{DS} given by ref. 1:

$$I_{DS} \approx AT^2 e^{\frac{-q\Phi_B}{k_B T}} \tag{1}$$

where A is the Richardson's constant, ϕ_B is the effective barrier height, k_B is the Boltzmann constant, q is the electronic charge, and T is the temperature. In order to extract the actual SBH (ϕ_{SB}), the temperature-dependent current values (shown in Fig. 1d) are used to generate an Arrhenius plot ($\log(I_{DS}/T^2)$ vs. 1000/T), and the slope of the Arrhenius plot results in a ϕ_B vs. V_{GS} plot, as shown in Fig. 1e. Note that using this technique over the entire gate voltage range means that ϕ_B is only capturing the "actual" barrier height for $V_{GS} \leq V_{FB}$. This allows to identify the Schottky barrier height ϕ_{SB}, given that for gate biases lower than V_{FB} the effective barrier height ϕ_B varies linearly with V_{GS} in the thermionic transport regime. This leads to the extraction of a Schottky barrier height, SBH ~90 ± 10 meV. It is important to note that (1) this value of SBH extracted from the transfer characteristics is significantly lower than the SBH obtained from TCAD simulations by fitting our experimental data, which will be discussed later in this paper and (2) the calculations have not been corrected for threshold voltage shifts in transfer characteristics at different temperatures, which is a common practice found in the literature[4,5]. Hence, to understand the effect of threshold voltage (V_T) correction on the SBH extraction and the underlying reason behind the V_T shift, the transfer characteristics are adjusted, as shown in Fig. 2a. Using these corrected current values, the Arrhenius plot ($\log(I_{DS}/T^2)$ vs. 1000/T) is again generated. This time, the slopes ($-q\phi_B/k_B$) are positive for all gate voltages as shown in Fig. 2b, resulting in a negative SBH extraction, which is not physically meaningful and also not consistent with our TCAD simulations. This erroneous SBH value extracted post V_T correction is a result of the fact that in reality, the V_T shifts with temperature in this device

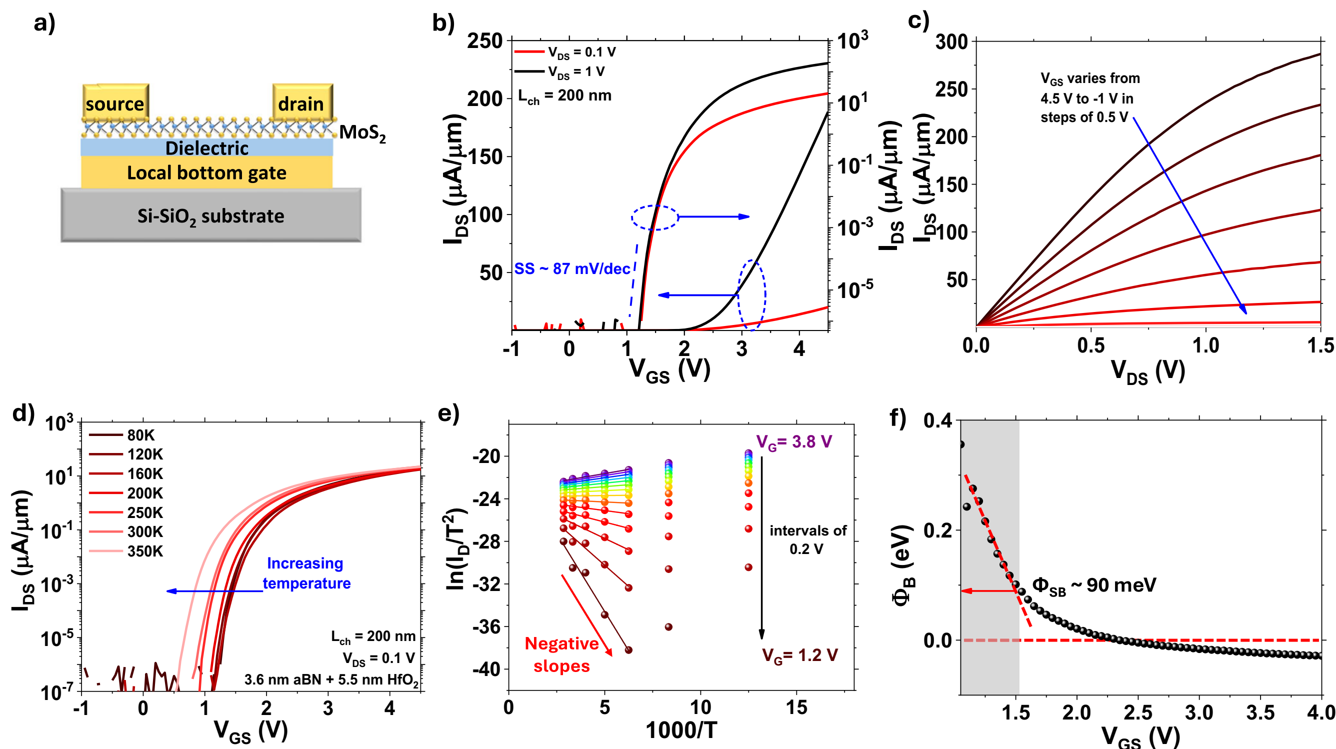

Fig. 1 | Electrical performance and SBH extraction of MoS_2 FET. **a** Schematic diagram of an as-fabricated device. **b** Transfer and **c** output characteristics of an exemplary transistor with a channel length of $L_{ch} = 200$ nm. **d** Temperature-dependent transfer characteristics and **e** Arrhenius plot ($\log(I_{DS}/T^2)$ vs. 1000/T) showing expected negative slopes for lower gate biases and unexpected positive slopes at high gate biases (**f**) extracted effective barrier height (ϕ_B) as a function of applied gate voltage. Note that negative effective barriers are extracted for gate voltages larger than ~2.3 V.

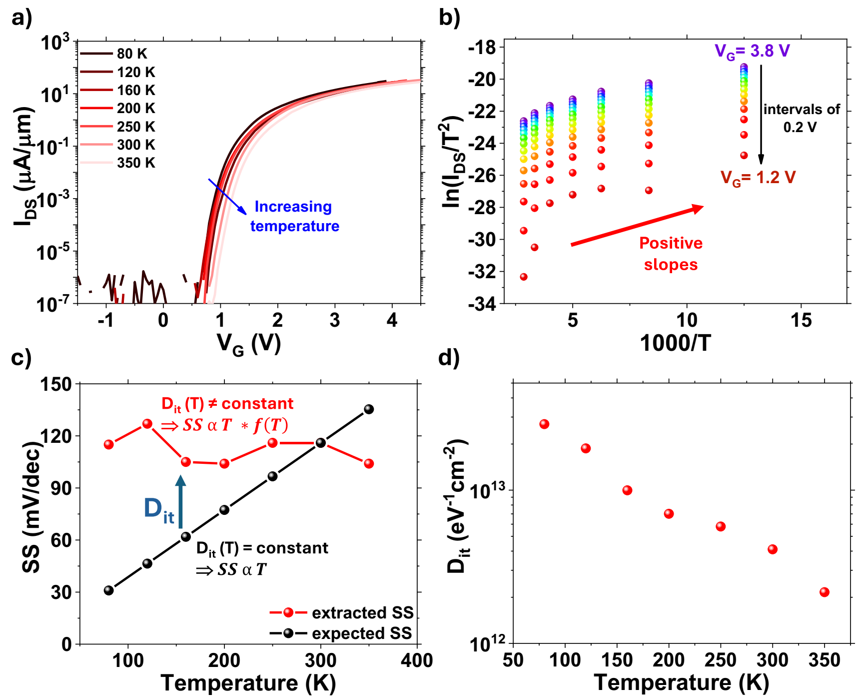

Fig. 2 | SBH extraction from V_T corrected transfer characteristics and D_{it} distribution. **a** Temperature-dependent transfer characteristics after correcting for the apparent threshold voltage shifts (V_T for all transfer characteristics was extracted by extrapolation in the linear regime. The V_T shift at different temperatures, with respect to room temperature V_T, was then subtracted from the gate voltage axis in the transfer characteristics, effectively aligning the curves across different temperatures.) and **b** Arrhenius plot ($\log(I_{DS}/T^2)$ vs. 1000/T) showing positive slopes. **c** Expected and extracted inverse subthreshold slope of the transistor in Fig. 1. **d** Interface trap density vs. temperature extracted from SS, evaluated between 1e-3 to 1e-4 μA/μm.

originate from a varying interface trap density profile, which we will demonstrate from our TCAD simulations in the next section.

Noticing that the small extracted Schottky barrier height (without any V_T correction) is a result of the very small temperature dependence of the subthreshold currents, we next extracted the inverse subthreshold slope (SS) in the deep off-state for currents between 1e-3 to 1e-4 μA/μm that correspond to the thermionic emission regime. Under these conditions, SS is expected to exhibit the following temperature dependence:

$$SS = \frac{k_B T}{q}\left(1 + \frac{C_D + C_{it}}{C_{ox}}\right) \tag{2}$$

where C_D is the depletion capacitance, C_{it} is the capacitance due to a finite interface trap density (D_{it}), given by $C_{it} = q^2 * D_{it}$ and C_{ox} is the gate oxide capacitance. Given the absence of any variation of depletion charge in the MoS_2 channel to the applied gate bias, C_D is zero in our fully depleted devices. Assuming no dependence of D_{it} on temperature, the subthreshold slope should linearly increase as the temperature rises, as represented by the black dots in Fig. 2c, assuming that at 300 K the actual D_{it} value had been extracted. However, the extracted SS values from the subthreshold characteristics at different temperatures, as shown by red dots in Fig. 2c are almost temperature independent. To explain the apparent absence of the expected temperature dependent trend from Eq. (2), one has to conclude that C_{it} is a function of T. The resulting $D_{it}(T)$ is plotted in Fig. 2d. Interestingly, D_{it} increases with decreasing temperature, reaching a maximum value of 3×10^{13} $eV^{-1}cm^{-2}$ at 80 K. This finding is consistent with previous results by the IMEC group[6] which show higher trap densities at lower temperatures from detailed capacitance measurements on TMDs as a function of T. The study combines the static model in the small signal regime with the distributed R-C network of the semiconductor to understand the dynamic nature of the MOS capacitor, focusing on segregating the effects of channel resistance from interface traps. The interface traps in such a way extracted for a 4 nm HfO_2/3–5 ML MoS_2 stack show an exponentially increasing amount of defect states toward the conduction band edge in the bandgap. In short, despite using different methodologies (temperature-dependent transfer characteristics in this study and C-V characteristics used in IMEC study[6]), both studies obtain an interface trap density distribution that increases approximately exponentially towards the MoS_2 conduction band edge at the MoS_2-dielectric interface. Hence, the expected decrease of SS with decreasing T is compensated for by an increase of $D_{it}(T)$ for decreasing temperature. This implies that, similar to ref. 3 and[4] our own MoS_2 data cannot be used to extract the Schottky barrier height at the source/drain metal to TMD channel interface employing the methodology proposed in ref. 1. Also, similar to refs. 2–4, when using the extraction methodology, nonetheless, a vastly underestimated ϕ_{SB}-value is extracted.

One may ask the question whether the strong dependence of our D_{it} on temperature is a unique result of the TMD-to-gate stack interface. The answer is "no". In fact, the observed temperature dependence can be translated into a D_{it} profile inside the TMD bandgap as a function of the energetic position relative to the band edges as discussed in the next section that is qualitatively consistent with what has been previously reported for other semiconducting channels, e.g., III–V[7,8] and silicon[9–11]. The difference, however, lies in the magnitude of D_{it}. While silicon technology has achieved D_{it}-values in the 10^{10} to 10^{11} eV^{-1} cm^{-2} range, our extracted D_{it}-values at room temperature are substantially higher. This is also the reason why the methodology in ref. 1 can readily be applied to other transistor materials for Schottky barrier extraction as long as C_{it} is sufficiently smaller than C_{ox}. To further understand the exact distribution of trap densities in MoS_2 devices, TCAD simulations are employed.

Dit distribution extraction with TCAD

Using TCAD simulations, we have extracted a $D_{it}(E)$ distribution that is consistent with the experimental temperature dependence of SS. The simulations are carried out with Synopsys Sentaurus Device (SDevice), in which the 2D material channel is represented as a bulk semiconductor with a 2D density of states[12]. Figure 3a shows the simulated structure, which mimics the experimental device. The source and drain contacts are modeled with a non-local Schottky barrier tunneling model[13]. An energy- dependent D_{it} distribution is assumed at the MoS_2-a-BN interface and specified in SDevice, using an energy-dependent-D_{it} lookup table with an overall resolution of 50 meV and a 15 meV refinement for the first point. To capture in particular the on-state performance of our devices, a temperature dependent mobility, μ has been used as obtained from our earlier extraction on the same gate stack[14] (see Fig. 3b). Other material parameters for MoS_2 are obtained from ref. 15. The remaining calibration parameters are the

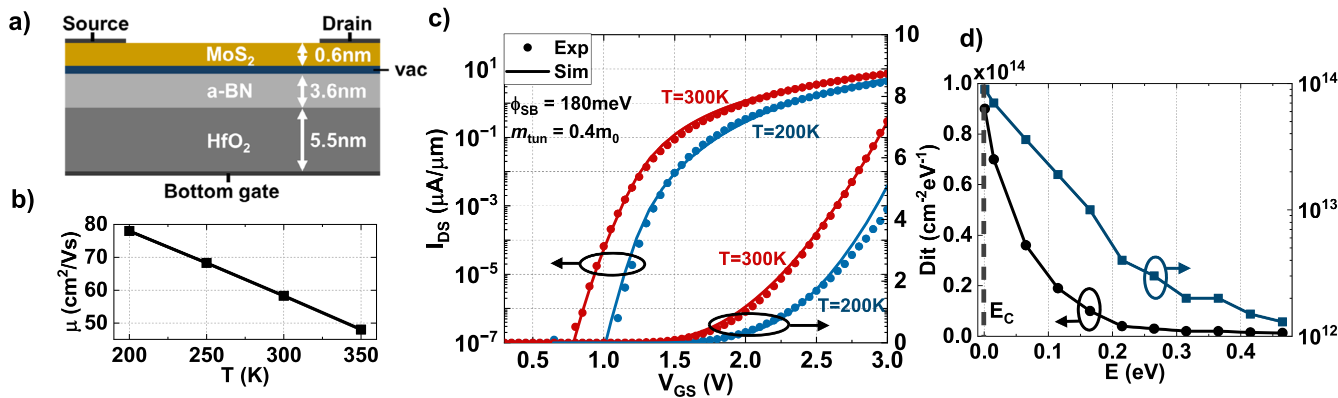

Fig. 3 | TCAD simulation calibration of SBH and D_{it} distribution. **a** Simulated structure mimicking the experimental structure of Fig. 1a, with a 0.2 nm van der Waals gap between the MoS_2 and a-BN, **b** temperature dependent mobility impacted by phonon scattering as used in these simulations, **c** calibration of temperature dependent simulated transfer characteristics to experimental measurements of Fig. 1d, **d** resulting calibrated D_{it} distribution.

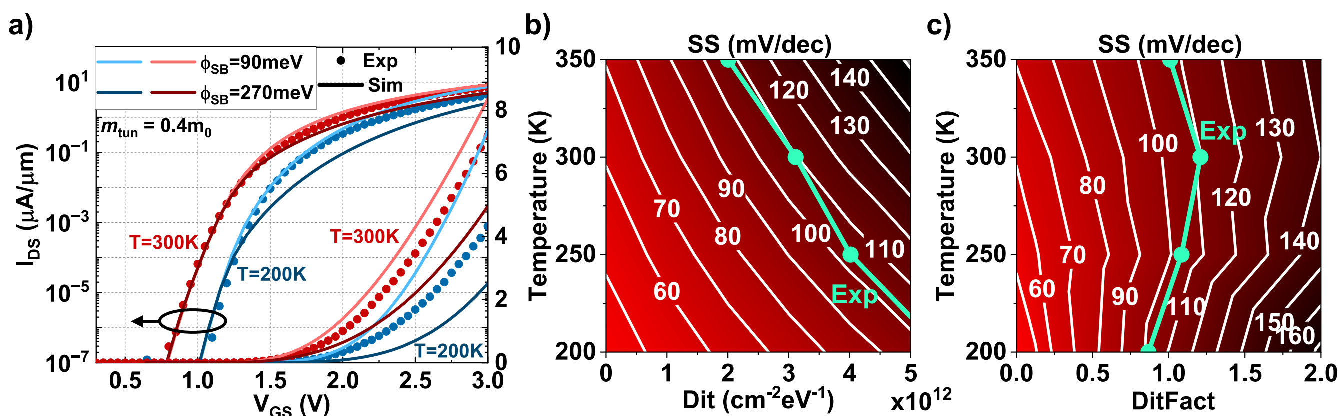

Fig. 4 | Assessment of uniqueness of TCAD calibration. **a** Comparison of temperature dependent experimental transfer characteristics with simulated curves for varying SBH values. **b** Simulated SS variation with temperature for a uniform D_{it} distribution throughout the MoS_2 bandgap. **c** Simulated SS variation with temperature for a calibrated D_{it} distribution of Fig. 3c. The D_{it} distribution is scaled by a constant factor (DitFact), such that D_{it}=Ditfact * (D_{it} profile in Fig. 3d). SS is extracted in the I_{DS} range of 1e-4 –1e-3 μA/μm. Indicated are also the extracted experimental values corresponding to Fig. 2c.

values of the D_{it} distribution at each energy inside the TMD bandgap (independent of temperature) and the contact Schottky barrier height. While the deep off-state in the thermionic transport regime is used to determine $D_{it}(E)$ from the various temperature-dependent measurements, the actual on-state performance is captured by the Schottky barrier height. Note that $D_{it}(T)$ in Fig. 2d is the result of the integrated impact of $D_{it}(E)$ for a particular temperature.

Figure 3c shows that the temperature dependence of the transfer characteristics can be well captured with a SBH of 180 meV and a D_{it} distribution that peaks towards the conduction band edge (E_C) as shown in Fig. 3d. It should be noted that the simulations also show a V_T-variation with temperature, even though no additional parameter had been varied with temperature, indicating that the shift between the 200 K and the 300 K curves arises from the interface trap density profile. The calibrated SBH of 180 meV is substantially larger than that obtained from the extraction methodology in the previous section, and Fig. 4a shows that the previously extracted value of 90 meV (calculated without threshold voltage correction of transfer characteristics) would result in a significant overestimation of the device currents, in particular for lower temperatures. For completeness, we also include the case of a higher SBH of 270 meV, showing the uniqueness of the calibrated value of 180 meV mentioned before.

We further demonstrate that the experimental temperature dependence of the SS cannot be captured using a uniform D_{it} energy distribution. Figure 4b shows that for any given value of the uniform D_{it}, the simulated SS increases with temperature as discussed above in the context of Eq. (2), in contrast to the relatively constant experimental SS values of Fig. 2a. On the other hand, Fig. 4c shows that with a temperature independent peaked $D_{it}(E)$ distribution, the temperature-induced SS increase is compensated as the Fermi-level shifts away from E_C and toward lower values of D_{it}. For the calibrated D_{it} distribution, the SS is nearly constant within the considered temperature range, which corresponds to the experimentally observed trend.

In conclusion, this study investigated the effect of interface traps on the extraction of Schottky barrier height. The SBH extracted from temperature-dependent transfer characteristics of MoS_2 transistors is significantly lower than the value extracted from TCAD simulations. TCAD simulations reveal that the calibrated SBH is two times higher than the experimentally extracted SBH using the approach described in ref. 1. This is due to the high interface trap densities at the 2D material/dielectric (MoS_2/a-BN/HfO_2) interface which results in underestimation of the SBH. The interface trap density is not only high, of the order of 10^{14} cm^{-2} eV^{-1} at the band edge, but also changes over an appreciable energy range inside the bandgap of MoS_2.

Data availability

All data supporting the findings of this study are included in the paper. The corresponding author can also provide additional data upon reasonable request.

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Author contributions

H.J. and D.V. contributed equally. H.J. analyzed the experimental data and results. D.V., S.S., C.J.L.R., and G.S.K. discussed the SBH extraction method using TCAD and D.V. performed the TCAD simulations. Z.S. fabricated the device and conducted the electrical characterization. H.J., D.V., Z.S., and J.A. wrote the manuscript. All authors reviewed the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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