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npj 2D Materials and Applications

https://doi.org/10.1038/s41699-026-00686-1

Article in Press

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Received: 22 September 2025

Accepted: 10 March 2026

Cite this article as: Wang, S.-T., Li, K.-W., Weng, T.-T. *et al.* Suppression of hysteresis in ultrathin tellurium transistors. *npj 2D Mater Appl* (2026). https://doi.org/10.1038/s41699-026-00686-1

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Suppression of Hysteresis in Ultrathin Tellurium Transistors

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ABSTRACT- Tellurium (Te) is a promising p-type semiconductor but suffers from pronounced electrical hysteresis that limits device stability. The origin of hysteresis in Te field-effect transistors is investigated, and effective suppression strategies are demonstrated. In exposed devices, large hysteresis and abrupt current switching are observed, governed by the direction and range of gate voltage sweeps rather than gate polarity, and are attributed to the dynamic reorientation of dipolar gas molecules adsorbed on the Te surface. Dielectric encapsulation using Al_2O_3 significantly suppresses gas-induced hysteresis, resulting in improved mobility of ~80 $cm^2\ V^{-1}\ s^{-1}$ and an I_{ON}/I_{OFF} ratio exceeding 10^5 under ambient conditions. Nevertheless, residual hysteresis associated with charge trapping persists in single-gate devices. To further stabilize channel electrostatics, a dual-gate architecture employing Al_2O_3 top and bottom dielectrics is implemented, achieving hysteresis below 1 V across a wide range of sweep rates and exhibiting minimal degradation under prolonged bias stress. These results establish a comprehensive understanding of hysteresis in Te and enable reliable, BEOL-compatible p-type transistors for advanced integration.

KEYWORDS**:** Tellurium, Hysteresis, Threshold voltage shift, Induced dipole, Field Effect Transistor, Beyond-Si

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INTRODUCTION

Continued transistor scaling is approaching fundamental and technological limits, constrained by interconnect and electrostatic constraints[1]. Vertical stacking has emerged as a solution to scaling limits, highlighting the need for new electronics materials with silicon process compatibility for back-end-of-line (BEOL) applications[2,3]. While various n-type materials, including indium oxide-based semiconductors[4,5] and 2D materials such as MoS_2[6,7,8], are readily available, efficient p-type counterparts remain scarce, limiting the development of fully complementary device technologies. Despite the challenges in realizing high-performance p-type semiconductors, their presence is essential in modern circuit design. Standard logic cells, such as complementary metal-oxide-semiconductor (CMOS), require pFET to achieve low power consumption[3]. In certain designs like capacitor-less two-transistor dynamic random-access memory (2T-DRAM), combining pFET and nFET can also reduce gate-coupling induced voltage drop at the storage node, improving data retention[9]. Recently, Te-based materials, characterized by their covalently-bonded helical atomic chains coupled via van der Waals forces and their favorable hole transport properties, have attracted increasing attention across a wide range of applications, including gas sensing, optoelectronics, photodetection, and neuromorphic computing[10,11,12,13,14,15,16,17,18]. Among them, tellurium (Te), especially its chiral trigonal phase, has emerged as a promising p-type semiconductor[19]. Te exhibits exceptionally high hole mobility[19,20], compatibility with low-temperature processing[20,21,22], scalability down to few-nanometer thicknesses and wafer-scale production[23].

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Despite these advantages, Te transistors still suffer from V_T drift and pronounced hysteresis under gate bias stress, which hinders their practical use in memory and logic applications[21,24,25,26]. Such hysteresis issues are common in other nanoscale systems such as CNTs, MoS_2, and graphene[27,28,29,30]. The increased surface-to-volume ratio of these nanomaterials makes them highly sensitive to attached molecules and interface states, which could strongly modulate the overall carrier concentration[31,32,33]. When carrier concentration changes dynamically during gate sweeps, a threshold voltage (V_T) shift between forward and reverse sweeps is observed as hysteresis. This hysteresis leads to inconsistent switching voltages, causing reliability issues and degradation of key electronic properties such as mobility and switching speed. Therefore, understanding and mitigating hysteresis is essential for the reliable integration of Te-based transistors into advanced integrated circuits.

In Te-based FETs, hysteresis is previously attributed to trap states at the Te/dielectric interface or within native oxides[21,24,25,26]. Moreover, the morphology of the Te layer, including its thickness and structural form (e.g., film or nanorod), can also influence the degree of hysteresis[34]. Thinner Te layers tend to exhibit more pronounced hysteresis due to enhanced surface and interface effects. A post-deposition annealing process is a common approach for reducing hysteresis by improving crystallinity. In addition, encapsulation serves as an effective strategy to reduce hysteresis by passivating defects and blocking interactions with ambient species. Although various studies have explored hysteresis suppression strategies, the underlying mechanisms of V_T shifts and hysteresis are still not fully understood.

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In this study, the hysteresis in Te-based transistors was systematically investigated under various electrical measurement conditions. The results reveal that V_T shift associated with hysteresis is strongly dependent on both the direction and the range of the gate voltage sweep. This behavior is attributed to gas adsorption, as evidenced by the observed reduction in hysteresis when measurements are conducted in a vacuum chamber. We show that dual-side Al_2O_3 encapsulation effectively isolates the Te channel from ambient gases, enhancing electrical performance to achieve a mobility of ~80 $cm^2 V^{-1} s^{-1}$, I_{ON}/I_{OFF} ratio of ~10^5, and long-term air stability with improved bias-stress reliability. In addition, sweep-rate-dependent measurements indicate that the dual-gate structure effectively suppresses the current degradation induced by hysteresis and maintains a small hysteresis window (< 1 V) even under slow gate voltage sweeping conditions (0.0025 $V s^{-1}$). By decoupling the Te channel from environmental factors through dual-side encapsulation, we show a stable p-type platform that resolves the reliability bottleneck for Te transistors.

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RESULTS

Tellurium thin-film properties and exposed device performance

Several approaches for synthesizing crystalline Te have recently been developed to improve film quality and device performance. Hydrothermal method is a widely used approach to achieve two-dimensional Te, which yields high-quality crystalline flakes[19]. Chemical vapor deposition techniques

were also developed to produce Te nanostructures, such as nanobelts and nanoplates, with high crystallinity and comparable transport performance[35, 36]. In this work, we employed a recently developed cryogenic thermal evaporation[21,22] to deposit Te onto bottom-gated substrates (details in Experimental Section). Amorphous Te was first deposited at cryogenic substrate temperatures and subsequently crystallized into nanocrystalline films with controllable domain sizes as a function of the substrate temperature. Using cryogenic thermal evaporation, Te films form micrometer-scale crystalline domains (Figure 1a and Figure S1) with smooth surfaces confirmed by atomic force microscopy (Ra = 0.47 nm, inset of Figure 1a). Moreover, this deposition approach is advantageous for lowering the thermal budget during film formation, making it a promising candidate for BEOL integration. Raman spectroscopy was used to analyze the crystallinity and interchain interactions of trigonal Te (Figure 1b). Te atoms form helical chains along the c-axis through covalent bonding with two nearest neighbors (inset, Figure 1b), resulting in an equilateral triangle projection on the basal plane. Three characteristic first-order Raman modes are clearly observed at 92 cm^{-1} (E1), 123 cm^{-1} (A1), and 140 cm^{-1} (E2). The A1 mode corresponds to in-plane chain expansion, while E1 and E2 are related to bond-bending and bond-stretching vibrations. X-ray photoelectron spectroscopy (XPS) confirms the elemental composition and chemical state of the evaporated Te film (Figure 1c). Peaks at ~572.9 eV ($3d_{5/2}$ orbitals) and ~583.3 eV ($3d_{3/2}$ orbitals) correspond to neutral Te (Te^0), while those at ~576.3 ($3d_{5/2}$ orbitals) and ~586.7 eV ($3d_{3/2}$ orbitals) indicate the presence of Te^{4+}. Depth profiling using Ar plasma etching reveals that Te^0 is the dominant species throughout the film, indicating a high-purity Te composition with minimal formation

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of TeO_x. Despite the high crystallinity of Te film, electrical measurements in ambient conditions reveal a large hysteresis in transfer characteristics I_D-V_G (Figure 1d; output characteristics in Figure S2). Compared to the measurement in air, hysteresis is reduced mainly by ~15 V while measuring in vacuum (10^{-5} Torr), indicating that adsorbed gas molecules play a significant role in the hysteresis and electrical performance of exposed Te transistors (the V_D-dependent I_D-V_G in Figure S3). Like other nanomaterials-based transistors, the carrier concentration of Te transistors could be modulated by the surrounding materials due to the high surface-to-volume ratio.

The hysteresis of exposed Te transistors is highly sensitive to gate bias conditions and becomes increasingly pronounced as the gate voltage sweep range expands. When the initial V_G is fixed at -30 V and the sweep range is extended from -10 V to +30 V, the hysteresis enlarges from ΔV_T = 5 to 36 V (Figure 1e). Notably, a sudden increase in I_D is consistently observed at the reversal point of the gate sweep, which is triggered by the change in sweep direction rather than the gate voltage polarity. This behavior persists even when V_G is swept entirely within the negative bias regime and is similarly observed when the initial V_G is fixed at +30 V (Figure S4), indicating that the hysteresis is governed by the sweep direction rather than the sign of the applied gate bias. Similar hysteretic behavior has also been reported in other p-type nanomaterials, such as WSe_2 and carbon nanotubes[7,28,37,38,39].

To explain this gate-polarity-independent switching behavior, a dynamic model involving interactions between atmospheric species adsorbed on the Te surface is proposed (Figure 1f). During gate voltage sweeping, modulation of the electrostatic potential alters the hole concentration and

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chemical potential of the Te channel, thereby driving the reorientation of surface-bound polar molecules. Sweep directions that induce hole depletion promote outward dipole reorientation and suppress carrier density, whereas sweep directions favoring hole accumulation induce inward dipole reorientation, enhancing hole density and leading to abrupt current changes. This dipole-mediated process is further supported by an Arrhenius activation energy of ~0.0405 eV (Figure S5), consistent with dipolar reorientation of weakly bound gas molecules[30,40,41,42]. In addition, reversible V_T shifts observed upon alternating between vacuum and ambient environments, a characteristic re-adsorption time constant of $\tau \approx 2$ s, and the pronounced sweep-rate dependence of hysteresis (Figure S6-S8) collectively confirm the gas-related and reversible nature of this hysteresis mechanism. In contrast, the lack of a noticeable reduction in hysteresis after device transfer or the insertion of an hBN interfacial layer suggests that interface traps play only a minor role in the hysteresis behavior of exposed Te devices (Figures S9 and S10).

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Electrical characteristics of different device configurations

To suppress hysteresis, different encapsulation layers were employed to limit gas molecule adsorption on the Te channel. Owing to the relatively low thermal stability of Te compared with other 2D materials or oxide semiconductors, SiO_2 and Al_2O_3 were selected as encapsulation layers due to their low process temperatures. As shown in Figures 2a and 2b, both encapsulation layers effectively

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reduce electrical hysteresis in the voltage sweep loop, confirming that restricting gas adsorption suppresses V_T drift induced by dipole reorientation. Despite this general suppression, devices encapsulated with Al_2O_3 consistently exhibit higher I_{ON} and long-term air stability than those with SiO_2 encapsulation (Figure S11-S12). This improvement is attributed to the denser structure of Al_2O_3, which provides superior gas barrier properties, as well as its higher dielectric constant that enhances dielectric screening of Coulomb scattering and mitigates mobility degradation. A similar trend is also observed in devices employing Al_2O_3 as the bottom-gate dielectric (Figures 2c and 2d). The extracted mobility and I_{ON}/I_{OFF} ratios for all device configurations are summarized in Figure 2e, showing that Al_2O_3-encapsulated devices outperform their SiO_2-encapsulated counterparts regardless of the bottom-gate dielectric. The dynamic stability of encapsulated devices was evaluated through sweep-rate-dependent I_D-V_G measurements. Compared with exposed devices, both SiO_2- and Al_2O_3-capped devices exhibit markedly reduced hysteresis at slower sweep rates, indicating partial suppression of dipole-induced hysteresis (Figure S13). However, residual hysteresis and V_T drift persist, suggesting the involvement of charge trapping.

Notably, the hysteresis of capped devices depends strongly on both sweep range and measurement frequency. At smaller sweep ranges, the hysteresis of SiO_2-capped devices exceeds that of Al_2O_3-capped devices only at lower measurement frequencies. However, as the sweep range increases, the crossover occurs at higher frequencies, with the hysteresis of SiO_2-capped devices surpassing that of Al_2O_3-capped devices even at relatively high measurement frequencies. This trend arises from differences in

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trap state distributions and trapping/detrapping time constants between the two dielectrics. Based on band-alignment considerations[43,44], an enlarged sweep range brings trap states in SiO_2 closer to the Te Fermi level, increasing the likelihood of charge trapping (Figure S14), whereas trap states in Al_2O_3 are energetically closer even at smaller sweep ranges, leading to earlier but more gradual trap participation. These results indicate that although dielectric encapsulation effectively suppresses gas-induced hysteresis, charge trapping associated with dielectric band alignment remains a limiting factor in single-gate capped devices. Similar residual hysteresis behaviors attributed to charge trapping have also been reported in other low-dimensional transistor systems[45,46,47,48,49,50,51,52,53,54,55,56,57,58] and a comparative summary is provided in Table S1. These limitations in single-gate capped devices motivate the adoption of a dual-gate architecture to further stabilize channel electrostatics.

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Electrical characteristics of dual-gate devices

A dual-gate device was subsequently fabricated using Al_2O_3 as both the top- and bottom-gate dielectrics, based on the superior performance of Al_2O_3 in both encapsulation and bottom-gate configurations. Figure 3a shows the I_D-V_G characteristics measured by sweeping the bottom-gate voltage while the top-gate bias was fixed. The device schematic is presented in the inset. As the top-gate voltage is varied from +2 V to -2 V, the threshold voltage shifts toward more negative values, confirming effective modulation of the channel carrier concentration by the top gate. Compared with single-gate configurations, the dual-gate Te transistor exhibits minimal hysteresis and no abrupt current

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fluctuations, indicating a more stable electrostatic environment during gate operation (Figure S15). The I_D-V_D characteristics (Figure 3b) display a linear response at low drain bias, suggesting good contact quality, and the output curves remain stable without noticeable current degradation. These results demonstrate that the dual-gate architecture provides enhanced electrostatic control beyond what can be achieved by encapsulation alone.

To independently evaluate the long-term stressing effects of the top and bottom gates, bias stress experiments were applied to each gate separately. In the positive bias stress (PBS, V_G = +3 V) and negative bias stress (NBS, V_G = -3 V) tests, dual-sweep I_D-V_G measurements were performed before and after each stress step in an interleaved measurement–stress–measurement (MSM) sequence. During the measurements, either the top or bottom gate was swept while the non-swept gate was fixed at 0 V. To minimize measurement-induced effects, a sweep rate of 250 V s^{-1} was used. The MSM cycle was repeated until the cumulative stressing time reached 1000 s. The corresponding I_D-V_G characteristics and extracted V_T changes are shown in Figures S16.

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The hysteresis was extracted from the V_T difference between forward and reverse sweeps of each I_D-V_G loop, whereas V_T shift was obtained from the evolution of the forward-sweep V_T after each stress interval. After either stress condition, the increase in hysteresis remains below 0.2 V, whereas a noticeable V_T shift is observed (Figures 3c and 3d). This behavior is attributed to charge storage within the gate dielectric, where the detrapping time constants are longer than the gate-voltage sweep time.

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Therefore, these charges do not significantly contribute to the measured hysteresis. Among the two gate operations, bottom-gate operation exhibits slightly improved hysteresis and V_T stability.

Sweep-rate-dependent electrical characteristics

To directly compare the dynamic stability of the dual-gate device with that of the exposed device, the sweep-rate dependence of the transfer characteristics was examined. The exposed device exhibits pronounced hysteresis broadening accompanied by severe I_{ON} degradation as the sweep rate decreases to 0.0025 V s^{-1} (Figure 4a). For the dual-gate device, sweep-rate dependence was evaluated separately for top-gate and bottom-gate operations, with the non-swept gate held at 0 V during measurements (Figures 4b and 4c). In contrast to the exposed device, neither gate operation shows pronounced hysteresis variation or significant I_{ON} degradation over the entire sweep-rate range. A direct comparison of I_{ON} as a function of sweep rate further reveals that bottom-gate operation consistently outperforms top-gate operation across all sweep rates, although both configurations effectively suppress I_{ON} degradation to well below one order of magnitude (Figure 4d). By converting the sweep rate to the corresponding measurement frequency (details provided in the Methods), the extracted V_T shift and hysteresis were further compared (Figures 4e and 4f). Regardless of whether top-gate or bottom-gate operation is employed, the dual-gate device maintains hysteresis below 1 V across the entire measurement frequency range. Among all device configurations, the dual-gate structure provides the most effective hysteresis suppression. Maintaining one gate electrode at a fixed potential stabilizes the

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electrostatic environment during operation of the opposite gate, thereby minimizing hysteresis arising from both dynamic carrier modulation and charge trapping. All sweep-rate-dependent measurements were independently repeated on two separate devices to verify reproducibility (Figures S17-S21). Collectively, these results demonstrate that the dual-gate architecture enables reliable and controllable operation of Te transistors. The improved hysteresis stability under ambient conditions highlights the suitability of the dual-gate Te device for practical applications.

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DISCUSSION

In this study, the hysteresis behavior of Te devices was systematically investigated. The primary origin of hysteresis in exposed Te FETs is attributed to remote electrostatic effects induced by ambient gas molecules possessing dipole moments. Notably, under different sweep rates, the I_{ON} of exposed Te devices can vary by more than one order of magnitude. Although vacuum measurement or thermal annealing can partially remove the adsorbed gas molecules and temporarily reduce hysteresis, the hysteresis rapidly recovers to its original level once the devices are returned to ambient conditions and room temperature. This behavior indicates that such approaches cannot permanently prevent gas adsorption and therefore cannot provide long-term suppression of hysteresis.

Building on this mechanistic insight, we demonstrate that capped Te device with a dense gas barrier significantly suppresses hysteresis. This suppression leads to substantial improvements in key performance metrics, including mobility (80~100 cm^2 V^{-1} s^{-1}) and I_{ON}/I_{OFF} ratio (~10^5) under ambient

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conditions, especially for ultrathin Te channels. For both the capped and dual-gate devices, the remaining hysteresis is primarily attributed to charge trapping effects. Notably, the dual-gate device exhibits markedly enhanced stability, showing minimal hysteresis variation (< 0.5 V) under prolonged bias stress for 1000 s. In addition, among all device configurations, the dual-gate structure exhibits the smallest hysteresis increase across all measurement frequencies and sweep ranges. These findings both deepen our understanding of hysteresis in Te and push the performance boundary of p-type semiconductors. Such enhancements support the practical integration of Te into BEOL technologies, including scalable 3D architectures and monolithic stacking schemes.

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METHODS

Fabrication of Te Thin-films

Te thin films were prepared through thermal evaporation at cryogenic temperatures. The Te source pellets (99.999%, Well Being) were loaded into a tungsten boat coated with Al_2O_3, which provided more stable deposition rate control and avoided interaction between Te and tungsten. Substrates such as SiO_2/p^+-Si or Al_2O_3/p^+-Si were attached to the chuck using polyimide tape (Kapton). Small channels on the outside of the chuck allowed liquid nitrogen to flow through and cool the chuck. Once the chamber

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pressure reached 10^{-6} Torr and the substrate cooled down to -80 °C, Te was deposited at a rate of 1 Å/s. During deposition, Te remained in the amorphous phase. After the deposition, the chuck was left to warm up for 30 minutes until the temperature reached 0 °C. It was then maintained at 0 °C to -5 °C for another 30 minutes to allow the Te film to crystallize. With this process, the Te film exhibited large domains under optical microscopy. After deposition, the substrate was gradually warmed to room temperature (~20 °C) before being exposed to ambient air, minimizing the risk of water condensation on the film surface.

Film characterizations

Raman spectroscopy was performed using a UniDRON confocal micro-Raman system (CL Technology Co., Ltd., Taiwan) with a 532 nm laser, focused to a 1 μm spot size through a 100× objective lens. Spectra were collected under a laser power of 1 mW. X-ray photoelectron spectroscopy (XPS) was employed to analyze the chemical composition of Te 3d, using a Mg Kα X-ray source (1253.6 eV). A flood gun was applied to neutralize surface charging. To obtain the depth profile, the Te thin film was further etched using an argon ion beam. A polarized optical microscope was employed in bright-field mode to observe the domain size of the Te film. The use of a linear polarizer in the illumination path enhanced the optical contrast between each crystalline domain, allowing for direct visualization of domain size and distribution. For improved identification of domain boundaries, dark-field imaging was also performed after removing the polarizer, which provided enhanced edge contrast.

Device fabrication

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For the SiO_2 bottom-gate device, a 50 nm thermal oxide layer was grown on the p^+-Si substrate via dry oxidation in a furnace. A photoresist (AZ5214E) was spin-coated onto the substrate and patterned by standard photolithography to define the active area prior to Te deposition. After the Te deposition, a 30 nm Ni layer was deposited to serve as the source/drain (S/D) metal contacts. The fabrication process for the Al_2O_3 bottom-gate device followed a similar flow, except that a 20 nm Al_2O_3 gate dielectric was deposited on the p^+-Si substrate by atomic layer deposition (ALD) at 150 °C, using trimethylaluminum (TMA) and H_2O as precursors. For device encapsulation, two types of dielectric layers were used. SiO_2 was deposited by e-beam evaporation, and Al_2O_3 was deposited using the same ALD process described above. Both encapsulation layers had a thickness of 20 nm. The dual-gate structure was fabricated by depositing an additional Ni pad as the top gate electrode on top of either encapsulated configuration. All fabricated devices had a channel length (L) of 3 μm and a width (W) of 10 μm.

Electrical characterizations

The electrical measurements were conducted under ambient conditions using a Keysight B2902B parameter analyzer. For all I_D-V_G transfer characteristics, the V_D was fixed at -0.5 V. For devices with a SiO_2 gate dielectric, the gate voltage was swept with a step size of 0.125 V and a dwell time of 20 ms per step, corresponding to an effective sweep rate of 6.25 V s^{-1} (for example, when sweeping from -30 V to +30 V). For devices with an Al_2O_3 gate dielectric, a smaller step size of 0.05 V was used with the same dwell time of 20 ms per step, yielding a sweep rate of 2.5 V s^{-1} (for example, when sweeping from -5 V to +5 V). The V_T was extracted using the constant-current method, where V_T was defined as the

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gate voltage corresponding to $I_D = 10^{-8}$ A. Hysteresis was calculated as the difference in V_T between the forward and reverse gate voltage sweeps. The field-effect mobility (μ_{FE}) was extracted using the equation $\mu_{FE}=g_m L V_D^{-1} Cox^{-1} W^{-1}$, where L and W are the channel length and width, V_D is the drain voltage, Cox is the gate oxide capacitance, and g_m is the transconductance, calculated as $g_m=dI_D/dV_G$. The extracted mobility and I_{ON}/I_{OFF} values were obtained from over twelve devices for each structure, providing the basis for the error bars. The I_D-V_D output characteristics were measured by sweeping V_D from 0 to -3 V, with the gate voltage fixed at values ranging from 0 to -5 V. The measurement frequency was defined as the inverse of the total duration of one complete dual gate-voltage sweep (forward and reverse). For example, for a sweep range of -3 V to +3 V operated at a sweep rate of 2.5 V s^{-1}, the total dual-sweep time is 4.8 s, corresponding to a measurement frequency of approximately 0.21 Hz. All devices measured in the frequency-dependent experiments use Al_2O_3 as their bottom-gate dielectric.

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Data Availability

The datasets generated and/or analyzed during the current study are not publicly available due to ongoing further studies but are available from the corresponding author on reasonable request.

COMPETING INTEREST

The authors declare no competing financial or non-financial interests.

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AUTHOR CONTRIBUTION

S.-T. W., K.-W. L. and D.-H. L. conceived the idea. S.-T. W. and K.-W. L. performed the device fabrication and the measurement. S.-T. W., K.-W. L., T.-T. W. and Y.-C. C. helped the thin film growth. C.-F. C. helped the device measurement. C.-C. Chung and C.-H. L. carried out the TEM and Raman analysis. C.-Y.C. carried out the XPS analysis. S.-C. C. designed and developed the Low-T PVD tools. T. A. assisted with device simulations. S.-T. W., K.-W. L., Y.-L. C. and D.-H. L. analyzed the data. S.-T. L., Y.-F. L., I. R., T. Y. T. H., and C.-C. Cheng provided scientific guidance throughout. Y.-L. C. and D.-H. L. supervised the research. S.-T. W., K.-W. L., Y.-L. C. and D.-H. L. prepared the paper draft. All the authors contributed to the discussion and manuscript preparation and read the final manuscript.

ACKNOWLEDGEMENTS

D.-H. L. acknowledges support from the National Science and Technology Council (NSTC 114-2112-M-A49-013), the NSTC T-Star Center Project: Future Semiconductor Technology Research Center (NSTC 114-2634-F-A49-001), the Ministry of Education (Yushan Scholar Program), and Taiwan Semiconductor Manufacturing Company. Y.-L. C. acknowledges support from the National Science and Technology Council, Taiwan (NSTC 113-2112-M-007-034-MY3, 114-2119-M-007-015-MBK, and 114-2628-E-007-001). We thank Integrated Service Technology (iST) for support with material characterization.

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Supporting Information

The Supporting Information is available.

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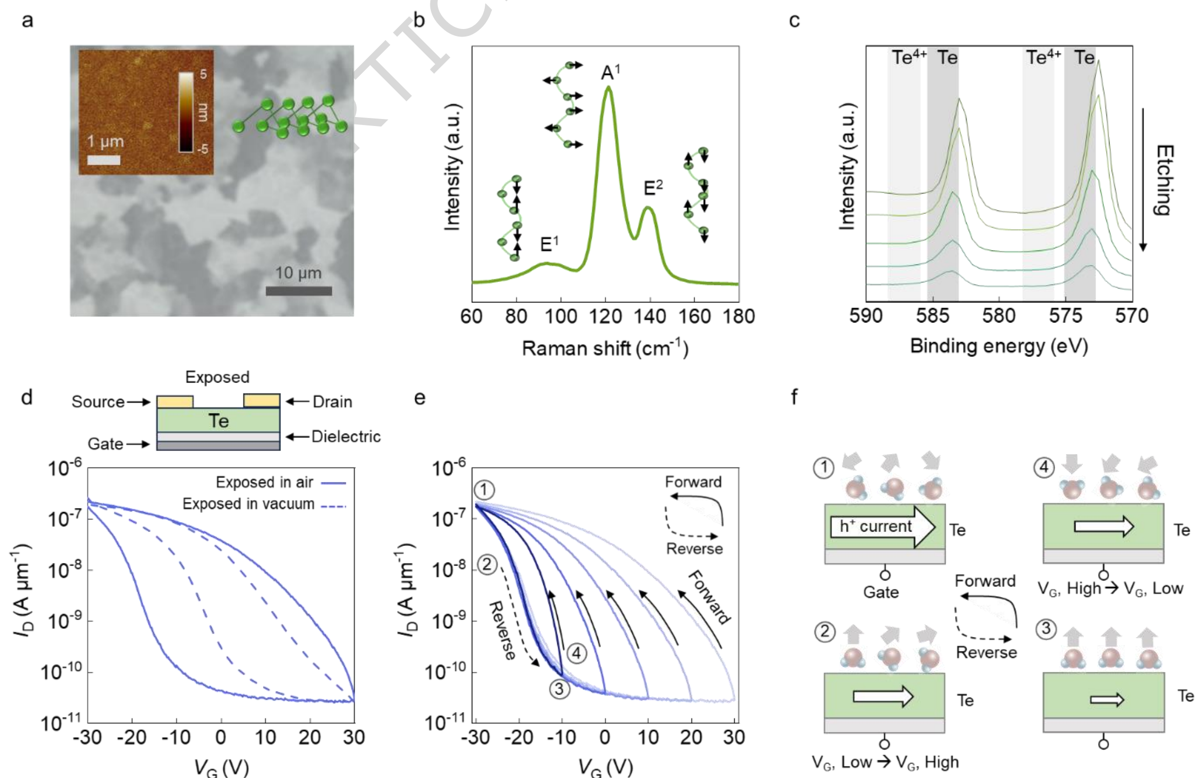

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Figure 1: Characterization of Te films and Te transistors. (a) Optical microscopy and atomic force microscopy (AFM) images of the Te film; the inset illustrates the chiral helical chain structure of tellurium. (b) Raman spectra of the evaporated Te thin film, showing characteristic E_1, A_1, and E_2 modes. (c) XPS depth profile of Te thin film, indicating the presence of Te^0 and minimal Te^{4+}. (d) Transfer characteristics of the Te FET measured in ambient air and under vacuum (10^{-5} Torr). (e) Dual-sweep transfer characteristics of the Te FET at a drain bias of V_D = -0.5 V, starting from -30 V and sweeping to -20, -10, 0, +10, +20, +30 V. (f) Schematic illustration of gas molecule adsorption and dipole moment interaction with the Te device during a dual-sweep gate voltage loop starting from -30 V.

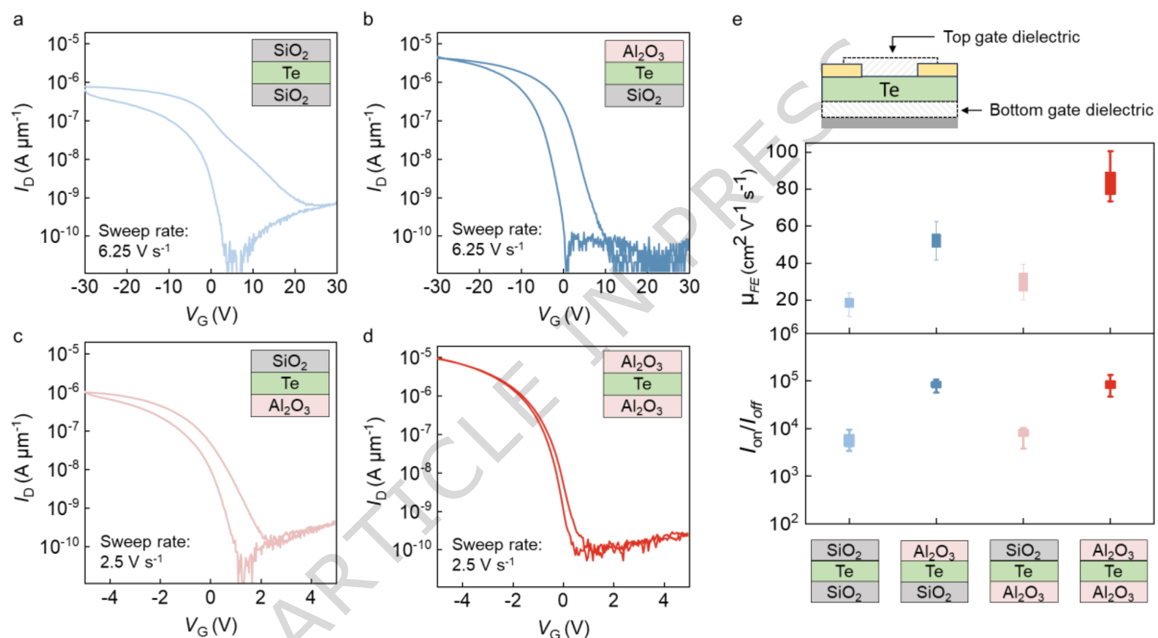

Figure 2: Transfer characteristics and extracted performance metrics of Te FETs with different encapsulation and bottom-gate dielectric layer configurations. Transfer characteristics of Te FETs (L = 3 μm, W = 10 μm) measured at a drain bias of V_D = -0.5 V, with the following combinations of encapsulation and bottom-gate dielectric layers: (a) SiO_2 encapsulation and SiO_2 bottom-gate dielectric, (b) Al_2O_3 encapsulation and SiO_2 bottom-gate dielectric, (c) SiO_2 encapsulation and Al_2O_3 bottom-gate dielectric, and (d) Al_2O_3 encapsulation and Al_2O_3 bottom-gate dielectric. (e) Extracted field-effect mobility and I_{ON}/I_{OFF} of four device structures described in (a)-(d), along with a schematic illustration of the device configuration.

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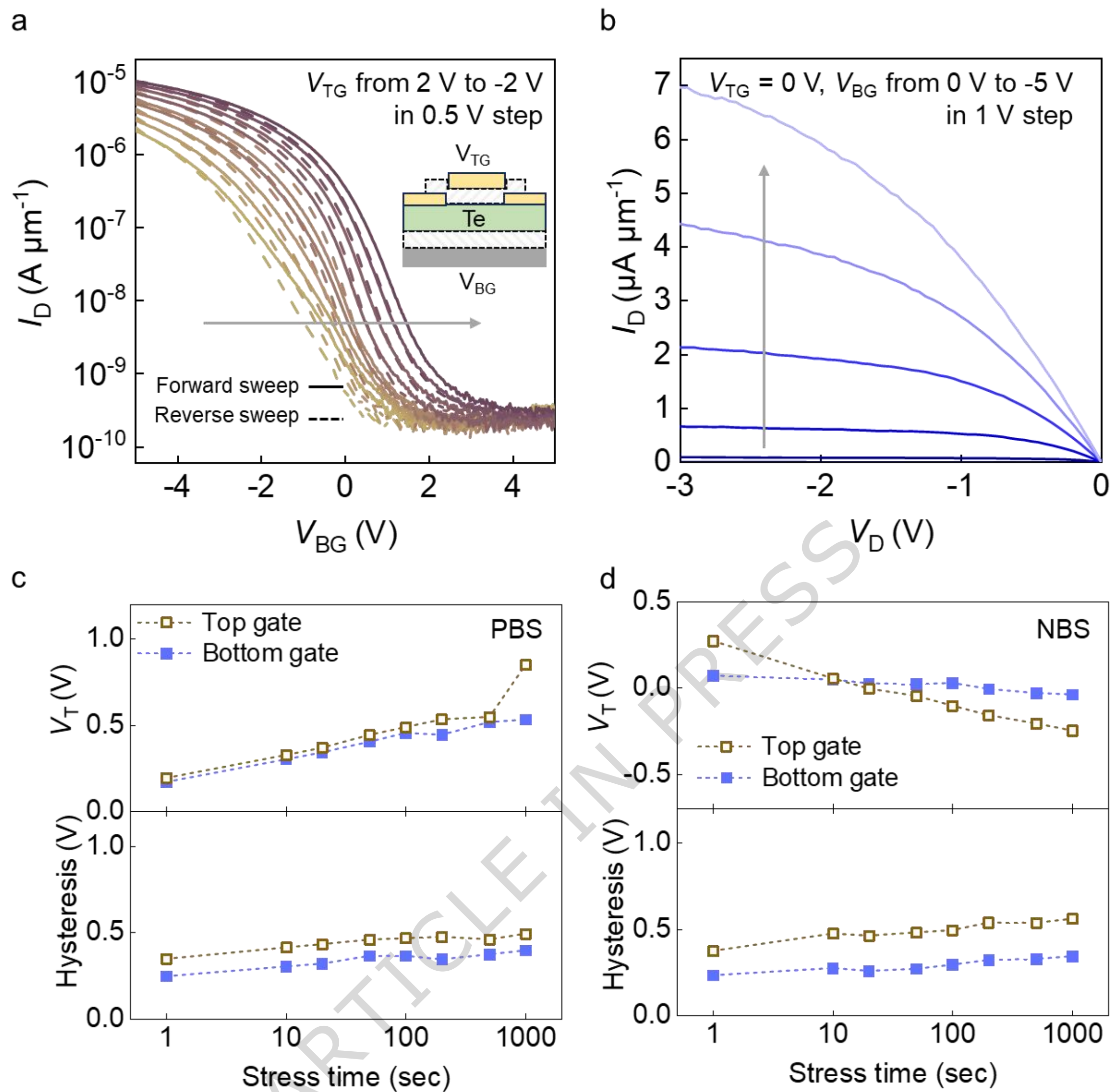

Figure 3. Electrical performance of dual-gate Te devices. (a) Transfer characteristics (I_D-V_G) of the dual-gate Te device measured with the back gate swept and the top gate fixed at different voltages. The sweep rate was 2.5 V s^{-1}. Insets show the device schematic. (b) Output characteristics (I_D-V_D) of the dual-gate Te transistor, measured by sweeping the drain voltage at different back-gate biases while keeping the top gate fixed at 0 V. (c) V_T extracted from forward sweeps and hysteresis extracted from dual sweeps of the dual-gate device under positive bias stress (PBS, V_G = +3 V) for 1000 s. (d) V_T extracted from forward sweeps and hysteresis extracted from dual sweeps under negative bias stress (NBS, V_G = -3 V) for 1000 s. The top gate and back gate were examined separately, while the other gate was fixed at 0 V during the stress tests. All devices have a channel length (L) of 3 μm and a width (W) of 10 μm, and measurements were performed at a drain bias of V_D = −0.5 V.

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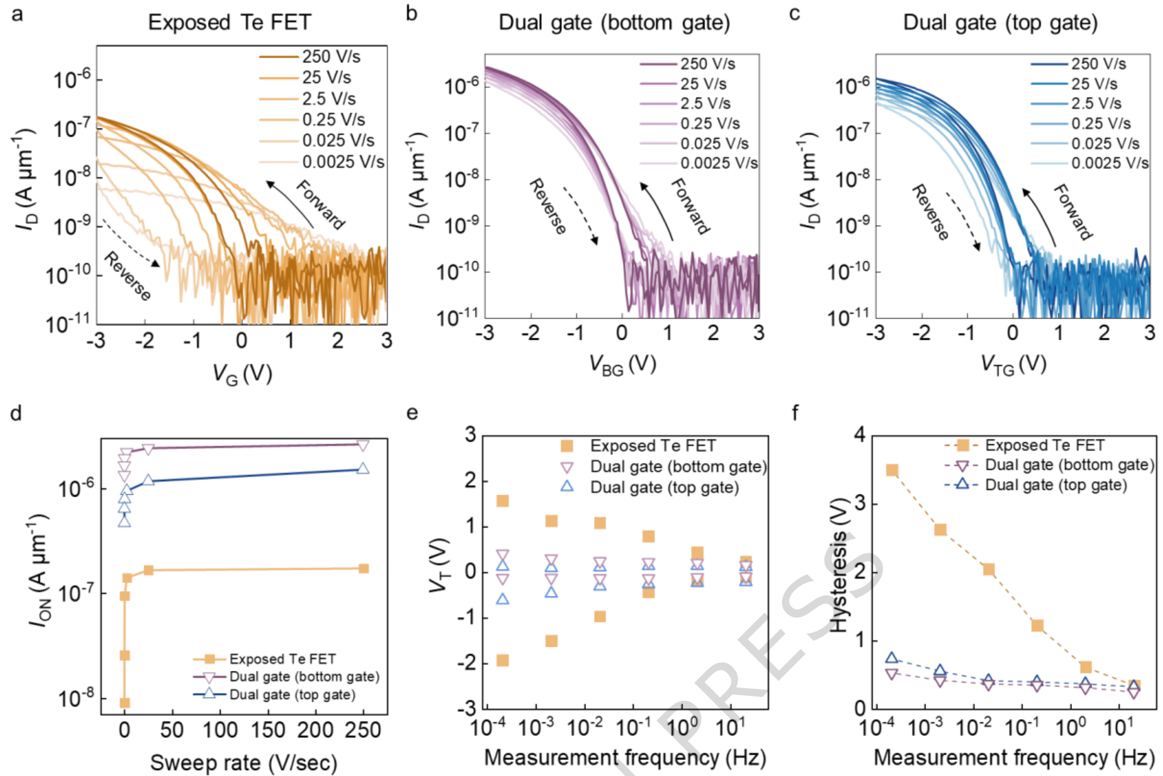

Figure 4. Electrical performance of Te devices under different sweep rates and device configurations. (a) Transfer characteristics (I_D-V_G) of the exposed Te FET measured at different sweep rates. (b) Transfer characteristics (I_D-V_G) of the dual-gate Te FET measured at different sweep rates with the back gate swept. (c) Transfer characteristics (I_D-V_G) of the dual-gate Te FET measured at different sweep rates with the top gate swept. All devices have a channel length (L) of 3 μm and a width (W) of 10 μm, and measurements were performed at a drain bias of V_D = -0.5 V. (d) I_{ON} as a function of sweep rate for different device configurations. (e) Extracted threshold voltage for different device configurations under different measurement frequencies. (f) Extracted hysteresis voltage for different device configurations under different measurement frequencies.

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