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Integration of freestanding hafnium zirconium oxide membranes into two-dimensional transistors as a high-κ ferroelectric dielectric

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Two-dimensional semiconductors could be used as a channel material in miniaturized transistors with high gate control. However, the lack of insulators that are both compatible with two-dimensional materials and suitable for integration into a fully scalable process flow limits development. Here we show that freestanding hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$; HZO) membranes can be integrated with two-dimensional semiconductors as a high-κ dielectric. The HZO membranes can be varied in thickness from 5 to 40 nm, and be transferred onto molybdenum disulfide (MoS_2) to create the top-gate dielectric in field-effect transistors. A 20-nm-thick HZO membrane exhibits a dielectric constant of 20.6 ± 0.5 and a leakage current (at 1 MV cm^{-1}) of under 2.6×10^{-6} A cm^{-2}, below the requirements of the International Technology Roadmap for Semiconductors, as well as typical ferroelectric behaviour. The MoS_2 transistors with HZO dielectric exhibit an on/off ratio of 10^9 and a subthreshold swing below 60 mV dec^{-1} across four orders of current. We use the transistors to create an inverter, logic gates and a 1-bit full adder circuit. We also create a MoS_2 transistor with a channel length of 13 nm, which exhibits an on/off ratio of over 10^8 and a subthreshold swing of 70 mV dec^{-1}.

Silicon-based complementary metal–oxide–semiconductor (CMOS) technology has advanced through the miniaturization of transistors such that more than 1 billion devices can now be integrated on a single chip[1,2]. However, the reduction in transistor size also introduces challenges, including heat dissipation and mobility degradation[3–5]. Two-dimensional (2D) semiconductors are a potential alternative channel material to silicon for next-generation electronics due to their atomically thin nature and excellent gate controllability[6–12]. However, to create logic circuits with such materials requires integrating high-quality, high-κ (κ denotes the relative dielectric constant) dielectrics onto the 2D semiconductor surfaces[10,13–27].

In silicon technology, high-κ dielectrics such as aluminium oxide (Al_2O_3) and hafnium oxide (HfO_2) can be easily deposited onto the semiconductor via atomic layer deposition (ALD), but applying ALD onto 2D semiconductors is challenging due to amorphous dielectrics and imperfect 2D interfaces[28,29]. One approach is to introduce thin polymer

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or molecular layers, which act as buffers to preserve the fragile 2D surfaces, but this can compromise stability and dielectric constant[14,19,26]. van der Waals insulators and ionic crystals, such as hexagonal boron nitride and mica, have been explored as ways to improve the insulator–channel interface and reduce trap states, but these remain difficult to integrate with silicon processing technology[13,20,24,30–32]. Recently, HfO_2-based high-κ oxides, carefully doped with zirconium ($Hf_{0.5}Zr_{0.5}O_2$; HZO), have been designed to achieve ferroelectric transitions while also being fully CMOS compatible and highly scalable[33]. In addition, developments in synthesis of freestanding (FS) oxide membranes have created a potential pathway for integrating high-κ HZO with 2D semiconductors[34,35].

In this Article, we show that freestanding ferroelectric HZO membranes can be created using a pulsed laser deposition (PLD) method and then transferred onto few-layer molybdenum disulfide (MoS_2) as the high-κ gate dielectric in field-effect transistors (FETs). To create freestanding membranes, a heterostructure of $La_{0.7}Sr_{0.3}MnO_3$ (LSMO)/HZO is epitaxially grown on a single-crystal $SrTiO_3$ (STO) substrate and the LSMO is sacrificed by immersing the samples in a dilute hydrogen chloride solution to detach the HZO. Capacitance–voltage measurements of 20-nm-thick freestanding HZO membranes show an average dielectric constant of $\varepsilon_r \approx 20.6 \pm 0.5$ and breakdown field strength of $E_{bd} \approx 2.2$ MV cm^{-1}, while robust ferroelectricity is confirmed through polarization–electric field measurements.

The MoS_2 FETs with HZO dielectric exhibit an on/off-current ratio (I_{on}/I_{off}) of about 10^9 at a source–drain voltage (V_{DS}) of 100 mV and within a top-gate voltage (V_{TG}) range of ±2.0 V, as well as an average subthreshold swing (SS) of 53 mV dec^{-1} at room temperature. The transfer curves exhibit a counterclockwise direction with nearly hysteresis-free operation, indicating the ferroelectric switching and effective gate controllability of the HZO membrane. Using noise fluctuations, we derive the density of interface states (D_{it}) to be about ~9×10^{10} cm^{-2} eV^{-1}. We use the HZO/MoS_2-based FETs to create inverters, logic gates and a 1-bit full adder. We also fabricate a short-channel MoS_2 FET with a 13-nm channel, which exhibits an I_{on}/I_{off} of nearly 10^8 and SS of 70 mV dec^{-1}.

Ferroelectricity of freestanding HZO membranes

Figure 1a illustrates the fabrication of high-quality freestanding HZO membranes via etching of the LSMO sacrificial layer grown epitaxially on a single-crystal STO substrate (Methods). Before transferring the membranes onto 2D semiconductors for device fabrication, we carefully investigated their crystallinity and ferroelectricity. High-resolution transmission electron microscopy (TEM) was carried out to reveal the microscopic lattice structure and phase distribution of the FS-HZO membranes. The plane-view atomic image of the 20-nm-thick FS-HZO, shown in Fig. 1b, exhibits well-defined HZO lattices with orthorhombic phase (o-phase), which occupies a large portion of the volume (details are available in Supplementary Fig. 1). The atomic force microscopy (AFM) topography of freestanding HZO, shown in Fig. 1c, reveals a smooth, flat surface. No visible cracks or residues are detected, indicating that the freestanding process has minimal impact on the structural integrity of the HZO. Figure 1d displays X-ray diffraction θ–2θ (θ denotes the Bragg angle, incident angle to the diffracting planes) scans for 10- and 20-nm-thick as-grown and freestanding HZO, using STO (001) and single-crystal silicon as substrates, respectively. The higher-angle shift and comparable full-width at half-maximum values of the Bragg peaks for o-phase HZO (111) suggest a minor relaxation of in-plane compressive strain and minimal crystallinity changes after freestanding[35]. Additionally, we collected thickness-dependent θ–2θ scans across a range of HZO thicknesses, from 5 to 40 nm, along with structural data in the off-normal direction, to confirm thickness-dependent behaviour and high crystallinity. Detailed results are provided in Supplementary Fig. 2. From the X-ray diffraction (XRD) and TEM results, we see that HZO thin films with thickness lower than 20 nm exhibit a relatively higher fraction of o-phase, primarily contributing to their ferroelectric properties. As a result, these films are considered ideal candidates for use as gate dielectrics.

To investigate the relationship between lattice symmetry and electronic structures in FS-HZO membranes of various thicknesses, we used linear polarization-dependent X-ray absorption spectroscopy (XAS), defining the difference between two orthogonal polarizations as linear dichroism, with the measurement geometry shown in Supplementary Fig. 3. Figure 1e shows the O *K*-edge XAS spectra of freestanding HZO membranes thinner than 20 nm, measured under linear polarized light. The insets display the thickness-dependent linear dichroism spectra for both as-grown and freestanding HZO. Supplementary Fig. 4 further provides spectra of additional thicknesses of FS-HZO for comparison. The spectral features are identified as e_g and t_{2g} of Hf 5*d* (Zr 4*d*) and Hf 6*sp* (Zr 5*sp*) in ascending energy order[36,37]. Benefitting from the d^0 configuration of Hf^{4+} (Zr^{4+}), the origin of the O *K*-edge linear dichroism in HZO is uniquely from the crystal field effect, reflecting the local lattice symmetry and structural distortion. Our primary focus is on the lowest energy peak of linear dichroism, the e_g states, which are highly excitonic in the XAS process, as depicted in the inset of Fig. 1e. The thick (here, 40 nm) HZO membrane shows a substantial negative linear dichroism ($E//c$–$E//ab$), indicating it remains in a non-polar centrosymmetric monoclinic phase (m-phase)[37,38]. With decreasing membrane thickness, the linear dichroism magnitude also reduces, ultimately becoming positive for the sub-10-nm HZO membrane, composed mainly of the o-phase. Such a reversal in linear dichroism sign points to a polar distortion in the o-phase HZO, hinting at the emergence of ferroelectric properties in thin HZO membranes[37] when film thickness is reduced. This observation agrees with the results obtained from XRD and TEM analyses. In addition, the trends of the linear dichroism spectra of as-grown HZO show limited differences compared to freestanding HZO, indicating that the overall quality of freestanding HZO membranes remains unchanged.

After identifying the lattice and electronic structures of freestanding HZO, contact Kelvin probe force microscopy (cKPFM) was conducted to investigate its ferroelectric properties at the microscopic scale. The cKPFM technique allows us to detect ferroelectricity resulting from spontaneous polarization while precluding artefacts caused by injected charges. Figure 1f,g displays the cKPFM measurements for the 10- and 20-nm-thick FS-HZO membranes, respectively. The nonlinear behaviour of cKPFM intensity as a function of read voltage with varying write voltages indicates strong ferroelectric responses in both membranes[39,40]. However, when the thickness exceeds 20 nm, a major suppression of ferroelectricity is observed, as shown in Supplementary Fig. 5.

To further investigate macroscopic ferroelectricity, Fig. 1h shows the piezoresponse force microscopy (PFM) image on a 20-nm-thick FS-HZO membrane. The observed box-in-box out-of-plane phase contrast verifies switchable polarization under an external electric field, showcasing resilient, non-volatile behaviour and low-leakage as a dielectric layer with robust ferroelectricity. Additionally, the spontaneous polarization of freestanding HZO was assessed through polarization–electric field (P–E) measurements, as shown in Fig. 1i. The 10-, 15- and 20-nm-thick FS-HZO membranes exhibit classic polarization hysteresis loops, confirming robust ferroelectricity. However, HZO membranes with thicknesses exceeding 20 nm, such as the 25-nm sample, display poor ferroelectricity, consistent with the dominance of the m-phase at greater thicknesses. Given the importance of scalability and practical application of freestanding HZO as gate layers, Fig. 1j demonstrates the successful transfer of a large-area 1×1 cm^2 HZO membrane. While this size is currently limited by laboratory-based PLD equipment, recent advancements in commercial PLD technology could enable the production of homogeneous epitaxial thin films up to 6–8 inches (roughly 15 to 20 cm) in size, thus overcoming this limitation and facilitating mass production.

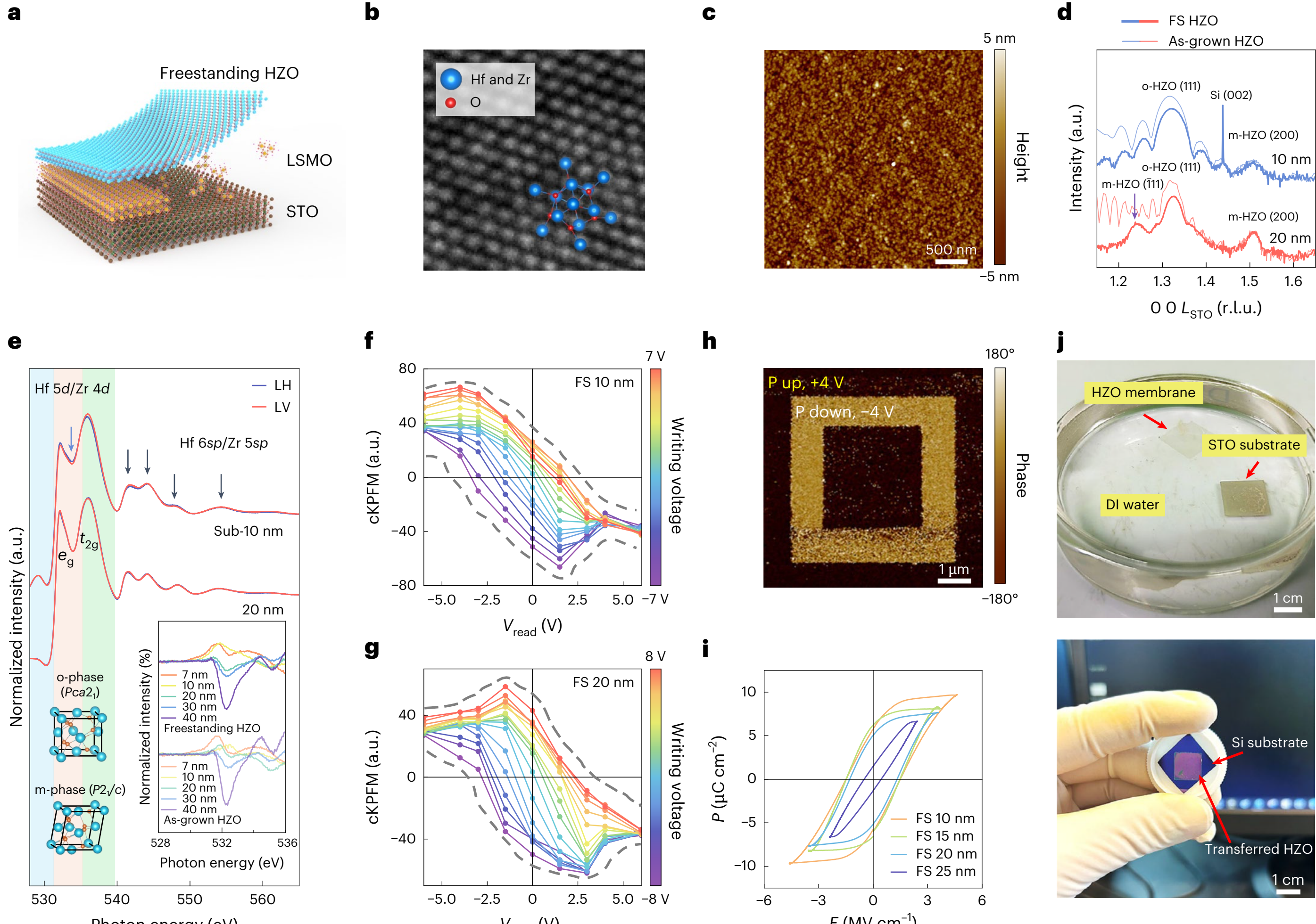

Fig. 1 | Fabrication and characterization of ferroelectric freestanding HZO membranes. a, Fabrication schematic for freestanding HZO membranes. **b**, TEM image showing the o-phase (111) of freestanding HZO, along with the corresponding lattice model. **c**, AFM image of a 20-nm freestanding HZO membrane, where the R_a value is 0.86 nm. **d**, XRD θ–2θ scans comparison between as-grown and freestanding HZO membranes at 10- and 20-nm thicknesses. The horizontal axis represents the out-of-plane (0 0 L_{STO}) reciprocal lattice vector, where 1 reciprocal lattice unit (r.l.u.) is defined as $2\pi/a_{STO}$, based on the lattice parameter of STO. **e**, Thickness-dependent grazing-incident XAS and X-ray linear dichroism (insets) of freestanding HZO near the oxygen *K*-edge, with schematic illustrations of the atomic lattices for both o- and m-phase HZO. The blue arrow indicates the splitting of the e_g band caused by the orthorhombic crystal field, while the black arrows highlight peaks in the *sp* hybridization region (>540 eV) consistent with monoclinic crystallinity. **f**,**g**, cKPFM measurements as a function of reading voltages for 10-nm (**f**) and 20-nm (**g**) FS-HZO membranes. The grey dashed lines are guides to the eye outlining the nonlinear cKPFM response, which is indicative of ferroelectric switching behaviour. **h**, Out-of-plane PFM image evidencing the switchable upward (P up) and downward (P down) ferroelectric polarization in freestanding HZO. **i**, Thickness-dependent polarization–electric field (*P*–*E*) hysteresis loops of freestanding HZO films. **j**, Large-area transfer of a 1 × 1 cm^2 HZO membrane onto a single-crystal silicon substrate. DI, deionized.

Dielectric and electrical properties of HZO membranes

The intrinsic electrical and dielectric properties of the dielectric gate layer are critical for device operations. A detailed investigation was carried out to explore the fundamental behaviour of freestanding HZO as a gate oxide, with a specific emphasis on its dielectric properties across different thicknesses. Figure 2a illustrates the schematic setup for measuring the dielectric and electrical properties, while Fig. 2b displays the dielectric constants across various thicknesses as a function of frequency. All freestanding HZO membranes exhibit high dielectric constants at room temperature, except for the 5-nm HZO membrane where increased defect contributions or leakage pathways degrade performance. Figure 2c plots the correlation between different HZO thicknesses and their dielectric constants at 1.5 kHz. The 20-nm-thick HZO exhibits an average dielectric constant of $\varepsilon_r \approx 20.6$, higher than other thicknesses and emphasizing the excellent quality and high-κ characteristics of the membranes.

To validate that freestanding HZO maintains its high dielectric performance under extreme conditions, the temperature-dependent dielectric frequency response was measured across a range of potential working temperatures, as shown in Fig. 2d. The primary focus here is to investigate the temperature-dependent behaviour of the 20-nm FS-HZO membrane, especially in light of its balance between strong ferroelectric and dielectric properties and minimal leakage. For comparison, Supplementary Fig. 6 shows frequency-dependent dielectric curves for FS-HZO membranes across various thicknesses. The 20-nm FS-HZO maintains a high dielectric constant of approximately $\varepsilon_r \approx 20.2$ at 100 °C and 1.5 kHz, despite a slight decrease with increasing frequency. Additionally, Fig. 2e shows that the dielectric properties of the 20-nm membrane consistently outperform those of other thicknesses across all temperatures, with reductions in dielectric constant remaining minimal (that is, less than 10%) from room temperature to 100 °C for all thicknesses.

In transistors, essential performance metrics include minimal leakage current and strong breakdown strength of the dielectric materials.

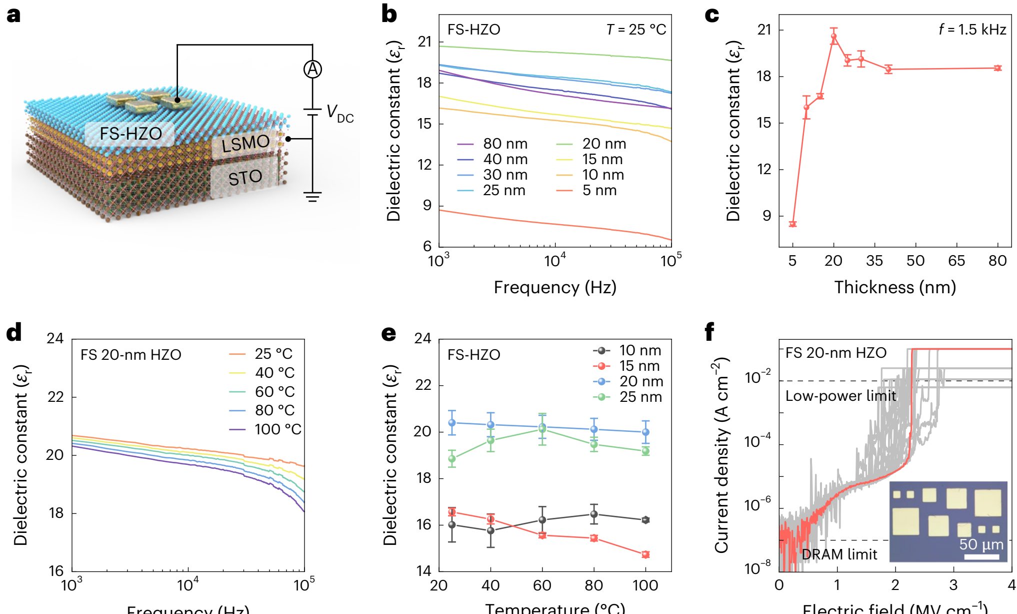

Fig. 2 | Dielectric and electrical properties of HZO membranes. a, The structure of the metal–insulator–metal device for dielectric characterizations, where the HZO membranes are transferred onto large-area LSMO-bottom-electrode buffered STO substrates, complemented by patterned Cr/Au top electrodes. **b**,**c**, Thickness-dependent frequency response versus dielectric response (**b**), along with the dielectric constants acquired at a frequency of 1.5 kHz as a function of thickness (**c**). **d**, Frequency dielectric response of 20-nm FS-HZO at various temperatures. **e**, Temperature-dependent dielectric behaviours of freestanding HZO across thicknesses at 1.5 kHz. **f**, Current density curve analysis in response to external electrical field for the 20-nm FS-HZO membranes. The inset shows different electrode areas ranging from 10 × 10 to 40 × 40 µm^2. Notice that data points in **c** and **e** represent mean values, with error bars indicating the standard deviation from three independently fabricated capacitor devices measured under identical conditions.

Figure 2f depicts the current density curves relative to the applied electrical field. The leakage current for the 20-nm HZO membrane, measured at below 2.6×10^{-6} A cm^{-2} under an external field of 1 MV cm^{-1}, is nearly four orders of magnitude below the low-power requirement (10^{-2} A cm^{-2}) from the International Technology Roadmap for Semiconductors. A marked current surge indicates electrical breakdown, occurring at approximately 2.2 MV cm^{-1} for the 20-nm FS-HZO membrane. No noticeable difference in leakage current was observed across electrode areas ranging from 10 × 10 to 40 × 40 µm^2, strongly indicating uniform film quality in the 20-nm HZO membrane. Results for other HZO thicknesses are provided in Supplementary Fig. 7, with detailed comparisons in Supplementary Table 1. These findings offer compelling evidence for the stable dielectric response of freestanding HZO across various conditions. Particularly, the 20-nm HZO membrane stands out as an ideal gate dielectric for 2D transistors.

Fabrication of exfoliated MoS_2 FETs using HZO membranes

The HZO membranes, with a high dielectric constant and capable of being fabricated into freestanding films, are similar to van der Waals insulating materials. In addition, they retain their ferroelectric switching properties. To apply these benefits, we fabricated 2D FETs using HZO as the dielectric and comprehensively analysed their performances. Few-layer (FL) MoS_2, a widely researched 2D semiconductor, was selected to test the feasibility of HZO as a dielectric in transistors. Few-layer graphene (FLG), which has a gate-tunable Fermi level enabling barrier-free charge carrier injection and a high tolerance for device fabrication and stability[41], was used for the drain-source electrodes in our HZO-gated MoS_2 FETs. Supplementary Note 1 provides additional reasons for FLG selection. FLG-contacted MoS_2 FETs were fabricated by sequentially transferring FLG, MoS_2 and 20-nm HZO onto 300-nm-thick SiO_2/Si substrates via mechanical exfoliation. The thicknesses of FLG and MoS_2 flakes are confirmed via optical images before device fabrication. The corresponding Raman characteristics of MoS_2 and FLG are shown in Supplementary Information (Supplementary Fig. 8). Device architecture is depicted in Fig. 3a. Figure 3b,c plots the transfer (I_{DS}–V_{TG}) and output (I_{DS}–V_{DS}) characteristics of a few-layer MoS_2 FET with dimensions L_{CH} = 4.3 µm and W_{CH} = 3.4 µm. High-resolution-TEM and energy-dispersive X-ray spectroscopy (EDS) images reveal the cross-sectional structure of the FET, displaying smooth interfaces that could assist charge transport and ferroelectric field modulation (Supplementary Figs. 9 and 10). The transfer curves show typical n-type transistor features, with an I_{on}/I_{off} of ~10^9 and negligible leakage current of <10^{-14} A (or <10^{-6} A cm^{-2}), measured under the V_{TG} of ±2 V at a low V_{DS} of 100 mV (Fig. 3b). The large rise in I_{DS} within the subthreshold region is marked by an SS value of around 55 mV dec^{-1}, that is, below the Boltzmann thermionic emission limit at room temperature, suggesting the superior quality of the HZO–MoS_2 interface. Furthermore, ferroelectric polarization switching in the HZO enables counterclockwise transfer curves by tuning polarization-bound charges. Minimal hysteresis (~50 mV) in the I_{DS}–V_{TG} curves suggests low interfacial trap density. Figure 3c shows linear output characteristics at low V_{DS}, indicating ohmic contacts, and saturation at higher V_{DS} due to MoS_2 channel pinch-off. SS points at a V_{DS} of 100 mV in both forward and reverse sweeps are shown in Fig. 3d. The sub-60 mV dec^{-1} region spans four orders of magnitude in I_{DS} for the forward sweep and five orders for the reverse sweep, ensuring SS value accuracy. The reduced SS demonstrates how the negative capacitance effect in the ferroelectric HZO membrane substantially enhances the electrical performance of the 2D transistor.

Dual-gate FET measurements were used to assess the dielectric constant of the freestanding HZO in FETs. The device configuration mirrors that depicted in Fig. 3a, with SiO_2 and HZO serving as the bottom- and top-gate dielectrics, respectively. The channel current in MoS_2 is simultaneously modulated by both the bottom and top gates. Supplementary Fig. 11 shows top-gate transfer curves shifting negatively with bottom-gate voltage (V_{BG}) changes from −80 to 80 V at a V_{DS} of 100 mV. Using the parallel-plate capacitor model for both gates, the slope of the V_{BG} versus V_{TG} at a fixed I_{DS} reveals the coupling ratio between

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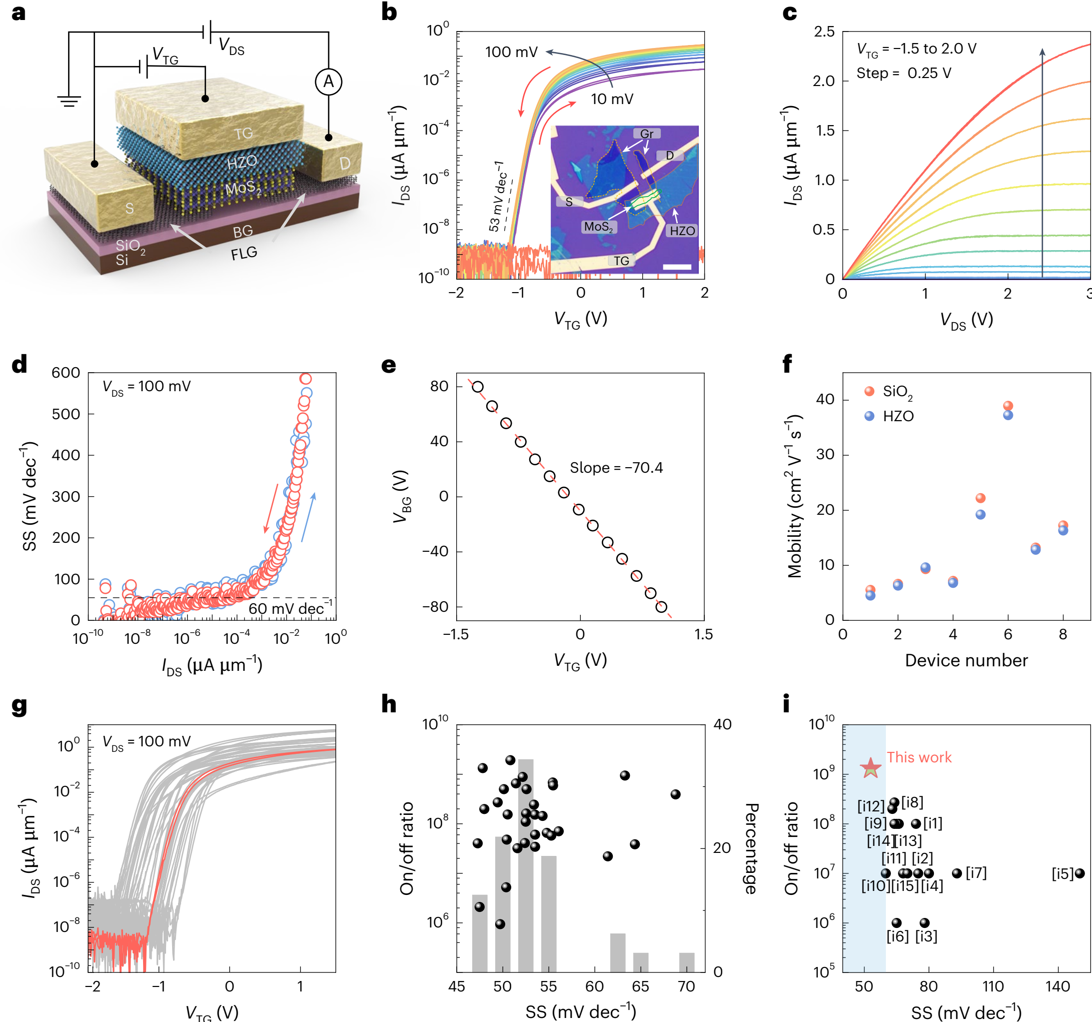

Fig. 3 | FLG-contacted MoS_2 FETs with freestanding HZO top-gate dielectric. **a**, Schematic of a dual-gate FLG-contacted MoS_2 FET with the HZO top-gate dielectric on a SiO_2/p-type Si substrate. S, D, TG and BG are the source, drain, top gate and bottom gate, respectively. **b**, Double-sweep transfer characteristics (I_{DS}–V_{TG}) of the device with a grounded bottom gate. The gate sweeping directions are indicated by the arrows. The inset displays the optical image of the device. The material boundaries are outlined by dashed lines. Scale bar, 10 µm. **c**, Output characteristics (I_{DS}–V_{DS}) of the same device with V_{TG} varying from −2 to 2 V at steps of 0.25 V. **d**, SS as a function of I_{DS} at a V_{DS} of 100 mV. **e**, The V_{TG} extracted under conditions where the channel current (I_{DS}) remains constant at 3 µA, as a function of V_{BG}. **f**, MoS_2 mobility (μ) measured by top- and bottom-gated configurations. **g**, I_{DS}–V_{TG} curves of 30 HZO-gated MoS_2 FETs. **h**, Scatter distribution (black) of on/off-current ratios and SS values, and statistical histogram (grey) from 30 devices. **i**, Comparison of the current on/off ratio and SS of our transistor with state-of-the-art MoS_2 FETs in the literature. The corresponding references are listed in Supplementary Information. The blue region represents an SS value below 60 mV dec^{-1}.

the top-gate capacitance (C_{TG}) and bottom-gate capacitance (C_{BG}), expressed as $C_{TG}/C_{BG} = (\varepsilon_{HZO} \times d_{SiO_2})/(\varepsilon_{SiO_2} \times d_{HZO})$ where ε_{HZO} and ε_{SiO_2} (3.9) are the dielectric constants of HZO and SiO_2, respectively, and d_{HZO} (20 nm) and d_{SiO_2} (300 nm) are the thickness of HZO and SiO_2, respectively. The linear variation of the V_{BG}/V_{TG} ratio, fitted to be −70.4 at a I_{DS} of 200 nA, is depicted in Fig. 3e. The derived ε_{HZO} value of ~18.3, in high agreement with the estimation from the C–V measurements, yields a C_{TG} of 0.44 µF cm^{-2} at an equivalent oxide thickness of 4.5 nm. We also explored the MoS_2 mobility in the SiO_2 (bottom)- or HZO (top)-gated FETs. Figure 3f reveals varied mobility across eight devices, with minor differences between the two FET configurations. The relatively unchanged mobility between the SiO_2- and HZO-gated FETs indicates that using freestanding HZO membranes in 2D FETs not only avoids additional charge doping effects[42] but also effectively mitigates the issue of direct damage to the 2D channels caused by the ALD process[28,29].

Figure 3g showcases the I_{DS}–V_{TG} curves for 32 MoS_2 FETs with transferred, freestanding HZO membranes as top-gate dielectrics, while Fig. 3h depicts the correlation between the I_{on}/I_{off} ratio and the SS values. More than 65% of the FETs achieve a current modulation ratio nearing 10^8, with an average SS value of 53 mV dec^{-1}. The red transfer curve shown in Fig. 3g corresponds to the data in Fig. 3b. Supplementary Table 2 details the 32 MoS_2 FETs. Figure 3i summarizes average SS and I_{on}/I_{off} values for our FETs coupled with 20-nm HZO high-κ dielectrics, compared to other 2D FETs reported in the literature. This work demonstrates that freestanding membranes pave the way for a broad spectrum of hybrid HZO-2D semiconductor interfaces.

Reliability and D_{it} extraction in HZO-gated MoS_2 FETs

Stability and reliability in 2D FETs pose major challenges in both back-end and front-end semiconductor processes. Voltage stress testing, also known as bias temperature instability testing, is crucial for assessing the reliability and longevity of FETs in real-world applications. This test accelerates degradation mechanisms—such as charge trapping, interface defect formation and oxide wear-out—by applying

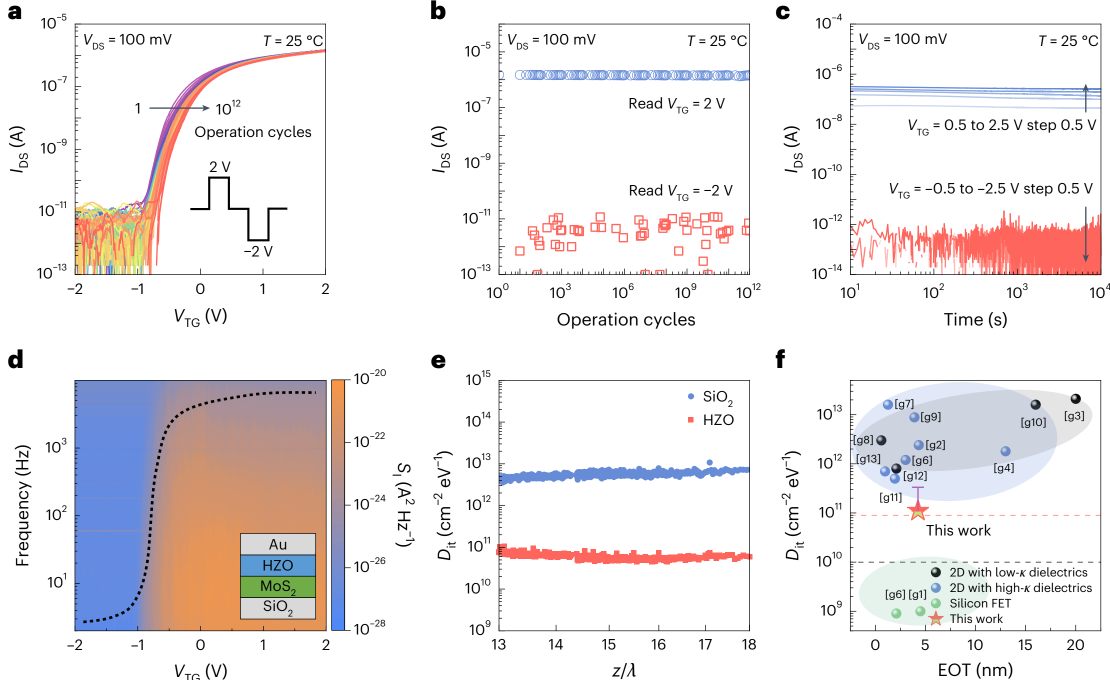

Fig. 4 | Room-temperature reliability and D_{it} extraction in HZO-gated MoS_2 FETs. a, Double-sweep transfer characteristics of HZO-gated MoS_2 FETs at V_{DS} = 100 mV after 10^{12} operation cycles. **b**, Endurance performance of 10^{12} operation cycles at the off-current state (V_{TG} = −2 V) and on-current state (V_{TG} = 2 V). V_{DS} = 100 mV is used. **c**, Retention performance of over 10^5 s. **d**, Mappings of current noise power spectral density (S_I) versus frequency and V_{TG} for HZO-gated MoS_2 FETs. **e**, Extracted D_{it} as a function of z/λ for the SiO_2- and HZO-gated FETs, where z and λ represent the trap depth and the tunnelling distance parameter, respectively. **f**, Comparison of D_{it} values measured for leading-edge 2D and silicon FETs. The corresponding references are listed in Supplementary Information. The black dashed line indicates a density of 1,010 cm^{-2} eV^{-1}. The grey, blue and green shaded regions correspond to 2D transistors with low-κ dielectrics, 2D transistors with high-κ dielectrics, and silicon FETs, respectively.

elevated gate voltages under controlled conditions. These mechanisms cause voltage shifts and leakage, impacting switching speed and efficiency. Voltage stress testing is also vital in refining transistor designs, optimizing materials and maintaining robust performance as device dimensions continue to shrink in advanced technologies. Figure 4a presents I_{DS}–V_{TG} characteristics of an HZO-gated MoS_2 FET at V_{DS} = 100 mV after 10^{12} operation cycles. Figure 4b illustrates the endurance at the off-state (V_{TG} = −2 V) and on-state (V_{TG} = 2 V), while Fig. 4c shows retention performance over 10^5 seconds. Supplementary Figs. 12–14 show additional bias temperature instability tests under varying V_{TG} values (−2.5 to 2.5 V) at temperatures of 300, 358 and 423 K, respectively. Further analysis of threshold voltage shifts is provided in Supplementary Fig. 14. Despite these harsh conditions, the devices exhibit high electronic stability and reliability, demonstrating the robustness of HZO-gated 2D FETs.

Unlike silicon technologies, which rely on covalent-bond accommodation at interfaces, 2D transistor interface quality depends mainly on insulator surface quality. Dielectric quality typically correlates with SS values from the transfer characteristics, assessed by D_{it} (ref. 16). Given the current 2D technology, relying only on SS for assessing insulator quality is not sufficient because channel defects and adsorbates can greatly affect SS values as well as D_{it}. Low-frequency noise characterization of few-layer MoS_2 transistors with HZO dielectrics assesses noise behaviour and interface quality. Figure 4d illustrates the current noise power spectral density (S_I) maps as a function of V_{TG} and frequency (f) for a HZO-gated FET. The S_I curve at a fixed gate bias follows a $1/f$ pattern, suggesting uniform distribution, in space and energy, of the charge trapping in the dielectric–MoS_2 interface. More details of their dynamic characterizations and comparisons with the SiO_2-gated FET are given in Supplementary Figs. 16 and 17. In addition, frequency dependency follows $S_I \propto I_{DS}{}^{\alpha}/f^{\beta}$ where α and β represent scaling exponents related to current and frequency, respectively[43]. Supplementary Fig. 17b presents β values as a function of V_{BG} or V_{TG}, with the average β values being 1.19 ± 0.12 for the SiO_2-gated FET and 1.07 ± 0.08 for the HZO-gated FET, again highlighting the accuracy of using the $1/f$ formula. Supplementary Fig. 17c shows S_I increasing quadratically under different frequencies at a V_{TG} of 2 V, averaging α at 2.1 ± 0.09. This suggests the $1/f$ feature arises from a resistor fluctuation[44]. S_I values are normalized by squaring the I_{DS} at various V_{DS} (Supplementary Fig. 17d). The normalized S_I are independent of V_{DS}, indicating that the signal fluctuations stem from the MoS_2 channel, rather than the metal contact barriers. The results confirm the HZO membranes as effective insulators, boosting gate control and minimizing the Schottky barrier effect[16]. Details regarding the SiO_2-gated FET can be found in Supplementary Fig. 18.

D_{it} values are further discussed based on the correlated mobility fluctuations (CMFs), illustrating the noise contribution from interface states and 2D channels[43–45]. Fluctuation analysis is detailed in Methods and Supplementary Fig. 19. HZO-gated FETs exhibit D_{it} of 9×10^{10} cm^{-2} eV^{-1}, greatly below that of SiO_2 and approaching the CMOS technology standard[16] of less than 10^{10} cm^{-2} eV^{-1} (Fig. 4e). Figure 4f benchmarks D_{it} against that of leading-edge 2D and silicon FETs. Despite the equivalent oxide thickness (~4.3 nm) not being optimized, integrating the dielectric layer on 2D semiconductors through a high-quality semiconductor-to-oxide interface has resulted in superior gate control over channel conductance. 2D FETs with an optimized freestanding HZO dielectric could achieve even more efficient gate controllability, allowing transistors with a high I_{on}/I_{off} and smaller operating voltage and SS.

Demonstrations of low-power CMOS logic circuits

Figure 5 demonstrates the capability of HZO-gated MoS_2 FETs to achieve actual electronic functionalities through various logic circuit operations. Low-power digital circuits are essential for prolonging

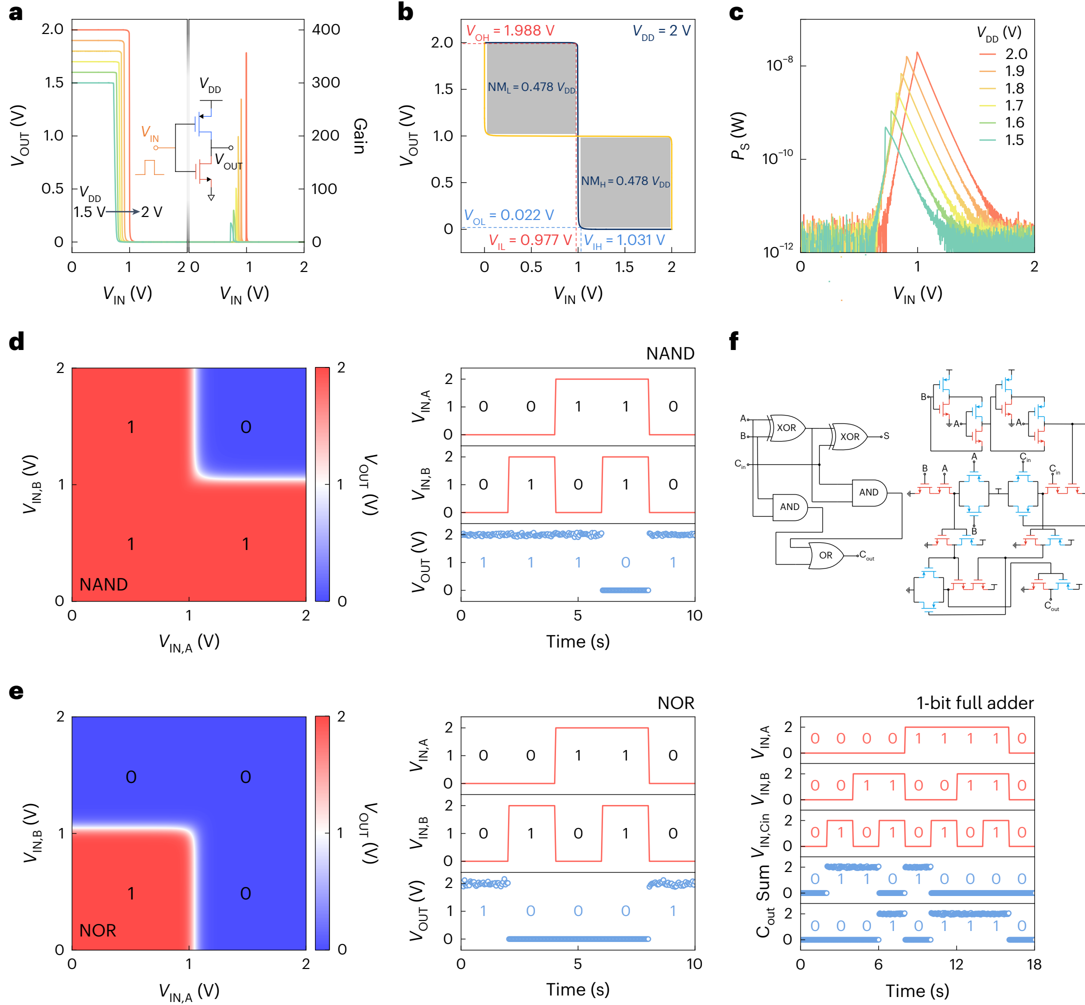

Fig. 5 | Low-power CMOS logic circuits based on high-κ HZO dielectrics. **a**, Transfer characteristics of an inverter operation at different V_{DD} varying from 1.5 to 2 V (left). Calculated gain ($|dV_{OUT}/dV_{IN}|$) of the inverter as a function of V_{IN} at different V_{DD} (right). **b**, Noise margin characteristics of the inverter at V_{DD} = 2 V. **c**, Calculated power consumption of the inverter as a function of V_{IN} at different V_{DD}. **d**–**f**, V_{OUT} results and the corresponding waveforms at V_{DD} = 2 V as functions of $V_{IN,A}$ and $V_{IN,B}$, shown for NAND (**d**) and NOR (**e**). **f**, Schematic of a 1-bit full adder and the corresponding waveforms at V_{DD} = 2 V as functions of $V_{IN,A}$ and $V_{IN,B}$. Sum and C_{out} denote the sum and carry-out outputs of the 1-bit full adder, respectively, reflecting the arithmetic result and the propagated carry bit.

battery life for widespread portable devices and preventing processor overheating. The potential of our HZO-gated FETs for low-power digital circuits was illustrated through the initial step of fabricating and testing inverters, a standard approach with new materials and technologies. A CMOS inverter, comprising series-connected p-type and n-type FETs, operates with a supply voltage (V_{DD}), regulating the conductance of both FETs using a singular gate voltage (V_{IN}) and measuring the resulting drain voltage (V_{OUT}). The inverter's performance is depicted in Fig. 5a–c. Supplementary Figs. 20 and 21 detail the operations of the p-type FET and CMOS, respectively. A symmetric full-swing output is achieved across various V_{DD} values, with a notable gain of 357 at V_{DD} = 2 V (Fig. 5a). Figure 5b demonstrates the inverter's noise tolerance, with total noise margins exceeding 96% (low-level (NM_L) and high-level (NM_H) margins both at 0.478; V_{DD} = 2 V). Furthermore, power consumption ($P_S = V_{DD} \times I_{DS}$) is analysed and presented in Fig. 5c, indicating a peak power of ~10 nW (V_{DD} = 2 V) that decreases with lower V_{DD}. Expanding on this, the functionalities of NAND and NOR gates, along with a 1-bit full adder, are depicted in Fig. 5d–f. Supplementary Fig. 22 shows additional AND, OR, XOR and XNOR logic functions. While demonstrations are confined to 2D MoS_2 channels, these findings strongly indicate that HZO-gated 2D FETs are promising for creating advanced digital logic circuits through cascading. As the channel length is scaled down, drain-induced barrier lowering becomes more pronounced, resulting in degraded electrostatic control by the gate as well as higher power consumption of devices. To confirm the HZO gate-to-2D channel controllability, a short-channel MoS_2 FET is fabricated, as shown in Supplementary Fig. 23. The device, which has a channel length of 13 nm, exhibits I_{on}/I_{off} modulation of nearly 10^8 and an SS of 70 mV dec^{-1} at V_{DS} = 100 mV. This may be influenced by the drain-side electric field extending into the channel, slightly weakening the gate's control. Supplementary Note 2 provides additional explanations of the short-channel influences. Detailed comparisons of device performances with the literature are provided in Supplementary Table 3. These results are consistent with the trends observed in previous studies, further underscoring the resilience of the HZO-based 2D FET structure against short-channel effects.

Conclusions

We have shown that freestanding high-κ ferroelectric HZO membranes can be created using PLD and transferred onto 2D semiconductors. We created MoS_2 FETs with a HZO top-gate dielectric. Due to the ferroelectricity, dielectric constant of 20.6 and excellent insulator–channel interfacial quality ($D_{it} \approx 9 \times 10^{10}$ cm^{-2} eV^{-1}) of HZO, the devices exhibit an I_{on}/I_{off} of about 10^9 at a V_{DS} of 100 mV and minimum SS of 53 mV dec^{-1}.

Using these transistors, we constructed functional logic gates and computational circuits, including an inverter, NAND, NOR, AND, OR, XOR, XNOR and a 1-bit full adder. To verify the influence of short-channel effects on HZO-gated FETs, we created a MoS_2 FET with a 13-nm channel length that exhibited an $I_{on}/I_{off} > 10^8$ and SS of 70 mV dec^{-1}. Our findings indicate that freestanding ferroelectric HZO membranes can offer a CMOS compatible solution for the high-κ dielectrics in 2D transistors and are promising for the development of 3D integrated circuits based on 2D materials.

Methods

HZO preparations

All HZO thin films in this study were grown using PLD with a krypton fluoride excimer laser (λ = 248 nm). To obtain freestanding HZO films with varying thicknesses, epitaxial HZO/LSMO heterostructures were synthesized on (001)-oriented STO (STO (001)) substrates. The LSMO sacrificial layers were grown at 690 °C and an oxygen pressure of 150 mTorr, while HZO layers with different thicknesses were deposited at 710 °C and an oxygen pressure of 100 mTorr. A laser power of 200 mJ and a laser repetition rate of 10 Hz were used for both layers. Subsequently, the samples were cooled to room temperature at an oxygen pressure of 760 Torr to reduce oxygen vacancies and maintain the high crystallinity of the heterostructures. After the PLD procedure, the as-grown HZO thin films underwent a freestanding process. This involved immersing the samples in a dilute hydrogen chloride (HCl) solution, which resulted in the separation of the HZO layers from the substrates. They were then transferred onto other templates for various applications. For polarization–electric field and frequency dielectric response measurements, freestanding HZOs were transferred onto LSMO/STO (001) substrates, with Au/Cr top electrodes (thicknesses of 50 and 5 nm, respectively) deposited onto the freestanding HZOs using an e-beam evaporator. For specimens destined for TEM and EDS measurements, the freestanding HZO thin films were transferred onto Cu grids with carbon films.

Structural analysis on HZO

The X-ray diffraction θ–2θ scans along the surface normal direction, azimuthal scans and reciprocal space mapping along the off-normal direction were acquired using a synchrotron-based X-ray high-resolution nine-circle diffractometer. The photon energy used was 10 keV, and the beam size was 800 × 800 μm^2. These measurements were conducted at beamlines TPS-09A and TLS-13A1 at the National Synchrotron Radiation Research Center, Taiwan. The 10 keV incident beam was monochromated using the Si (111) double crystal mirror, which was then focused by a Rh-coated horizontal focusing mirror. Each scan was acquired with an integral time of 2 s per data point and plotted in the reciprocal lattice unit, normalized to the STO substrates (1 r.l.u. = $2\pi/a_{STO}$). The plane-view, cross-section TEM images and EDS mappings of HZO thin films with various thicknesses for the investigation of lattice structure and chemical composition at the microscale were collected using a JEOL JEM-2100F equipped with a spherical aberration (coefficient Cs) corrector in scanning TEM mode at the Core Facility Center, National Cheng Kung University, Taiwan. To prepare the cross-section TEM specimens, the focused ion beam milling method was used using a Thermo Fisher Scientific Inc., Helios NanoLab G3 CX at MSSORPS Co., Ltd, also at the Core Facility Center, National Cheng Kung University, Taiwan.

Electronic structure investigation on HZO

The thickness-dependent electronic structure of freestanding HZO with various thicknesses was investigated using XAS, conducted at beamline TPS-45A in the National Synchrotron Radiation Research Center, Taiwan. The spectra were collected around photon energy near the oxygen K-edge (526–540 eV), with a beam size of 3 × 3 μm^2 and five-axis manipulation under ultra-high vacuum. X-ray linear dichroism measurements were acquired with a grazing-incident angle of 20°, where the electric field is parallel to the a, b or c axis. The X-ray linear dichroism curves were derived as the difference between the XAS acquired with horizontally polarized light and vertically polarized light, and the normalized intensity was calculated by dividing by the intensity of the e_g band peak of each thickness taken with horizontally polarized light.

Scanning probe characterization (PFM and cKPFM) on HZO

The PFM images and cKPFM curves were acquired by using a commercial scanning probe microscope multimode VIII (Bruker) with the software Nanoscope v.9.14. Out-of-plane PFM and cKPFM measurements were conducted at room temperature using Pt-/Ir-coated tips, whose elastic constant is ~2.8 N m^{-1} (NANOSENSORS PPP-EFM60), to apply an external bias to the film surface. The driven a.c. frequency was approximately 380 kHz. In PFM measurement, an internal lock-in amplifier was used to record the out-of-plane phase difference. For cKPFM curve collection, the switching spectroscopic technique was applied, with a waveform generator (cat. no. G5100A, Picotest), to vary write voltages at a range of read voltages.

Polarization–electric field measurements

The Sawyer–Tower circuit was used for polarization–electric field measurements. In this resistor–capacitor circuit, a square wave serves as the excitation voltage (V_e) applied across the entire system. The voltage (V_R) measured across a reference resistance (R) is the difference between V_e and the response voltage (V_r), which comprises the voltage attributable to the sample and the circuit. The leakage current through the sample is monitored by a parallel resistance (V_L) component. In this context, we consider the current contribution of the sample (I_R) to include the leakage current term, parasitic term and ferroelectric term (the sample), denoted as I_L, I_p and I_s, respectively. The parasitic capacitor is denoted as C_p. Subsequently, the resistance of the leakage current term (R_L) and the corresponding (Q_p and Q_s) can be calculated using the current expressions provided below. This information enables the relationship between polarization and applied electric field to be determined using the following equations:

$$I_R(t) = I_s(t) + I_p(t) + I_L(t)$$

$$\frac{V_R(t)}{R} = \frac{dQ_s(t)}{dt} + \frac{dQ_p(t)}{dt} + \frac{V_r(t)}{dt}$$

$$\frac{V_R(t)}{R} = \frac{dQ_s(t)}{dt} + C_p\frac{dV_p(t)}{dt} + \frac{V_r(t)}{dt}$$

The time-dependent sample current can be derived from:

$$\frac{dQ_s(t)}{dt} = \frac{V_R(t)}{R} - \frac{V_r(t)}{R_L} - \frac{dQ_p(t)}{dt}$$

Integration:

$$\int_0^t \frac{dQ_s(t)}{dt}dt = Q_s(t=t) - Q_s(t=0)$$

A 20-kHz switching square wave was used as an excitation source, generated by a wave generator. Additionally, commercial tungsten tips with a peak dimension of approximately 1 μm in diameter were used during the measurement.

Dielectric property measurement

The dielectric frequency response measurements for various freestanding HZOs were conducted using a commercial impedance–gain-phase analyser (HP 4194A). Initially, we acquired the capacitor

response curve as a function of frequency in parallel mode, wherein the reference resistor is in parallel to the measured samples due to the large impedance (>100 kΩ) of HZO. After obtaining the capacitor curve, the formula $\varepsilon_{\rm eff} = \frac{C_{\rm eff} d_{\rm HZO}}{\varepsilon_0 A}$ was used to calculate the dielectric constant of the whole system, where ε_0 is the permittivity in vacuum, A is the top electrode area and $d_{\rm HZO}$ is the thickness of freestanding HZO films. $C_{\rm eff}$ is the value of effective capacitor defined as $\frac{1}{C_{\rm eff}} = \frac{1}{C_{\rm ui}} + \frac{1}{C_{\rm HZO}} + \frac{1}{C_{\rm di}}$ including the contribution from freestanding HZO ($C_{\rm HZO}$), the upper Cr–freestanding HZO interface ($C_{\rm ui}$) and down freestanding HZO–LSMO interface ($C_{\rm di}$). For dielectric measurements, top electrodes measuring 100 × 100 µm^2 were deposited via electron beam evaporation to define the capacitor structure. The temperature points from room temperature to 100 °C, including 25, 40, 60, 80 and 100 °C, were selected to explore the dielectric features within the potential operation temperature window.

Device fabrication and electrical measurements

Heavily doped Si substrates with a 300-nm-thick SiO_2 layer underwent sonification cleaning before device fabrications. Sequential deposition of few-layer MoS_2 and graphene flakes onto the Si substrates was achieved through mechanical exfoliation of their bulk crystals (SPI Supplies) using the Scotch tape method. Subsequently, a precise transfer of an individual HZO membrane using a polydimethylsiloxane (Gel-Pak, PF-40-X4) stamp onto the target material formed a heterostructure. The sample morphology and thickness were characterized using optical microscopy (BX53M microscope equipped with a DP26 digital camera; Olympus Corp.) and AFM (Solar TII, Tokyo Instruments Inc.). Raman spectroscopy measurements were conducted using a Nanofinder 30 system (Tokyo Instruments Inc.) with a 532-nm excitation laser. Device contact areas (source, drain and gate) were delineated using an e-beam lithography system (JEOL JSM-IT700HR for SEM and Raith ELPHY Quantum module for lithography), followed by Ti/Au (20/60 nm) metal contact deposition via thermal evaporation at 2×10^{-6} Torr. Device electrical measurements were performed with a Keysight B1500A semiconductor parameter analyser on a Lakeshore TTPX cryogenic probe station under vacuum (<10^{-5} Torr). To quantify the effective density of interface states in HZO-gated MoS_2 transistors, dynamic measurements were conducted using low-frequency noise technology via a programmable point probe noise measurement system (3PNMS, Synergie Concept Co.) with a system noise floor of ~1×10^{-27} A^2 Hz^{-1}. Source-drain current fluctuations were then monitored under specific gate and source-drain voltages at room temperature for carrier charge fluctuation analysis. To reduce external electrical interference affecting the monitored charge fluctuations, all low-frequency noise measurements took place in a grounded metal chamber on top of a vibration-isolated table, under vacuum (<10^{-5} Torr) and dark conditions.

FET mobility extraction

FET mobility is determined from the transfer curve using the standard equation: $\mu = (\frac{L_{\rm CH}}{W_{\rm CH}})(\frac{d}{\varepsilon_r \varepsilon_0 V_{\rm DS}}) \times g_{\rm m}$, where $L_{\rm CH}/W_{\rm CH}$ is the channel length to width ratio, ε_0 is the permittivity in a vacuum, ε_r is 20.6 (3.9) for freestanding HZO (SiO_2), d is 20 nm (300 nm) for the thickness of the dielectric HZO (SiO_2) and $g_{\rm m} = \frac{dI_{\rm DS}}{dV_{\rm TG(BG)}}$ is the channel transconductance.

Noise fluctuations and interface-state extraction

Low-frequency noise is regarded as a crucial diagnostic tool for identifying the primary mechanisms behind carrier fluctuations in the active regions of solid-state electronics, especially in layered conducting channels due to their high surface-to-volume ratio. In conventional metal–oxide–semiconductor FETs (MOSFETs), carrier number fluctuations (CNFs) stem from dynamic trapping and release of carriers near the dielectric–semiconductor interface. Additionally, fluctuations in the inversion layer mobility, attributed to trap charge fluctuations, must be accounted for, a phenomenon known as the surface effect. In noise models for silicon-based transistors, $1/f$ current fluctuations are explained from two principal perspectives[46]. The variation in carrier numbers (Δn) in the channel, causing random and uncontrolled perturbations, leads to numerous carrier trapping–detrapping processes near the semiconductor interface, modulating the flat-band potential. Considering the CMFs, attributed to scattering rate modulation by interface charge fluctuations, current noise power spectral density ($S_{\rm I}$) can be further normalized by squaring the drain-source current ($I_{\rm DS}$) values, resulting in $\frac{S_{\rm I}}{I_{\rm DS}^2} = (1 + \frac{\alpha_{\rm sc}\mu I_{\rm DS}}{g_{\rm m}} \times \frac{\varepsilon_r \varepsilon_0}{d}) \times (\frac{g_{\rm m}}{I_{\rm DS}})^2 \times S_{\rm Vfb}$, where $S_{\rm Vfb} = (\frac{q^2 k_{\rm B} T D_{\rm it}}{f W_{\rm CH} L_{\rm CH}}) \times (\frac{d}{\varepsilon_r \varepsilon_0})^2$ is the flat-band voltage spectral density. $\alpha_{\rm sc}$ is the Coulomb scattering coefficient associated with mobility fluctuation. q, $k_{\rm B}T$ and $D_{\rm it}$ are the elementary charge, thermal voltage and density of interface states, respectively. This model is called CNF-CMF. If the sensitivity of mobility fluctuations to trapped charges is sufficiently low rendering them negligible, then the normalized current fluctuations $\frac{S_{\rm I}}{I_{\rm DS}^2}$ is proportional to $(\frac{g_{\rm m}}{I_{\rm DS}})^2$. This simplified model, termed CNF, posits that surface effects predominantly govern the system. Conversely, when mobility fluctuations ($\Delta\mu$) result from variations in the mean free path due to charged defect scatterings, culminating in electrical noise, the normalized current fluctuations can be represented with the formula $\frac{S_{\rm I}}{I_{\rm DS}^2} \propto \frac{1}{I_{\rm DS}}$. This model, known as the Hooge mobility fluctuation, describes the behaviour of electric noise under bulk conditions. Assuming $1/f$ noise behaviour is valid at low frequencies, we can analyse the normalized $S_{\rm I}$ as a function of $I_{\rm DS}$ on a log–log scale. It can be observed that for both CNF-CMF and CNF models, the normalized $S_{\rm I}$ values depend on $(\frac{g_{\rm m}}{I_{\rm DS}})^2$ due to the scattering's impact on electric noise, whereas in the Hooge mobility fluctuation model they inversely scale with $I_{\rm DS}$.

Furthermore, noise fluctuations, caused by tunnelling between charge traps and the semiconductor channel, have a trap depth (z) that varies with frequency as $z = \lambda \ln(\frac{1}{2\pi f \tau_0})$, with τ_0 (the time constant) typically at 10^{-10} s and λ indicating the tunnelling distance[47]. Determining λ accurately is challenging due to complex trap processes; thus, a typical value of λ is about 10^{-8} cm for silicon-based transistors. The density of interface states can be assessed by the ratio $\frac{z}{\lambda}$. Note that the $\frac{z}{\lambda}$ ratio only indicates the relative distance from the semiconductor channel. If $D_{\rm it}$ is not affected by $\frac{z}{\lambda}$, it suggests that low-frequency noise, due to tunnelling, needs a uniform trap state distribution, consistent with $1/f$ noise observations.

Data availability

The data that support the plots within this paper and other findings of this study are available from the corresponding authors on reasonable request.

Code availability

The codes used for simulation and data plotting are available from the corresponding authors on reasonable request.

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Author contributions

J.-C.Y. and Y.-F.L. conceived and designed the entire experiment. For HZO membranes, B.-C.C., Y.-C.L. and Y.-C.C. fabricated and characterized the freestanding HZO membranes. Y.-C.L., C.-Y.K. and C.-F.C. conducted XAS/LD and analysed the corresponding data. For 2D transistors, C.-Y.L., S.-F.K. and H.-C.T. fabricated transistors and conducted the electrical measurements. C.-Y.L. further realized low-frequency noise measurements and logic circuits. C.-Y.L. and Y.-M.C. completed the data analysis and wrote the draft. The paper

was reorganized and co-written by J.-C.Y. and Y.-F.L. with contributions from all co-authors. J.-C.Y. and Y.-F.L. supervised the research. All the authors discussed the results and commented on the paper.

Competing interests

The authors declare no competing interests.

Additional information

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