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Low-temperature wafer-scale growth of ultrathin tungsten disulfide for bifunctional interconnect barriers and liners

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In the future, the miniaturization of integrated circuits will require copper wires to be scaled down in the back-end-of-line (BEOL) process. This will, in turn, require a scaling down of the barrier and liner coatings that prevent copper diffusion and ensure metal adhesion to the dielectric. Here we show that thin (<1 nm) and conformal tungsten disulfide (WS_2) layers can be grown on the wafer-scale using thermal atomic layer deposition without plasma at BEOL-compatible temperatures (350 °C) and can function as both barriers and liners for interconnects. We show that the WS_2 can reduce the resistivity of 10-nm-thick copper films by more than six orders of magnitude compared with a reference system (without the WS_2 layer) due to the improved wettability of copper. Monolayer WS_2 can prevent copper diffusion into silicon dioxide (SiO_2) under thermal stress, and it is projected to improve wire lifetimes under electrical stress. Density functional theory calculations also highlight the potential of multilayer WS_2 films as diffusion barriers due to misaligned grain boundaries.

Integrated circuits (ICs) rely on networks of wires interconnecting the active IC components that perform logic and memory functions. In standard ICs, these networks constitute the back end of line (BEOL): a stacked structure of metal wires embedded in dielectric layers laid on top of the active semiconductor components (such as transistors) that constitute the front end of line (Fig. 1a). As the size of ICs has shrunk, advances in the performance of these metal interconnects have been driven by the integration of new materials. For example, aluminium (Al) interconnects were eventually replaced with copper (Cu) as the industry-standard main wire metal in the 1990s due to the high resistivity of Al in smaller interconnect sizes and its propensity to electromigration[1]. This material switch increased the complexity of the overall interconnect structure, as more layers must be placed between the Cu/dielectric contact to address the high diffusivity and poor adhesion of Cu on industry-relevant dielectric materials. These two extra layers are called the barrier and the liner and are typically made of tantalum nitride (TaN) and tantalum (Ta), respectively.

The need for the barrier/liner bilayer creates challenges for modern electronics given that the migration of Cu atoms is one of the main failure mechanisms in interconnects, even at the current technology node of 5 nm. As the semiconductor industry advances towards the 3-nm technology node, the interconnect half pitches and wire diameters will reach a sub-20-nm region[2]. At that point, the barrier/liner bilayer itself would occupy a substantial fraction (up to 50%) of

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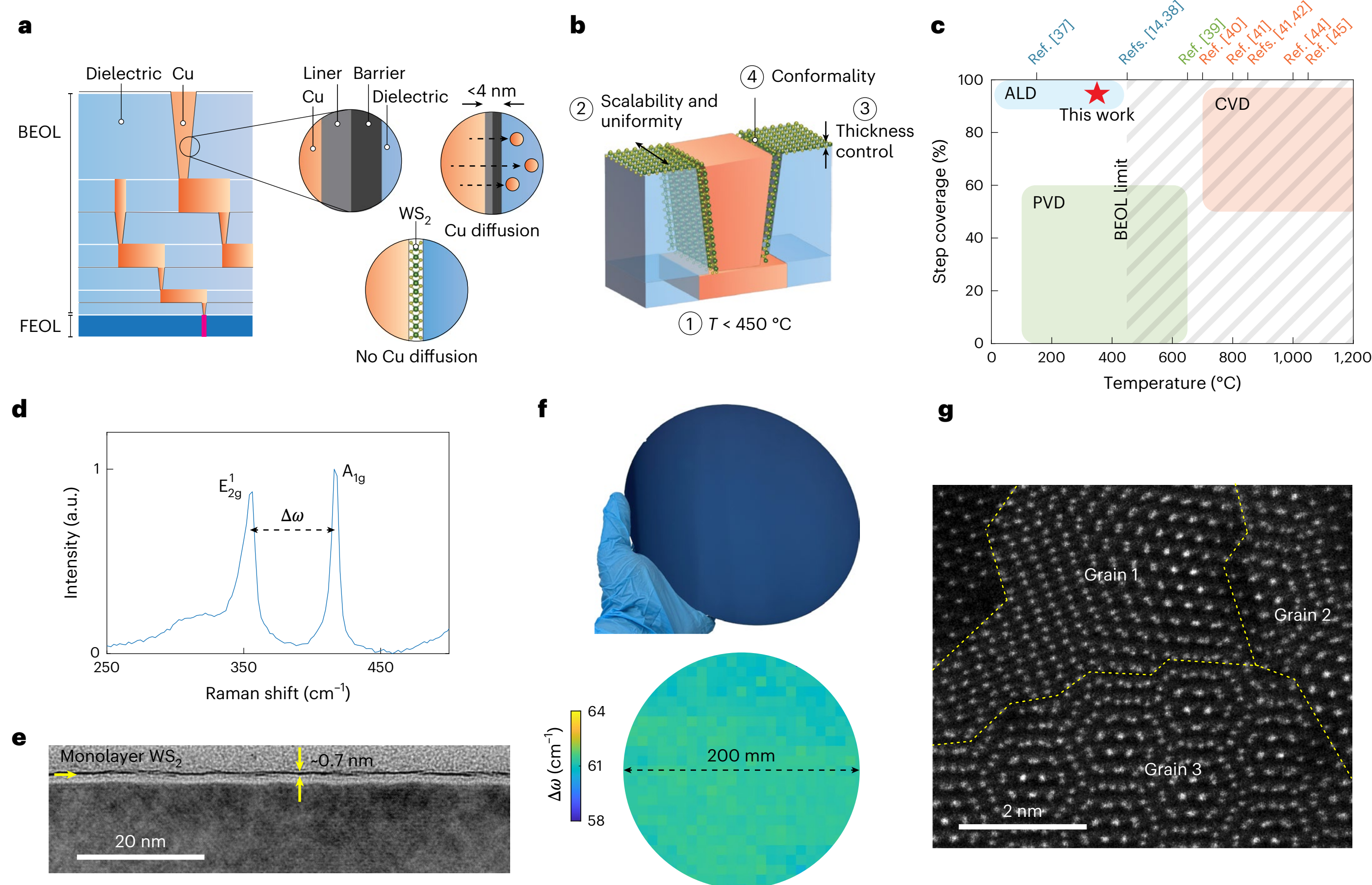

Fig. 1 | BEOL components and requirements for further miniaturization. **a**, Schematic of a multilayer BEOL structure with a focus on the Cu/dielectric interface and scenarios for further interconnect downscaling. **b**, BEOL requirements for material integration as a bifunctional barrier and liner layer. **c**, Step coverage versus deposition temperature for WS_2 reported in recent works in the literature (references given at the top) and in our approach (red star). Shaded areas correspond to typical ranges for different growth methods, including chemical vapour deposition and physical vapour deposition[14,37–46]. **d**, Representative Raman spectrum of our ALD-grown WS_2. **e**, Cross-sectional phase-contrast TEM image of monolayer WS_2 grown using our ALD process. Yellow arrows show the single-layer WS_2 film and its thickness. **f**, Photograph of the ALD-grown WS_2 over a 200 mm SiO_2/Si wafer (top) and the corresponding Raman map (bottom) of the peak separation $\Delta\omega$ demonstrating the film uniformity. Complete wafer mapping from 504 spectra is shown in Supplementary Section 2. **g**, Plan-view STEM image of polycrystalline WS_2 with several grains marked. A hexagonal lattice composed of W atomic positions is observed in the upper left corner. CVD, chemical vapour deposition; FEOL, front end of line; PVD, physical vapour deposition.

the cross section of the wire because the absolute thickness of Ta/TaN must be ≥4 nm to maintain effective barrier properties[2,3] (Fig. 1a). This would lead to a substantial increase in the wire resistance (more than 200% for a wire of thickness 16 nm; for example, ref. 2) and, in turn, a slowing down of ICs due to the increased resistor–capacitor delay. Therefore, materials that have efficient barrier properties at subnanometre thicknesses or that can perform simultaneously as a barrier and liner are critically needed for future technology nodes.

Two-dimensional (2D) materials[2,4–7] could potentially act as both the diffusion barrier and liner (Fig. 1b). At subnanometre thicknesses, 2D materials are predicted to provide a high energy barrier against Cu diffusion compared with conventional industry-standard materials[8]. Furthermore, the absence of dangling bonds in 2D films reduces interface surface scattering, which may prevent the Cu resistivity from increasing in thinner wires (<15 nm)[2]. The use of monolayer 2D materials for front-end-of-line applications (such as transistors) has been extensively explored[9–11], but the integration of single-layer 2D materials into the BEOL remains challenging due to four key growth requirements (Fig. 1b). First, the growth temperature of BEOL materials must be less than 450 °C to prevent damage to the underlying IC structure[12,13]. Second, the 2D deposition must be scalable and uniform over the entire area of industry-standardized wafers. Third, layer growth has to be achieved with atomic precision to enable control of the thickness for specific feature sizes in the relevant BEOL stack layer. Finally, the deposition should be conformal (uniform within high-aspect-ratio structures). So far, no growth approach has been able to satisfy all these requirements (Fig. 1c and Supplementary Section 1).

In this Article, we report the wafer-scale growth of crystalline tungsten disulfide (WS_2) layers down to the monolayer regime and thicknesses of 0.7 nm. We use thermal atomic layer deposition (ALD) without plasma, sacrificial layers or post-annealing, which would make the deposition incompatible with the BEOL[14–18] (see Supplementary Section 1 for a comparison of growth approaches). We show that a single WS_2 layer grown on a silicon (Si)-based substrate can function as both an efficient liner and a Cu barrier. As a liner, single WS_2 layers reduce the resistivity of 10-nm-thick Cu films by more than six orders of magnitude compared with a Cu film directly deposited onto SiO_2. As a barrier, the layers prevent Cu migration under thermal stress and are projected to delay electrical-stress-induced breakdown. We also examine Cu migration through WS_2 films using density functional theory (DFT) simulations, finding that the grain arrangement between layers can help prevent Cu diffusion. Our work shows that single-layer transition-metal dichalcogenides can be integrated as a bifunctional barrier and liner into the BEOL and are a viable route for current and future technology nodes, with a thickness even below that projected for the 0.5-nm-equivalent node due in 2037[19].

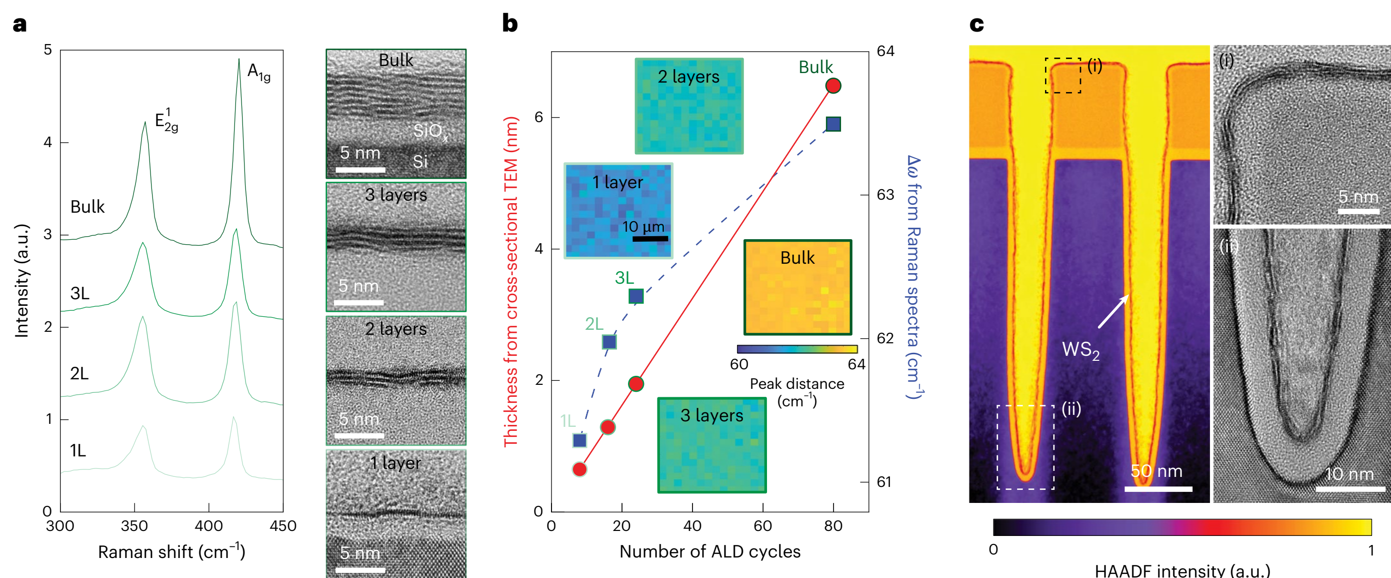

Fig. 2 | Thickness control and conformality of WS_2 ALD growth. a, Raman spectra of single-layer (1L), bilayer (2L), trilayer (3L) and bulk WS_2 films grown using ALD, with the corresponding cross-sectional phase-contrast TEM images of WS_2 films of different thicknesses. **b**, Thickness of WS_2 films determined from cross-sectional TEM (red line) and Raman spectra (dashed blue curve), both as a function of the number of ALD growth cycles. Insets: Raman maps of the films. **c**, Phase-contrast cross-sectional TEM images of trench structures with 2L WS_2 verify conformal growth (false colour used to enhance the contrast). Dashed rectangles indicate areas enlarged in (i) and (ii) to show conformality at the top and at the bottom of the trench.

Growth of monolayer WS_2 below the BEOL temperature limit

To achieve BEOL-compatible growth of 2D materials, we developed a fully thermal ALD process without any plasma assistance that satisfies all four abovementioned requirements. We focus on WS_2 because recent DFT calculations[8] indicate that this material system has the highest barrier energy for Cu diffusion among common transition-metal dichalcogenides. WS_2 thin films were synthesized via thermal ALD at the BEOL-compatible temperature of 350 °C using pulsed bis(tert-butylimido)-bis(dimethylamido)-tungsten (W-$(NMe_2)_2(N^tBu)_2$) as the tungsten source and H_2S gas as the co-reactant (details of the growth are given in Methods). A halide-free W precursor was used to avoid any corrosion and impurity effects and, thus, to improve the film quality by making the process compatible with advanced semiconductor applications. The growth was performed on standard-industry 200-mm wafers (Fig. 1f, top), namely Si substrates with either a 2-nm-thick native SiO_2 layer ($SiO_{2|nat}$) or a 100-nm-thick, thermally grown SiO_2 layer ($SiO_{2|100\,nm}$), depending on the characterization requirements. The characteristic in-plane E^1_{2g} and out-of-plane A_{1g} vibrational Raman modes confirmed that the as-deposited film was crystalline WS_2 (ref. 20). The separation between these peaks, $\Delta\omega = 61–62\ cm^{-1}$, corresponds to a single-layer film[20] (Fig. 1d). The Raman results were confirmed using cross-sectional transmission electron microscopy (TEM) imaging, which shows a continuous film over the entire TEM field of view (Fig. 1e and Supplementary Section 3). Raman mapping across the entire 200-mm wafer shows an average $\Delta\omega$ of $61.3 \pm 0.2\ cm^{-1}$ and demonstrates excellent uniformity with monolayer WS_2 coverage across the wafer (Fig. 1f).

To assess the crystallinity and grain orientation of the films between stacked layers, we deposited a bilayer WS_2 film using the same ALD process. The crystalline nature of the film is evident in atomically resolved plan-view high-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) images of the bilayer (Fig. 1g). The STEM results further show that individual layers are polycrystalline with an average grain size of 5–10 nm (Supplementary Section 4). The presence of moiré patterns observed in the STEM images indicates that the grains are not vertically aligned between the two layers, and because both the periodicity and orientation of the moiré patterns vary across the field of view, it can be concluded that the individual grains do not have preferential orientations within a single layer. We later show that this structural morphology likely offers a unique advantage for the diffusion barrier properties of our ALD-grown WS_2. Further spectroscopic and microscopic characterization of the film is detailed in Supplementary Section 5.

Thickness-controlled conformal growth of WS_2

As a third requirement, we demonstrate that the deposited WS_2 thickness can be controlled with single-layer precision by controlling the number of ALD cycles (Fig. 2a). As we increased the number of ALD cycles, the Raman frequency of the A_{1g} mode shifted towards higher wavenumbers, whereas the E^1_{2g} mode remained fixed, consistent with the layer-by-layer increase of the film thickness[20]. The Raman results were corroborated with the thickness measurements using cross-sectional TEM and are summarized in Fig. 2b. By establishing a linear correlation of the WS_2 film thickness as a function of the number of ALD cycles, we demonstrated that our approach enables controlled growth of single-layer, bilayer, trilayer and bulk (more than 5-nm-thick) WS_2 films. Raman mapping over $25 \times 25\ \mu m^2$ areas confirmed the uniform film thickness and high crystalline quality, as no substantial variations were observed in the mapped $\Delta\omega$ values (Fig. 2b) or the full-width at half-maximum of the E^1_{2g} and A_{1g} peaks (Supplementary Section 6).

Finally, conformality is a main BEOL requirement for which most 2D growth techniques fail; however, conformality is required to enable deposition in 3D BEOL structures, particularly in deep trenches with high depth-to-width aspect ratios. Recent research efforts have attempted to address conformality in ALD-grown transition-metal dichalcogenides, but these have been limited to low-aspect-ratio structures (4:1) at the expense of film coverage and quality[21,22]. As the future BEOL will include deep structures with trenches reaching aspect ratios approaching 10:1 in the 3-nm technology node and below[23], we demonstrate the compatibility of our growth process with these future sizes. The conformality was determined by comparing the thickness of the WS_2 layer at the bottom and top of the trench

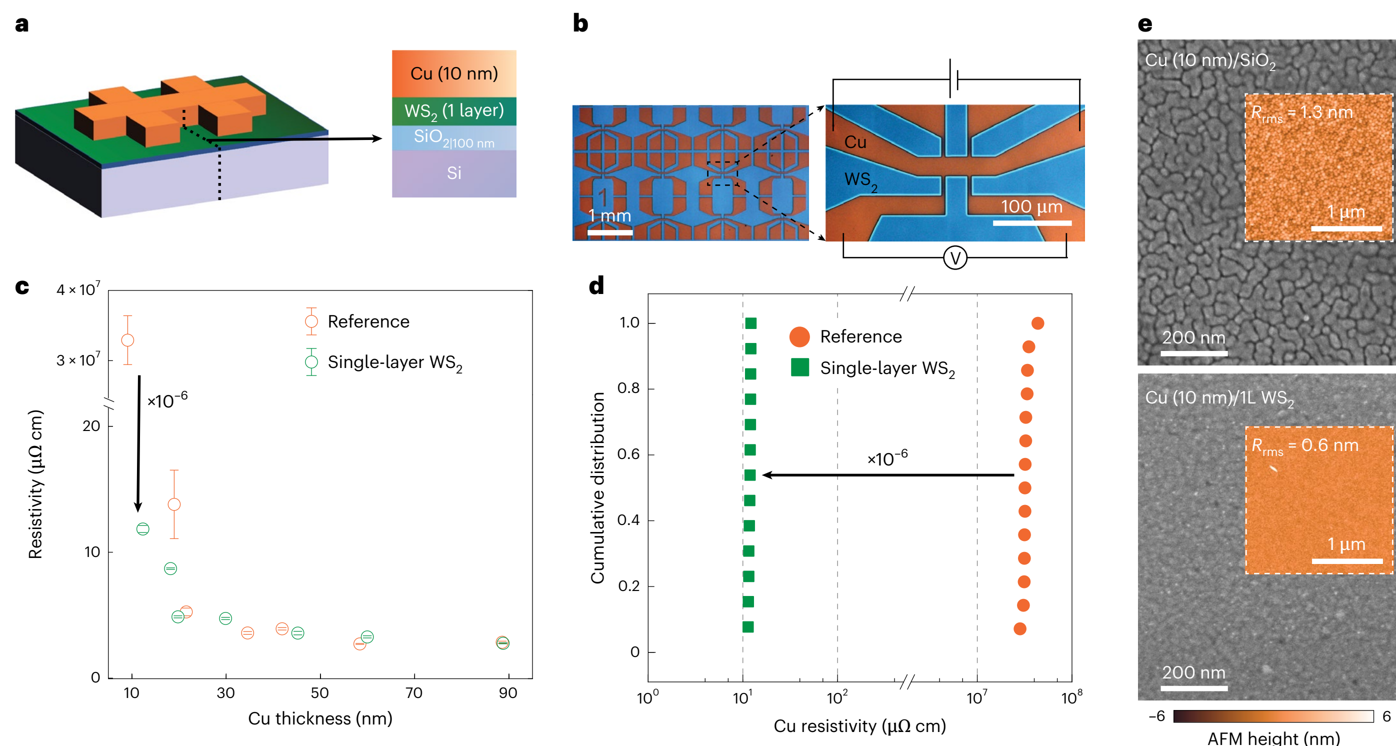

Fig. 3 | Liner properties of the WS_2 film. a, Schematic of the device used for resistivity measurements of Cu using WS_2 as a liner. **b**, Optical micrographs of the liner assessment devices. The electrical connection for the four-terminal measurement is annotated. **c**, Resistivity of Cu films as a function of film thickness with a WS_2 liner and without a liner (reference). The centres of the circles represent the average resistivity values, based on 13–16 independent devices for each Cu thickness. The error bars show the standard deviation. **d**, Cumulative distribution of resistivity values for an ~10-nm Cu film with a single-layer WS_2 liner and without a liner (reference). **e**, SEM and AFM images (inset) of 10-nm-thick Cu films without a liner (reference, top) and with single-layer WS_2 liner (bottom). The root-mean-square roughness, R_{rms}, is indicated on the respective panels.

(Supplementary Section 7). Figure 2c shows a cross-sectional TEM image of a representative patterned structure with an aspect ratio of 10:1. The enlarged views of the side and bottom of the trench demonstrate uniform conformal deposition of WS_2. Through a systematic analysis over a large area, we measured the conformality of our ALD-grown WS_2 to be >95% for the bilayer structure shown in Fig. 2c and for thicker films shown in Supplementary Section 7. Taken together, our ALD WS_2 growth process fulfils all four main requirements for BEOL integration outlined in Fig. 1b.

ALD-grown WS_2 as an effective liner

We next show that our BEOL-compatible WS_2 films function uniquely well as liners for interconnects: they enable good Cu wettability (important for effective Cu seeding and electroplating) and enhanced conductivity for thin Cu wires, even in the ultrathin (0.7 nm) monolayer limit of WS_2. Cu thin films of various thicknesses ranging from 10 nm to 80 nm were thermally evaporated onto a single-layer $WS_2/SiO_{2|100\,nm}$/Si substrate and a reference $SiO_{2|100\,nm}$/Si substrate without any liner. These films were then patterned into Hall bar structures (Fig. 3a,b) to perform four-terminal point probe measurements. We measured the Cu conductivity of more than 15 devices per Cu film.

Figure 3c shows the thickness-dependent resistivity of the Cu films. For thicker Cu films, where the film integrity can be considered thickness-independent, the devices with and without liners do not exhibit noticeable differences in Cu resistivity (Fig. 3c). An analysis using a combination of the Fuchs–Sondheimer and the Mayadas–Shatzkes models[24] to account for surface scattering and grain boundary scattering, respectively, yielded similar values for the device and the reference (Supplementary Section 8). However, for a Cu film thickness of approximately 10 nm, there was a notable drop of more than 6 orders of magnitude in the resistivity between the reference and the WS_2-lined substrates, which had undergone the same Cu deposition. Furthermore, monolayer WS_2 outperformed the industry-standard Ta/TaN stack structure by a factor of ~5 for 10-nm-thick Cu films, despite the monolayer WS_2 liner being much thinner (~0.6 nm) compared with the Ta/TaN stack (5.8 nm), as described in Supplementary Section 8. The results were consistent among devices for the same Cu film, further demonstrating the spatial homogeneity of our films.

To understand the origin of the resistance drop, we conducted scanning electron microscopy (SEM) measurements, which showed that the Cu film morphology was smoother and more continuous for samples with the WS_2 liner compared with the reference sample (Fig. 3e) or indeed that of the Ta/TaN stack (Supplementary Section 8). These results indicate that the WS_2 liner improves Cu wettability, thus enabling continuous and, consequently, less resistive films at lower thicknesses. Atomic force microscopy (AFM) measurements quantified that the surface roughness decreases by more than 50% for Cu films deposited on the WS_2 liner (Fig. 3e). The smoother surface reduced roughness-induced scattering, which in Cu films on WS_2 layers implies less directional scattering at interfaces, leading to a resistance decrease (Supplementary Section 8).

The improvement in Cu resistivity for thinner Cu films is important for future technology nodes, as the Cu wire cross-sectional width is expected to be less than 20 nm. In addition to the absolute change of the resistivity for a fixed Cu thickness, the role of the liner thickness on the interconnect performance must also be considered. For a 20-nm interconnect pitch, the current 4-nm-thick TaN/Ta industry bilayer stack would occupy 40% of the cross-sectional diameter (64% of the cross-sectional area for a wire), implying a lower Cu thickness and higher resistivity. By contrast, our single-layer WS_2 films would only occupy 7% of the cross-sectional diameter (13% of the cross-sectional

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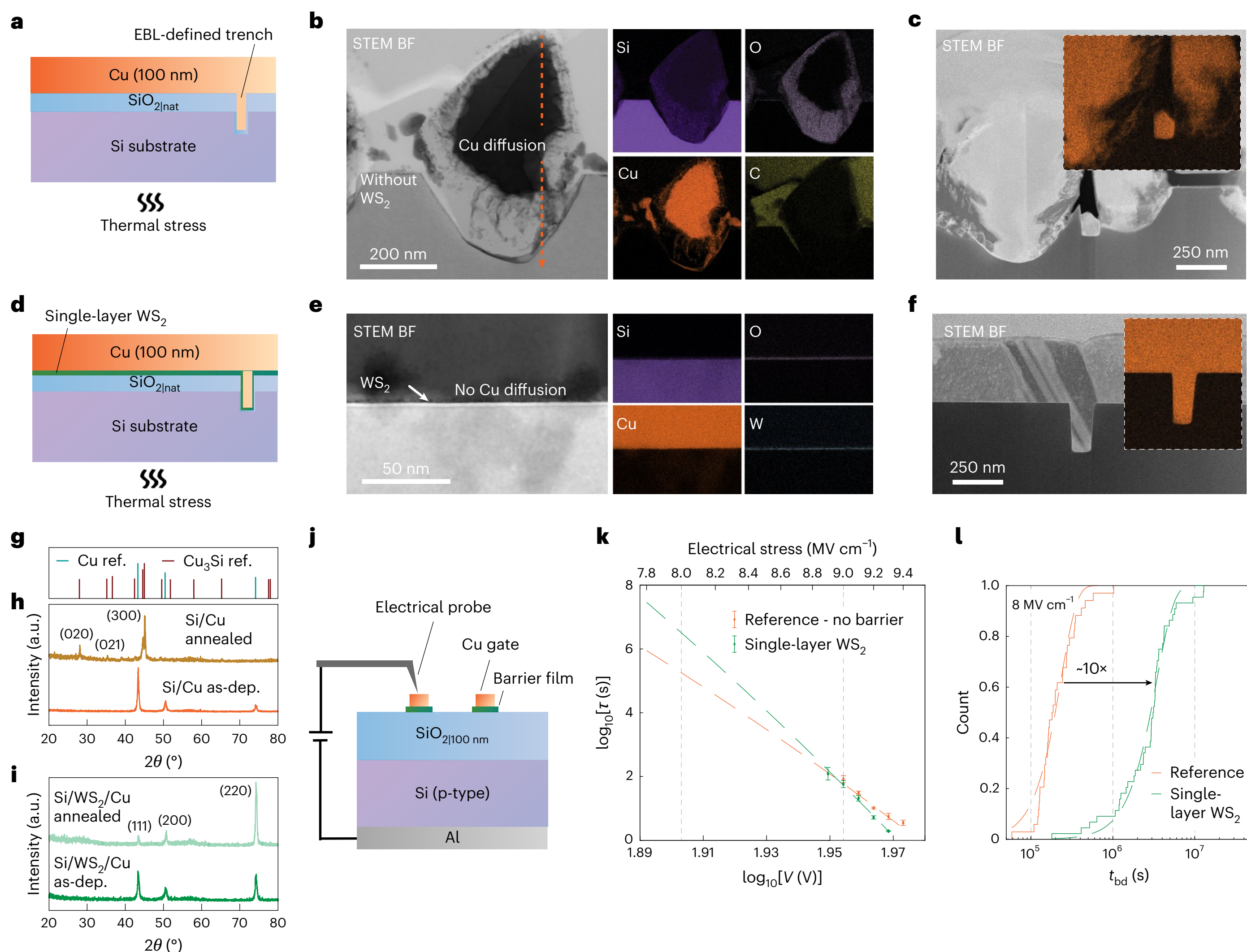

Fig. 4 | WS_2 films as a diffusion barrier. **a**, Schematic of the $Cu/SiO_{2|nat}/Si$ structures used for the thermal stress tests. **b**,**c**, Elemental distribution maps of $Cu/SiO_{2|nat}/Si$ after the thermal stress on a plain Si substrate (**b**) and on a substrate with trench structure (**c**), with EDS elemental mapping of Cu as inset. **d**, Schematic of the Cu/single-layer $WS_2/SiO_{2|nat}/Si$ structures used for assessing WS_2 film as diffusion barriers under thermal stress. **e**,**f**, Elemental distribution maps of Cu/single-layer $WS_2/SiO_{2|nat}/Si$ after the thermal stress on a plain Si substrate (**e**) and on a substrate with trench structure (**f**), with EDS elemental mapping of Cu as inset. **g**–**i**, GIXRD analysis before and after the thermal stress. **g**, Reference Cu and Cu_3Si peaks (Methods). **h**,**i**, GIXRD spectra for the $Cu/SiO_{2|nat}/Si$ (**h**) and Cu/single-layer $WS_2/SiO_{2|nat}/Si$ (**i**), both before and after annealing. **j**, Device structure used for electrical breakdown measurements to assess WS_2 films as diffusion barriers under electrostatic stress. **k**, Measured characteristic breakdown time τ as a function of applied voltage for single-layer WS_2 and a reference without a barrier. Dashed lines show extracted E model projections for the reference (orange) and a single-layer WS_2 barrier (green). Each τ value was extracted from 5–10 breakdown-time measurements in different junctions. Error bars show the standard deviation of $\log_{10}[\tau\ (s)]$. Individual breakdown-time data points are displayed in Supplementary Section 10. **l**, Cumulative distribution of the projected breakdown time for an electrical stress of 8 MV cm^{-1} from the measurements. as-dep., as deposited; BF, bright field; ref., reference.

area), thereby increasing the absolute Cu content and consequently enhancing the Cu conductivity and integrity, as confirmed by our benchmarking results for a Ta/TaN stack.

ALD-grown WS_2 as an effective diffusion barrier

We next focus on testing the performance of our ALD-grown WS_2 films as a Cu diffusion barrier, using two experimental approaches to demonstrate that they prevent Cu migration into the dielectrics and also circuit failure. First, to investigate Cu diffusion under thermal stress, we deposited 100 nm of Cu on both the reference $SiO_{2|nat}/Si$ wafer (Fig. 4a) and on our single-layer $WS_2/SiO_{2|nat}/Si$. The samples were then annealed at 400 °C for 30 min, and the extent of Cu migration and intermixing was characterized through cross-sectional STEM energy-dispersive X-ray spectroscopy (EDS) mapping. A representative STEM bright-field image of the $Cu/SiO_{2|nat}/Si$ reference (Fig. 4b) shows that in the absence of a barrier, Cu reacted with the substrate and formed three-dimensional core–shell structures with dimensions of 300–500 nm. The corresponding EDS elemental maps reveal substantial intermixing between Cu, O and Si, with the outer layer consisting predominantly of Si and O. The inner region comprises mostly Si and Cu. Similar intermixing and morphological disruption are seen on trench structures defined by electron-beam lithography (EBL) on a similar substrate (Fig. 4c). On the other hand, no reaction or intermixing among the layers was observed in the sample with single-layer ALD-grown WS_2 between SiO_2 and Cu (Fig. 4d), indicating that WS_2 acts as an efficient diffusion barrier, as seen in the intact structures in bright-field STEM images in Fig. 4e,f. Similar results are seen in EBL-defined trench structures (analogous to BEOL trenches), as shown in Fig. 4c,f and Supplementary Section 9. These results were confirmed using grazing-incidence X-ray diffraction (GIXRD)

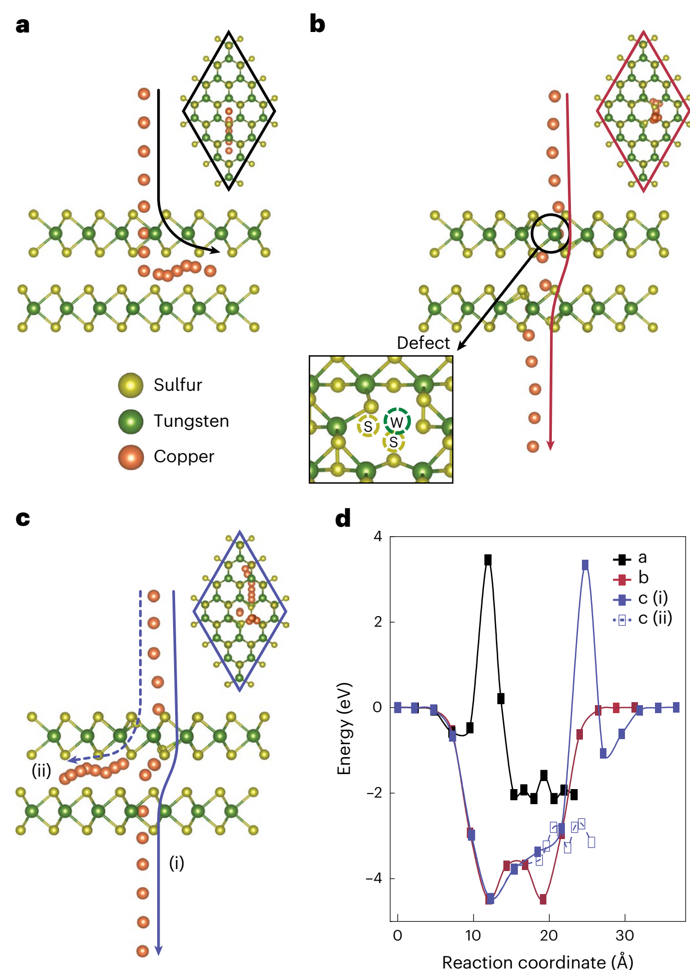

Fig. 5 | Computational diffusion barriers for Cu through WS_2. **a**–**c**, Side and top views of Cu diffusion. **a**, Ideal WS_2 bilayer. **b**, Defective WS_2 bilayer with aligned defects. Inset: the generated defect. **c**, Defective WS_2 layer over an ideal WS_2 layer mimicking a bilayer with misaligned grains. There is another pathway (dashed blue line) for intralayer migration. **d**, Corresponding energy profiles calculated for the different pathways. Visualization in **a**–**c** created with VESTA[47].

before and after annealing (Fig. 4g–i). Before the annealing, only Cu peaks were observed in the GIXRD spectra of both the reference and the sample containing the WS_2 layer. After annealing, the Cu peak decreased notably for the reference sample, and it was replaced by a strong Cu_3Si peak (Fig. 4h), showing substantial Cu migration and intermixing with the underlying Si substrate. By contrast, for the single-layer $WS_2/SiO_{2|nat}/Si$, the Cu peaks were retained post-annealing, denoting no Cu–Si intermixing (Fig. 4i). Furthermore, dynamic secondary-ion mass spectrometry (SIMS) results (Supplementary Section 9) confirm that Cu penetrated deep into the Si after the annealing of samples without a barrier, whereas a single-layer WS_2 barrier prevented this diffusion.

Finally, we conducted time-of-flight (ToF) SIMS, SEM and EDS analyses to investigate the thickness dependence of this barrier behaviour and to provide a comparative analysis with the industry standard. Samples of the same structure with WS_2 barriers of different thicknesses, an ALD-grown TaN barrier (1.6 nm), and a reference without a barrier were subjected to an anneal process optimized to produce the onset of observable changes in the sample with single-layer WS_2, that is 45 min at 500 °C. The results (Supplementary Section 9) show that single-layer WS_2 outperformed thicker 1.6-nm TaN in suppressing intermixing between Si and Cu and preventing morphological disruption of the Cu film. They also demonstrate scalable barrier performance with WS_2 thickness, as the minor changes resulting from the annealing process observed in the sample with single-layer WS_2 were absent for two-layer and thicker WS_2 barriers.

In addition to the thermal stress measurements, our second approach focuses on measuring the time-dependent dielectric breakdown[2,4,5,8] to test the performance of the barrier of the ALD-grown WS_2 films under electrical stress. Upon growth of the WS_2 films, the devices shown in Fig. 4j were fabricated using an all-dry process that was agnostic to the surface chemistry and, thus, prevented material-specific chemical reactions. The $Cu/WS_2/SiO_{2|100\,nm}/Si$ junctions were subjected to a fixed voltage V, and the current was monitored in real time until a breakdown occurred in the form of a sudden increase in current, corresponding to dielectric breakdown or Cu migration into the dielectric. The breakdown time t_{bd} was recorded for 50 junctions and for a range of applied voltages, which enabled us to determine the relation between V and t_{bd} in the standard E model approximation, $t_{bd} \propto \exp(-\gamma V)$, whereby γ is known as the acceleration factor (Supplementary Section 10), which delivers more conservative lifetime estimates compared with other common approximations[5] (Methods and Supplementary Section 10).

Figure 4k,l compares the devices with single-layer WS_2 with a reference device that does not contain a barrier. For each device and each value of applied voltage, the cumulative distribution of the several t_{bd} values measured were fitted with a Weibull cumulative distribution function, $F(t_{bd}) = 1 - \exp[-(t_{bd}/\tau)^{\beta}]$, to extract the characteristic breakdown time τ, where β is the shape parameter of the function, and consequently γ. Our results show that γ is higher for devices with WS_2, at 1.10 ± 0.05 V^{-1}, compared with 0.8 ± 0.1 V^{-1} for the reference device without a barrier. This higher value means that for lower electrostatic stresses, such as the ones relevant for normal operation, junctions with a WS_2 barrier have a higher projected lifetime than the reference (Supplementary Section 10). A projection of the measured breakdown times to 8 MV cm^{-1} using the power law and the extracted acceleration factors (Fig. 4l) shows that the WS_2 barriers are projected to extend the characteristic breakdown time τ to 3×10^6 s for single-layer WS_2, compared with 2×10^5 s for the reference. Taken together, our tests under thermal and electrical stresses confirm that our ALD-grown WS_2 films are effective as Cu diffusion barriers, even in a monolayer regime.

Furthermore, we conducted a similar study for WS_2 samples of different thicknesses to establish the thickness dependence of barrier performance under an electrical stress and compared these with TaN barriers (Supplementary Section 10). This study revealed that single-layer WS_2 performed much like thicker 1.6-nm TaN barriers, whereas thicker WS_2 barriers clearly outperformed TaN with a projected breakdown time that scaled with WS_2 thickness.

Influence of defect alignment on Cu diffusion through WS2 barriers

To better understand Cu diffusion in our WS_2 films, we conducted simulations to examine Cu diffusion through ideal and defective (finite-grain) WS_2 layers using climbing image-nudged elastic band calculations. The resulting diffusion pathways are shown in Fig. 5a–c, and the corresponding energy profiles in Fig. 5d. The first pathway represents the energy profile for Cu diffusion through an ideal (defect-free) WS_2 layer, which reveals an energy barrier ΔE (the difference between the highest and lowest energy points in the diffusion path) of 5.6 eV. Within the same pathway, the energy barrier for Cu diffusion between ideal WS_2 layers (15 Å into the pathway of Fig. 5a with energy profile shown in Fig. 5d) was found to be 0.5 eV. With defective WS_2 layers, atomic vacancies of 1W and 2S were generated to mimic a small grain boundary (inset of Fig. 5b), where Cu is found to be favourably adsorbed at the W vacancy site with an adsorption energy $E_{ads} = -4.5$ eV. This energy value represents the energy required for Cu to break away from that adsorption site, regardless of the

type of layers Cu needs to diffuse through (as illustrated in Fig. 5d). As depicted in Fig. 5b, when the defects (or grain boundaries) are aligned between WS_2 layers, Cu requires only a minimal amount of energy (ΔE = 0.8 eV) to diffuse from one layer to the next. Throughout the pathway, there is only one instance where a maximum energy barrier of 4.5 eV occurs, making it comparable in effectiveness with a defective single layer (Supplementary Section 11). By contrast, within a bilayer structure where defects on each layer are not in close proximity to each other (Fig. 5c), Cu requires a higher energy to traverse an ideal bottom WS_2 layer (indicated by solid blue markers in Fig. 5d(i), ΔE = 7.8 eV) or diffuse between layers (depicted by hollow blue markers in Fig. 5d(ii), ΔE = 1.7 eV).

In the context of conventional diffusion barriers, Cu diffusion through a film typically occurs preferentially along grain boundaries and crystal defects[2]. However, for multilayer ALD-grown WS_2 films, the random misalignment between layers reduces the likelihood of the superposition of these paths, including Cu migration through the film. Therefore, our simulations indicate that the distinctive structure of our multilayered WS_2 offers further benefits for applications that do not need a monolayer film. This result is in accordance with the thickness scaling seen in our barrier characterization under thermal and electrical stress.

Conclusions

We have reported on a scalable approach for creating ultrathin WS_2 films that fulfil the requirements for BEOL integration at sub-5-nm technology nodes and can function as both interconnect barriers and liners. The ALD growth process produces scalable and uniform films over 200-mm wafers without the need to transfer WS_2. The film thickness is controlled with single-layer precision, from monolayer to bulk thicknesses, by varying the number of ALD cycles. We have shown that the deposition is highly conformal, with conformality of >95% achieved for high-aspect-ratio structures such as those predicted for sub-5-nm technology nodes. The inclusion of our WS_2 films as liners for Cu films leads to a resistivity decrease in the metal wire, and the films also acts as a diffusion barrier, preventing Cu migration and dielectric breakdown under thermal and electrical stresses.

Investigating the 2D interface at a microscopic level could provide a better understanding of the relation between crystalline grains and failure mechanisms. Obtaining more control over the grain structure during or after growth could also lead to further improvement of the liner and barrier properties. A previous study of hexagonal boron nitride[25] indicated that van der Waals stacking of 2D films can improve resistance to electromigration, which may be another parameter to consider for our films. More broadly, other 2D films as well as substrate materials beyond SiO_2 could be explored with a similar approach for further specialized use or better compatibility with specific integration requirements. For instance, low-κ dielectric materials (such as those based on porous SiO_2; ref. 26) may be affected by the ALD processes, which could be addressed by adjusting the growth cycle sequences. Future requirements may involve material-selective growth to confine the growth to specific regions of the interconnect structure, such as using self-assembled monolayers as protective layers during growth[27].

Methods

WS_2 ALD growth process

WS_2 thin films were synthesized in a thermal ALD reactor (Atomic-Premium ALD, CN1). Bis(tert-butylimido)-bis(dimethylamido)-tungsten (W-$(NMe_2)_2(N^tBu)_2$; Sigma-Aldrich) was used as the tungsten (W) source, and H_2S gas as the co-reactant. Each cycle consisted of a W precursor pulse (2 s, with N_2 as the carrier gas), followed by N_2 and O_3 pulses (75 s), a H_2S gas pulse (60 s) and an N_2 pulse (30 s). The substrate temperature was 350 °C. The growth rate was 0.65 Å per cycle, and repeating such ALD cycles resulted in the growth of the desired WS_2 layers on Si-based substrates. WS_2 films of various thickness were also deposited on conformal structures having an aspect ratio of 10:1 provided by Applied Materials Inc. In samples used for studying the thickness-dependent and time-dependent dielectric breakdown, the substrate temperature was 300 °C.

Raman characterization of WS_2 films

Raman spectroscopy measurements were carried out on the WS_2 thin films using a Horiba Jobin-Yvon HR800 Raman instrument with a laser excitation wavelength of 488 nm. The laser was set to 2 mW power with a 1 µm^2 spot size. The individual Raman modes were deconvolved using Lorentzian fitting.

TEM sample preparation and imaging

Electron-transparent samples for cross-sectional TEM imaging were prepared using the in situ lamella lift-off method, and plan-view samples for STEM imaging were prepared through the standard transfer process: spin-coating poly(methyl methacrylate), KOH etching and adhesion to a holey carbon grid. Atomically resolved STEM images were acquired with a JEOL JEM-ARM200F equipped with a cold field emission gun and a fifth-order ASCOR aberration corrector operated at 200 kV and a probe convergence angle α of ~31 mrad. Phase-contrast high-resolution TEM images, and STEM/EDS images were acquired with a FEI Talos operated at 200 kV.

Fabrication of Hall bar devices for liner characterization

Hall bar devices, 50 µm wide and 65 µm long, were fabricated by a reverse etching process. Cu films with various thicknesses (10 mm, 15 mm, 20 mm, 30 mm, 40 mm, 50 mm and 80 nm) were deposited at a slow rate (0.15 Å s^{-1} for the first 20 nm and then 0.5 Å s^{-1} for the remaining thickness if any) on a single-layer WS_2 film on SiO_2/Si, on an unlined SiO_2/Si substrate (reference) and on a Ta/TaN/SiO_2/Si structure with a thermal and electron-beam evaporator (AJA). The Ta/TaN bilayer consisted of 2.7 nm of TaN deposited via ALD and 3.1 nm of Ta deposited via sputtering using a sputter system (AJA). We chose a slow Cu growth rate to reduce the kinetic damage to the underlying WS_2 films. Cu-coated samples were spin-coated with a photoresist (Shipley S1805) at 5,500 rpm for 1 min and then baked at 115 °C for 1 min. The Hall bar structures were patterned on the photoresist with a laser writer (Microtech LW-405). The exposed samples were developed in Microposit MF-319 developer for 40 s. A 0.05 M ammonium persulfate solution was used to etch away the exposed Cu area, while the Hall bar device regions remained protected by the unexposed photoresist. The WS_2 was not etched. Before the electrical resistivity measurement, the photoresist was lifted off by rinsing with acetone and isopropyl alcohol. The Cu thickness was obtained by profiling edges using a Bruker AFM and a Park Systems AFM in four locations for each chip.

Hall bar measurement for liner characterization

The patterned devices were bonded with Al wires to a leadless chip carrier. The four-terminal resistance measurements were performed using a physical property measurement system (Quantum Design) and a Keithley Source Meter for more than ten devices for each Cu thickness, with connections as shown in Fig. 3b. The resistivity was extracted from the four-terminal resistivity and the physical dimensions of the Hall bar channel.

Assessment of Cu migration under thermal stress

To evaluate the Cu thermal stress properties, we thermally evaporated 100 nm Cu onto $SiO_{2|nat}$/Si (reference) and single-layer WS_2 onto $SiO_{2|nat}$/Si. The samples were post-annealed at 400 °C for 30 min under an Ar atmosphere at 2 Torr. The as-deposited and post-annealed samples were used to evaluate the performance of single-layer WS_2 films as Cu diffusion barriers under thermal stress using X-ray diffraction, STEM/EDS and SIMS.

Fabrication of trench structures for assessing Cu migration under thermal stress

Trenches of width 100 nm, 200 nm, 500 nm and 1 μm were patterned onto Si substrates using an EBL system (Raith). The trenches were then etched in an inductively coupled plasma reactive-ion etching system (Oxford Instruments) using a combination of SF_6 and C_4F_8 as reactive gases. The trenches were measured to be 250 nm deep using AFM. On some trench samples, the ALD process was applied to grow single-layer WS_2 onto the structures; other trench samples were left without a barrier as a reference. Next, 300 nm of Cu was deposited onto all samples using thermal evaporation. All samples then underwent annealing (500 °C, Ar under 0.5 Torr for 45 min). The resulting samples were then imaged using optical imaging, TEM and EDS.

GIXRD

GIXRD ($\omega = 5°$) was carried out for the as-deposited and annealed Cu (100 nm)/$SiO_{2|nat}$/Si, with and without a single-layer WS_2 film at the Cu/Si interface, using Bruker D8 Advance, equipped with Cu Kα radiation of wavelength 1.542 Å. The reference X-ray diffraction peaks were taken from the *Joint Committee on Powder Diffraction Standards* expected for Cu (reference 00-004-0836) and Cu_3Si (reference 00-051-0916).

Fabrication of devices for breakdown testing due to bias-induced Cu migration

The devices used for electrical breakdown measurements to assess the performance of WS_2 films as Cu diffusion barriers were fabricated in an all-dry fabrication process. Single-layer WS_2 films were deposited onto 2 cm × 2 cm $SiO_{2|100\,nm}$/Si coupons. In addition, a $SiO_{2|100\,nm}$/Si reference sample from the same wafer was subjected to a thermal treatment reproducing the temperature conditions of this growth without WS_2 deposition. Following this, we affixed stainless steel shadow masks onto the samples and the reference. The shadow masks defined arrays of 150 μm × 150 μm junctions. The samples were placed inside a thermal evaporator (AJA) together, and a 100-nm Cu film was evaporated onto the samples through the shadow masks, at a rate of 0.2 Å s^{-1} for the first ~10 nm and 0.5 Å s^{-1} for the remaining thickness, so as to obtain 10 × 10 arrays of Cu/WS_2/$SiO_{2,100\,nm}$/Si junctions (Cu/$SiO_{2|100\,nm}$/Si for the reference). The back surfaces of the samples were mechanically scratched to expose the p-doped Si and placed in a thermal evaporator (Lesker) where 100 nm of Al was evaporated onto the back to form contacts with the Si substrates.

Electrical measurement of breakdown devices

The electrical breakdown of the devices was measured, as in previous reports[4,5,8], in an electrical probe station at room temperature. For each junction, the Cu gate was contacted while the substrate was grounded, and a fixed voltage was applied while the current was recorded. Breakdown was defined as the point at which the current reached a threshold of 0.9 mA (typically as a sudden jump); the time elapsed from voltage application to breakdown was recorded. The threshold was adjusted in the thickness-dependence study to account for the different post-breakdown currents and capacitive spikes (0.1 mA for TaN and single-layer WS_2 and 0.5 mA for three- and four-layer WS_2 as it was affected by capacitive charging). A range of voltage values was applied for each sample, such that a relation between t_{bd} and V could be extracted while keeping the measurement times practical. Each value was repeated 5–10 times for each sample to account for possible deviations (3–5 for the TaN reference due to fabrication limitations). More details of the data and error analysis are given in Supplementary Section 10.

Computation of energy profiles for Cu migration through WS_2 layers

All geometry optimizations and climbing image-nudged elastic band[28] calculations were performed with VASP software[29–32] using DFT[33] with projector augmented wave pseudopotentials[34] and the Perdew–Burke–Ernzerhof exchange-correlation functional[35]. Both monolayer and bilayer WS_2 were generated by cleaving a pre-optimized WS_2 unit cell along the (001) plane and building a 4 × 4 supercell with layers centred in a 20 Å vacuum. A 2 × 2 × 1 Γ-centred k-point mesh was then used to sample the Brillouin zone, and a cutoff energy of 400 eV was applied. Gaussian smearing with a width of 0.05 eV was used to specify how the electron partial occupancies were set for each orbital. All geometries were optimized with fixing cells until the forces on all atoms were below 0.02 eV Å^{-1}. The DFT-D3 method in Grimme[36] was applied to estimate the van der Waals corrections among atoms. Spin polarization was also employed due to the odd number of electrons.

AFM

AFM imaging was performed to extract roughness parameters and film thicknesses for Cu films. The images were acquired on Bruker and Parks AFM systems in tapping mode. Images were processed with the software Gwyddion and Nanoscope.

Scanning electron microscopy

SEM images were obtained using a FE-SEM Hitachi Regulus system in image mode at 1 kV.

ToF-SIMS

The ToF-SIMS elemental analysis was performed using a focused ion beam microscope (TESCAN GAIA 3) connected to a mass spectrometer (Tofwerk). The primary beam was a 30 keV, 200 pA Ga^+ beam. The mass spectra were collected in positive polarity mode. A 128 × 128 pixel hyperspectral map was recorded over the analysis area of 30 × 30 μm^2 using a dwell time of 12 μs. The Si peak at 28 m/z and the Cu peak at 63 m/z were extracted from the spectra and shown in the figures as intensity maps. The vertical map of the first ten frames from the surface is displayed below each spatial map.

SEM imaging and EDS elemental mapping

SEM images and EDS maps were acquired on a Zeiss Sigma 300, equipped with an Oxford Ultim Max 65 mm^2 SDD operated at 5 kV. Images shown were collected from the in-lens secondary electron detector.

Data availability

The data that support the findings of this study are available from the corresponding author upon request.

Code availability

The MATLAB codes used to analyse the data from this study are available from the corresponding author upon request.

References

1. Li, B., Sullivan, T. D., Lee, T. C. & Badami, D. Reliability challenges for copper interconnects. *Microelectron. Reliab.* **44**, 365–380 (2004).
2. Lo, C. L. et al. Enhancing interconnect reliability and performance by converting tantalum to 2D layered tantalum sulfide at low temperature. *Adv. Mater.* **31**, 1902397 (2019).
3. Witt, C. et al. Testing the limits of tan barrier scaling. In *Proc. 2018 IEEE International Interconnect Technology Conference (IITC)* 54–56 (IEEE, 2018).
4. Lo, C.-L. et al. Studies of two-dimensional h-BN and MoS_2 for potential diffusion barrier application in copper interconnect technology. *npj 2D Mater. Appl.* **1**, 42 (2017).
5. Deijkers, J. H. et al. MoS_2 synthesized by atomic layer deposition as Cu diffusion barrier. *Adv. Mater. Interfaces* **10**, 2202426 (2023).
6. Li, L. et al. Vertical and lateral copper transport through graphene layers. *ACS Nano* **9**, 8361–8367 (2015).

7. El Kazzi, S. et al. Assessing ultrathin wafer-scale WS_2 as a diffusion barrier for Cu interconnects. *ACS Appl. Electron. Mater.* **5**, 5074–5081 (2023).
8. Lo, C.-L. et al. Opportunities and challenges of 2D materials in back-end-of-line interconnect scaling. *J. Appl. Phys.* **128**, 080903 (2020).
9. Radisavljevic, B., Radenovic, A., Brivio, J., Giacometti, V. & Kis, A. Single-layer MoS_2 transistors. *Nat. Nanotechnol.* **6**, 147–150 (2011).
10. Liu, Y. et al. Promises and prospects of two-dimensional transistors. *Nature* **591**, 43–53 (2021).
11. Jiang, J., Xu, L., Qiu, C. & Peng, L.-M. Ballistic two-dimensional InSe transistors. *Nature* **616**, 470–475 (2023).
12. Zhu, K. et al. The development of integrated circuits based on two-dimensional materials. *Nat. Electron.* **4**, 775–785 (2021).
13. Zhu, J. et al. Low-thermal-budget synthesis of monolayer molybdenum disulfide for silicon back-end-of-line integration on a 200 mm platform. *Nat. Nanotechnol.* **18**, 456–463 (2023).
14. Balasubramanyam, S. et al. Area-selective atomic layer deposition of two-dimensional WS_2 nanolayers. *ACS Mater. Lett.* **2**, 511–518 (2020).
15. Scharf, T., Prasad, S. V., Mayer, T., Goeke, R. & Dugger, M. Atomic layer deposition of tungsten disulphide solid lubricant thin films. *J. Mater. Res.* **19**, 3443–3446 (2004).
16. Delabie, A. et al. Low temperature deposition of 2D WS_2 layers from WF_6 and H_2S precursors: impact of reducing agents. *Chem. Commun.* **51**, 15692–15695 (2015).
17. Balasubramanyam, S. et al. Edge-site nanoengineering of WS_2 by low-temperature plasma-enhanced atomic layer deposition for electrocatalytic hydrogen evolution. *Chem. Mater.* **31**, 5104–5115 (2019).
18. Cai, J., Han, X., Wang, X. & Meng, X. Atomic layer deposition of two-dimensional layered materials: processes, growth mechanisms, and characteristics. *Matter* **2**, 587–630 (2020).
19. *International Roadmap for Devices and Systems. 2022 Update. More Moore* (IEEE, 2022); http://irds.ieee.org/images/files/pdf/2022/2022IRDS_MM.pdf
20. Berkdemir, A. et al. Identification of individual and few layers of WS_2 using Raman spectroscopy. *Sci. Rep.* **3**, 1755 (2013).
21. Jang, Y., Yeo, S., Kim, H. & Kim, S.-H. Wafer-scale, conformal and direct growth of MoS_2 thin films by atomic layer deposition. *Appl. Surf. Sci.* **365**, 160–165 (2016).
22. Groven, B. et al. Two-dimensional crystal grain size tuning in WS_2 atomic layer deposition: an insight in the nucleation mechanism. *Chem. Mater.* **30**, 7648–7663 (2018).
23. Montero, D. et al. Enabling 3-level high aspect ratio Supervias for 3nm nodes and below. In *Proc. 2022 IEEE International Interconnect Technology Conference (IITC)* 48–50 (IEEE, 2022).
24. Shen, T. et al. MoS_2 for enhanced electrical performance of ultrathin copper films. *ACS Appl. Mater. Interfaces* **11**, 28345–28351 (2019).
25. Jeong, Y. et al. Mitigation of electromigration in metal interconnects via hexagonal boron nitride as an ångström-thin passivation layer. *Adv. Electron. Mater.* **7**, 2100002 (2021).
26. Hatton, B. D. et al. Materials chemistry for low-*k* materials. *Mater. Today* **9**, 22–31 (2006).
27. Mackus, A. J., Merkx, M. J. & Kessels, W. M. From the bottom-up: toward area-selective atomic layer deposition with high selectivity. *Chem. Mater.* **31**, 2–12 (2018).
28. Henkelman, G., Uberuaga, B. P. & Jónsson, H. A climbing image nudged elastic band method for finding saddle points and minimum energy paths. *J. Chem. Phys.* **113**, 9901–9904 (2000).
29. Kresse, G. & Hafner, J. Ab initio molecular dynamics for liquid metals. *Phys. Rev. B* **47**, 558–561 (1993).
30. Kresse, G. & Hafner, J. Ab initio molecular-dynamics simulation of the liquid-metal–amorphous-semiconductor transition in germanium. *Phys. Rev. B* **49**, 14251 (1994).
31. Kresse, G. & Furthmüller, J. Efficiency of ab-initio total energy calculations for metals and semiconductors using a plane-wave basis set. *Comput. Mater. Sci.* **6**, 15–50 (1996).
32. Kresse, G. & Furthmüller, J. Efficient iterative schemes for ab initio total-energy calculations using a plane-wave basis set. *Phys. Rev. B* **54**, 11169 (1996).
33. Kohn, W. & Sham, L. J. Self-consistent equations including exchange and correlation effects. *Phys. Rev.* **140**, A1133 (1965).
34. Kresse, G. & Joubert, D. From ultrasoft pseudopotentials to the projector augmented-wave method. *Phys. Rev. B* **59**, 1758 (1999).
35. Perdew, J. P., Burke, K. & Ernzerhof, M. Generalized gradient approximation made simple. *Phys. Rev. Lett.* **77**, 3865 (1996).
36. Grimme, S., Antony, J., Ehrlich, S. & Krieg, H. A consistent and accurate ab initio parametrization of density functional dispersion correction (DFT-D) for the 94 elements H–Pu. *J. Chem. Phys.* **132**, 154104 (2010).
37. Kim, D.-H., Ramesh, R., Nandi, D. K., Bae, J.-S. & Kim, S.-H. Atomic layer deposition of tungsten sulfide using a new metal-organic precursor and H_2S: thin film catalyst for water splitting. *Nanotechnology* **32**, 075405 (2020).
38. Groven, B., Tomczak, Y., Heyns, M., Radu, I. & Delabie, A. Two-dimensional WS_2 crystals at predetermined locations by anisotropic growth during atomic layer deposition. *J. Appl. Phys.* **128**, 175302 (2020).
39. Hossain, E., Rahman, A. A., Shah, A. P., Chalke, B. A. & Bhattacharya, A. Large-area, thermally-sulfurized WS_2 thin films: control of growth direction and use as a substrate for GaN epitaxy. *Semicond. Sci. Technol.* **35**, 035011 (2020).
40. Xie, Y. et al. Growth of monolayer WS_2 single crystals with atmospheric pressure CVD: role of temperature. *MRS Adv.* **4**, 255–262 (2019).
41. Chen, J. et al. Synthesis of wafer-scale monolayer WS_2 crystals toward the application in integrated electronic devices. *ACS Appl. Mater. Interfaces* **11**, 19381–19387 (2019).
42. Tang, L. et al. Vertical chemical vapor deposition growth of highly uniform 2D transition metal dichalcogenides. *ACS Nano* **14**, 4646–4653 (2020).
43. Cohen, A. et al. Growth-etch metal–organic chemical vapor deposition approach of WS_2 atomic layers. *ACS Nano* **15**, 526–538 (2020).
44. Chubarov, M. et al. Wafer-scale epitaxial growth of unidirectional WS_2 monolayers on sapphire. *ACS Nano* **15**, 2532–2541 (2021).
45. Zhang, Z. et al. Ultrafast growth of large single crystals of monolayer WS_2 and WSe_2. *Natl Sci. Rev.* **7**, 737–744 (2020).
46. Xu, H., Akbari, M. K. & Zhuiykov, S. 2D semiconductor nanomaterials and heterostructures: controlled synthesis and functional applications. *Nanoscale Res. Lett.* **16**, 94 (2021).
47. Momma, K. & Izumi, F. VESTA 3 for three-dimensional visualization of crystal, volumetric and morphology data. *J. Appl. Crystallogr.* **44**, 1272–1276 (2011).

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Author contributions

S.G. and J.S. conceived and supervised the project. M.J.M. and C.D. developed the ALD growth process. H.P.A.G.A., M.J.M., H.T., S.S. and T.C.C. fabricated devices for electrical characterization. H.T., H.P.A.G.A. and M.J.M. performed the resistivity measurements for the liner characterization. H.T., T.C.C. and L.M.S. performed the AFM characterization of the copper films and devices. H.P.A.G.A. and P.Z. performed the time-dependent dielectric breakdown measurements. H.P.A.G.A. and H.T. analysed the electrical characterization data. M.J.M. and C.D. conducted the thermal stress test. J.-Y.C. performed the STEM, SEM and EDS imaging and analysis. S.S. conducted the X-ray diffraction measurements and analysis. M.J.M. and H.T. conducted the Raman measurements. Y.C. and M.W.W. performed the DFT calculations for copper diffusion through WS_2 layers. Y.X. conducted the SIMS. E.K.N. and J.-Y.C. performed the grain-size analysis. M.J.M., H.P.A.G.A., J.-Y.C. and S.G. wrote the article with input from all authors.

Competing interests

The authors declare no competing interests.

Additional information

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