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Co-Packaged Electronics with Microfluidics for Direct-to-Package Cooling

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Abstract

Power semiconductors operating under high heat fluxes and elevated temperatures rely on liquid-cooled heat sinks with substantial coolant volumes. Recent advancements in direct-to-chip (D2C) cooling techniques have shown enhanced thermal performance, reduced energy consumption, compact form factor, and minimized coolant usage. However, integrating microchannels onto semiconductor substrates poses significant fabrication challenges. Hence, we propose a direct-to-package (D2P) cooling approach that embeds microchannels within the package substrate, thereby bypassing the need for Thermal Interface Materials and complex fabrication processes. This D2P approach achieves high heat flux dissipation (up to ~ 625 W cm^{-2}) tested in this study, while consuming a fraction of the coolant volume ($\sim 2-4$ mL). The co-packaged architecture demonstrates $\sim 6-7\times$ lower junction temperatures and thermal resistances than ambient-air cooling and $\sim 2-3\times$ lower than heat sink cooling. A very high coefficient of performance is achieved, with an effective global Nusselt number > 10. This work establishes D2P liquid cooling integration as a scalable and energy-efficient approach for high-power systems.

Introduction

The drive towards miniaturization and increasing power densities exacerbates thermal management challenges in discrete power semiconductor devices. Power inverters in electric vehicles (EV) experience temperature fluctuations exceeding >110°C, with heat flux ranging from ~ 100 W cm^{-2} to ~ 1000 W cm^{-2}, respectively[1;2].

Medium	h W m^{-2} K^{-1}	Q W cm^{-2}
Free convection		
Gases	2 – 25	0.06 – 0.69
Liquids	50 – 1000	1.38 – 27.5
Forced convection		
Gases	25 – 250	0.69 – 6.88
Liquids	100 – 20000	2.75 – 550.0
Convection with phase change		
Boiling or condensation	2500 – 100,000	68.75 – 2750.0

Table 1: Typical values of convective heat transfer coefficient h of different fluids[3], and their corresponding heat flux Q limits determined for a ΔT of 275 °C.

Consequently, traditional cooling methods based on free and forced air convection are thermally limited due to their low convective heat transfer coefficients compared to those of liquids and steam under forced convection (see Table 1). Up to $\sim 55\%$ failures in power converters are associated with thermal stresses[4], and prolonged exposure to elevated temperatures reduces the device lifespan and compromises the system efficiency and performance. Hence, there is a strong demand for innovative thermal management approaches, which is reflected in the global market for thermal management technologies, projected to reach USD 8.9 billion in 2024[5].

Electric vehicles predominantly use liquid-cooled heatsinks for their traction inverter and rectifier modules. For example, the 2015 Tesla Model-S 70D features 36 paralleled TO-247 discrete packaged IGBTs enclosed within an internal cavity heat sink[6;7]. Likewise, the Chevrolet Volt, Toyota Prius, and Nissan Leaf employ liquid-cooled heat sinks for their IGBT modules[6;8–11]. Although liquid-cooled heat sinks are prevalent in EVs, their integration mostly requires Thermal Interface Materials (TIM) for electrical isolation and to reduce contact thermal resistances. The impact of TIM

	Heat Sink Cooling (Current Commercial Technology)	**Direct-to-Chip** (D2C) Cooling (State-of-the-Art Technology)	**Direct-to-Package** (D2P) Cooling (Proposed Technology)
Integration Method	Integrated (mostly) using TIM	Integrated within the semiconductor substrate	Integrated within the package substrate
Thermal Network	Chip → Die-Attach → Package Substrate → TIM → Liquid-cooled Heat Sink	Chip → Liquid-cooled Semiconductor Substrate	Chip → Die-Attach → Liquid-cooled Package Substrate
Advantages	1. Size and geometry similar to traditional heat exchangers. 2. Multiple devices can be cooled. 3. Easy to manufacture and scale. 4. Low integration complexity. 5. High mechanical robustness. 6. No electrical isolation concerns.	1. Substantially lower thermal resistance. 2. Enables maximum device performance. 3. Lowers energy consumption. 4. Very small footprint area. 5. Less coolant consumption.	1. Low thermal resistance. 2. Comparable performance to direct-to-chip cooling. 3. Lowers energy consumption. 4. Small footprint area. 5. Less coolant consumption. 6. Low integration complexity. 7. Feasible on lateral and vertical transistors (needs electrical isolation). 8. Easy to manufacture and scale. 9. Supports heterogeneous integration (chiplets, multi-chip packages). 10. Thermo-mechanical stresses better managed.
Limitations	1. Relatively high thermal resistance (poor TIM conductivity). 2. Complexity in TIM management. 3. Limits maximum device performance. 4. High energy consumption. 5. Requires large footprint. 6. Large coolant volumes needed. 7. Poor scalability with increasing power density.	1. Very high integration complexity (wafer-level fabrication and a thick passive semiconductor). 2. Not suitable for vertical transistors. 3. Hard to commercialize at scale. 4. Devices must be individually cooled. 5. Maintenance challenges.	1. Devices must be individually cooled. 2. Maintenance challenges.
Application	Mid-to-high power electronics	High-power, high-density (AI accelerators)	Mid-to-high power, chiplets, multi-chip packages

Table 2: Comparison of cooling technologies: Heat Sink, Direct-to-Chip, and Direct-to-Package.

on device thermal coupling has been discussed in [12–14]. In addition, liquid-cooled heat sinks are bulky and require substantial coolant volumes. For example, the inverter module on the Tesla Model S 2015 weighs 5.8 kilograms and has 6.4 liters of internal volume [6]. Furthermore, liquid-cooled heat sinks are positioned farther from the device thermal junctions, making conduction heat losses more significant than convection through the heat sink. An overview of trends and challenges in thermal management for power converters is provided in [15–18].

In contrast, direct-to-chip (D2C) liquid cooling solutions based on micro-channel and micro-convection are gaining interest, particularly for data centers and high-performance computing applications [19–22]. A co-designed GaN-on-Silicon AC-DC converter with monolithically integrated microchannels on a passive silicon substrate was demonstrated in [23;24]. Likewise, TSMC developed a liquid cooling solution directly to silicon by embedding microchannels into a silicon lid [25]. Chip-level integration minimizes the thermal gap and substantially reduces thermal resistances, while offering the benefits of high performance, low energy consumption, smaller footprint area, and reduced coolant volumes. Despite their benefits, direct-to-chip liquid cooling encounters integration complexities and scalability issues, as highlighted in [26].

Hence, we introduce an alternative integration approach of co-packaging electronics with microfluidics that enables direct-to-package (D2P) cooling. In Table 2, a comparative summary listing the advantages and limitations of commercial heat sink cooling, D2C

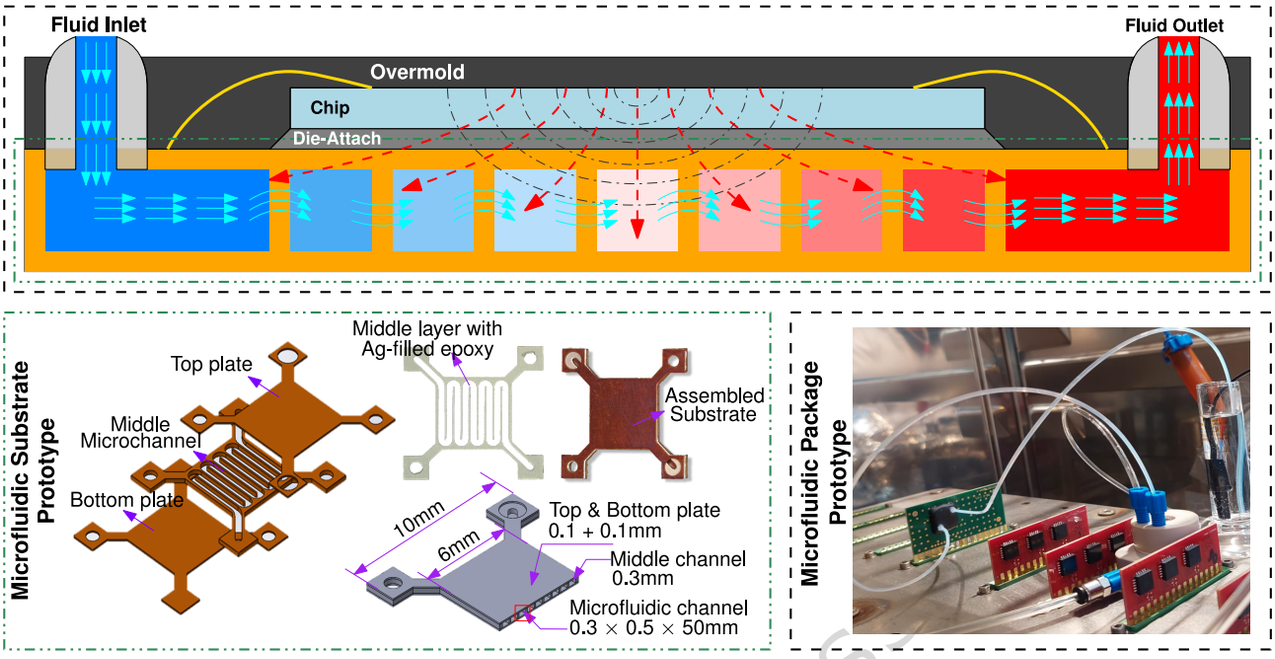


Figure 1: Design and prototype of the direct-to-package cooling concept demonstrated in this study.

cooling, and the proposed D2P cooling technologies is provided. The benefits of integrating cooling at a package-level reduce integration complexities and favor scalability, while eliminating the need for complex TIM management as required in most traditional heat sinks. Figure 1 illustrates the design and prototype of the direct-to-package cooling concept demonstrated in this study. A quad-flat no-leads (QFN) surface mount package type was chosen due to ease of demonstration, which encloses a silicon chip sintered onto a copper substrate with embedded microchannels. In this paper, the heat dissipation capability of the D2P cooling approach was demonstrated up to ~ 625 W cm^{-2} with a maximum coolant flow rate of 0.2 ml s^{-1}, and the maximum junction temperature capped at 300 °C. Based on the experimental results, the following observations were drawn:

1. $\sim 6-7\times$ lower junction temperature and thermal resistance is achieved when compared to packages with ambient air convection cooling.
2. $\sim 2-3\times$ lower junction temperature and thermal resistance is achieved when compared to packages mounted on a liquid-cooled heat sink (30ml s^{-1}) with TIM.
3. High Coefficient of Performance (COP) exceeding 10^3 at a ΔT of 60 °C, and 10^4 at a ΔT of 275 °C is achieved, with very high effective Global Nusselt numbers ($Nu_{\text{eff-G}} > 10$), which is in par to D2C cooling methods.

The convective heat transfer of the proposed concept can be further improved by optimizing the microchannel topology and coolant parameters. Notably, the proposed D2P solution is not limited to single-phase fluids, but can facilitate phase transition with latent heat of evaporation to enhance heat absorption[27–30].

Results

Performance Analysis

To quantify the benefits of D2P cooling, two surface mount package configurations were realized:

- Reference packages with bulk copper substrate.
- Microfluidic packages with micro-channel integrated copper substrate.

In this study, Thermal Test Chips (TTCs) with integrated heaters and temperature sensors were used as an active device. Calibration of both heaters and temperature sensors is explained under the methods section. It is important to note that the heating elements cover $\sim 62\%$ of the total chip area. Hence, the heat flux needs to be computed based on the area of the heating elements. The reference packages with bulk copper substrate were tested as follows:

- Reference packages on PCB with ambient air convection cooling, and
- Reference packages on PCB with forced convection cooling using a liquid-cooled heat sink.

The thermal vias on the PCB transfer the heat from the package to the heat sink through the thermal interface material (TIM). The results of the reference packages were further compared to microfluidic packages tested at 0.1 ml s^{-1}, 0.15 ml s^{-1}, and 0.2 ml s^{-1} (see Figure 2a).

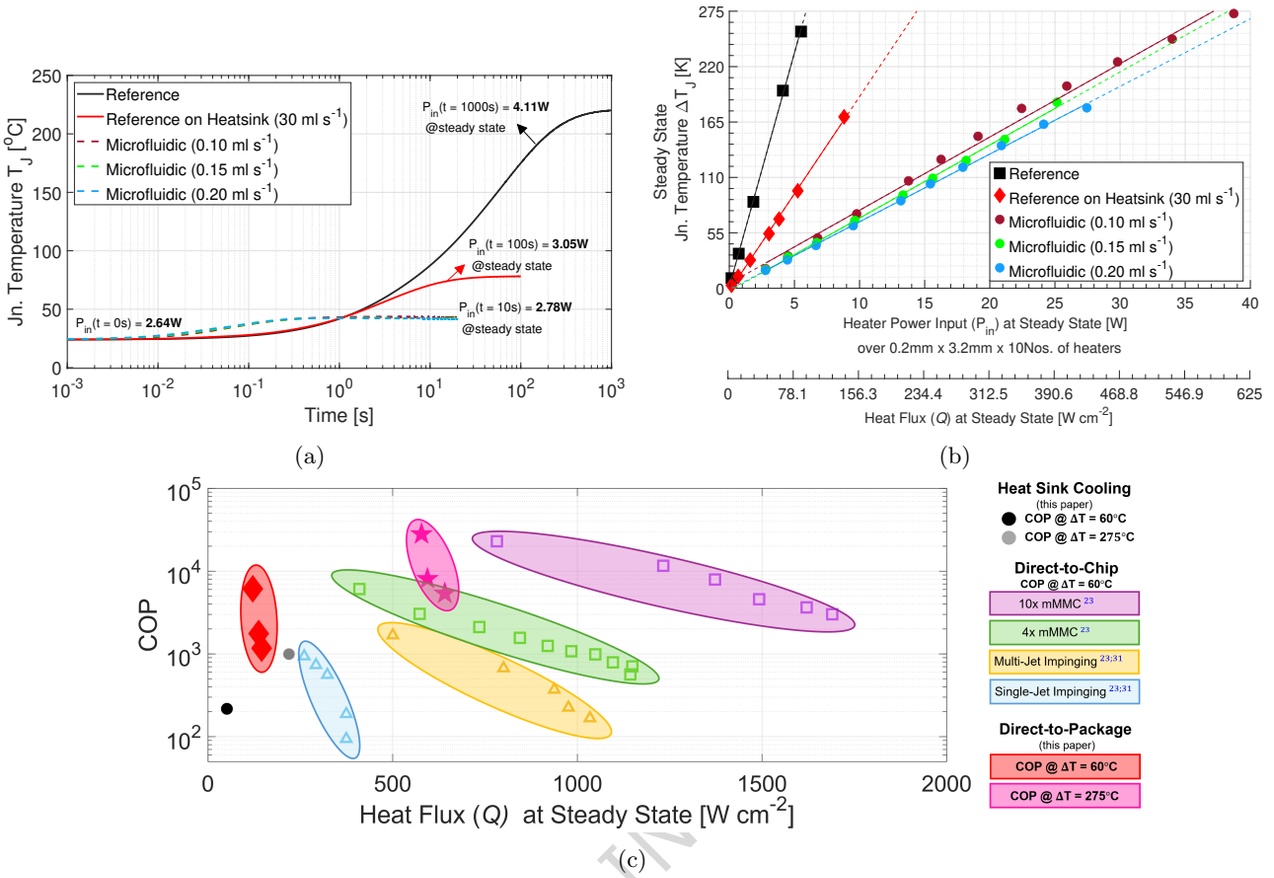


Figure 2: Overview of thermal performance characterization and comparison across different cooling strategies. **(a)** Transient to steady-state thermal measurements comparing the reference package (with ambient cooling and heat sink cooling - 30 ml s^{-1}), and the microfluidic-cooled package at 0.1 ml s^{-1}, 0.15 ml s^{-1}, and 0.2 ml s^{-1} flow rates. **(b)** Steady-state junction temperature variation as a function of power input and heat flux in W $cm^{-}2$. A linear slope was fitted to the measurements. **(c)** Coefficient of Performance (COP) plotted against heat flux for different cooling technologies. COP values are based on steady-state ΔT of 60 °C and 275 °C. The COPs for monolithic manifold microchannels are experimental-based at ΔT of 60 °C reported in[23], while jet-impingement results are simulation-based at ΔT of 60 °C reported in[23;31].

An input power of 2.64 W (Current I = constant) was applied onto the heaters that are distributed over the TTC surface, and the junction temperature (T_J) was measured using the temperature sensor until thermal equilibrium (steady-state) was reached. Due to the increasing surface temperature, the electrical resistance of the heaters also increases, resulting in higher input power as the device reaches steady-state conditions. The temperature sensitivity of the heaters was determined to be $\sim 0.047\ \Omega\ °C^{-1}$, which is explained under the methods section. Accordingly, the resulting power input P_{in} at steady-state was determined for all test case conditions, i.e., for reference packages with and without a heat sink, and also for microfluidic packages at different flow rates (see Figure 2a)

The reference packages with ambient convection cooling reached a steady-state T_J of $\sim$ 220 °C over 1000 seconds with P_{in} increasing from 2.64 W to 4.11 W (see Figure 2a). Likewise, the reference packages mounted onto a heat-sink reached a steady state T_J of $\sim$ 78 °C over 100 seconds with P_{in} increasing from 2.64 W to 3.05 W, and consumed three liters of coolant flowing at a constant rate of 30 ml s^{-1}. In contrast, the microfluidic packages, attained a steady-state T_J of $\sim$ 43°C in under 20 seconds with P_{in} increasing from 2.64 W to 2.78 W (see Figure 2a). The microfluidic packages were tested at different flow rates, 0.1 ml s^{-1}, 0.15 ml s^{-1}, and 0.2 ml s^{-1}, with a maximum coolant volume of less than four milliliters to reach a steady-state T_J. The transient response of the microfluidic packages indicates a shift in time scale due to lower thermal capacitance (less copper) than bulk copper substrates. Also, marginal variations in ΔT_J ($\pm$ 0.5 °C) were observed at different flow rates, likely due to insufficient heating with the applied power input. The experiments were further repeated with varying power inputs (see Figure 2b).

The maximum T_J was constrained to the solder reflow temperature of 300 °C, thereby limiting a maximum ΔT of 275 °C. A linear slope was fitted to the measurement results. With a heating power of less than 6 W at steady state conditions, the reference packages with ambient convection cooling reach a maximum steady-state ΔT of $\sim$ 275 °C. Likewise, the reference packages

with liquid-cooled heat sink reach a ΔT of $\sim$ 170 °C at $\sim$ 9 W, when further extrapolated to a ΔT of 275 °C, indicates $\sim$ 14 W input power. This highlights that with proper thermal management, the device's power dissipation capability can be improved.

In case of microfluidic packages, the distance between the thermal junctions and the cooling components is significantly smaller, which enables to dissipate higher power over the same device footprint. At 0.1 ml s^{-1}, a ΔT of $\sim$ 275 °C was reached at $\sim$ 37 W, marking a $\sim 6-7\times$ increase over the reference packages under ambient air convection and a $\sim 2-3\times$ increase over the reference packages mounted onto a heat sink. At 0.15 ml s^{-1} and 0.2 ml s^{-1}, a ΔT of $\sim$ 275 °C corresponds to $\sim$ 38 W and $\sim$ 41 W, respectively. The maximum input power at a ΔT of 275 °C for all three cases is tabulated in Table 3. The corresponding heat flux Q at steady state, highlighted in Figure 2b, was determined by dividing the heater power input at steady state by the heating element area.

It is important to realize that the choice of surface mount package configuration in this study necessitates a PCB between the package and the heat sink. However, this does not adequately represent the current commercial technology, where Through Hole (TO) packages come in direct contact with the heat sink. Hence, we addressed this discrepancy through thermal simulations (see Supplementary Figure 4), where the reference packages mounted onto a heat sink are simulated with and without a PCB.

To further quantify the performance of direct-to-package cooling, the Coefficient of Performance (COP) parameter was determined. In[23], the COP is defined as the ratio of extracted power to the pumping power while maintaining a steady-state temperature difference ΔT_{max} of 60 °C as expressed in Equation 1,

$$COP = \frac{\Delta T_{max}}{P_{pump} R_{total}} \tag{1}$$

where P_{pump} is the pumping power ($P_{pump} = f\Delta P$), which is the product of the volumetric flow rate f and the pressure drop ΔP (see Supplementary Figure 2), and R_{total} is the total thermal resistance (junction-to-ambient). The R_{total} can be determined from Equation 2, which corresponds to the slope of the linear line fitted in Figure 2b.

$$R_{total} = \frac{\Delta T_J}{\Delta P_{in}} \tag{2}$$

Accordingly, the COP was determined at a ΔT_{max} of 60 °C and 275 °C for both reference packages on heat sink cooling and the microfluidic packages (see Figure 2c). The coefficient of performance (COP) at a ΔT of 275 °C is representative of transistors operating at higher temperatures. For comparative analysis, the COP of direct-to-chip (D2C) cooling is shown for both monolithically integrated manifold microchannel (4× and 10× integration density) demonstrated in[23], and the jet-impinging cooling technology simulated in[31]. A relatively high COP exceeding 10^3 at a ΔT of 60 °C, and 10^4 at a ΔT of 275 °C, was observed with direct-to-package (D2P) cooling, which is in par with the direct-to-chip (D2C) cooling technology at the lower heat flux range.

Heat Transport Efficiency Analysis

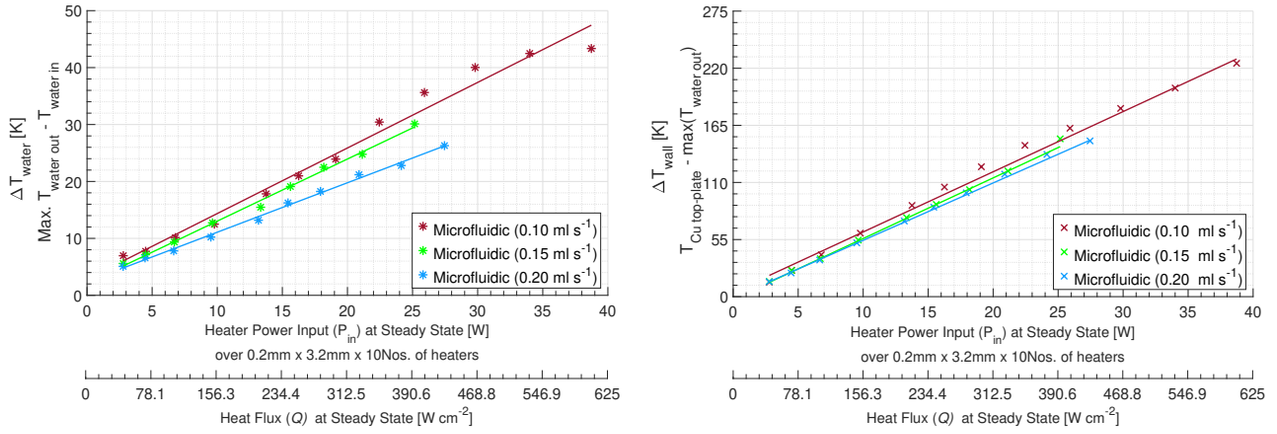
The R_{total} of the microfluidic packages indicates the lowest system resistance as compared to reference packages. For microfluidic packages, the R_{total} is the summation of caloric thermal resistance $R_{caloric}$, convective thermal resistance R_{conv}, and conductive thermal resistance R_{cond}.

$$R_{total} = R_{caloric} + R_{conv} + R_{cond} \tag{3}$$

In principle, $R_{caloric}$ can be determined based on the change in coolant temperature ($\Delta T_{water} = T_{water\ out} - T_{water\ in}$) and the power dissipated through the coolant ($P_{coolant} = f\rho c_p \Delta T_{water}$), where ρ and c_p are the coolant properties. While the inlet water temperature is in a steady state, the outlet temperature exhibits a transient behavior, though the device junction has reached a thermal equilibrium. Ideally, the local temperature of the coolant directly beneath the chip needs to be recorded. In practice, this temperature cannot be measured directly; therefore, the maximum outlet temperature of the coolant recorded using a thermocouple was used as an approximation to determine ΔT_{water} (see Figure 3a). Consequently, the fraction of power dissipating through the coolant ($P_{coolant}$) is unknown. Hence, an effective caloric resistance $R_{caloric\text{-}eff}$ was determined from Equation 4, where the applied input power ΔP_{in} was considered, which corresponds to the slope of the line fitted in Figure 3a. The derived $R_{caloric\text{-}eff}$ is provided in Table 3.

$$R_{caloric\text{-}eff} = \frac{\Delta T_{water}}{\Delta P_{in}} \tag{4}$$

Likewise, to determine the convective thermal resistance R_{conv}, the wall temperature ΔT_{wall} must be obtained, i.e., the temperature difference between the top copper plate of the microfluidic channel (T_{Cu}) and the coolant. To determine T_{Cu}, a one-dimensional heat transfer model was assumed, which also accounts for the lateral heat spreading resistance within the top plate (see Supplementary Figure 1). It is important to note that the coolant temperature relevant to ΔT_{wall} should ideally correspond to the local bulk temperature of the coolant near the wall surface, since there are thermal losses along the ferrules and outlet tubing. Consequently, the recorded maximum outlet temperature is an underestimation of the actual coolant temperature near the wall surface. However, the maximum outlet coolant temperature is expected to be a more realistic estimate to determine ΔT_{wall} than the mean



(a) (b)

Figure 3: Temperature variations across the microfluidic cooling system under different power inputs. **(a)** Variation in coolant (water) temperature and **(b)** Variation in wall temperature as a function of power input and heat flux. A linear relationship was established in each plot (a and b).

coolant temperature between the inlet and outlet. Furthermore, the $P_{coolant}$ is not known. Hence, an effective convection resistance $R_{conv\text{-}eff}$ based on ΔP_{in} was derived from Equation 5, which corresponds to the slope of the linear line in Figure 3b. The derived $R_{conv\text{-}eff}$ is provided in Table 3.

$$R_{conv\text{-}eff} = \frac{\Delta T_{wall}}{\Delta P_{in}} \tag{5}$$

It is important to note that only $\sim 78\%$ of the total chip area (A_{chip} = 3.2 mm × 3.2 mm) is in direct contact with the coolant, i.e., the wetted area = $\sim 78\%$ of A_{chip}, and the remaining $\sim 22\%$ is bonded via a silver-filled epoxy adhesive. As a result, the $R_{conv\text{-}eff}$ parameter represents an effective thermal resistance from the top copper plate to the fluid outlet. The obtained $R_{conv\text{-}eff}$ accounts for the convective heat transfer through the coolant-contacted region, the conductive heat transfer through the epoxy-bonded region, and the lateral heat spreading resistance on the top copper plate. Consequently, $R_{conv\text{-}eff}$ includes parallel thermal paths and should not be interpreted as a pure convective resistance. The obtained $R_{conv\text{-}eff}$ shows relatively less dependence on the flow rate as compared to $R_{caloric\text{-}eff}$ (see Table 3).

Subsequently, R_{cond} can be determined from Equation 3, where the effective caloric and convective resistances are considered. The obtained R_{cond} includes the conductive resistance contribution from the die to the top copper plate predominantly, and it remains independent of the fluidic flow rates. A summary of thermal resistances is provided in Table 3. It is explicit that the $R_{conv\text{-}eff}$ is higher than $R_{caloric\text{-}eff}$ and R_{cond}, due to additional components such as heat spreading resistance and conductive resistance through the epoxy-bonded region. However, optimizing the microfluidic design and the coolant parameters will facilitate reducing the convective resistances.

Furthermore, the effective global heat transfer coefficient $h_{eff\text{-}G}$ was obtained from the experimentally determined convective resistance $R_{conv\text{-}eff}$ and the total chip footprint area A_{chip} (see Equation 6).

$$h_{eff\text{-}G} = \frac{1}{R_{conv\text{-}eff} \cdot A_{chip}} \tag{6}$$

Since $R_{conv\text{-}eff}$ was determined based on a one-dimensional model (see Supplementary Figure 1), the extracted $h_{eff\text{-}G}$ is a lumped (area-averaged) heat transfer coefficient referenced to the total chip area A_{chip}. To further evaluate the heat-transfer performance, an effective global Nusselt number ($Nu_{eff\text{-}G}$) was calculated using Equation 7.

$$Nu_{eff\text{-}G} = \frac{h_{eff\text{-}G} \cdot D_H}{k_f} \tag{7}$$

where D_H is the hydraulic diameter of the microchannel, and k_f is the thermal conductivity of the coolant (for water $k_f = 0.6065$ W m^{-1} K^{-1} [32]). Accordingly, a $Nu_{eff\text{-}G} > 10$ was obtained, indicating very high dissipation capability of the microfluidic packages. $Nu_{eff\text{-}G}$ determined in Equation 7 yields an overall, dimensionless measure of the device's thermal performance representing the system-level heat transfer. The obtained $h_{eff\text{-}G}$ and $Nu_{eff\text{-}G}$ is reported in Table 3.

Despite relatively higher $R_{conv\text{-}eff}$, the effective heat transfer performance, denoted as $Nu_{eff\text{-}G}$, of the microfluidic integrated system indicates very high dissipation capability, which must be due to the convective heat transfer through the coolant integrated closer to the device thermal junction. Optimizing the microchannel substrate design and the coolant parameters can further improve the heat transport efficiency of the microfluidic packages. Erp. et. al.,[23] reports Nusselt numbers for microchannels integrated on semiconductor substrates, which ranges from 2.6 to 6 for straight parallel microchannels and a maximum of 16

for monolithic manifold microchannels. Though the localized convection-based Nusselt number was not determined in this study, the effective global Nusselt numbers demonstrated are in a comparable range to direct-to-chip cooling methods reported in[23].

	Reference ambient air convection	**Reference** on heatsink 30 ml s^{-1}	**Microfluidic** package		
			0.1 ml s^{-1}	0.15 ml s^{-1}	0.2 ml s^{-1}
Max. P_{in} [W] @ T_j = 300°C	6	14	37	38	41
R_{total} [K W^{-1}]	46.42	19.30	7.27	7.25	6.72
$R_{caloric\text{-}eff}$ [K W^{-1}]	–	–	1.15	1.09	0.87
$R_{conv\text{-}eff}$ [K W^{-1}]	–	–	5.80	5.84	5.53
R_{cond} [K W^{-1}]	–	–	0.32	0.32	0.32
$h_{eff\text{-}G}$ [W m^{-2} K^{-1}]	–	–	16844	16722	17672
$Nu_{eff\text{-}G}$ [-]	–	–	10.41	10.34	10.93
Coolant volume [ml]	–	3000	2	3	4

Table 3: Comparative summary of experimental results for all three test cases.

Discussion

In this study, a co-packaging approach was introduced for Direct-to-Package (D2P) cooling solution. This is particularly important as commercial solutions rely on bulky heat sinks with Thermal Interface Materials (TIM) and substantial coolant volumes to yield optimal thermal performance. Recent state-of-the-art developments focus on chip-level integration by either embedding micro-channels onto semiconductor substrates or micro-convection through jet-impingement. Despite the performance advantages of Direct-to-chip (D2C) cooling solution, they are complex, significantly expensive, and require a thick passive semiconductor substrate (for embedding micro-channels).

In contrast, our proposed D2P approach integrates micro-cooling channels onto the package substrate, thereby providing comparable thermal performance to D2C techniques, without the associated complexities. In this paper, a significant reduction in total thermal resistance was demonstrated with D2P cooling, leading to a lower steady-state junction temperature compared to ambient air cooling and liquid-cooled heat sinks. Notably, the proposed solution consumed a fraction of the coolant volume required by traditional heat sinks. The Coefficient of Performance (COP) exceeded 10^3 at a ΔT of 60 °C, and 10^4 at a ΔT of 275 °C with a relatively high effective global Nusselt number comparable to D2C techniques.

- Design optimization and material compatibility: While this work validates the feasibility of D2P cooling solution, future research should explore optimization strategies for channel geometry, fluidic flow, fabrication methods, and other dielectric fluids that are corrosion resistant.
- Alternative coolants and two-phase systems: Additional performance gains can be achieved by exploring different coolants, such as nanofluids, phase change materials, and phase transition fluids that use the latent heat of evaporation for heat absorption. However, two-phase systems require heat exchangers and condensers. Implementation of phase-change materials can potentially act as a thermal buffer.
- Scalability and packaging integration: A key future focus should be on integrating the D2P concept into standard packaging, especially in high-volume or automotive-grade systems. This includes ensuring mechanical reliability, manufacturability, and compatibility with assembly processes.
- Applicability to different transistor architectures: The D2P cooling strategy is not limited to lateral transistors. It can potentially be extended to vertical power devices as well, provided proper electrical insulation of the coolant needs to be ensured to mitigate parasitic leakage paths or shorting risks for both lateral and vertical transistors.
- Reliability and long-term operation: The microfluidic structures are subjected to thermal and mechanical stresses. Hence, it is important to assess the long-term reliability and pressure stability of the system.

The demonstrated co-packaged architecture for D2P cooling holds immense potential in realizing high-power electronic systems. Bridging the thermal gap by integrating cooling components closer to the device junction is broadly applicable across a wide range of applications, namely sustaining high power operation in SiC devices to enhancing RF power added efficiency in GaN amplifiers. Thus, the D2P cooling strategy can contribute to the development of reliable and sustainable electronics.

Methods

Selection and Calibration of the Semiconductor Device

The choice of semiconductor device is crucial as it influences the package thermal performance analysis. Thermal Test Chips (TTC) are specialized devices fabricated through processes similar to semiconductor devices. The design of TTCs is intended to simulate device junction (surface) heating through lithographically defined heating elements, and the junction temperature is recorded using Resistance-based Temperature Detectors (RTDs). Hence, a commercial silicon-based TTC was used in this study (see Figure 4).

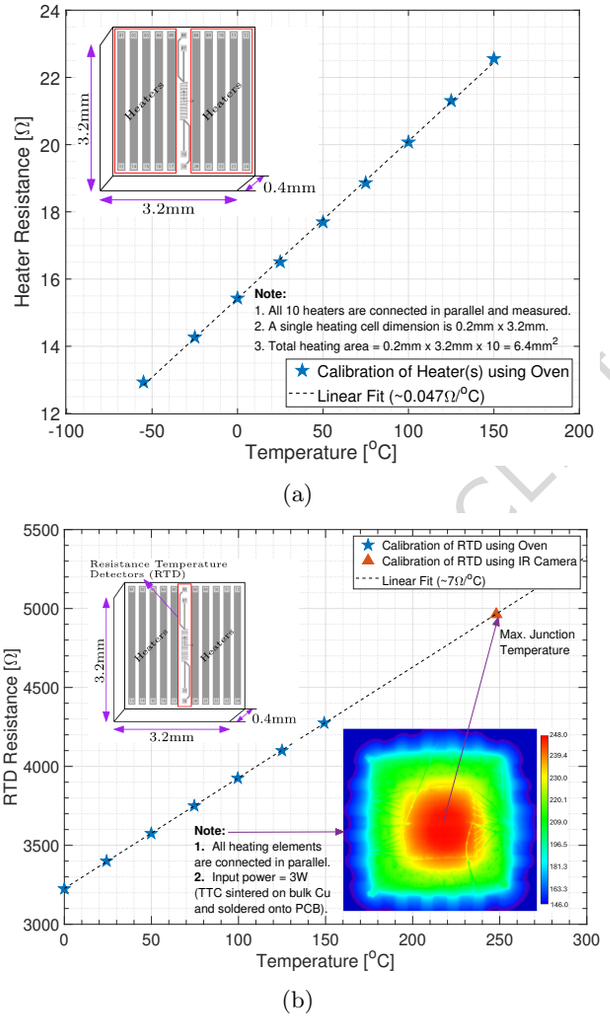


Figure 4: Calibration of heating elements and Resistance-based Temperature Detector (RTD). **(a)** The resistance of all parallely connected heaters was measured at nine different temperatures between −55°C to +150°C. **(b)** The RTD resistance was measured at seven different temperatures between 0°C and +150°C. To determine the RTD sensitivity at higher temperatures, 3W power input was applied to the heaters, while the steady state temperature was recorded using an IR camera, and the RTD resistance was simultaneously measured. Both plots **(a)** and **(b)** exhibit a linear relation.

The heating elements on TTC were connected in parallel to achieve a uniform temperature distribution along the surface. The RTD is located centrally with 4-point Kelvin contacts. It is essential to determine the temperature sensitivity of the heating elements and the RTD. In Figure 4a, the resistance of the parallelly connected heating elements was measured at nine different temperatures from −55 °C to 150 °C. A perfectly linear relationship was determined with a sensitivity of 0.047 Ω °C^{-1}. Likewise, the temperature sensitivity of the RTD was determined through a two-step calibration process. For calibration below 150 °C, the RTD was measured inside an oven at different ambient temperatures. For temperatures above 150 °C, an input power of 3W was applied to the heaters by connecting all heating elements in parallel, and the change in RTD resistance was measured while simultaneously measuring the device junction temperature using an Infra-Red (IR) camera.

The measured RTD resistance and the junction temperature were in a steady state. A linear relationship was established by fitting both calibration measurements, resulting in a sensitivity of ~ 7 Ω °C^{-1} (see Figure 4b). For IR measurements, the TTC was sintered on a bulk copper substrate, which was further soldered onto a PCB and wire bonded. The backside of the TTC (Silicon substrate) is metalized with TiPtAu (100/100/100nm) to promote adhesion to the die-attach interface material.

Design and Fabrication of Microfluidic substrate

The design of the microchannel was chosen based on fabrication feasibility. A three-layered copper substrate with top and bottom copper plates was designed to enclose a serpentine-structured microchannel middle layer. The serpentine-channel design was realized through a laser-cut process. While optimizing the microchannel geometry is beyond the scope of this study, the serpentine configuration is expected to induce localized turbulence and enhance heat dissipation compared to straight microchannels. The serpentine microchannels have a dimension of 0.3 mm × 0.5 mm with a total channel length of ∼ 50 mm between the inlet and outlet. The top and the bottom copper plates with 0.1 mm thicknesses each were attached to the microchannel middle layer using conductive Ag-filled epoxy adhesive. The coolant inlet and outlet were placed diagonally along the substrate through the top plate, with alignment markers positioned along the counter-diagonal. All details relevant to the embedded microchannel substrate are provided in Figure 1.

Though the design optimization was not investigated in this study, we suggest the following improvements to be considered in the future. Simplifying the three-layered substrate into a two-layered substrate with half-etched microchannels bonded using thermal compression can be a scalable and efficient approach. Furthermore,

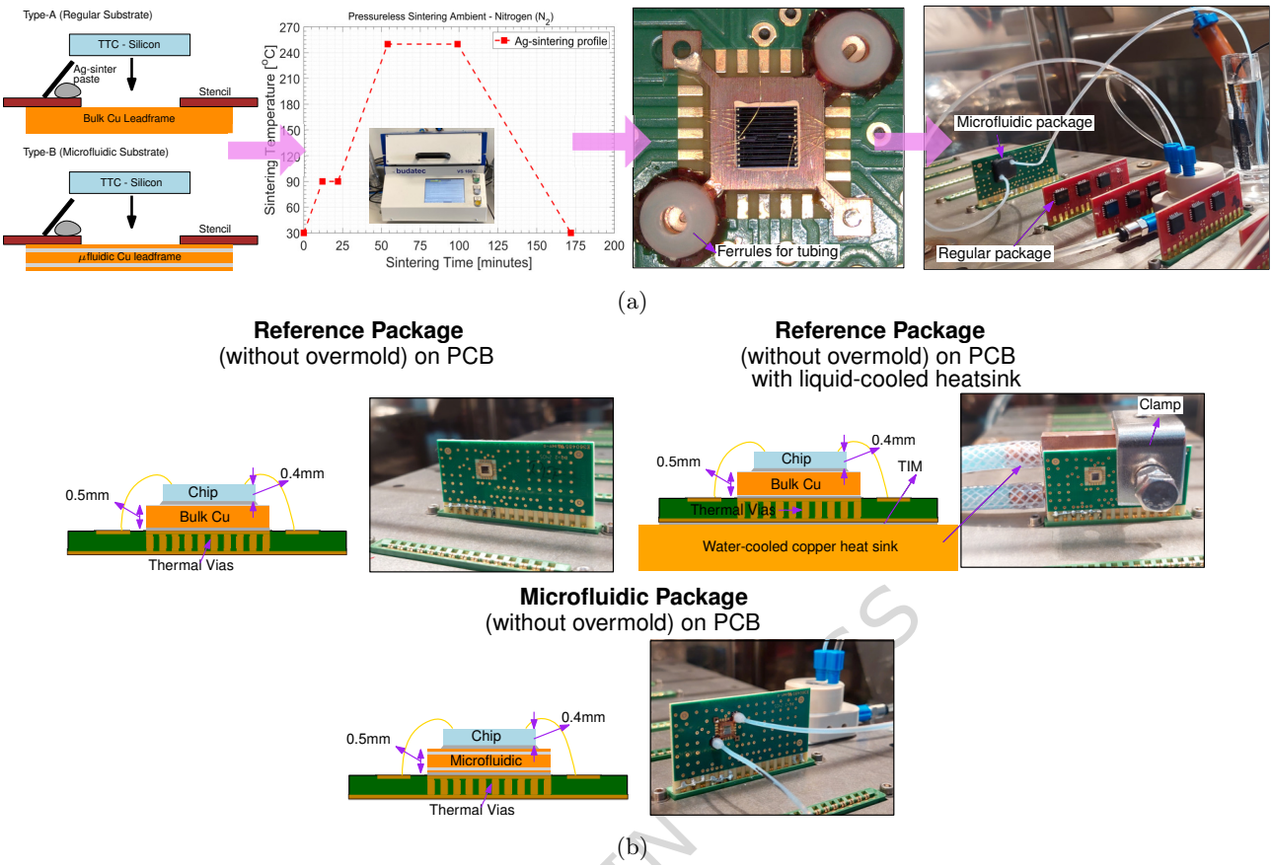


Figure 5: Overview of packaging assembly processes and experimental configurations for comparative thermal testing. **(a)** Step-by-step illustration of the package assembly process. **(b)** Visualization of different test cases featuring reference package configuration and microfluidic package. For the reference package with a liquid-cooled heat sink, two clamps were used to ensure uniform compression; using a single clamp may result in uneven force distribution, leading to tilting or lift-off.

coolant delivery in real-life applications could be implemented through PCBs.

Package Assembly Processes

The devices were assembled using classical back-end packaging processes, which involve three primary steps: Die-bonding, Wire-bonding, and Encapsulation. The selected TTCs were bonded onto the substrate using Ag-sinter die-attach material. Ag-paste in wet form was stencil-printed on the microfluidic substrate. The TTCs were placed over the wet paste using a force-controlled die-bonder and sintered pressureless under Nitrogen ambient at 250 °C. Ag-sintering material was chosen because of low processing temperatures and a high melting point after sintering. The die-bonding process is identical for reference samples with a bulk copper substrate. Upon sintering, the complete stack is soldered onto a printed circuit board (PCB) and subsequently wire-bonded onto the bond pads of the PCB using 99.99% pure Au-wire bonds. For microfluidic packages, inlet and outlet ferrules were securely placed using an adhesive. Finally, the assembled devices can be optionally encapsulated using a dam and fill encapsulant.

In this study, the devices were not encapsulated since the glass transition temperature of the encapsulant is less than the desired testing temperatures. An illustration of the package assembly processes is provided in Figure 5a. In Figure 5b, the two package configurations with different test cases are provided for experimental evaluation. In case of reference packages mounted onto a liquid-cooled heat sink, a silicone-free heat sink compound from Techspray was used as Thermal Interface Material (TIM), which has a conductivity of ~ 0.92 W/mK with functional temperature range of -40 °C to $+200$ °C. For heat sink cooling, the channel radius is 2 mm, and the estimated channel length is 10 cm.

Experimental Setup for Performance Evaluation

To evaluate the package performance, a dedicated experimental setup was developed, as illustrated schematically in Figure 6. Devices soldered to the PCB were securely mounted in a test socket, enabling electrical connections between the TTC and the measurement equipment via a multiplexer. The input currents for the heaters were sourced using a parallelly connected Source Measurement Unit (SMU) with compli-

ance of 40V up to 2A continuous current. The change in RTD resistance was measured using a Digital MultiMeter (DMM), which has a resolution of 1 μV for measurements up to 10V and an accuracy of $\pm$ 0.1 mV. The SMU, DMM, and Multiplexer were synchronized through a Trigger Synchronization and Communication (TSP) protocol, and the measurement sequence was programmed using a user-defined MATLAB program. An open-loop microfluidic system was implemented to evaluate the cooling performance. A pressure dispenser with a maximum pressure of 675 kPa was connected to a 10 ml syringe carrying demineralized water as the coolant. Inlet coolant temperature was recorded, and the coolant was subsequently passed through a 300 μl degasser to remove air bubbles from the coolant, preventing blockage and localized explosions. The pressure difference before and after entering the microfluidic package was recorded using two pressure sensors. The coolant outlet was collected in a reservoir, and the outlet temperature was measured with a thermocouple at one-millisecond intervals.

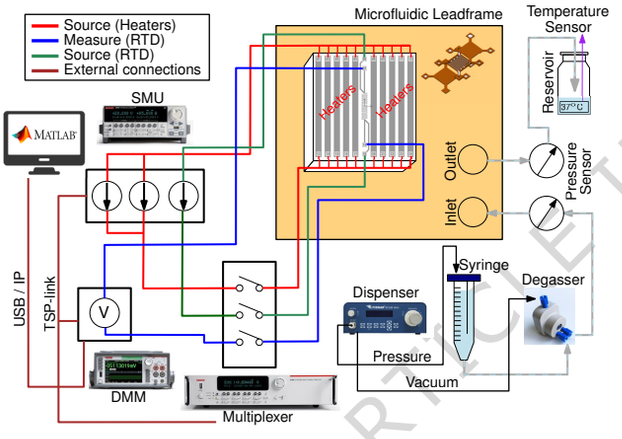


Figure 6: Schematic electrical and microfluidic circuit illustration.

Data Availability Statement

This manuscript is part of the corresponding author's (Henry A. Martin) Phd dissertation that is stored publicly as Prognostics and thermal management of power electronic packages. The experimental data that pertains to this manuscript is stored in the public repository https://doi.org/10.6084/m9.figshare.31073227.

Code Availability Statement

No custom code or mathematical algorithm that is deemed central to the conclusions has been developed for this manuscript.

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Author Contributions

- **Henry A. Martin:** Conceptualization; Methodology; Validation; Formal analysis; Investigation; Resources; Data curation; Writing – Original Draft; Writing – Review & Editing; Visualization.
- **Zihan Zhang:** Software (thermal simulations); Validation support.
- **Mahad Saeed:** Investigation.
- **Sander Dorrestein:** Conceptualization; Resources.
- **Edsger C. P. Smits:** Conceptualization; Supervision; Project administration.
- **Rene H. Poelma:** Conceptualization; Supervision.
- **Willem D. van Driel:** Supervision.
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Competing Interests

The authors declare no competing interests.